A Dissertation on

REALIZATION OF OTRA BASED ANALOG CIRCUITS

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CERTIFICATE

It is certified that Nishant Sharma (2K11/VLS/17), student of Master of Technology, VLSI Design & Embedded Systems, Department of Electronics & Communication Engineering, Delhi Technological University, have submitted the report entitled **"Realization of OTRA based analog circuits"** under my guidance towards partial fulfillment of the requirements for the award of the degree of Master of Technology (VLSI Design & Embedded Systems). This dissertation is a bonafide record of project work carried out by him under my guidance and supervision. I wish him success in all his endeavors.

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Abstract

Over the last few decades, the circuit designers have used the voltage mode signaling technique for the designing of analog circuits. Through this technique was very reliable yet with the progress of technology it is facing some serious problems. The evolutions of submicron technologies has resulted in the requirement to use low power supply voltage which makes it difficult to design voltage mode circuits with high level of linearity in a wide dynamic range. Also as the signal processing moves to high frequencies, the constant gain bandwidth product of this techniques makes it unfit to the used. The sluggish slew-rate of this technique is also a problem for upcoming faster circuits.

Theses problems can be solved by implementing analog signal processing circuits using current mode techniques. The major benefits associated with current mode signaling are larger dynamic range and better linearity, higher bandwidth; higher slew-rate besides others. Different analog circuit building blocks working on current mode signaling techniques are available such as various generations of current conveyor, CFOA, CDTA, CDBA, OTA, OTRA etc.

This thesis is dedicated to OTRA based analog circuits. A brief introduction to current mode signaling and some of its blocks is given followed by a literature review of OTRA which includes its realization techniques and applications. Some OTRA simulated structures and its application circuits are using PSPICE. Then OTRA based inverse filter topologies are proposed and their workability is verified using PSPICE.

Table of Contents

LIST OF FIGURES

LIST OF Tables

CHAPTER 1

INTRODUCTION

1.1 Background

The field of Digital signal processing is becoming technically more and more powerful and important with the advances in IC technology which provides compact and efficient implementation of these algorithms in silicon circuits. Indeed many type of signal processing today require Digital Signal Processing, yet the importance of Analog Signal Processing circuits has not reduced. This is due to the fact that most of the signals available in the nature which are required to be processed are analog in nature like speech signals, voice signals, signals generated inside earth's crust etc. For utilizing these signals in various useful applications, they are first captured with the help of sensors, than processed in there analog form and then converted into digital form for further processing and communication process. Hence it can be said that the analog circuits also behave as a bridge between analog signal world and digital signal processing systems [1-3]. As we are improving our technology and exploring new spaces, we require processing of different types of analog signals and therefore the importance of improved analog signal processing blocks and circuits is increasing rapidly.

From the initial stages, operational amplifier [4] is an unavoidable block available for developing analog circuits. It is a voltage signal processing block which is still the favourite for analog circuit application because of its various advantages. But on the other hand due to its various limitations like constant gain bandwidth product, low slew rate etc. the analog circuit designers are now finding ways to develop new blocks which could replace the existing operational amplifier.

One of such way is switching to current signal processing blocks. Current mode blocks have advantages like higher signal bandwidth, high slew rate, improved linearity, simpler circuit [5] etc. which are making them important for analog signal processing field. There are various current mode active building blocks developed in recent times few of which are various generations of current conveyors (CCI, CCII, CCIII), operational trans-conductance

amplifiers (OTA), current-feedback op-amps (CFOA), four terminal floating nullors (FTFN), differential voltage current conveyor (DVCC), differential difference current conveyor (DDCC), dual X current conveyors (DXCCII), current controlled current conveyors (CCCII), operational trans-resistance amplifier (OTRA) etc. Employing these new active elements for analog design and using CMOS technology for implementation of the circuit's designs obtained new possibilities in signal processing field.

In this project OTRA has been explored for realising various analog signal processing circuits.

1.2 Current Mode Signalling

Current-mode circuits, in which information is represented by the branch current of the circuit rather than the nodal voltages (as in voltage-mode circuits), possess many unique and attractive characteristics over their voltage-mode counterparts including a small nodal time constant, high current swing in the presence of a low supply voltage, reduced distortion, a low input impedance, a high output impedance and less sensitive to switching noise. CMOS current mode circuits have found increasing applications in telecommunication systems, instrumentation, analog signal processing, multiprocessors, high speed computer interfaces, and the backplane of complex electronic systems.

Various advantages of current mode processing include:

- Larger dynamic range.
- Higher signal bandwidth.
- Greater linearity.
- Simpler circuitry.
- Low power consumption.
- Higher slew rate.
- Reduced distortions.

1.3 Various Current mode signalling Blocks

In the field of analog circuit designing, a large number of current mode signalling blocks are developed till date and the counting is increasing rapidly due to various advantages inherited by them as discussed in previous section. In this section, some of the current mode signalling blocks have been discussed.

1.3.1 Current Conveyors

The current conveyor (CC) is the basic building block of a number of contemporary applications both in the current and the mixed modes. The principle of the current conveyor of the first generation was published in 1968 by K. C. Smith and A. S. Sedra [6]. Two years later, today's widely used second-generation CCII was described in [7], and in 1995 the third-generation CCIII was developed.

However, initially, during that time, the current conveyor did not find many applications because its advantages compared to the classical operational amplifier (OpAmp) were not widely appreciated and any IC implementation of Current Conveyors was not available commercially as an off-the shelf item. An IC CC, namely PA630, was introduced by Wadsworth in 1989 (mass produced by Photo electronics Ltd. of Canada) and about the same time, the now well known AD844 (operational trans-impedance amplifier or more popularly known as a Current Feedback Op-Amp) was recognized to be having internally a CCII+ followed by a voltage follower. This AD844 is used in designing one of the OTRA design discussed later in this literature.

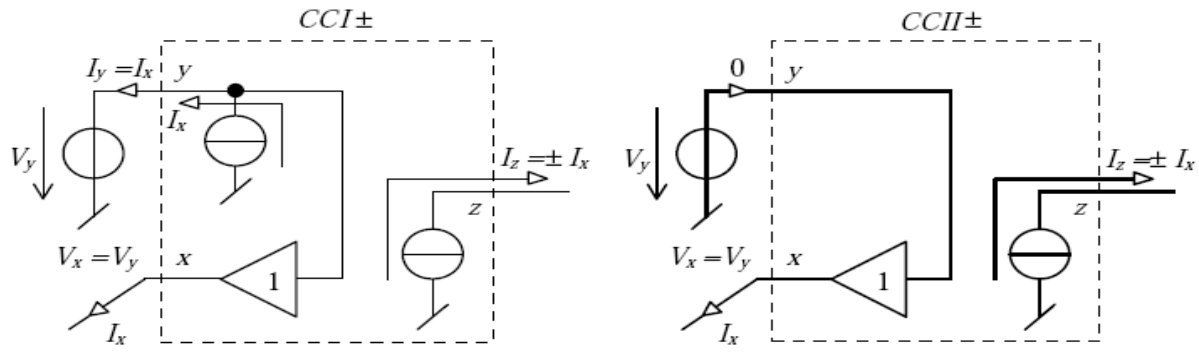

Fig 1.1: Current Conveyers CCI and CCII.

1.3.2 Current Feedback Operational Amplifier (CFOA)

Before looking at any circuits, let us define voltage feedback, current feedback, and trans-impedance amplifier. *Voltage feedback*, as the name implies, refers to a closed-loop configuration in which the error signal is in the form of a voltage. Traditional operational amplifiers use voltage feedback, which means their inputs will respond to voltage changes and produce a corresponding output voltage. *Current feedback* refers to any closed-loop configuration in which the error signal used for feedback is in the form of a current. A current feedback op amp responds to an error current at one of its input terminals, rather than an error voltage, and produces a corresponding output voltage. Notice that both open-loop architectures achieve the same closed-loop result: zero differential input voltage, and zero input current. The ideal voltage feedback amplifier has high impedance inputs, resulting in zero input current, and uses voltage feedback to maintain zero input voltage. Conversely, the current feedback op amp has a low impedance input, resulting in zero input voltage, and uses current feedback to maintain zero input current.

The current feedback operational amplifier is simply a combination of a positive second generation current conveyor $CCII_+$ and a voltage buffer at the conveyor current output. The input current received by the inverting input of the CFOA is transferred to the high impedance current conveyor output, causing a large change in output voltage. The transfer function of any trans-impedance amplifier is expressed as a voltage output with respect to a current input. As the function implies, the open-loop gain is expressed in ohms. Hence a current-feedback op amp can be referred to as a trans-impedance amplifier [8]. The current feedback operational amplifier has a trans-resistance equal to the impedance level at the conveyor Z-output.

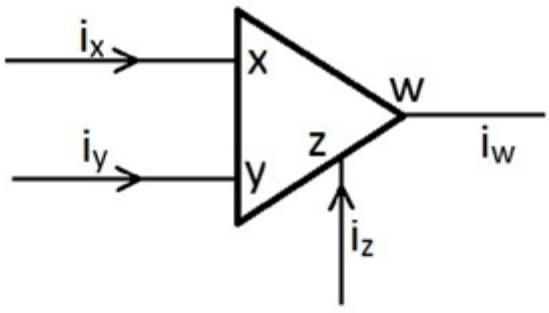

Fig 1.2: Block diagram for CFOA.

The voltage-current equations for CFOA are given in equation *(1.1)* to *(1.4).*

$$V_x = V_y \qquad (1.1)$$

$$i_y = 0 \qquad (1.2)$$

$$i_z = i_x \qquad (1.3)$$

$$V_w = V_z \qquad (1.4)$$

In voltage feedback amplifiers (VFA), dynamic performance is limited by the gain-bandwidth product and the slew rate. Current feedback amplifier (CFA) uses a circuit topology that emphasizes current-mode operation, which is inherently much faster than voltage-mode operation because it is less prone to the effect of stray node-capacitances. When fabricated using high-speed complementary bipolar processes, CFAs can be orders of magnitude faster than VFAs. With CFAs, the amplifier gain may be controlled independently of bandwidth. This constitutes the major advantages of CFAs over conventional VFA topologies.

Limitations of CFAs include poorer input offset voltage and input bias current characteristics. Additionally, the DC loop gains are generally smaller by about three decimal orders of magnitude. Given their substantially greater bandwidths, they also tend to be noisier. CFA circuits must never include a direct capacitance between the output and inverting input pins as this often leads to oscillation. CFAs are ideally suited to very high speed applications with moderate accuracy requirements.

1.3.3 Current Differencing Buffered Amplifier (CDBA)

CDBA, current differencing buffered amplifier, is a multi-terminal active component with two inputs and two outputs. Its block diagram can be seen from Fig 1.3. It is derived from a current feedback amplifier (CFA).

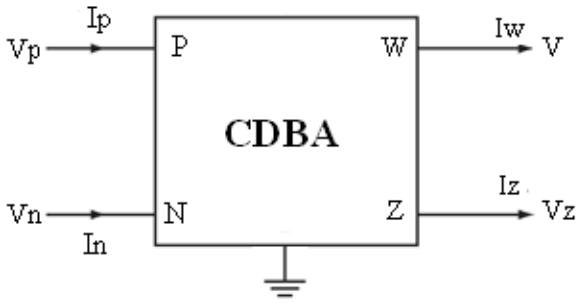

Fig. 1.3: Block Diagram for CDBA.

The characteristic equation of this element can be given as:

$$V_P = V_N = 0 \qquad (1.5)$$

$$I_Z = I_P - I_N \qquad (1.6)$$

$$V_W = V_Z \qquad (1.7)$$

Here, current through z-terminal follows the difference of the currents through p-terminal and n-terminal. Input terminals p and n are internally grounded. The difference of the input currents are converted into the output voltage V_W, therefore CDBA element can be considered as a special type of current feedback amplifier with differential current input and grounded 'y' input.

The CDBA is simple for the implementation, free from parasitic capacitances, able to operate in the frequency range of more than hundreds of MHz (even GHz), and suitable for current mode operation while, it also provides a voltage output. Several voltage and current mode continuous-time filters, oscillators, analog multipliers, inductance simulators and a PID controller have been developed using this active element.

The CDBA offers several advantageous features viz., high slew rate, improved bandwidth, and accurate port tracking characteristics when configured with a pair of matched current feedback amplifier (AD-844-CFA) devices which leads to extremely low active circuit sensitivity.

1.3.4 Current Differencing Trans-conductance Amplifier (CDTA)

CDTA (Current Differencing Trans-conductance Amplifier) is an analog active element which was first described by Dr. Biolek. It has difference current inputs *p* and *n*. The difference of these currents flows from terminal *z* into an outside load. The voltage across the *z* terminal is transferred by a trans-conductance *g* to a current that is taken out as a current pair to the *x* terminals. This last element part is the familiar trans-conductance operational amplifier (OTA).

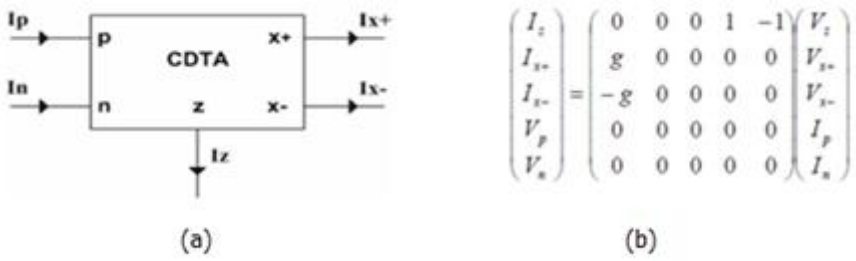

Fig 1.4: (a) Block diagram of CDTA, (b) transfer matrix for CDTA.

The voltage-current equations for CDTA are given in equations *(1.8)* to *(1.11)*

$$V_p = V_n = 0 \qquad (1.8)$$

$$I_z = I_p - I_n \qquad (1.9)$$

$$I_x = g.V_z \qquad (1.10)$$

$$I_x = -g.V_z \qquad (1.11)$$

1.4 Motivation

As the requirement for frequency spectrum is increasing with technology, the proper exploitation of very high frequencies has become the need of hour. This also leads the signal processing field to extend to higher frequencies. To wisely use the resources available the circuit designers are not today satisfied with the traditional design methods based on voltage op-amps. It is well known that a traditional operational amplifier has a bandwidth which is dependent on the closed-loop voltage gain. In order to overcome this disadvantage circuit designers are getting interested in circuits which operate in current mode. A related device, the current feedback operational amplifier (CFOA) is commercially available**.** The circuits using this device employ current-processing techniques due to which they have advantages like improve dynamic speed capability, low power consumption, larger dynamic range, greater linearity etc. A particular feature of these designs is their ability to provide a constant bandwidth virtually independent of gain, that is, there gain-bandwidth product is not constant. In this tradition another two-port general purpose analog building block is invented, termed an operational trans-resistance amplifier (OTRA) [9]. In terms of transmission properties it is very much similar to CFOA, but it has two low-impedance inputs and one low-impedance output. The output voltage of this device is dependent on the current signal given to its input.

Being a member of current mode processing blocks' family, it also inherits various advantages of current mode signalling.

1.5 Operational Trans-Resistance Amplifier's Introduction

The output voltage of OTRA device is dependent on the current signal given to its input and the dependency can be shown as the transfer matrix shown in Fig 1.5.

$$\begin{bmatrix} V_+ \\ V_- \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_+ \\ I_- \\ I_o \end{bmatrix}$$

Fig 1.5: Transfer matrix for an OTRA.

Where R_m represents the trans-resistance gain of the OTRA.

It can be predicted from the above matrix that both the inputs are internally grounded and hence voltage at both the input terminals (V_+ and V_-) is zero leading to a circuit that is insensitive to stray capacitances [10]. Also the output is a voltage signal represented as V_0 which is the difference of current at the two input terminals multiplied by the trans-resistance gain (R_m) [11].

$$V_0 = R_m(I_+ - I_-) \qquad (1.12)$$

Ideally the trans-resistance gain (R_m) approaches infinity, and applying external negative feedback will force the two input currents, I_+ and I_- , to be equal.

The block diagram of an OTRA is shown as in Fig 1.6.

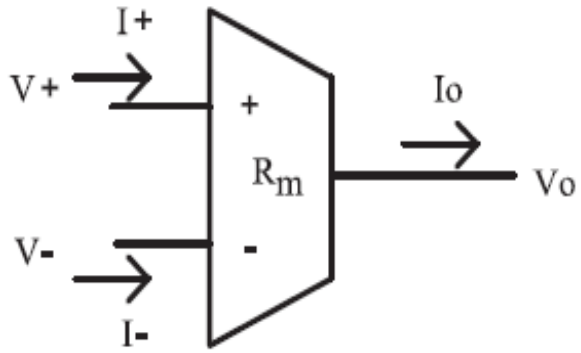

Fig 1.6: Block diagram of an OTRA.

It is worth noting that the OTRA is sometimes termed as Norton's amplifier or current differencing amplifier.

Like operational amplifier there are two configurations possible for OTRA namely Inverting configuration and Non-Inverting configuration [9]. The inverting configuration is as shown in Fig 1.7.

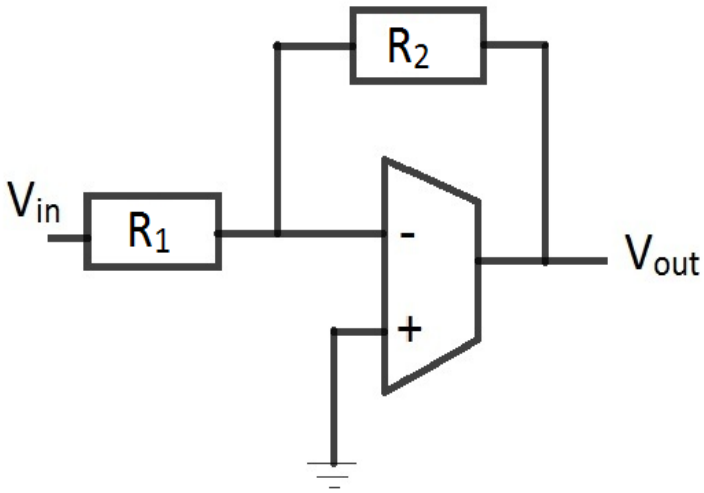

Fig 1.7: OTRA in inverting configuration.

Gain in inverting configuration is given as:

$$\frac{V_0}{V_{in}} = -\frac{R_2}{R_1}$$

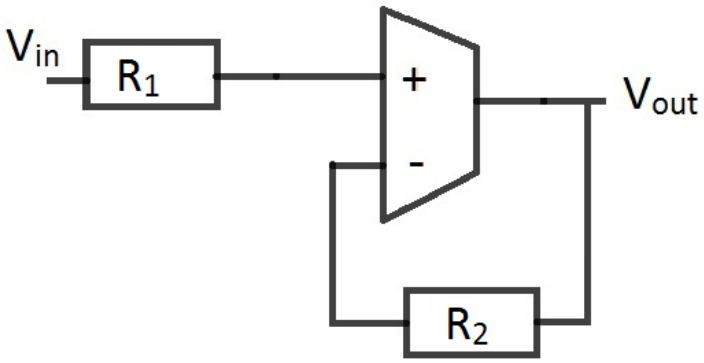

Fig 1.8: OTRA in non-inverting configuration.

Gain in non-inverting configuration as shown in Fig 1.8 can be given as:

$$\frac{V_0}{V_{in}} = \frac{R_2}{R_1}$$

It needs to be noted here that the gain in both of these configurations of OTRA is same in magnitude (which is the ratio of feedback impedance to input impedance) but opposite in sign.

1.6 Organization of this thesis

Chapter 2: It gives a review about literature of the OTRA. It includes various topologies of OTRA realized along with various applications of OTRA including filter applications, oscillators and multivibrators designed using OTRA.

Chapter 3: In this chapter, two topologies of OTRA are synthesis and their results are shown. One of the designs is CMOS based while other is CFOA IC AD844 based.

Chapter 4: Some of the OTRA based applications given in chapter 2 are synthesized in this chapter and their PSPICE simulated results are shown.

Chapter 5: OTRA based Inverse filters are designed in this chapter. Two topologies for the designing of OTRA based inverse filters are proposed and their PSPICE based simulation results are shown.

Chapter 6: In this section conclusion of the thesis work and future scope of the work are presented.

CHAPTER 2

LITERATURE SURVEY

2.1 Introduction

Since OTRA was first introduced by H. Tsao, C. Chen's [9] in 1992 various new OTRA circuits have been designed. Besides that due to its various advantages like non-constant gain-bandwidth product, high slew rate, low parasitic effects etc. OTRA is becoming popular and a large number of analog applications are designed using OTRA. In this chapter various realization methods of OTRA are discussed. Also an overview of OTRA's different applications is given.

2.2 Realization of OTRA

Looking at the advantages of current mode building blocks, a large number of circuit designers are now using current mode devices for circuit implementation. Traditionally, most analog signal processing operations have been accomplished employing the voltage as the signal variable. In order to maintain compatibility with existing voltage processing circuits, it is necessary to convert the input and output signals of a current-mode signal processor to voltage using trans-conductors. This leads to increasing both the chip area and power dissipation [11-13]. The OTRA is commercially available from several manufacturers under the name current differencing or Norton amplifier, but it has not gained much attention. The disadvantage of these commercial realizations is that they do not provide internal ground [14] at the input port which leads to limited functionality of the OTRA. Also they allow the input current to flow in one direction only which forces the use of external dc bias current leading to complex and unattractive designs. In recent years, several high-performance CMOS OTRA realizations have been presented due to which there is a growing interest of the designers in the OTRA-based analog signal processing and non-linear circuits.

Various CMOS OTRA realizations available in literature are briefly described in following sections.

2.2.1 Chen, H. Tsao, C. Chen's Operational transresistance amplifier [9]

The OTRA design first presented by Chen, H. Tsao, C. Chen [9], and their proposed circuit is shown in Fig 2.1

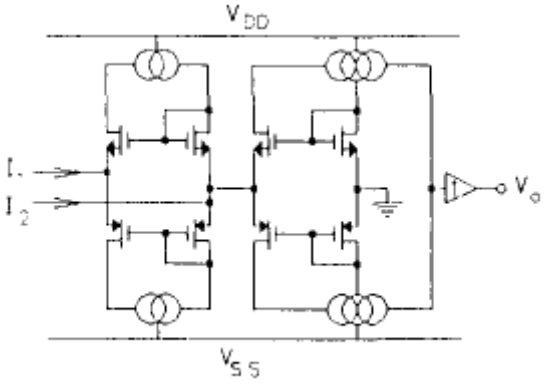

Fig 2.1: The circuit representation of Chen, H. Tsao, C. Chen's OTRA [9].

All simple current mirrors as shown in Fig 2.1 provide a bias current I are implemented using CMOS transistors. Considering the their channel length modulation factor being "λ" and transconductance parameter "β" of the PMOS transistors are equal to those of the NMOS transistors, then the transresistance R_m, can be expressed as:

$$R_m = \frac{1}{2\lambda . I}$$

If all the current mirrors used are cascade current mirrors then the value of R_m can be modified as:

$$R_m = \frac{(0.5\beta . I)^{0.5}}{(\lambda . I)^2}$$

As the value of R_m is very high, its value can be taken as infinity for all practical uses.

2.2.2 K.N. Salama, A.M. Soliman's OTRA proposed in [12]

The OTRA design proposed by K. N. Salama and A. M. Soliman [12] is shown in Fig 2.2 and is based on the cascaded connection of the modified differential current conveyor (MDCC) [8] and a common source amplifier. The common source amplifier was used to provide high

gain stage while MDCC provides the current differencing operation. For ideal operation, the trans-resistance gain approaches infinity and negative feedback forces the two input currents to be equal. Practically, the trans-resistance gain is finite and its effect was considered. Also, the frequency limitations associated with the practical OTRA was considered.

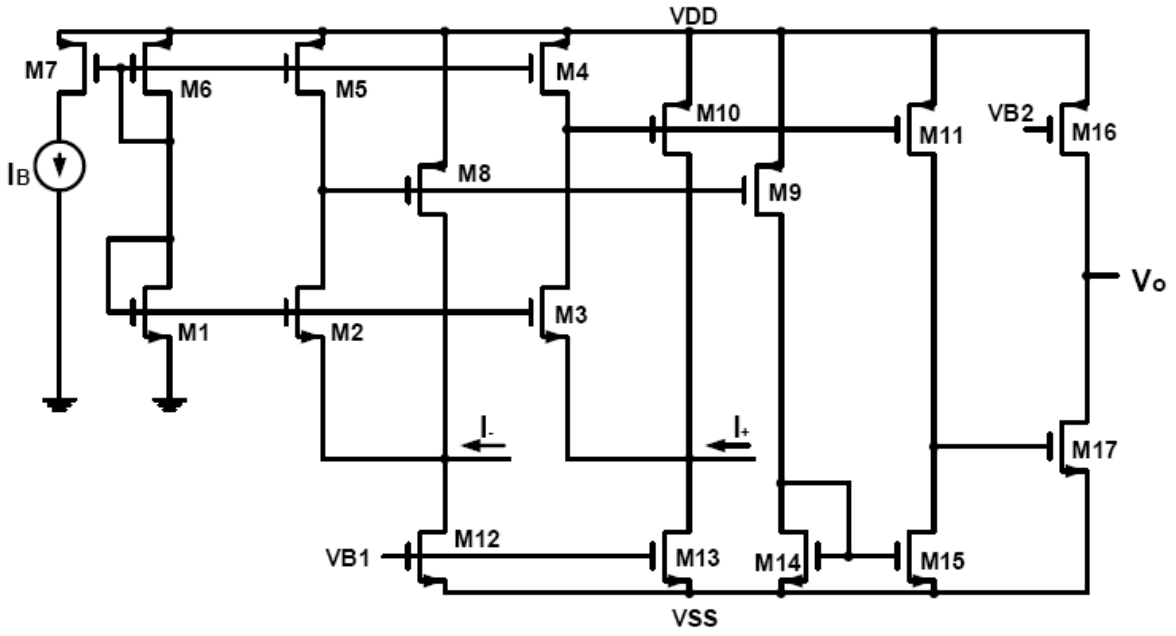

Fig. 2.2: CMOS Realization of Salama and Soliman's OTRA [12].

To explain the operation of this OTRA it is presumed that each of the groups of the transistors (M1-M3), (M4-M7), (M8 and M9), (M10 and M11), (M12 and M13) and (M14 and M15) are matched and all the transistors are operating in the saturation region. The transistors (M4-M7) forms a current mirror which forces equal currents (I_B) in the transistors M1, M2 and M3. Due to this the gate to source voltages of M1, M2 and M3 will become equal and thereby making the two input terminals are virtually grounded. The current differencing operation is provided by the current mirrors formed by the transistor pairs (M4 and M5), (M8 and M9), (M10 and M11) and (M14 and M15) while the (M17) tied in common source amplifier configuration provides the high gain.

2.2.3 Current Tunable CMOS Operational Transresistance Amplifier [15]

Yet another OTRA design consisting of R_m cell, common source negative feedback and the output driver circuit is presented in [15] and is shown in Fig 2.3. The negative feedback and output driver circuits reduce the input and output impedances of the circuit. The voltage buffer is uses for the output driver circuit. The circuit has nearly constant gain-bandwidth

product. The feedback network particularly increases bandwidth and enhances the linearity of the transresistance amplifier.

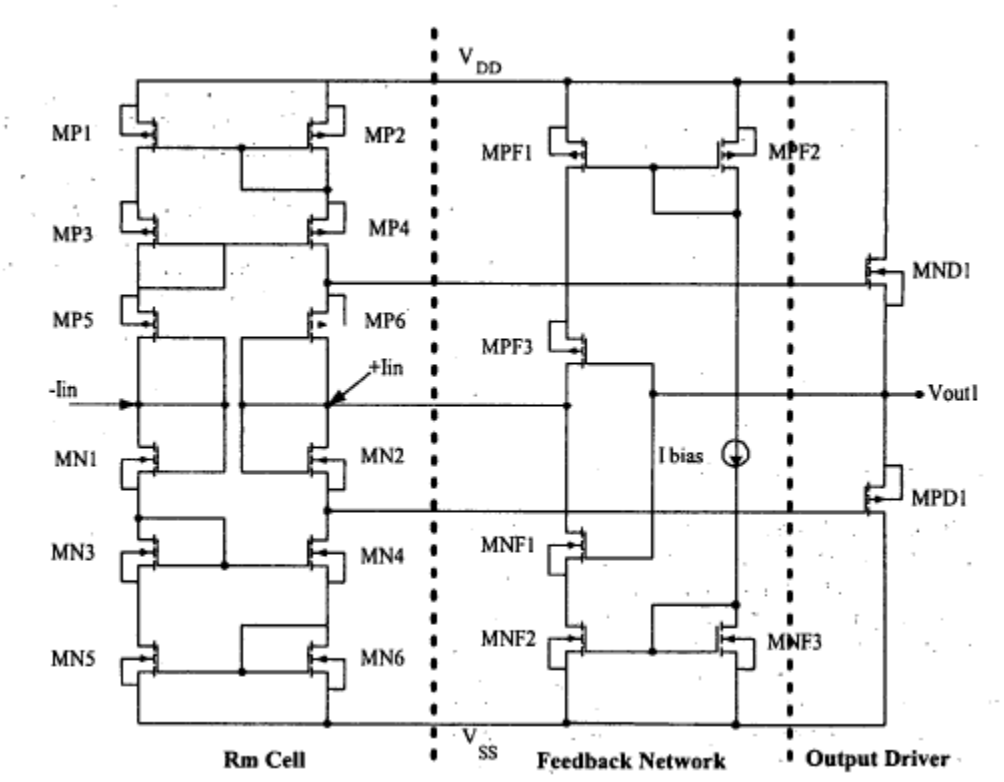

Fig 2.3: Circuit of current tunable CMOS OTRA [15].

As shown in Fig. 2.3, 6 PMOS transistors are cascaded with 6 NMOS transistors. MP1-MP4 are connected to form a Wilson current mirror. MP5 and MP6 are connected to this current mirror and their drains act as the input terminals for the OTRA. The NMOS transistors MN1-MN6 are connected in symmetry to their PMOS counterparts. The drain of MP4 and MN4 act as output terminals for the OTRA.

2.2.4 Hassan Mostafa, Ahmed M. Soliman's OTRA [13]

This design of OTRA was proposed by Mostafa and Soliman in 2006. This design was also based upon based the cascaded connection of the modified differential current conveyor (MDCC) and a common source amplifier. This OTRA as shown in Fig 2.4 has smaller number of current mirrors than Salama and Soliman OTRA [12] which reduces the transistor mirror mismatch effect and also increases the frequency capabilities. Moreover, this OTRA uses smaller number of transistors (14) which reduces the power dissipation. Also the offset

current in this OTRA is less as compared to Salama and Soliman's OTRA, and it exhibits more DC open loop trans-resistance gain and better gain bandwidth product than Salama and Soliman's OTRA.

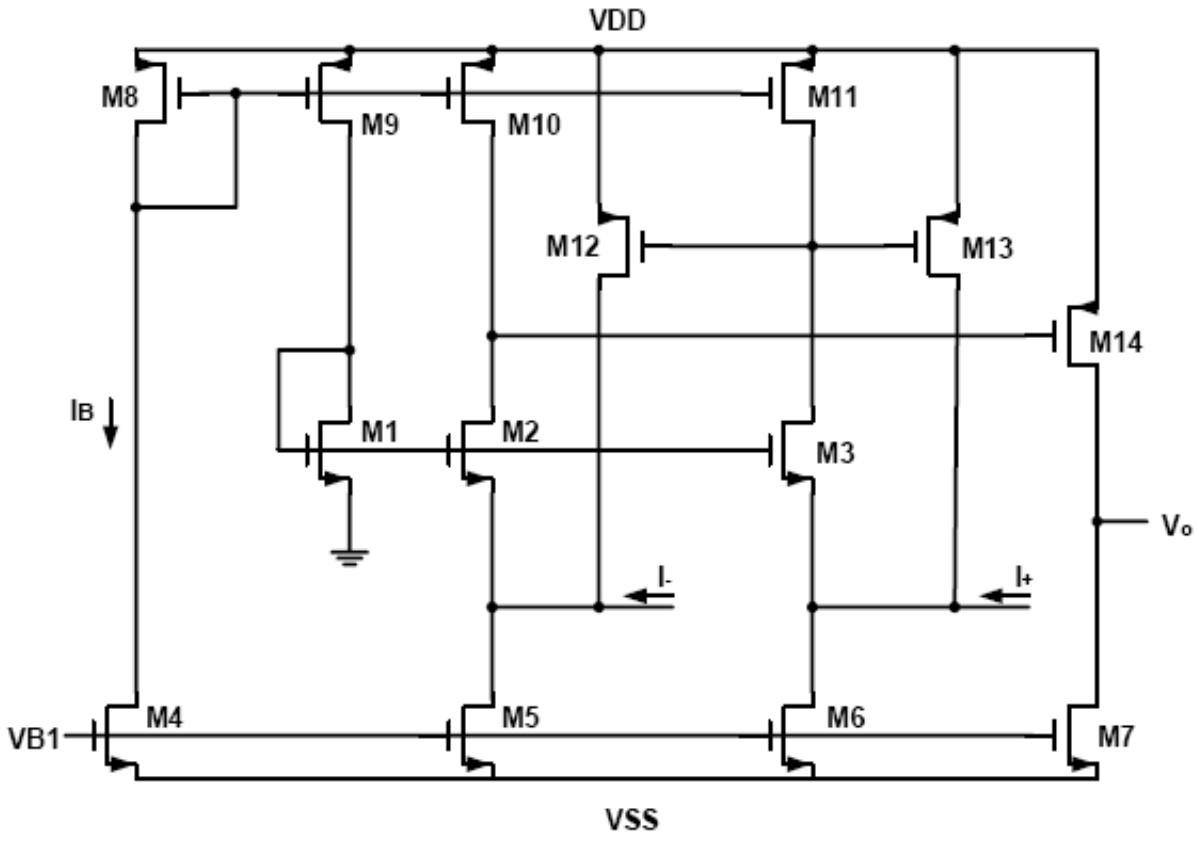

Fig 2.4: Hassan Mostafa and Ahmed M. Soliman's OTRA [13].

To explain the working of circuit shown in Fig 2.4 it is assumed that the transistors (M1-M3), (M5-M6), (M8-M11) and (M12-M13) are matched and that all the transistors in the circuit are working in saturation region. The current mirrors formed by, (M8-M11) provide equal currents to transistors (M1-M3). This in turn makes gate-source voltage of (M1-M3) equal by virtue of which both input terminals are internally grounded. The current differencing operation is provided by transistors pairs (M10-M11) and (M12-M13) while (M14) acts as the common source amplifier to provide high gain.

2.2.5 Abdelrahman K. Kafrawy, Ahmed M. Soliman' OTRA I [16]

The OTRA proposed in [16] is shown in Fig 2.5. It is based on the same input stage as that of OTRA in [13] and a differential gain stage is used instead of a common source amplifier. A

compensation circuit is used to compensate the difference between the drain voltages of the transistors M2 and M3. The transistors Mx4, Mx5, Mx6 and Mx7 represent the gain stage that produces the non inverting output and the transistors MC1-MC5 represent the compensation circuit.

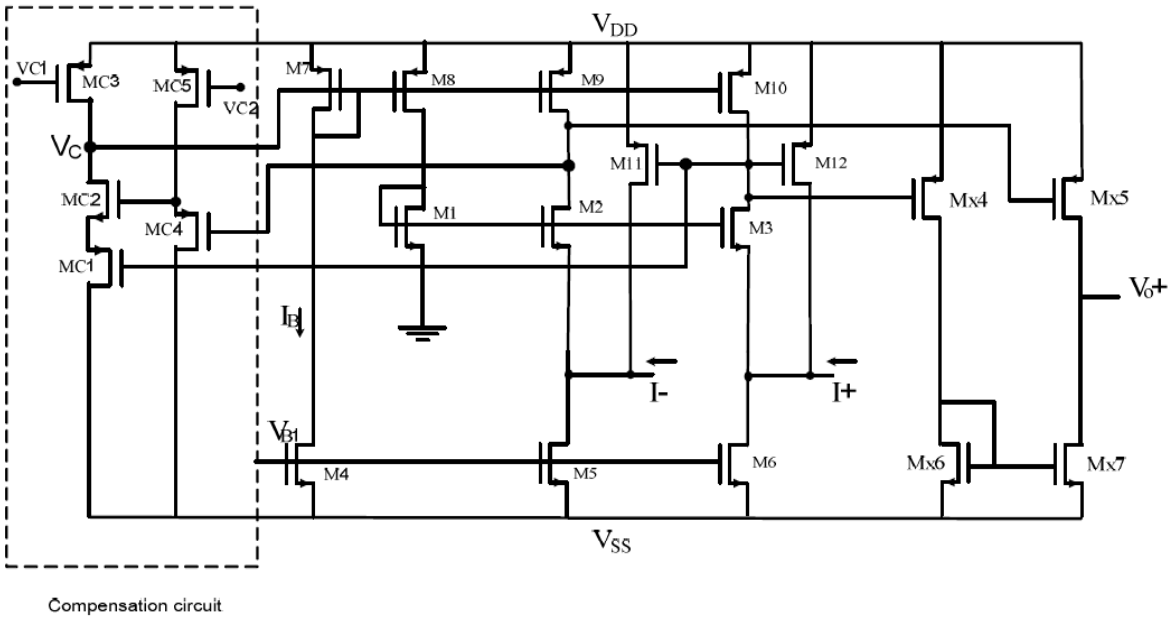

Fig 2.5: Abdelrahman K. Kafrawy and Ahmed M. Soliman's OTRA I [16].

2.2.6 Abdelrahman K. Kafrawy and Ahmed M. Soliman's OTRA II [17]

The CMOS realization of the low power wide band OTRA proposed in [17] is shown in Fig 2.6. It is based on the cascaded connection of the modified differential current conveyor (MDCC) and a common source amplifier. As compared to Hassan OTRA in this circuit only 12 transistors were used and as result there is less power dissipation. The major difference from OTRA in [13] is that instead of using single common source amplifier as gains stage it uses a differential gain stage. Also the Vb1 was reduced to -0.25v which give better Dc response than Hassan OTRA [13].

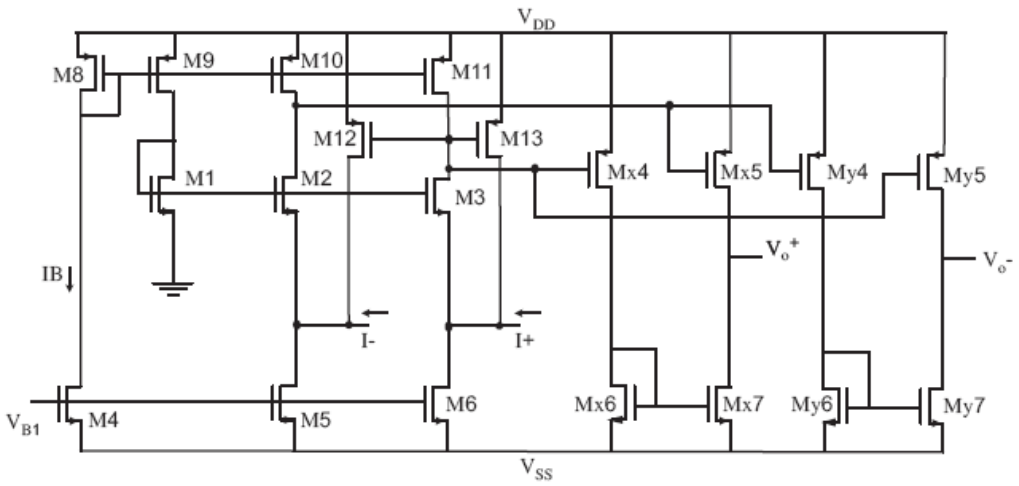

Fig 2.6: Abdelrahman K. Kafrawy and Ahmed M. Soliman's OTRA II [17].

2.2.7 CMOS Rm-variable OTRA topology [18]

The R_m-variable OTRA topology proposed in [18] has capability to operate at very low voltage power supplies. The proposed CMOS Rm-variable OTRA is illustrated in Fig 2.7. This circuitry includes a power-down signal generator stage of the OTRA and the power-down transistors. OTRA is functional when the input "EN" is at the VSS voltage level. When the input "EN" is at the VDD voltage level, all the system is in the power-down mode and the output "VO" forms a high impedance output.

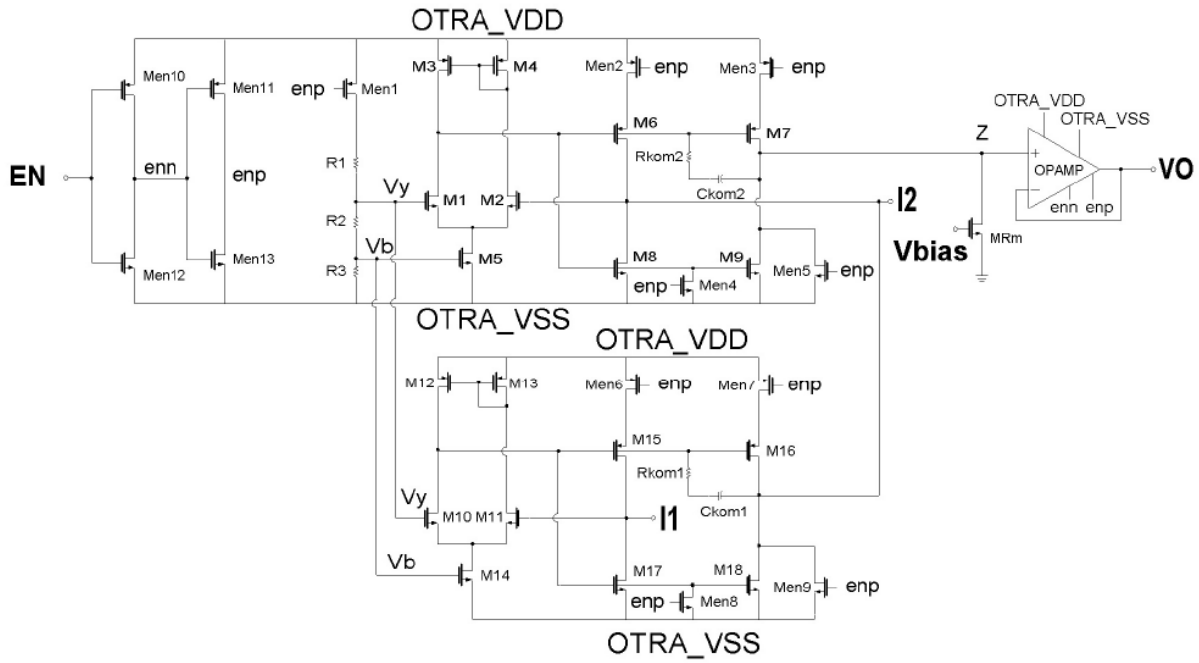

Fig 2.7: CMOS variable-Rm OTRA topology [18].

This OTRA topology is based on the idea of using CCII+ blocks as shown in Fig 2.8. The input currents named as i1 and i2 are applied to the low impedance inputs of the two CCII+. The current difference is mirrored to the "Z" node of the second CCII+. This current forms the unbuffered output voltage. Finally, the non-buffered output voltage over the R_m resistor is applied to a unity-gain buffer composed, designed using an OPAMP, in order to have low output impedance. Two differential amplifiers generated with the NMOS transistors M1 - M4 and M10 – M13 are biased equally with the bias voltage V_y. The current mirror bias voltage V_b is generated in the bias stage. In the input stage, i1 is the positive, i2 is the negative node. The use of Class AB structure in the CCI+ with the transistors M6 – M9 and M15 - M18 makes it possible to operate with very low voltage power supplies. The negative feedbacks in the input nodes generated with the transistors M2, M6 and M11, M15 forms low input impedances. Compensation capacitances, Ckom1, Ckom2 and resistors Rkom1, Rkom2 reduce the phase delay between the input currents i1 and i2, and the transferred current I_z in the CCII+. The mirrored current difference forms the output voltage on the (MR_m) NMOS transistor used as resistor. The resistor value is variable and controlled by the external V_{bias} voltage.

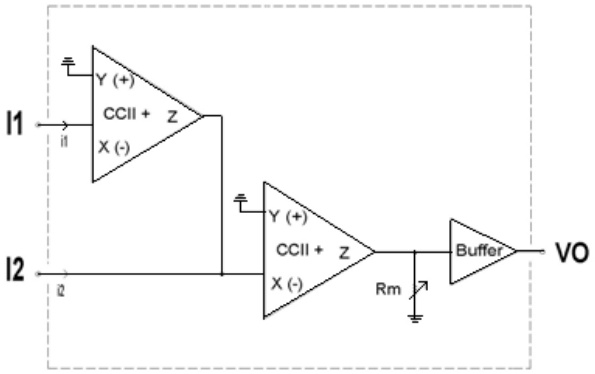

Fig 2.8: CCII+ based variable-Rm OTRA topology [18].

2.2.8 AD844 Based OTRA realization

The AD844 is a high speed monolithic amplifier integrated circuit. It is fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. It combines high bandwidth and very fast large signal response with excellent dc performance. The AD844 can be used in place of traditional op amps. It has current feedback architecture which results in much better ac performance, high linearity and an exceptionally clean pulse response. This type of op amp provides a closed-loop bandwidth which is determined primarily by the feedback resistor and is almost independent of the closed-loop gain. The AD844 is free from

the slew rate limitations inherent in traditional op amps. The OTRA can be designed using AD844 as shown in Fig 2.9 [19]. We require virtual ground at the two input terminals of the OTRA. In AD844AN the inverting input terminal follows the voltage of non-inverting input terminal. In order to achieve virtual ground at two input terminals of OTRA the non-inverting terminals of the AD844ANs have been grounded. Thus a virtual short exists between these two terminals without any external negative feedback path.

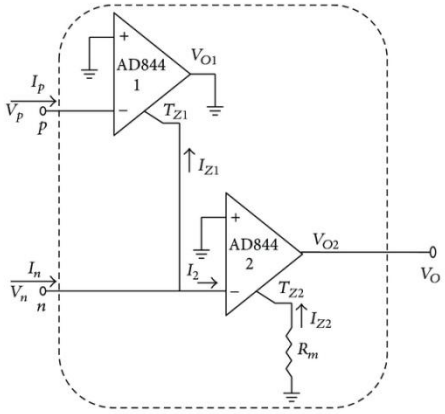

Fig 2.9: CFOA Realization of OTRA using AD844 [19].

2.3 OTRA applications

During the last few decades, the current mode processing has emerged as a useful mean for analog circuits design and has become an alternative to the voltage mode circuits. Since OTRA was first presented in 1992, a large numbers of analog signal processing circuits are developed using OTRA. A literature review of various applications developed with OTRA is presented in this section.

2.3.1 OTRA based filter applications

Various filters applications have been designed using OTRA since it was first realized.

In [20] a Mosfet-C integrator using OTRA is proposed. The proposed integrator is found to be insensitive to the effects of parasitic capacitances and also the chip area required is less because only one capacitor is required for the simulation. The problem of capacitor mismatch has also been eliminated.

References [21] and [22] gave integrator and differentiator designs using OTRA. Using these integrator and differentiator circuits universal biquad filters are designed which were found to

be tuneable by varying the gate voltages of various MOS transistors. A third-order Chebyshev lowpass filter is also designed using the integrator.
A second order differential low pass filter based on Tow-Thomas biquad has been proposed in [23] which works with OTRA as building block at a low voltage of 0.8V

A structurally first order all-pass filter using an OTRA was implemented in [24] which does not require any component matching constraint. This circuit operates in transimpedance-mode and employs only a single OTRA along with a few passive components.
In [25] and [26], a new filter topology is presented which can give first order all pass, second order all pass and notch filters while [27] gives another OTRA based configuration for all-pass filter which can provide both first and second order all pass filter through proper component selection.
Reference [28] Discuss a biquadratic filter design using operational transresistance amplifier. The proposed circuit was designed using MOS-C design which makes the circuit electronically tunable.

A new design for band pass filter is proposed in [29] which as reported has high value of quality factor and also its quality factor can be governed by a single resistance.

In [30] a multi-input single-output (MISO) type voltage mode biquadratic filter using a single Operational transresistance amplifier as the active element is given, which is able to realizes all the five filter functions, i.e., low pass filter, high pass filter, band pass filter, notch filter and all pass filter, without changing the circuit topology. The circuit has the advantage of low output resistance hence can easily be cascaded without addition of buffer element.

Reference [31] presents voltage-mode high-order linear transformation MOSFET-C active filters OTRA with only virtual grounded capacitors and MOSFET resistor circuits (MRSs). The design principal is supported by a third-order Chebychev lowpass filter design. The filters designed are having reduced parasitic effects.

OTRA based current mode MOSFET-C filters using linear transformation principal are presented in [32].

Second order analog filter designs using single OTRA along with their MOS-C realization are presented in [33].

In [34], a circuit design configuration for the realization of voltage-mode second-order filters using an OTRA as the active element is presented. This topology can be used to synthesize highpass, lowpass, allpass, bandpass and notch filtering functions. The presented filters parameters can be electronically tuned and are suitable for MOS-C implementation.

Reference [35] presents the designing of fourth order filter structures using the OTRA. Along with that in [35] OTRA based second order low pass and high pass filter are designed and verified and fourth order notch filter and band pass filter topologies are obtained.
Tow-Thomas biquad circuit topology using OTRA is presented in [12]. As the functionality of Tow-Thomas biquad depends on addition of current which is done in conventional operational circuits by introducing a virtual ground at the input terminal. Three operational amplifiers are required in the conventional design on the other hand; in OTRA as already there exists internally grounded input terminals hence Tow-Thomas biquad can be implemented using only two OTRA.

Along with their Tow-Thomas biquad design, Salama and Soliman in [12] also presented the Kerwin–Huelsman–Newcomb biquad circuit. The classical KHN biquad [36] was not able to produce all the possible combination polarities of the highpass, bandpass and lowpass responses. This limitation is removed when OTRA was used to design the Kerwin–Huelsman–Newcomb biquad circuit. The gain, quality factor and operating frequency can be orthogonally tuned.

OTRA based second order universal filter configurations is also presented by Salama and Soliman in [12]. However, the universal filter derived from that filter configuration have a drawback that the circuit employs 3 capacitors, to obtain the required second-order transfer functions, which means that the filters is not canonical in the number of capacitors used. As we know that the capacitors require a large silicon area on integrated circuits, hence the resulting filters would not be economical for on-chip applications. In [37] an OTRA-based Fleischer-Tow-biquad is presented for the realization of second-order filters transfer functions, which requires only 2 capacitors. Therefore, the filters realized using topology of [37] are canonical with respect to the number of capacitors used and hence will require lesser silicon area on the integrated chip. Furthermore, the quality factor and the resonant frequency of the filters are mutually orthogonally controllable. All of the resistors used in the filters were realized by MOS transistors.

Reference [38] gives single input multiple output structure of a first order multi function filter topology using three OTRA. This topology provides Low pass, high pass and all pass filter function simultaneously.

An OTRA based third order universal voltage mode filter is proposed in [39]. The proposed circuits is designed using a single OTRA and is able to produce all five filter functions as low pass, high pass, band pass, notch and all pass filters. All the capacitances used are either grounded or virtually grounded which makes the design more suitable for monolithic IC implementations. The design is also able to control the effect of finite transimpedence gain by self compensation technique. The circuit requires a large number of passive components matching.

Reference [40] presents an OTRA based universal biquadratic single input multiple output filter based on [12]. The proposed structure is able to deliver all standard filter structures namely band pass filter, high pass filter, low pass filter, notch filter and all pass filter simultaneously. The structure has advantage over previously reported structures that it does not require change in component or removal of component for realizing various filter responses. However this structure requires matching conditions on component values to be fulfilled. This structure provides orthogonal controllability of operating frequency, quality factor and gain.

In [41], a biquadratic filter configuration using a single OTRA is presented which is based on Sallen Key approach. The circuit designed is able to realize the lowpass (LP), highpass (HP), and bandpass (BP) filter functions with independent tuning of angular frequency and quality factor by appropriate admittance selection. It provides the possibility of high Q realization with moderate component spread.

Another voltage mode OTRA based multifunction biquadratic filter is proposed in [42] having advantage of not having any capacitance in feedback network and only having capacitances either grounded or virtually grounded. The circuit as shown in employing three OTRAs is able to provide low pass, high pass and band pass responses.

2.3.2 OTRA based Multivibrators

In [19], two novel square wave generators circuits are proposed. These circuits are made up of a single OTRA with few external passive devices. The square wave generator is shown in Fig 2.10 (a) have an OTRA along with two resisters and one capacitor. The first circuit provides a square wave output with fixed on duty cycle and the other circuit shown in Fig 2.10 (b) is able to provide square wave with variable duty cycle.

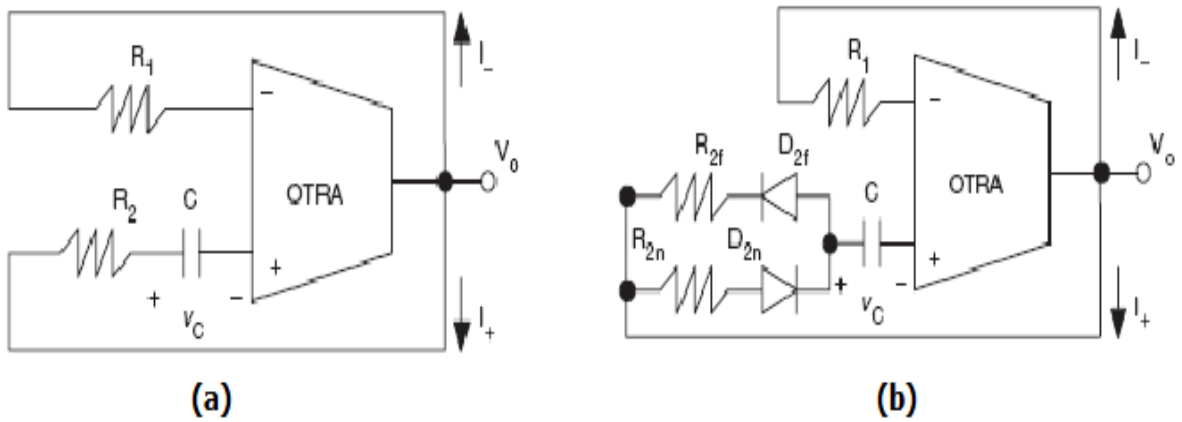

Fig 2.10: OTRA based Square wave generators presented in [19].

(b) Fixed duty cycle. (b) Variable duty cycle.

Reference [43] presents three topologies for monostable multivibrators, the first circuit is triggered via a rising edge signal to produce pulse. The width of this output pulse is predetermined and cannot be changed. The second circuit is designed to operate with a negative triggering signal. The third circuit is comparatively complex in construction having one OTRA along with one capacitance, three resistance and three diodes. It has the advantage of having both triggering modes along with tunable recovery time.

The recovery time of two monostable multivibrators circuits explained in [43] is dependent on pulse width of output. This shortcoming is overcome in a current mode current mode monostable multivibrator proposed in [44] which uses an analog switch in place of the clamping diode of the design proposed in [43]. The presented circuit in Fig 2.11 can be operated under both positive and negative triggering modes

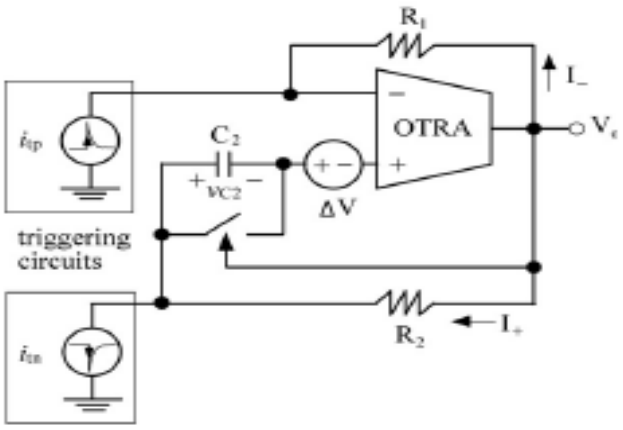

Fig 2.11: Current-mode monostable multivibrator [44].

A number of bistable multivibrator configurations are explained in [45].

The first proposed general configuration is operated with a positive feedback network from the output terminal to the non-inverting input of the OTRA. The positive feedback network can be made of passive components. Because of the positive feedback network, the OTRA saturates with its output voltage either at the positive saturation level or at the negative saturation level and hence generating bistable multivibrator output. In second proposed configuration, the diode resistor topology is used to provide the asymmetrical threshold voltages.

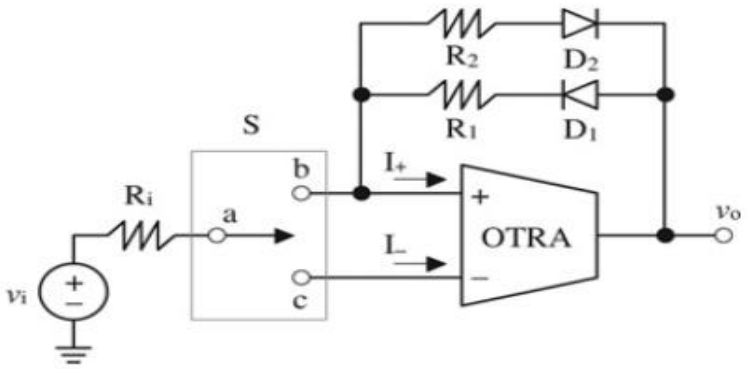

Fig 2.12: Diode-resistor topology of bistable multivibrator [45].

This configuration makes the threshold voltages of different levels and also different polarities. As some of the applications of bistable multivibrator require threshold voltages of same polarities, such bistable multivibrators output can be generated by using an external reference voltage through another SPDT switch as shown in Fig 2.13. A multiple-output

general configuration, as shown in Fig 2.14 is presented which can be used for extended applications.

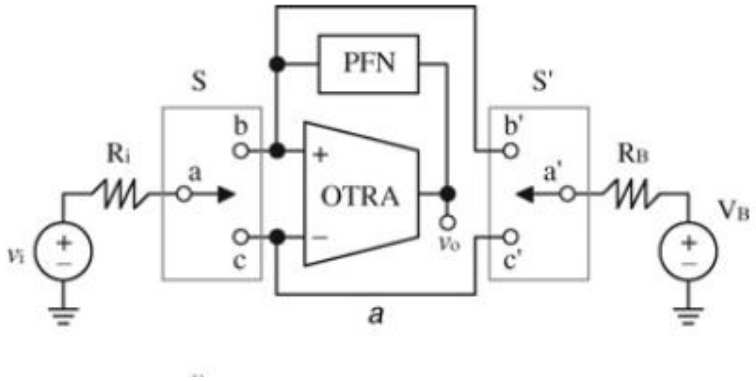

Fig 2.13: Bistable multivibrator with external reference voltages [45].

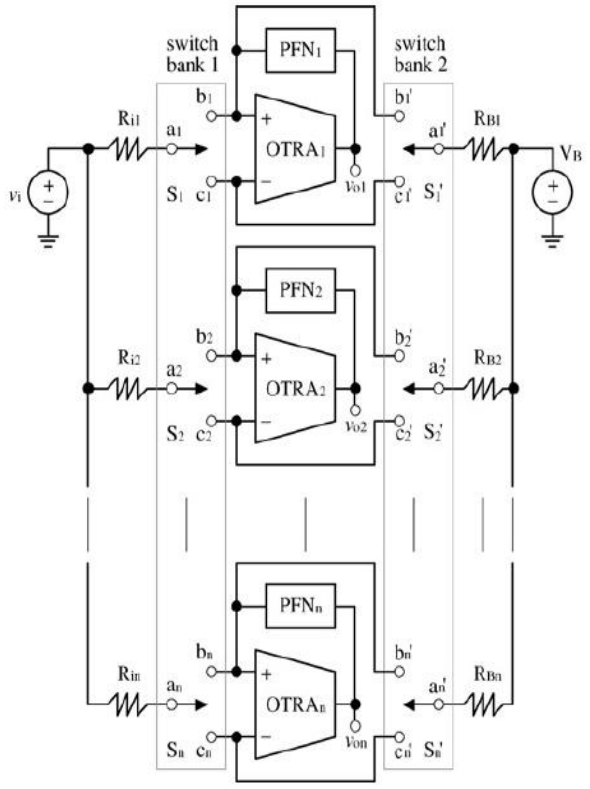

Fig 2.14: Multiple-output configuration of bistable multivibrator with external reference voltage [45].

2.3.3 OTRA based oscillator applications

An oscillator is an electronic circuit which is used to generate periodically oscillating electronics signals generally a sine wave, cosine wave or a square wave. Oscillators are used in Computers, radio transmitters, television transmitters, watches, metal detectors etc.

A large number of sinusoidal oscillators designed using operational amplifier (op amp) are widely used. But due to the finite gain bandwidth product of the op amp their high frequency operation is limited. To overcome this problem, oscillators can be designed using current mode active blocks. A brief review of OTRA based oscillators available in literature in presented below.

Reference [46] presents some oscillators circuits using single OTRA as well as two OTRAs. The circuit shown in Fig 2.15 (a) represents an oscillator with just two resistance and two capacitances and hence have minimum number of passive components among all three. However in this circuit the condition of oscillation and the frequency of oscillation cannot be independently controlled.

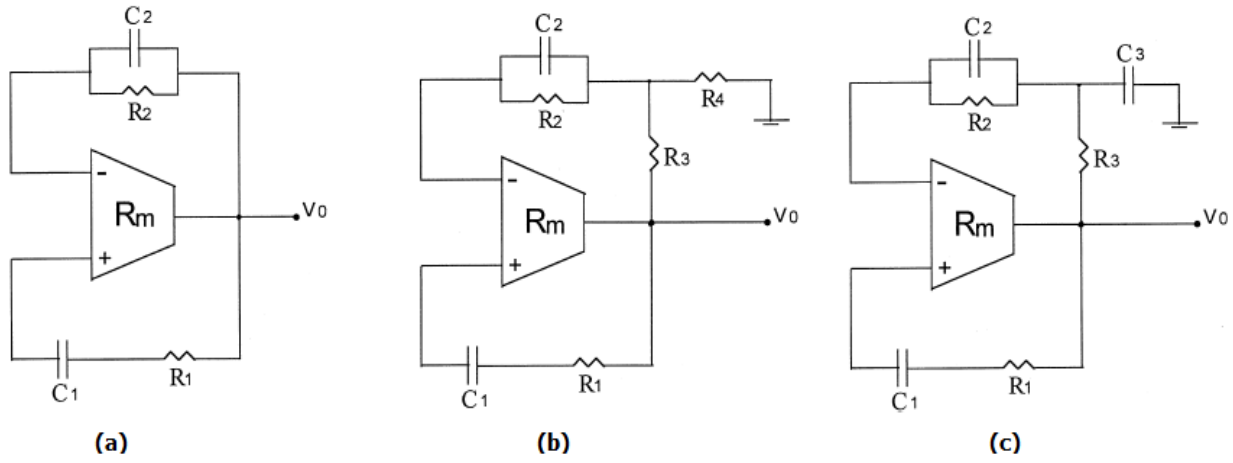

Fig 2.15: Single OTRA Oscillator structures [46].

The circuit shown in Fig 2.15 (b) is having two extra resistances by virtue of which this circuit achieves independent control of frequency and conditions of oscillations. The circuit shown in Fig 2.15 (c) is yet another design which supports tuning of frequency of operation and condition of oscillations. Reference [46] also presents three structures for oscillators employing two OTRAs which include an oscillator structure based on the novel grounded inductor. The frequency of operation and condition of oscillations for all of them can be independently tuned.

A single resistance controlled sinusoidal oscillator design is proposed in [47]. This circuit includes single OTRA along with three resistors and two capacitors, which are the minimum numbers for the single resistance controlled oscillator realization. The circuit provide

independent control of oscillation frequency without disturbing oscillation condition by changing the value a resistor.

In [48] three circuits of multiphase sinusoidal Oscillator designed using OTRA are proposed. The first circuit is able to produce n-odd phased oscillations having equal amplitude by utilizing n OTRAs. The circuit is simple in its structure and gives good frequency performance but is having disadvantage of the lack of tunability. In second structure *(n+1)* OTRAs are used to produce *n* odd or even phase oscillations which are equally spaced in phase. Though the circuit lacks tunability but it have a simple Automatic Gain Control circuitry. The third circuit employs a single phase single-resistance-controlled (SRCO) sinusoidal oscillator circuit constructed using a single OTRA, which drives a subsequent phase shifter network. The phase shifter circuit gives *n*+1oscillations by using n-OTRA-based phase shifter blocks.

Another OTRA based sinusoidal oscillator configuration is presented in [49]. The circuit utilizes two OTRAs along with three capacitances and three resistances. The circuit provides non interactive control on frequency of oscillation and condition of oscillation.

Two voltage controlled oscillators using OTRAs are presented in [50]. As shown in Fig. 2.16 (a), the circuits consist of two OTRAs, four resistors and one capacitor. The circuit can be seen as two cascaded blocks. OTRA I is used to form a simple integrator, while the OTRA II, R2 and R4 are part of a Schmitt trigger working in the clockwise mode. The circuit given in Fig. 2.16 (b) is a modified version of previously described voltage controlled oscillator in which the Schmitt trigger is connected in the counter clock wise mode while the integrator is connected in the inverted mode. These modifications allow the circuit to give outputs differing in phase as obtained from the previous configuration. These circuits have two limitations. Firstly, the nonlinearity of the output signals with respect to the control voltage and secondly, the non-uniform duty cycle of the output signals which changes with the frequency. The reason behind the non-uniform duty cycle is the increasing difference between TON and TOFF. These limitations can be overcome by using another circuit shown in Fig 2.17. This circuit uses an analog SPDT (Single Pole Double Throw) switch in addition to the components used in the previously mentioned circuits. It can also be viewed as two cascaded blocks. The SPDT switch transform the circuitry associated with OTRA I from an inverting integrator to a non-inverting integrator and vice versa. The OTRA II is used as a Schmitt trigger.

Reference [51] presents a third order quadrature oscillator which consists of a second order low pass filter with an integrator in feedback, both constructed from OTRA.

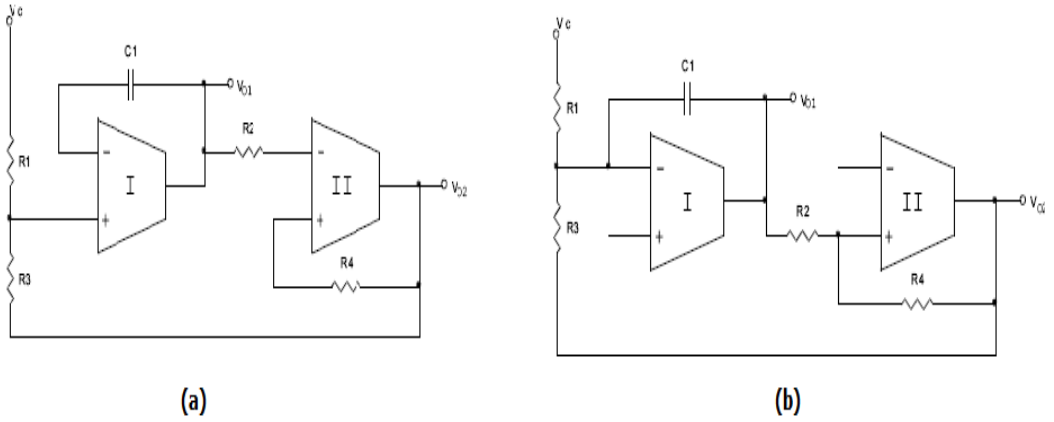

Fig 2.16: The voltage controlled Oscillators I [50].

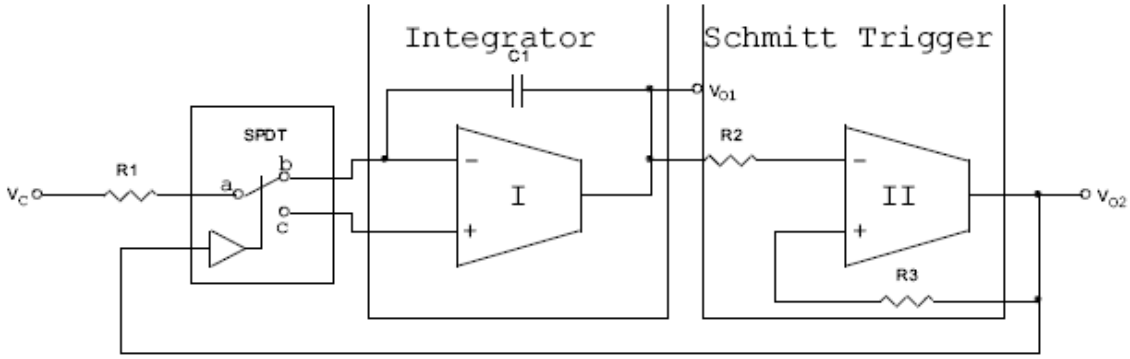

Fig 2.17: The voltage controlled Oscillators II [50].

2.4 Conclusion

This chapter presents an overview of the available literature on OTRA and gives insight into the scope of work for this thesis.

CHAPTER 3

OTRA REALIZATION AND CHARACTERIZATION

3.1 Introduction

Recently, great interest has been devoted to the design of the operational Transresistance amplifiers (OTRA). This interest is mainly because the OTRA being a current mode active block inherits all the advantages of current mode processing such as high slew rate, high bandwidth independent of gain etc. Additionally due to low input impedances the response limitations due to parasitic capacitance are eliminated thereby making circuits useful for high frequency application.

The literature review of all the available OTRA designed (to best of the author's knowledge) has been presented in chapter 2. In this chapter CMOS based Hassan and Soliman's OTRA [13] and CFOA IC-AD844 based OTRA are realized which have been discussed in section 2.2. The A.C. response, D.C. response and the transient response of the OTRAs are shown and on the basis of them some of the properties of OTRAs are calculated and are listed in Table 3.1.

3.2 Hassan and Soliman's OTRA [13]

The CMOS based OTRA design proposed by Hassan and Soliman [13] the schematic design of which is as shown in Fig. 3.1, is simulated as a part of this project. This OTRA design is made up of 14 transistors.

3.2.1 D.C. response

The D.C. response obtained by D.C. sweep of both the input currents is as shown in Fig 3.2. The input current dynamic range is found to be -50 µA to 50 µA.

3.2.2 A.C. response

The A.C. gain response and A.C. phase response of the OTRA are as shown in Fig 3.3 and Fig 3.4. The D.C. gain of the OTRA is 84 dB while its gain-Bandwidth product can be calculated as 0.9 GHz.

3.2.3 Transient response

The Transient response of Hassan and Soliman's OTRA is as shown in Fig 3.5. The transient response is helpful in the calculation of slew rate of OTRA. The slew rate calculated is 2554.433 V/µs.

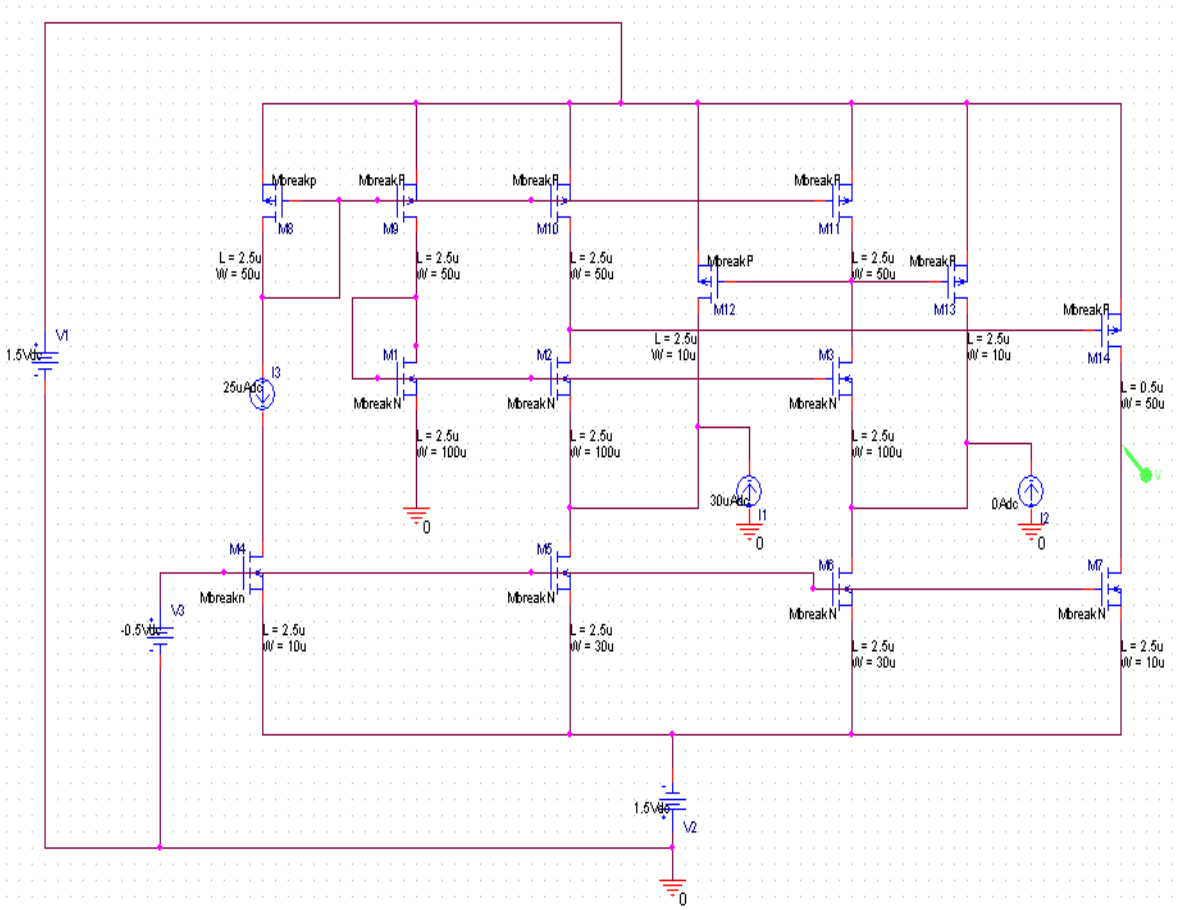

Fig 3.1: Circuit Schematic of Hassan and Soliman's OTRA.

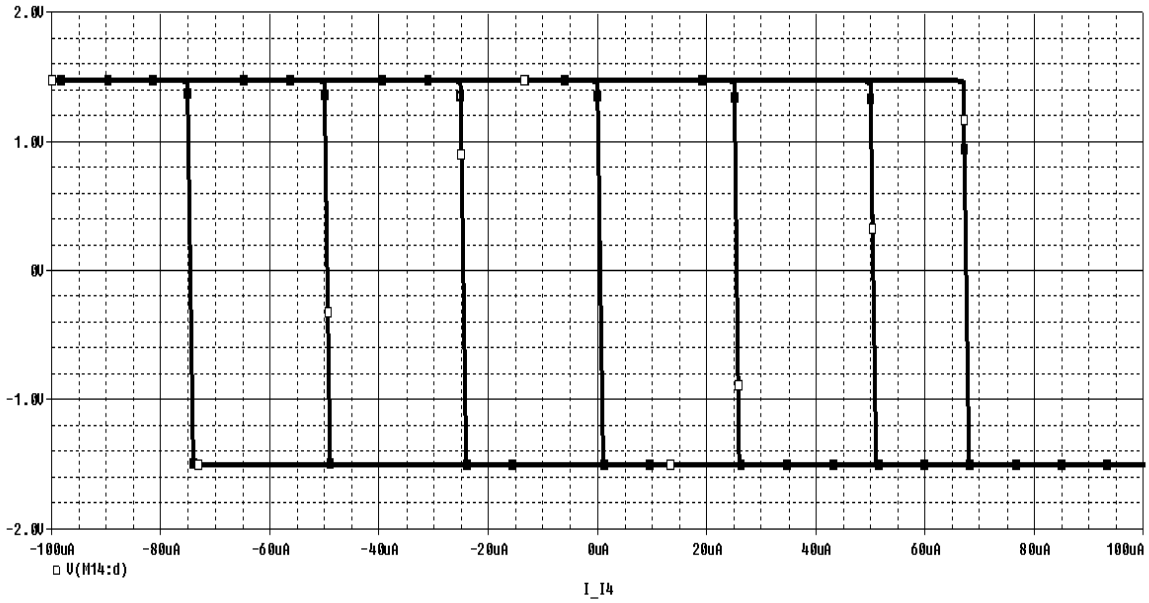

Fig 3.2: D.C. sweep response of Hassan and Soliman's OTRA.

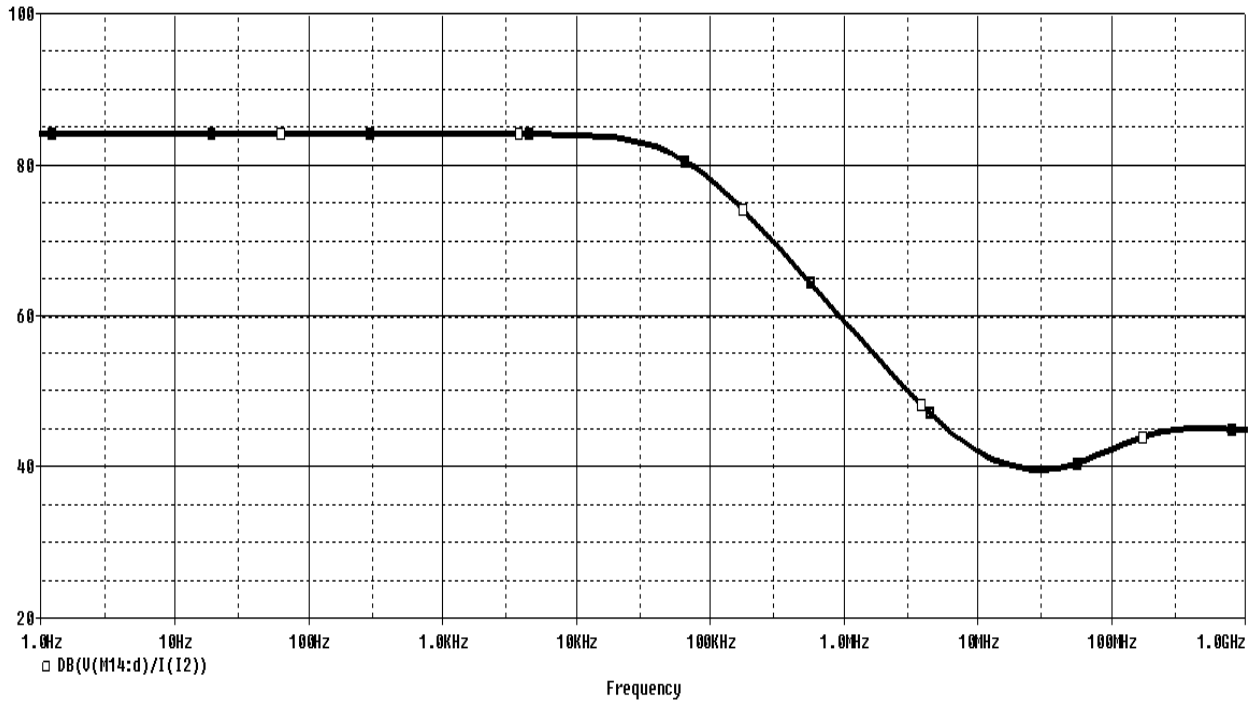

Fig 3.3: A.C. Gain response of Hassan and Soliman's OTRA.

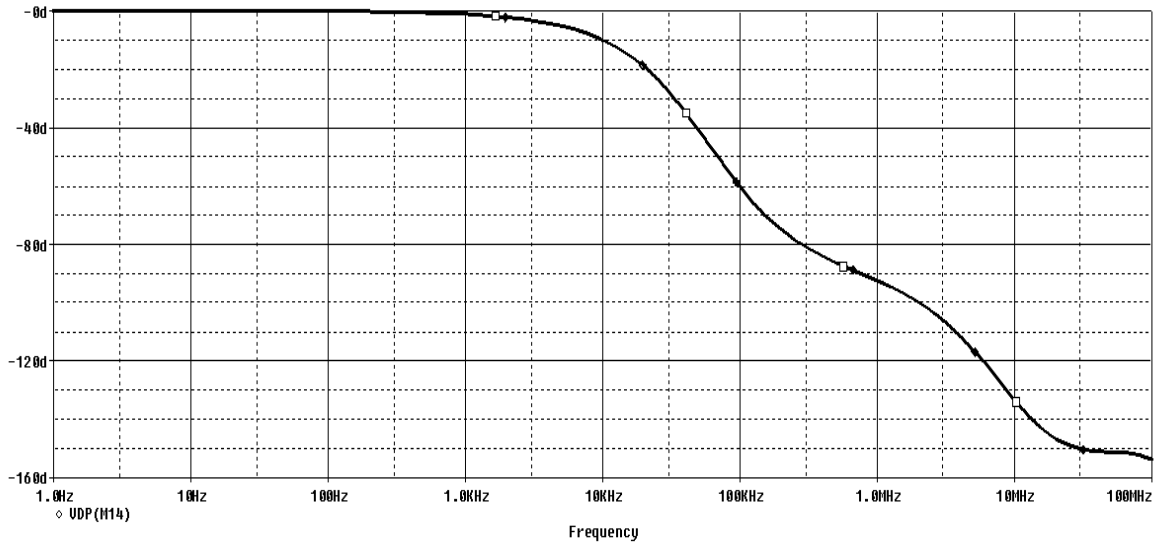

Fig 3.4: A.C. Phase response of Hassan and Soliman's OTRA.

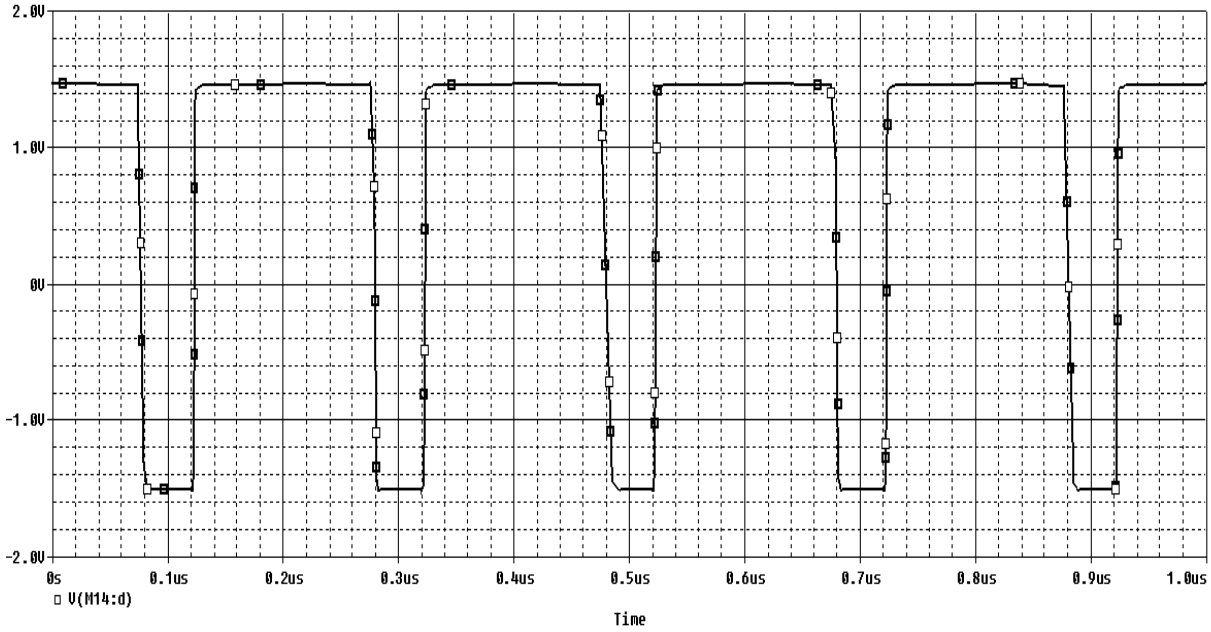

Fig 3.5: Transient response of Hassan and Soliman's OTRA.

The simulations were performed on ORCAD PSPICE simulation tool using 0.5 micron CMOS parameters provided by MOSIS (AGILENT). The DC characteristics of the OTRA is shown in Fig. 3.2 where the current difference $I_p - I_n$ is varied from -100uA to +100 uA. The AC characteristics of the OTRA are shown in Fig. 3.3 and Fig. 3.4 where in both magnitude and phase responses are depicted. The simulations results are found to be in close proximity

with the results shown in [13]. The characteristics of OTRA depicted from these responses are listed in Table 3.1.

3.3 CFOA based OTRA design

An OTRA can also be designed by using two CFOA ICs (AD844) [19], by connecting them as shown in Fig 2.9. The schematic diagram of the circuit is shown in Fig 3.6.

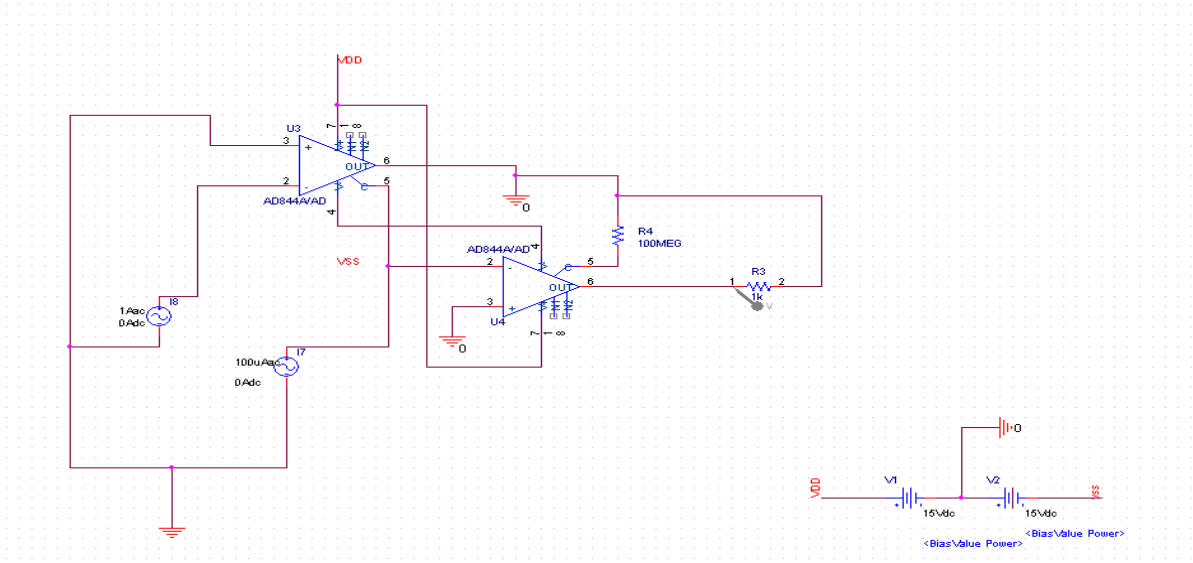

Fig 3.6: Schematic design of CFOA based OTRA design.

3.3.1 D.C. response

The D.C. sweep response of the CFOA based OTRA is obtained by sweeping both the input terminals currents and is shown in Fig 3.7. The D.C. responses conclude that the input current dynamic range of the CFOA based OTRA is -50µA to 50 µA.

3.3.2 The A.C. response

The A.C. gain response and A.C. phase response of the CFOA based OTRA are given in Fig 3.8 and Fig 3.9, from which it can be said that the D.C. gain of simulated OTRA is 130 dB and the gain-bandwidth product is given as 31.63 GHz.

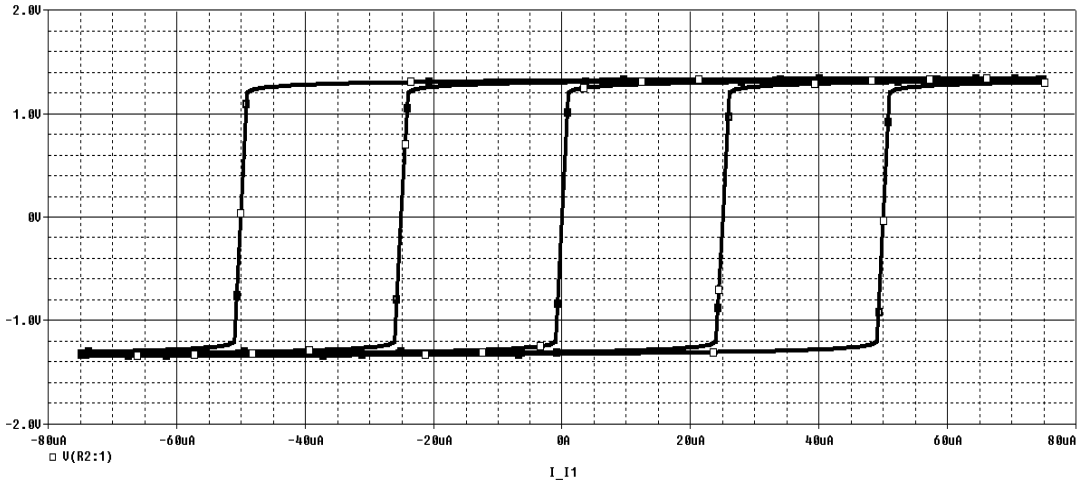

Fig 3.7: D.C. sweep response of CFOA based OTRA.

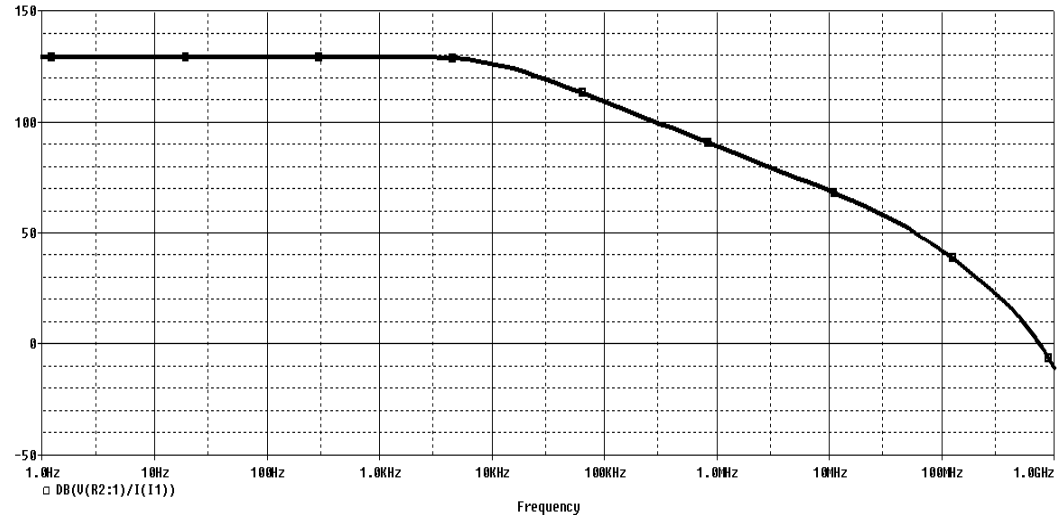

Fig 3.8: A.C. gain response of CFOA based OTRA.

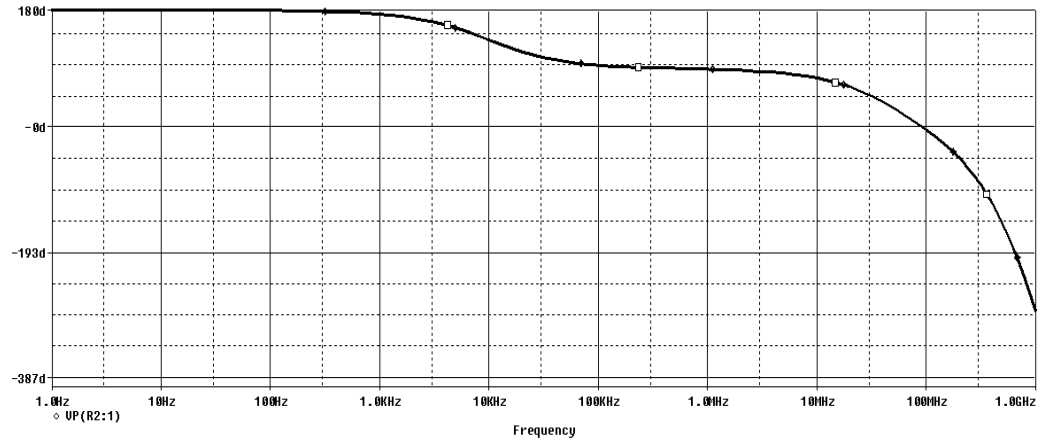

Fig 3.9: A.C. phase response of CFOA based OTRA.

The above mentioned design of OTRA using CFOA IC-AD844 can be used for hardware implementation of OTRA.

3.4 Comparison of Hassan and Soliman's OTRA with CFOA based OTRA

On the basis of responses shown in this chapter, the characteristics of two topologies of OTRA discussed in this chapter are calculated and listed in Table 3.1

Parameter	Hassans's OTRA	CFOA based OTRA
Power Supply	-1.5V, 1.5V	-5V, 5V
Power dissipation	7.73×10^{-4} W	1.40×10^{-1} W
D.C. transresistance gain	84 dB	130 dB
3 dB bandwidth	58.61 KHz	10 KHz
Gain-bandwidth product	0.9 GHz	31.63 GHz
Input current dynamic range	-50 µA to 50 µA	50 µA to 50 µA

Table 3.1: Comparison of Hassan and Soliman's OTRA with CFOA IC AD844 based OTRA.

3.5 Conclusion

In this chapter, Hassan and Soliman's OTRA and CFOA IC AD844 based OTRA topologies are simulated to obtain A.C., transients and D.C. responses and their performance characteristics. The Hassan and Soliman's OTRA and AD844 based OTRA topologies are compared on the basis of their performance criteria.

CHAPTER 4

OTRA BASED APPLICATIONS REALIZATION

4.1 Introduction

The OTRA is a high gain current input voltage output device. Both input and output terminals of the OTRA are characterized by low impedance resulting in circuits that are insensitive to stray capacitances making OTRA appropriate for high frequency applications. Various OTRA based applications are discussed in chapter 2. In this chapter some of the OTRA based applications such as analog filters, oscillator and analog multiplier are simulated using PSICE simulator.

4.2 Fleisher Tow Biquad [37]

The circuit diagram of the Fleisher Tow biquad is given in fig 4.1. The circuit is designed using three OTRA eight resistances and two capacitances. The conditions required for generating a particular filter application are listed in Table 4.1

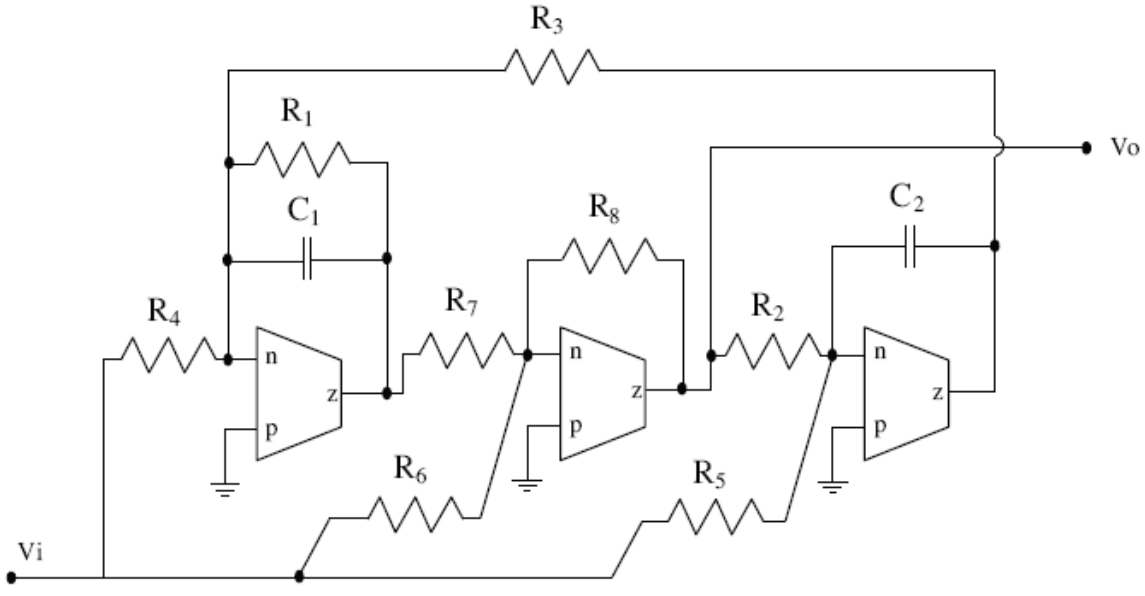

Fig 4.1: OTRA based realization of Fleischer-Tow biquad [37].

Filter application	Condition
Low Pass Filter	$R_4 = \infty\,;\ R_6 = \infty$
High Pass Filter	$R_4 = R_1\,;R_5 = \infty\,;R_6 = R_7 = R_8$
Band Pass Filter	$R_4 = R_1\,;R_5 = R_6 = \infty\,;$
Band Reject Filter	$R_4 = \frac{R_6 R_1}{R_8}\,;R_7 = R_8$
All Pass Filter	$R_4 = \frac{R_1}{2}\,;R_5 = R_2\,;R_6 = R_7 = R_8$

Table 4.1: Conditions requires obtaining various filter responses from Fleisher Tow Biquad [37].

The simulated output response of Low Pass Filter, High Pass Filter, Bans Pass Filter, Band Reject Filter and All pass filters for Fleisher Tow Biquad are as given in Fig 4.2-Fig 4.6 respectively.

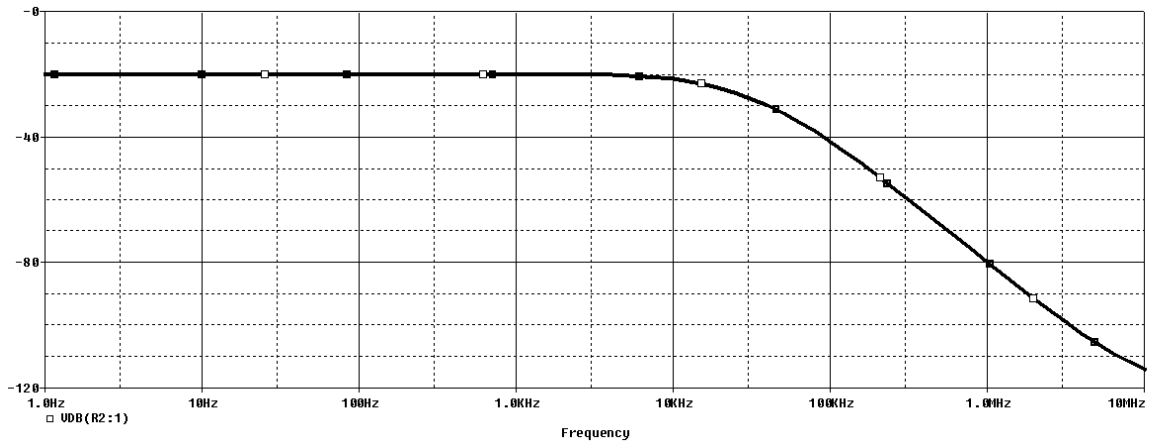

Fig 4.2: Fleisher Tow Biquad Low pass filter output.

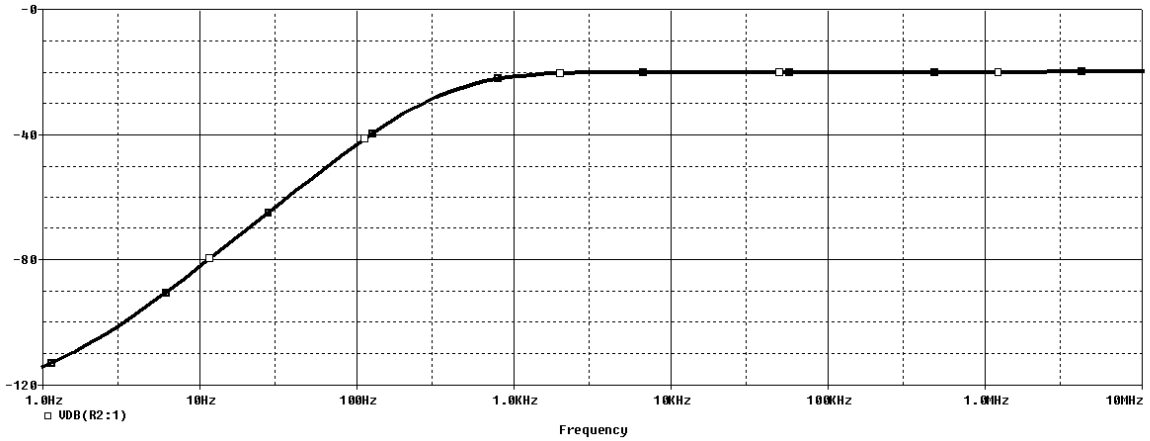

Fig 4.3: Fleisher Tow Biquad High pass filter output.

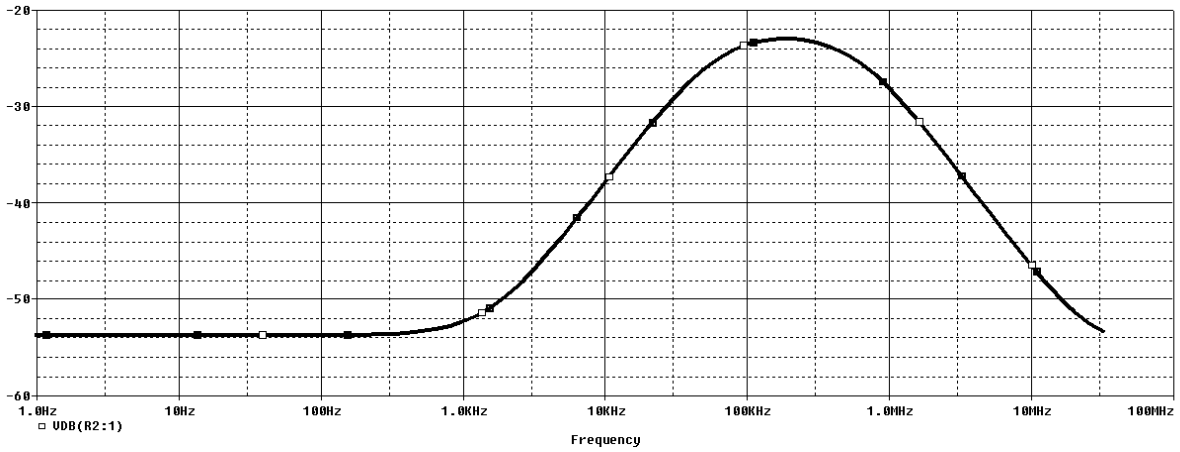

Fig 4.4: Fleisher Tow Biquad Band pass filter output.

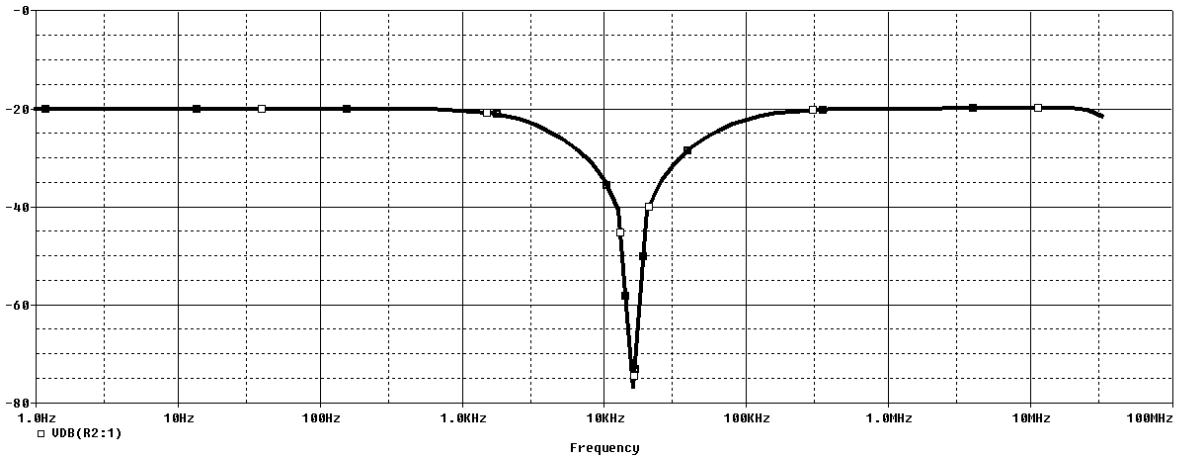

Fig 4.5: Fleisher Tow Biquad Band reject filter output.

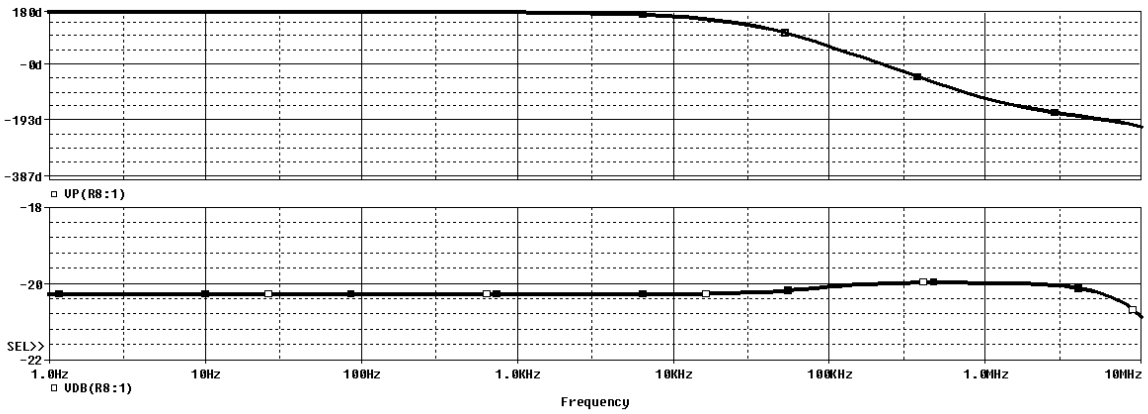

Fig 4.6: Fleisher Tow Biquad All Pass filter output.

4.3 Voltage Mode Biquad using single OTRA [41]

This circuit is developed to generate Low pass filter, High pass filter and Band pass filter responses using a single OTRA with appropriate admittances choices as given in [41]. The circuit topology is given in Fig 4.7.

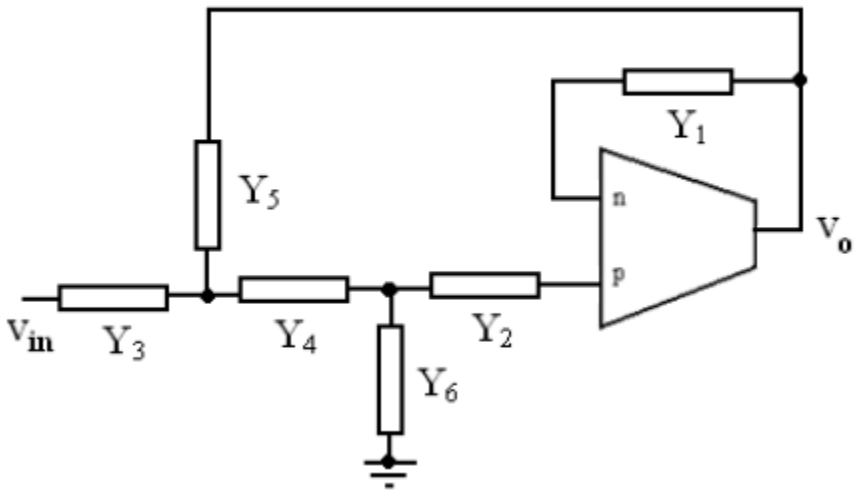

Fig 4.7: Circuit topology for voltage mode biquad using single OTRA [41].

Various filter responses obtained from this topology are as shown in Fig 4.8-Fig 4.10.

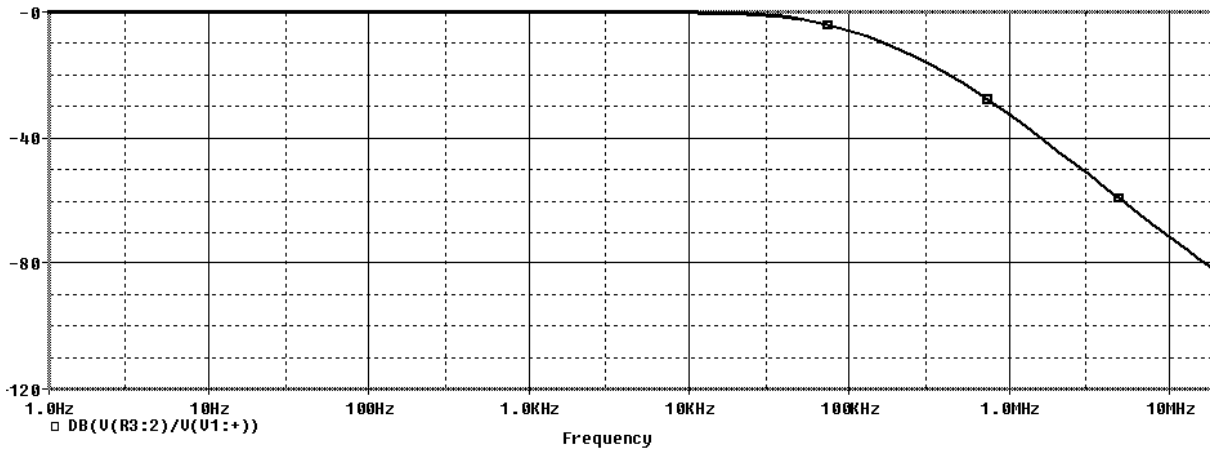

Fig 4.8: Low pass filter response for voltage mode biquad using single OTRA.

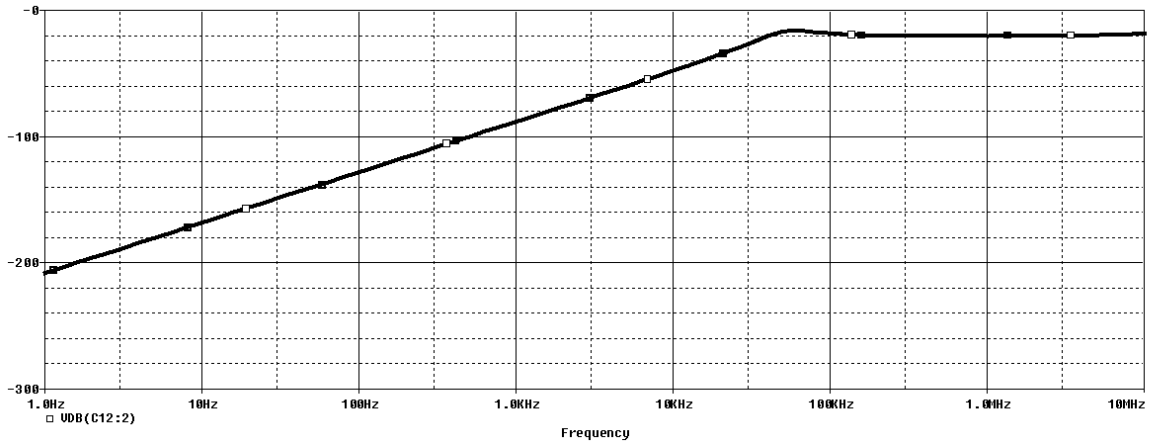

Fig 4.9: High pass filter response for voltage mode biquad using single OTRA.

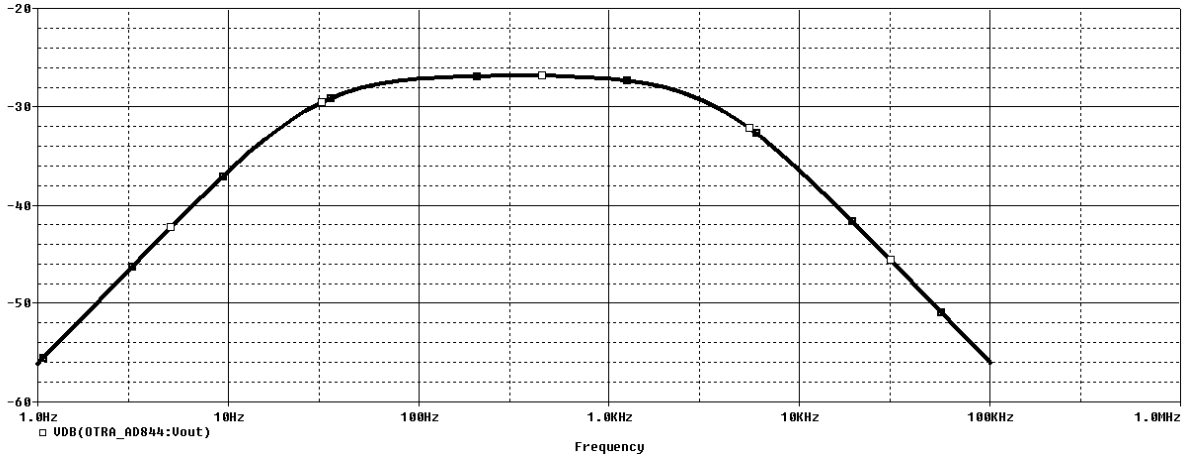

Fig 4.10: Band pass filter response for voltage mode biquad using single OTRA.

4.4 OTRA based Multi-function Biquad [42]

The voltage mode multifunction biquadatic circuit is able to produce Low pass filter, High Pass filter and Band Pass Filter responses simultaneously. The circuit employs three OTRA as shown in Fig 4.11. The simulation output for this biquadatic circuit is as shown in Fig 4.12.

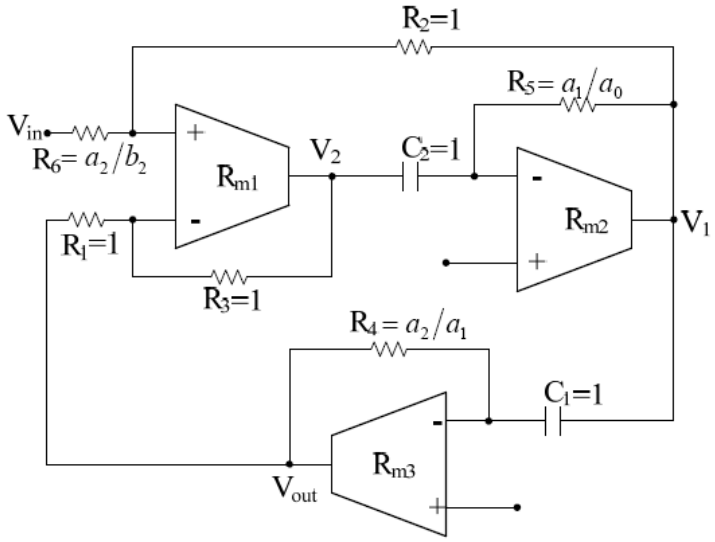

Fig 4.11: Multi function Biquad [42].

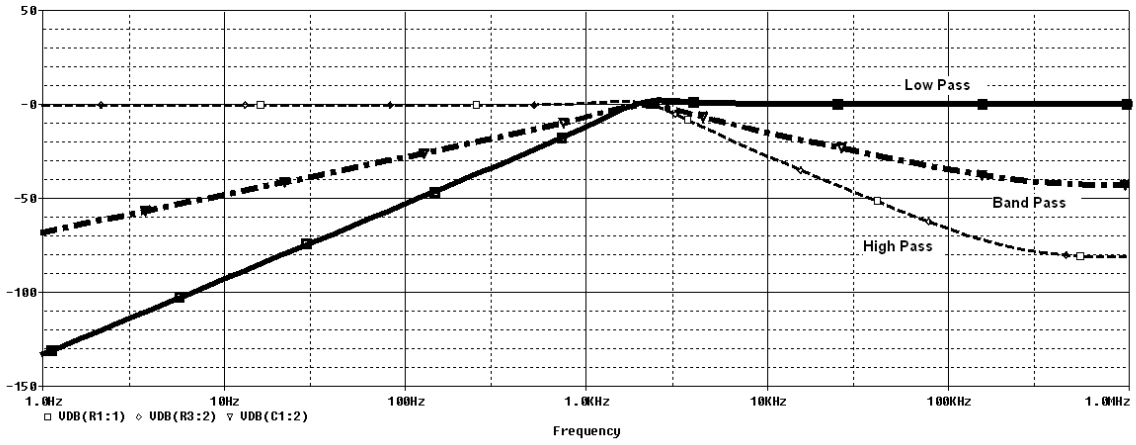

Fig 4.12: Simulation output for multifunction biquadatic circuit.

4.5 OTRA based Novel non-interactive type Oscillator [49]

Harmonic oscillators consist of an amplifier that provides adequate gain and a resonant circuit that feeds back signal to the input and by controlled working of them it produces sinusoidal waveforms. Oscillation occurs at the resonant frequency where a positive gain arises around the loop. Some examples of harmonic oscillators are crystal oscillators and LC-tank oscillators.

The circuit of simulated oscillator given in [49] is as shown in Fig. 4.13.

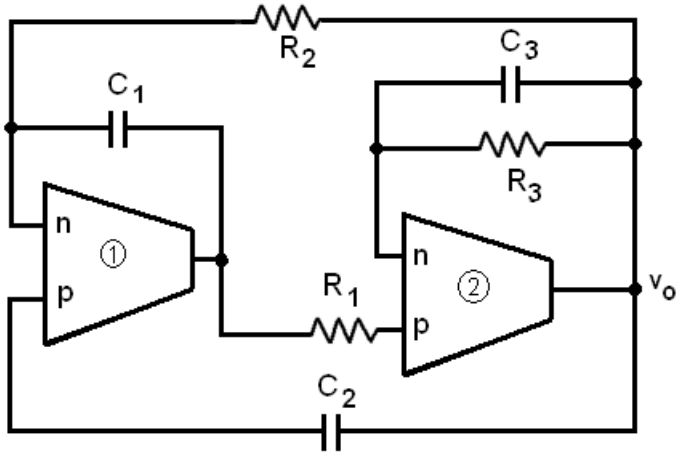

Fig 4.13: OTRA based oscillator [49].

By circuit analysis, the characteristic equation for the circuit in Fig. 4.13 can be given as:

$$s^2C_1C_3 + s(C_1G_3 - C_2G_1) + G_1G_2 = 0 \qquad (4.1)$$

By analyzing equation *(4.1),* the condition of oscillation and frequency of oscillation can respectively be derived as equations *(4.2)* and *(4.3).*

$$C_1G_3 = C_2G_1 \qquad (4.2)$$

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{G_1G_2}{C_1C_3}} \qquad (4.3)$$

From equations *(4.2)* and *(4.3),* it can be said that the condition of oscillations and the frequency of oscillation can be independently controlled with the help of C_2 and R_2 respectively.

The given oscillator is simulated for frequency of oscillations of 159 KHz. The resistive component values for this design are computed as $R_1 = 10\ K\Omega$, $R_2 = 50\ K\Omega$ and $R_3 = 10\ K\Omega$

for chosen values of $C_1 = 20\ pF$, $C_2 = 30\ pF$ and $C_3 = 100\ pF$. The resulted oscillations obtained are shown in Fig. 4.14 and the frequency spectrum is as shown in Fig 4.15.

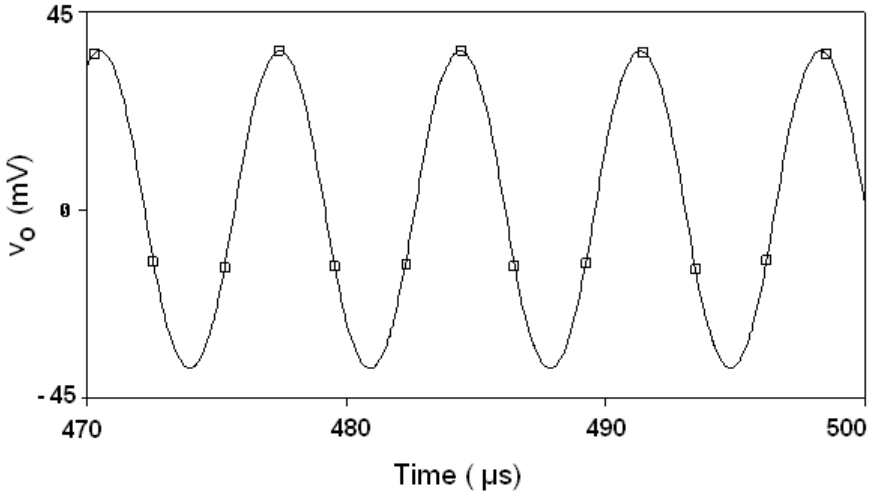

Fig 4.14: Simulated Oscillator outputs.

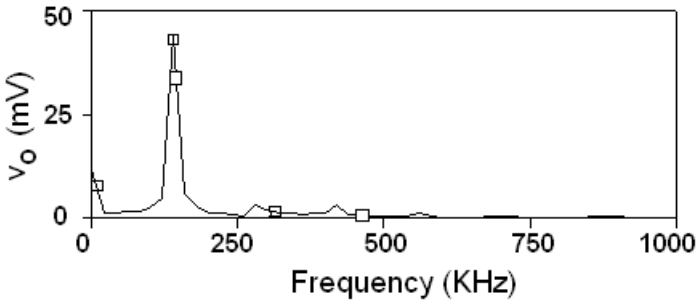

Fig 4.15: Frequency spectrum of resulting oscillations.

The frequency of output waveform obtained is found to be 156.82 KHz and is in a close agreement with the theoretical value.

4.6 OTRA based Multiplier and its application [52]

Analog signal multipliers are used in a large number of applications in the field of telecommunication, control, instrumentation, measurement, and signal processing. The single OTRA based multiplier circuit is explained in [52] whose circuit is given in Fig. 4.16.

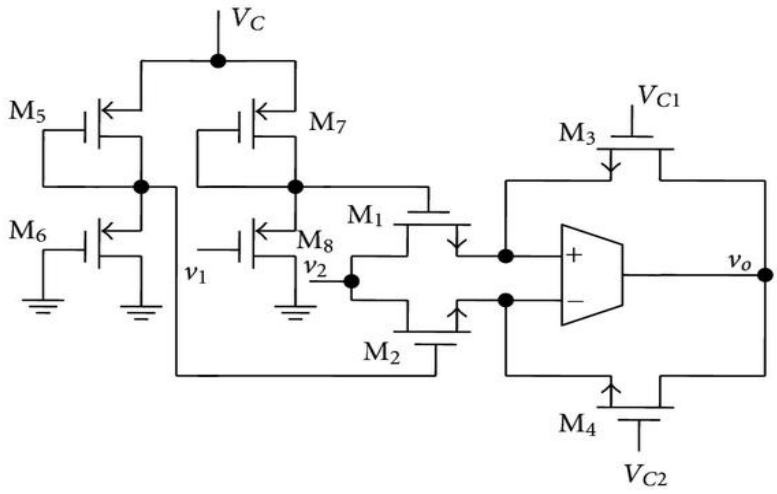

Fig 4.16: OTRA based analog signal multiplier [52].

The transistors M_1, M_2 M_3, and M_4 are all matched transistors and working in the linear region. Voltages v_1 and v_2 are representing small signals, whereas V_{C1}, V_{C2}, and V_C are the D.C. bias voltages. The transistors M_5, M_6, M_7 and M_8 are used to superimpose small signals over D.C. values. The sources of the two NMOS transistors M_1 and M_2 are connected to OTRA input terminals and hence virtually grounded. The drain current for the MOS transistor operating in triode region is given by:

$$I_D = k_n \frac{W}{L}\left((V_{GS} - V_T) - \frac{V_{DS}}{2}\right)V_{DS} \qquad (4.4)$$

Where, k_n is constant for a MOS-transistor and W and L respectively represent the channel width and length of the MOSFET. The other terms are having their usual meaning.

Using equation *(4.4)* the currents through p and n terminals of OTRA, that is, i_p and i_n respectively, can be expressed as

$$i_p = k_n \frac{W}{L}\left(((V_{DC} + v_1) - V_T) - \frac{v_2}{2}\right)v_2 + k_n \frac{W}{L}\left(V_{C1} - V_T) - \frac{v_o}{2}\right)v_o \qquad (4.5\ a)$$

$$i_n = k_n \frac{W}{L}\left(V_{DC} - V_T) - \frac{v_2}{2}\right)v_2 + k_n \frac{W}{L}\left(V_{C2} - V_T) - \frac{v_o}{2}\right)v_o \qquad (4.5\ b)$$

As R_m approaches infinity the input currents are forced to be equal, which results resulting in

$$v_o = \frac{v_1 v_2}{(V_{C2} - V_{C1})} = K v_1 v_2 \qquad (4.6)$$

Where *K* is proportionality constant and is the inverse of differences of gate voltage of M_3 and M_4.

The simulated multiplication results for both the D.C. inputs are shown in Fig 4.17. Based on the given multiplier, DSB-SC signal, ASK signal and PSK signal are obtained and shown in Fig 4.18 - Fig 4.20 respectively.

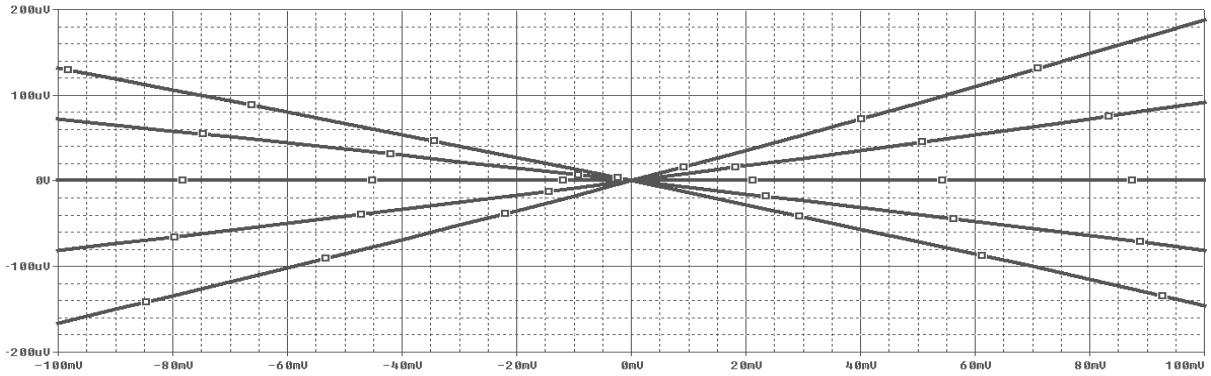

Fig 4.17: Multiplication output of D.C. voltages.

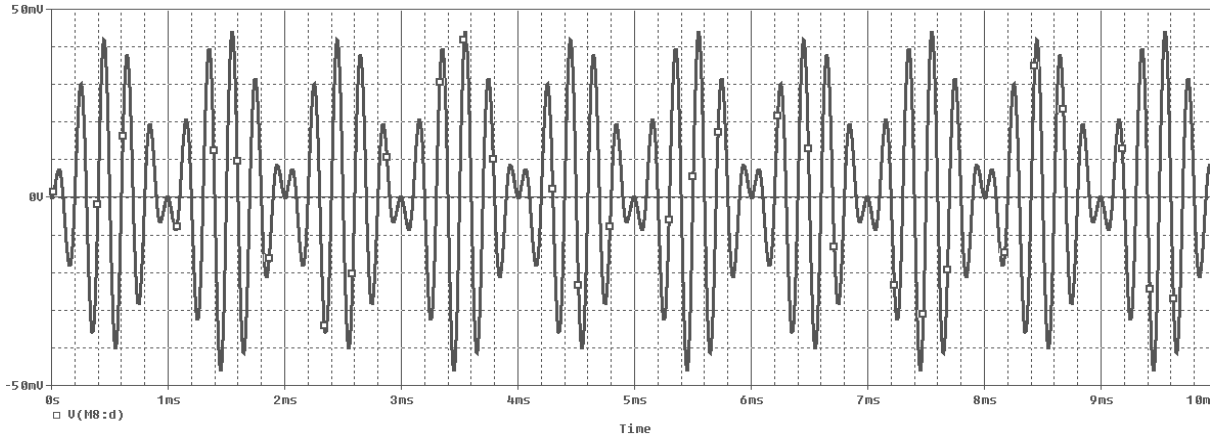

Fig 4.18: DSB-SC signal realized from OTRA based analog multiplier.

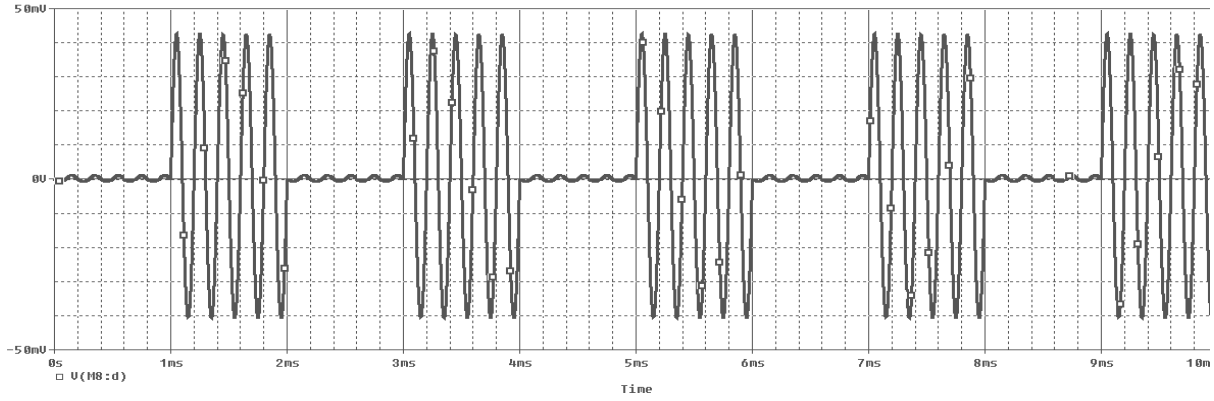

Fig 4.19: ASK signal realized from OTRA based analog multiplier.

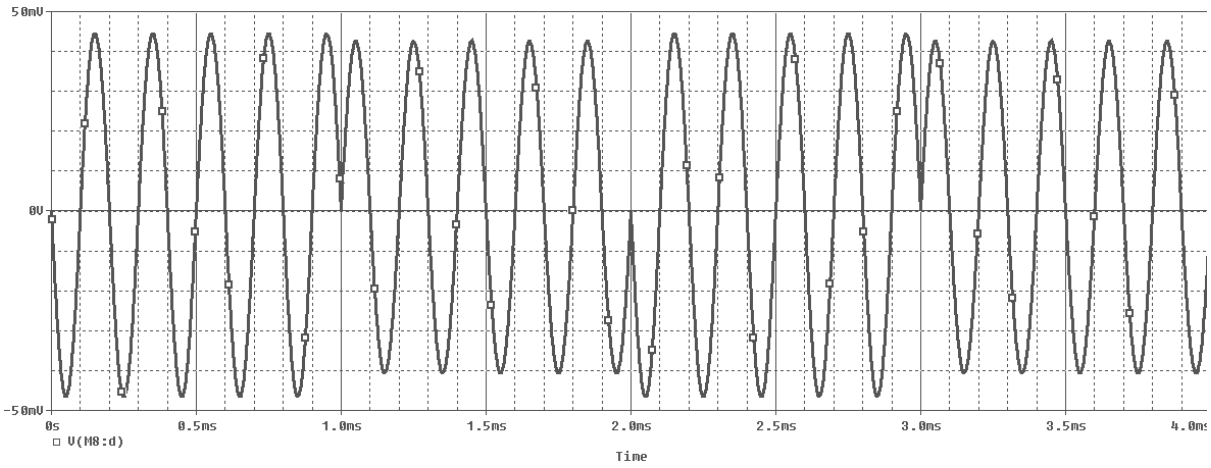

Fig 4.20: PSK signal realized from OTRA based analog multiplier.

4.7 CONCLUSION

In this chapter some the existing applications of OTRA are implemented and verified through SPICE simulation. The structures simulated are Fleisher Tow biquad [37], voltage mode biquad using single OTRA [41] and OTRA based multi-function biquad [42]. The simulations of these circuits are done using IC AD844 based OTRA [19] which has been described in section 2.2.8 and whose simulation results are shown in section 3.3. The results obtained are in close agreement with the theoretical results.

OTRA based Oscillator [49] and Multiplier [52] along with its application are simulated using CMOS OTRA topology discussed in section 2.2.4 and whose simulation results are shown in section 3.2. The results are obtained using 0.5µm parameters provided by MOSIS (AGILENT) and are also found to be in close agreement with the expected results.

CHAPTER 5

PROPOSED INVERSE FILTERS

5.1 Introduction

There are numerous applications in the field of communication, instrumentation and control systems where the signals get distorted while processing and then there is a requirement to correct the distortions of the signal caused by the signal processors or transmission system. While it is highly impossible to create a signal processor or transmission system which do not cause these distortions, these distortions can be simply corrected by using an inverse filter. An inverse filter of a system is one which has frequency response, which is reciprocal of the frequency response of the system that caused the distortion. The area of digital signal processing has various techniques for performing inverse digital filtering; however, the field of analog filter processing is vey wretched in this case and very few methods and circuits are known for realizing continuous-time analog inverse filters and only the earlier works [53-56] deal with this topic although there have been a few general techniques of generating inverse transfer functions such as [57, 58].

The study of OTRA literature reveals that no OTRA based inverse filter configuration has been proposed in the literature so far, to the best of authors' knowledge. Therefore in this thesis, two topologies of OTRA based inverse filters which realize LP, HP and BP inverse filter functions by appropriate admittance selection are proposed.

5.2 Proposed Inverse Filters topology I

5.2.1 The Proposed Circuit

The proposed inverse filter configuration is shown in Fig. 5.1.

Applying KCL at output node, the transfer function can be deduced as:

$$(V_0 - V_1)y_6 = \left(V_1\frac{y_1y_3}{y_2y_4} - V_0\right)y_5$$

$$V_0(y_6 + y_5) = y_5\left(\frac{y_1 y_3 y_5}{y_2 y_4} + y_6\right)$$

$$\frac{V_0}{V_1} = \frac{y_1 y_3 y_5 + y_2 y_4 y_6}{y_2 y_4 y_6 + y_2 y_4 y_5} \qquad (5.1)$$

By proper selection of admittances as listed in Table 5.1, the Inverse low pass filter (ILP) and Inverse high pass (IHP) filter can be designed from the configuration shown in Fig. 5.1.

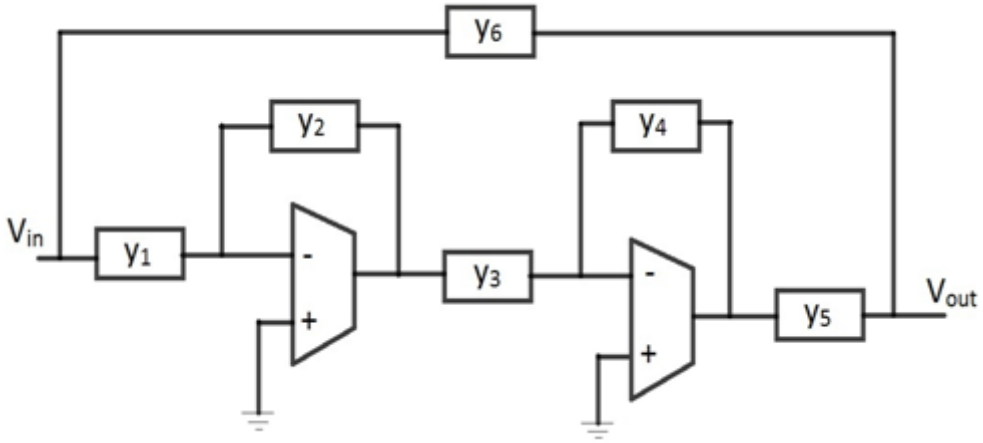

Fig. 5.1: Proposed Inverse Filter topology I.

Admittances	ILP	IHP
y_1	$sC_1 + \frac{1}{R_1}$	$sC_1 + \frac{1}{R_1}$
y_2	$\frac{1}{R_2}$	sC_2
y_3	sC_3	$\frac{1}{R_3}$
y_4	$\frac{1}{R_4}$	sC_4
y_5	$\frac{1}{R_5}$	$\frac{1}{R_5}$
y_6	$\frac{1}{R_6}$	$\frac{1}{R_6}$

Table 5.1: Admittances for ILP and IHP filters for inverse filter topology I.

5.2.2 Inverse Low Pass Filter

By selecting admittances as shown in Table 5.1, the ILP transfer function can be written as:

$$\frac{V_0}{V_1} = \frac{\left(sC_1 + \frac{1}{R_1}\right)\frac{sC_3}{R_5} + \frac{1}{R_2R_4R_6}}{\frac{1}{R_2R_4R_6} + \frac{1}{R_2R_4R_5}}$$

$$\frac{V_0}{V_1} = \frac{\frac{s^2C_1C_3}{R_5} + \frac{sC_3}{R_1R_5} + \frac{1}{R_2R_4R_6}}{\frac{1}{R_2R_4}\left(\frac{1}{R_5} + \frac{1}{R_6}\right)}$$

$$\frac{V_0}{V_1} = \frac{1}{\frac{\frac{1}{C_1C_3R_2R_4}\left(1+\frac{R_5}{R_6}\right)}{s^2+s\frac{1}{C_1R_1}+\frac{R_5}{C_1C_3R_2R_4R_6}}} \qquad (5.2)$$

From equation *(5.2)* the resonant angular frequency (ω_0) and the quality factor (Q_0) can be characterized as:

$$\omega_0 = \sqrt{\left(\frac{R_5}{C_1C_3R_2R_4R_6}\right)} \qquad \{5.3)$$

$$Q_0 = R_1\sqrt{\left(\frac{C_1R_5}{C_3R_2R_4R_6}\right)} \qquad (5.4)$$

It can be noticed from equations (5.3) and *(5.4)* that ω_0 and Q_0 can be orthogonally tuned by setting ω_0 to the desired value and then by changingR_1, Q_0 can be modified as required.

5.2.3 Inverse High Pass Filter

Selecting admittance as per Table 5.1, the transfer function for IHP can be expressed as:

$$\frac{V_0}{V_1} = \frac{\left(sC_1 + \frac{1}{R_1}\right)\frac{1}{R_3R_5} + \frac{s^2C_2C_4}{R_6}}{\frac{s^2C_2C_4}{R_6} + \frac{s^2C_2C_4}{R_5}}$$

$$\frac{V_0}{V_1} = \frac{\frac{s^2C_2C_4}{R_6} + \frac{sC_1}{R_3R_5} + \frac{1}{R_1R_3R_5}}{s^2C_2C_4\left(\frac{1}{R_6} + \frac{1}{R_5}\right)}$$

$$\frac{V_0}{V_1} = \frac{1}{\frac{s^2\left(1+\frac{R_6}{R_5}\right)}{s^2+s\frac{C_1R_6}{C_2C_4R_3R_5}+\frac{R_6}{C_2C_4R_1R_3R_5}}} \qquad (5.5)$$

The resonant angular frequency (ω_0) and the quality factor (Q_0) are given as

$$\omega_0 = \sqrt{\left(\frac{R_6}{C_2C_4R_1R_3R_5}\right)} \qquad (5.6)$$

$$Q_0 = \frac{1}{C_1}\sqrt{\left(\frac{C_2C_4R_3R_5}{R_1R_6}\right)} \qquad (5.7)$$

ω_0 and Q_0 can be orthogonally tuned with the help of capacitor C_1.

5.2.4 Simulations Results

The frequency response of ILP is shown in Fig. 5.2 for which component values are chosen as $C_1 = C_2 = 1.59$nF and resistive components are chosen as 100 KΩ each. The simulated value of f_0 is observed to be 2.738 KHz.

The frequency response of IHP is depicted in Fig. 5.3. The component values are chosen as $C_1 = C_2 = C_4 = 1.59$ nF ,$R_1 = R_3 = 100$ KΩ and $R_5 = R_6 = 100$ Ω. For the components chosen the simulated f_0 of the responses is found to be 3.8619 KHz.

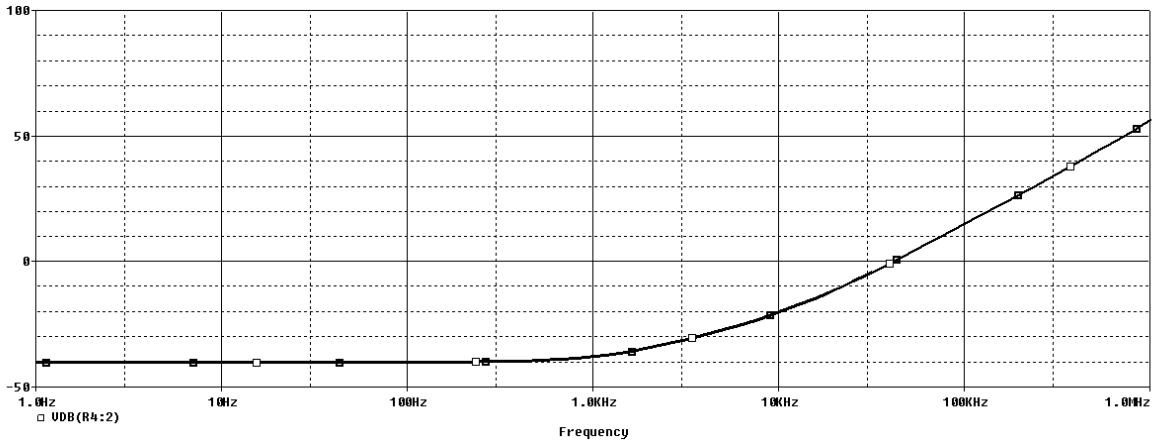

Fig. 5.2: Inverse Low pass Filter (using Topology I) simulation results.

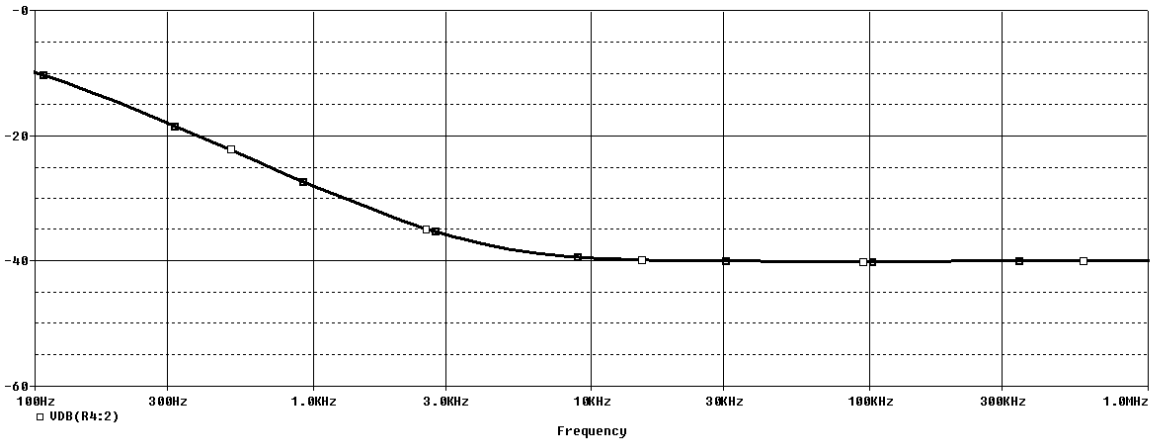

Fig. 5.3: Inverse High pass Filter (using Topology I) simulation results.

5.3 Proposed Inverse Filters topology II

5.3.1 The Proposed Circuit

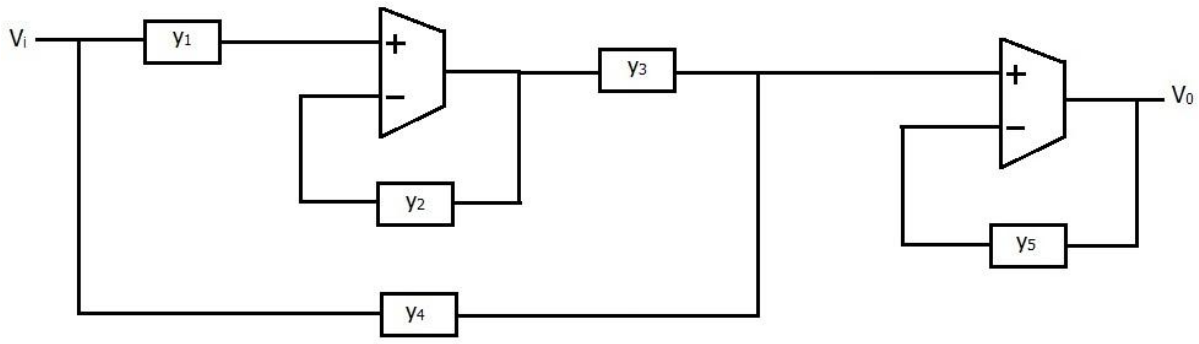

Fig. 5.4: Proposed Inverse Filter topology II.

The proposed inverse filter configuration is shown in Fig. 5.4.

Applying KCL at output node, the transfer function can be deduced as:

$$\frac{v_o}{v_i} = \frac{Y_2Y_4+Y_1Y_3}{Y_2Y_5} \qquad (5.8)$$

By proper selection of admittances as listed in Table 5.2, the Inverse low pass filter (ILP) and Inverse high pass (IHP) filter can be designed from the configuration shown in Fig. 5.4.

Admittances	ILP	IHP	IBP
y_1	$sC_1 + \frac{1}{R_1}$	$sC_1 + \frac{1}{R_1}$	$sC_1 + \frac{1}{R_1}$
y_2	$\frac{1}{R_2}$	sC_2	$\frac{1}{R_2}$
y_3	sC_3	$sC_3 + \frac{1}{R_3}$	$sC_3 + \frac{1}{R_3}$
y_4	$\frac{1}{R_4}$	$\frac{1}{R_4}$	$\frac{1}{R_4}$
y_5	$\frac{1}{R_5}$	sC_5	sC_5

Table 5.2: Admittances for ILP, IHP and IBP filters for inverse filters topology II.

5.3.2 Inverse Low Pass Filter

By selecting admittances as shown in Table 5.2, the ILP transfer function can be written as:

$$\frac{v_o}{v_i} = \frac{\frac{1}{\frac{1}{C_1C_3\,R_2R_5}}}{S^2+S\frac{1}{R_1C_1}+\frac{1}{C_1C_3R_2R_4}} \qquad (5.9)$$

From equation *(5.9)* the resonant angular frequency (ω_0) and the quality factor (Q_0) can be characterized as:

$$\omega_0 = \sqrt{\frac{1}{C_1C_3R_2R_4}} \qquad (5.10)$$

$$Q_0 = R_1\sqrt{\frac{C_1}{C_3R_2R_4}} \qquad (5.11)$$

It can be noticed from equations *(5.10)* and *(5.11)* that ω_0 and Q_0 can be orthogonally tuned by setting ω_0 to the desired value and then by changingR_1, Q_0can be modified as required.

5.3.3 Inverse High Pass Filter

Selecting admittance as per Table 5.2, the transfer function for IHP can be expressed as:

$$\frac{v_o}{v_i} = \frac{\frac{1}{S^2\frac{C_2C_5}{C_1C_3}}}{S^2+S\left[\frac{1}{C_1R_1}+\frac{1}{C_3R_3}+\frac{C_2}{C_1C_3R_4}\right]+\frac{1}{R_1R_3C_3C_1}} \quad (5.12)$$

The resonant angular frequency (ω_0) and the quality factor (Q_0) are given as:

$$\omega_0 = \sqrt{\frac{1}{R_1R_3C_1C_3}} \quad (5.13)$$

$$Q_0 = \frac{R_4\sqrt{R_1R_3C_1C_3}}{[R_1R_2C_2+R_1R_4C_2+R_3R_4C_3]} \quad (5.14)$$

ω_0 and Q_0 can be orthogonally tuned with the help of resistance R_4.

5.3.4 Inverse Band Pass Filter

Selecting admittance as per Table 5.2, the transfer function for IBP can be expressed as:

$$\frac{v_o}{v_i} = \frac{\frac{1}{\frac{SC_5}{C_1C_3R_2}}}{S^2+S\left[\frac{1}{R_1C_1}+\frac{1}{R_3C_3}\right]+\frac{1}{C_1C_3}\left[\frac{1}{R_1R_3}+\frac{1}{R_2R_4}\right]} \quad (5.15)$$

The resonant angular frequency (ω_0) and the quality factor (Q_0) are given as:

$$\omega_0 = \sqrt{\frac{1}{C_1C_3}\left[\frac{1}{R_1R_3}+\frac{1}{R_2R_4}\right]} \quad (5.16)$$

$$Q = \frac{1}{R_1C_1+R_3C_3}\sqrt{R_1R_3C_1C_3\left[1+\frac{R_1R_3}{R_2R_4}\right]} \quad (5.17)$$

5.3.5 Simulations Results

The Inverse Low Pass filter is designed for f_0 = 2 KHz for which C_1 and C_3 are chosen as 1nF and the resistive component values are computed as 79.617 KΩ each. The frequency response of ILP is shown in Fig. 5.5. The simulated value of f_0 is observed to be 2.36 KHz which is in the close agreement to theoretical value.

The components C_1, C_2, C_3 and C_5 are chosen as 1 nF each respectively for Inverse High Pass for f_0 = 1 KHz accordingly resistive components are computed as R_2 = R4 = 159 KΩ. The

frequency response of IHP is depicted in Fig. 5.6. The simulated f_0 of the responses is found to 1.4 KHz which is in close proximity with the theoretical value.

The components C_1, C_3 and C_5 are chosen as 1 nF each respectively for Inverse Band Pass for f_0= 10 KHz and accordingly resistive components are computed as R1 = R_2 = R_3 = R_4 = 22.519 KΩ. The frequency response of IBP is depicted in Fig. 5.7. The simulated f_0 of the responses is found to 10 KHz.

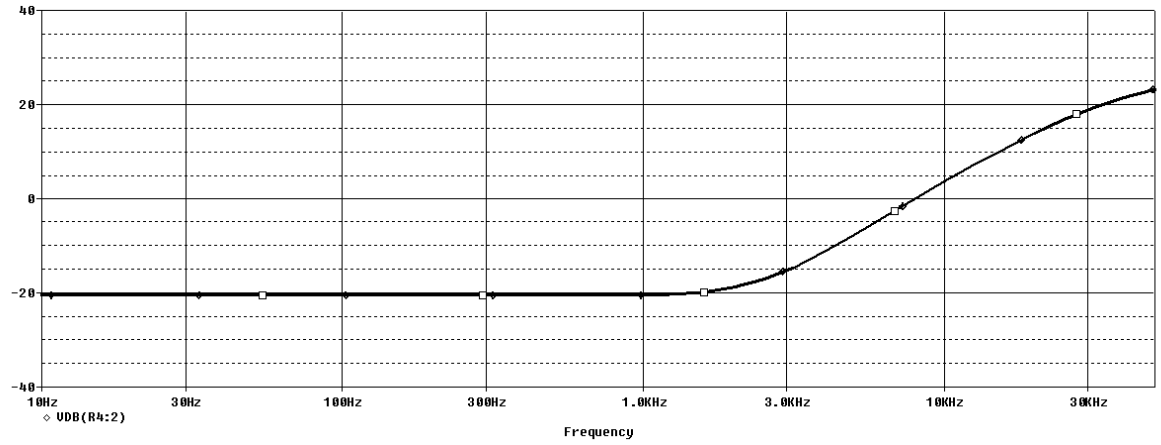

Fig. 5.5: Inverse Low Pass Filter (using Topology II) simulation results.

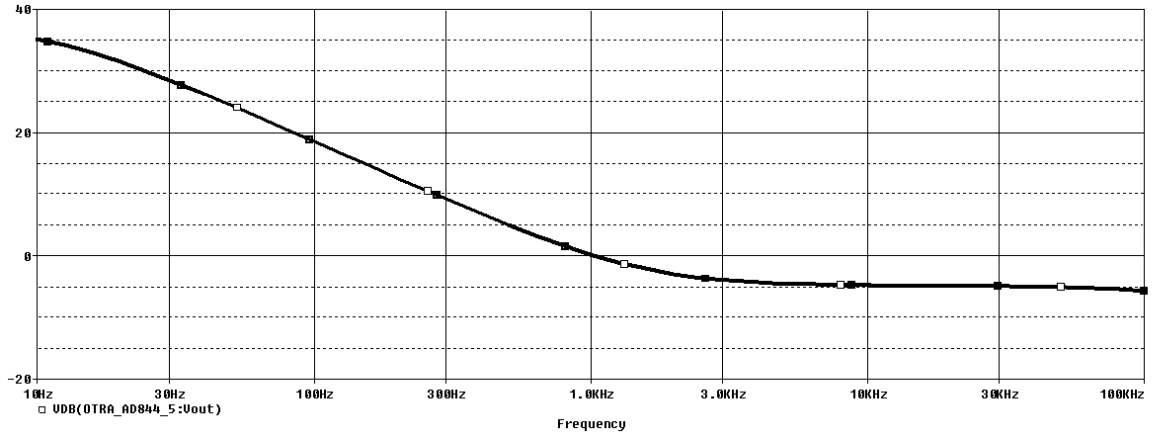

Fig. 5.6: Inverse High Pass Filter (using Topology II) simulation results.

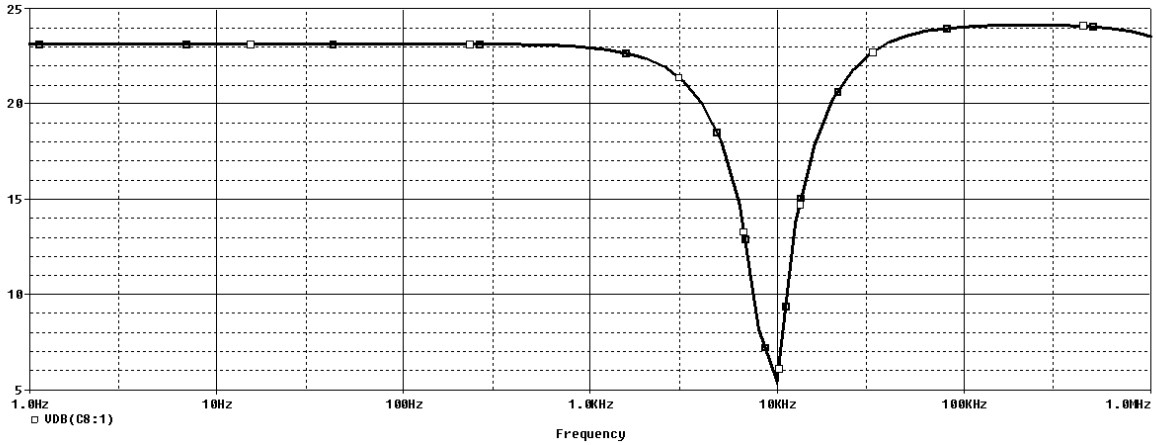

Fig. 5.7: Inverse Band Pass Filter (using Topology II) simulation results.

5.4 Conclusion

Two new topologies of OTRA based inverse filters are presented, both the topologies are single input and single output circuits. From topology I, inverse high pass filter and Inverse low pass filters can be designed by proper selection of impedances while from topology II; inverse high pass filter, inverse low pass filter as well as inverse band pass filters can be designed by proper selection of impedances values. The workability of the proposed configurations is verified through SPICE simulation. The proposed configuration offers new alternatives to analog circuit designers and thus providing further flexibility in design.

CHAPTER 6

CONCLUSION

6.1 Conclusion

In this thesis, a detailed study of the Operational Transresistance Amplifier (OTRA) has been presented. OTRA being a current mode building block inherits the advantage of current mode processing such as large dynamic range, higher slew rate, low power consumption and higher signal bandwidth. Also because of its internally grounded input terminals, parasitic capacitance effect is minimized. OTRA can operate in both voltage and current mode, thus provides further flexibility and enables a variety of circuit design.

The presented work is broadly divided in five sections. In the first section an introduction to current mode signalling and its active blocks including OTRA is give. Extensive literature review on OTRA realization techniques and its applications has been done and is presented in second section. In third section CMOS realizations of OTRA presented in [13] and CFOA ICs (AD844) based OTRA [19] is simulated and characterized. The OTRA block is then used for verification of OTRA based applications available in literature. In concluding section two new circuit applications of OTRA are proposed. These circuits give two topologies for OTRA based inverse filter realization. For each of the proposed circuit, a detailed analysis is formulated. Also, to verify the working of these proposed circuits SPICE simulations are carried out.

The need for low-voltage low power circuits is immense in portable electronic equipments like laptop computers, pace makers, cell phones etc. During the last few decades, the current mode processing has emerged as low voltage design technique for analog design and has become a viable alternative over voltage mode circuits and is becoming powerful tool for the development of high performance analog circuits and systems. Keeping the benefits of current mode processing and the advantages offered by OTRA in view there is a tremendous scope of utilizing OTRA in analog circuit design.

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APPENDIX I

0.5um Mosis Agilent Technology Parameter

NMOS

LEVEL=3 UO=460.5 TOX=1E-8 TPG=1 VTO=.62 JS=1.8E-6 XJ=.15E-6 RS=417 RSH=2.73 LD=4E-8 ETA=0 VMAX=130E3 NSUB=1.71E17 PB=.761 PHI=.905 THETA=.129 GAMMA=.69 KAPPA=0.1 AF=1 WD=1.1E-7 CJ=76.4E-5 MJ=.357 CJSW=5.68E-10 MJSW=.302 CGSO=1.38E-10 CGDO=1.38E-10 CGBO=3.45E-10 KF=3.07E-28 DELTA=0.42 NFS=1.2E11

PMOS

LEVEL=3 UO=100 TOX=1E-8 TPG=1 VTO=-.58 JS=.38E-6 XJ=.1E-6 RS=886 RSH=1.81 LD=3E-8 ETA=0 VMAX=113E3 NSUB=2.08E17 PB=.911 PHI=.905 THETA=.12 GAMMA=.76 KAPPA=2 AF=1 WD=1.4E-7CJ=85E-5 MJ=.429 CJSW=4.67E-10 MJSW=.631 CGSO=1.38E-10 CGDO=1.38E-10 CGBO=3.45E-10 KF=1.08E-29 DELTA=0.81 NFS=.52E11