A DISSERTATION ON

Simulation and Designing of Triple Gate 3D BOI(body on insulator) FINFET Structure using ATLAS

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CERTIFICATE

This is to certify that the dissertation entitled "***simulation and designing of triple gate 3d BOI FINFET structure using atlas*** " submitted by **Mr**. **Rahul Singh** in the partial fulfillment of the requirement for the award of the degree of M.Tech. in Nano Science and Technology from the Department of Applied Physics, Delhi Technological University, Delhi is a record of candidate's own work carried out by him under my supervision.

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I hereby declare that the work presented in this dissertation entitled "**Simulation and designing or triple gate 3d BOI FINFET structure using atlas**" has been carried out by me under the guidance of **Dr. Rishu Chaujar**, Assistant Professor of Engineering Physics department, Delhi Technological University, Delhi and hereby submitted for the partial fulfillment for the award of degree of Master of Technology in Nano Science and Technology at Applied Physics Department, Delhi Technological University, Delhi.

I further undertake that the work embodied in this major project has not been submitted for the award of any other degree elsewhere.

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ABSTRACT

In the past few decades the minimum size of transistor has been downscaled according to the Moore's law. But now further downscaling of MOSFET is facing challenges like SCE(short channel effects), gate insulator tunnelling. To overcome these challenges FinFET, a type of multigate device, is the most promising device structure.

FinFET technology has the calibre to continue with the Moore’s law. FinFET has started replacing conventional MOSFETs. The gate in FinFET is wrapped around a thin silicon fin for better control over the conducting channel i.e. fins. 3nm FinFET has been demonstrated in university labs.

This thesis analyses the effects of variation in fin width, fin height, oxide thickness on the various device parameters like drain current(Ion), leakage current(Ioff), threshold voltage(Vt), DIBL and subthreshold swing(S) of FinFET by using simulation tools 3D Silvaco ATLAS version5.16.3.R and Devedit version 2.6.0.R.

Chapter 1

Introduction

1.1 Scaling of CMOS and its Challenges

As devices shrink further and further, the problems with conventional (planar) MOSFETs are increasing. Industry is currently at the 90nm node (ie. DRAM half metal pitch, which corresponds to gate lengths of about 70nm). As we go down to the 65nm, 45nm, etc nodes, there seem to be no viable options of continuing forth with the conventional MOSFET. Severe short channel effects (SCE) such as V_T rolloff and drain induced barrier lowering (DIBL), increasing leakage currents such as subthreshold S/D leakage, D/B (GIDL), gate direct tunnelling[3] leakage, and hot carrier effects that result in device degradation is plaguing the industry (at the device level; there are other BEOL (back-end of the line) problems such as interconnect RC delays which we won't discuss here). Reducing the power supply V_{dd} helps reduce power and hot carrier effects, but worsens performance. Performance can be improved back by lowering V_T but at the cost of worsening S/D leakage. To reduce DIBL and increase adequate channel control by the gate, the oxide thickness can be reduced, but that increases gate leakage. Solving one problem leads to another. Efforts are on to find a suitable high-k gate dielectric so that a thicker physical oxide can be used to help reduce gate leakage and yet have adequate channel control, but this search has not been successful to the point of being usable. There are problems with band alignment (w.r.t Si) and/or thermal instability problems and/or interface states problems (with Si). The thermal instability problem has led researchers to search for metal gate electrodes instead of polysilicon (because insufficient activation leads to poly depletion effects). But metal gates with suitable work functions haven't been found to the point of being usable. In the absence of this, polysilicon continues to be used, whose work function demands that V_T be set by high channel doping. High channel doping in turn leads to random dopant fluctuations (at small gate lengths) as well as increased impurity scattering and therefore reduced mobility. Indeed, it is felt that instead of planar MOSFETs, a double gate device will be needed at gate lengths below 50nm [1] in order to be able to continue forth on the shrinking path.

1.2 Silvaco ATLAS and DEVEDIT

This thesis uses DevEdit 3D[12] version 2.6.0.R and Silvaco Atlas version 5.16.3.R to perform SOI FinFET simulation.

ATLAS is a modular and extensible framework for one, two and three dimensional semiconductor device simulation. It is implemented using modern software engineering practices that promote reliability, maintainability, and extensibility. Products that use the ATLAS Framework meet the device simulation needs of all semiconductor application areas.

DevEdit is a device structure editor. It can be used to generate a new mesh on an existing structure or can be used to create or modify a device. DevEdit can be used as a simulator under DeckBuild[17] or through a Graphical User Interface (GUI). DevEdit allows structures to be created or read into DevEdit in the form of SILVACO Standard Structure Files. ATLAS is a physically-based two and three dimensional device simulator. It predicts the electrical behaviour of specified semiconductor structures and provides insight into the internal physical mechanisms associated with device operation[9].

The DeckBuild run-time environment is used in this thesis. The DeckBuild run-time environment receives the input files. Within the input files, Silvaco Atlas is called to execute the code. And finally, TonyPlot is used to view the output or results of the simulation.

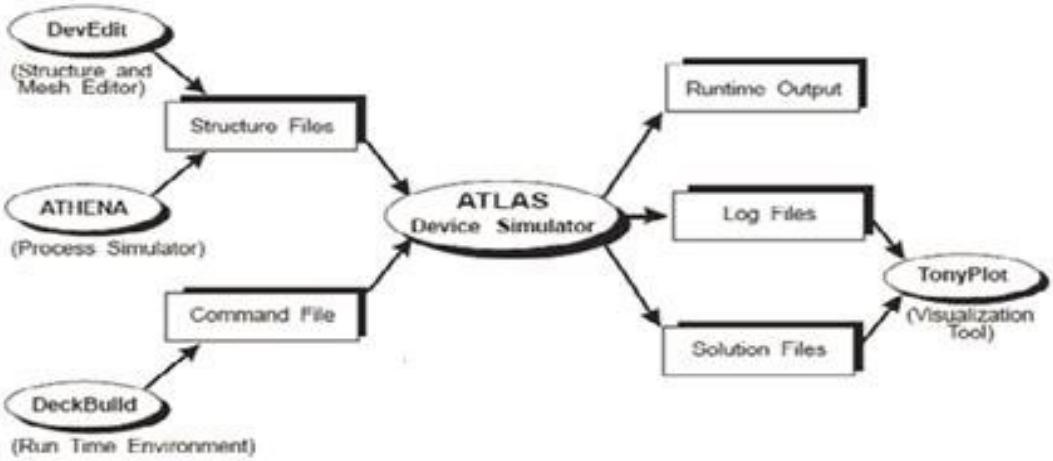


Figure 1.1 Data flow in ATLAS[9]

All 3-D programs in ATLAS supports structures defined on 3D prismatic meshes. Structures may have arbitrary geometries in two dimensions and consist of multiple slices in the third dimension There are two methods for creating a 3D structure that can be used with ATLAS. One is through the command syntax of ATLAS and the other through an interface to D EVEDIT3D. A direct interface from ATHENA to 3D ATLAS is not possible, however DEVEDIT3D provides the ability to read in 2D structures from ATHENA and extend them non-uniformly to create 3D structures for ATLAS

1.3What is FINFET

FinFET is a non planar, double-gate transistor built on an SOI substrate, based on the earlier DELTA (single-gate) transistor design.[10] The term FinFET was coined by University of California, Berkeley researchers (Profs. Chenming Hu, Tsu-Jae King-Liu and Jeffrey Bokor). The distinguishing characteristic of the FinFET is that the conducting channel is wrapped by a thin silicon "fin", which forms the body of the device. The thickness of the fin determines the effective channel length of the device. Because of the vertically thin channel structure, it is referred to as a fin because it resembles a fish□s fin; hence the name FinFET. If only side gates are effective then it is called a double gate FinFET. A gate can also be fabricated at the top of the fin, in which case it is a triple gate FinFET. Or optionally, the oxide above the fin can be made thick enough so that the gate above the fin is as good as not being present.

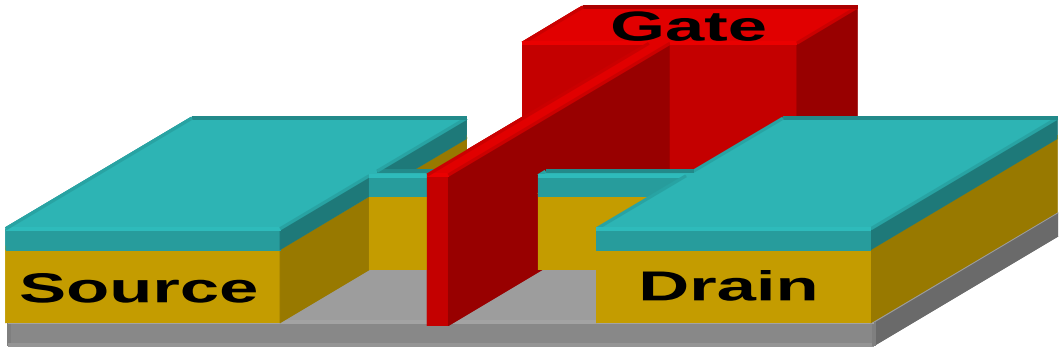


Figure 1.2 FinFET structure[10]

FinFET’s are usually fabricated on an SOI substrate. It starts by patterning and etching thin fins on the SOI wafer using a hard mask. The hard mask is retained throughout the

process to protect the fin. The fin thickness is typically half or one third the gate length, so it is a very small dimension. It is made by either e-beam lithography or by optical lithography using extensive linewidth trimming [7].

1.3 Research Objectives & Outline

The ultimate goal is to study thoroughly literature survey and with this help simulation the triple gate FINFET structure and taken its various characterstics with the help of ATLAS simulation. this work that how threshold voltage, leakage current and drive current are affected by varying various parameters of FinFET like fin width, fin height, oxide thickness, different oxide materials are varied and the effects are studied.

Outline

This thesis is outlined as follows:

Chapter 2 mainly focused on downscaling and the effect of downscaling on conventional FINFET structure.

Chapter 3 basics of FINFET and comparision to MOSFET'S and why it is better than others structures..

Chapter 4 Simulation of the FINFET structure and its various characterstics such as thesold voltage, DIBL(drain induced voltage lowering), Ion ,Ioff, Vt roll of..etc..

Chapter 5 conclusion

Chapter 2

MOSFET Basics

The reliance of the power electronics industry upon bipolar devices was challenged by the introduction of a new MOS gate controlled power device technology in the 1980s. The power MOS field effect transistor (MOSFET) evolved from the MOS integrated circuit technology. The new device promised extremely low input power levels and no inherent limitation to the switching speed. Thus, it opened up the possibility of increasing the operating frequency in power electronic systems resulting in reduction in size and weight. The initial claims of infinite current gain for the power MOSFET were, however, diluted by the need to design the gate drive circuit to account for the pulse currents required to charge and discharge the high input capacitance of these devices. At high frequency of operation the required gate drive power becomes substantial. MOSFETs also have comparatively higher on state resistance per unit area of the device cross section which increases with the blocking voltage rating of the device. Consequently, the use of MOSFET has been restricted to low voltage (less than about 500 volts) applications where the ON state resistance reaches acceptable values. Inherently fast switching speed of these devices can be effectively utilized to increase the switching frequency beyond several hundred kHz

2.1 MOSFET SCALING BENEFITS

First stated in 1965, Moore's law describes the unparalleled technologyadvancement over the past 40 years which has allowed the number of transistors on achip to double about every two years [1]. This phenomenal progress has been madepossible by continual downscaling of the metal-oxide-semiconductor field-effecttransistor (MOSFET) to smaller physical dimensions. MOSFETs have the remarkablefeature that as they become smaller they also become cheaper, consume less power,become faster, and enable more functions per unit area of silicon. As a result, denser silicon integrated circuits (ICs) can be realized, offering superior performance at reduced.

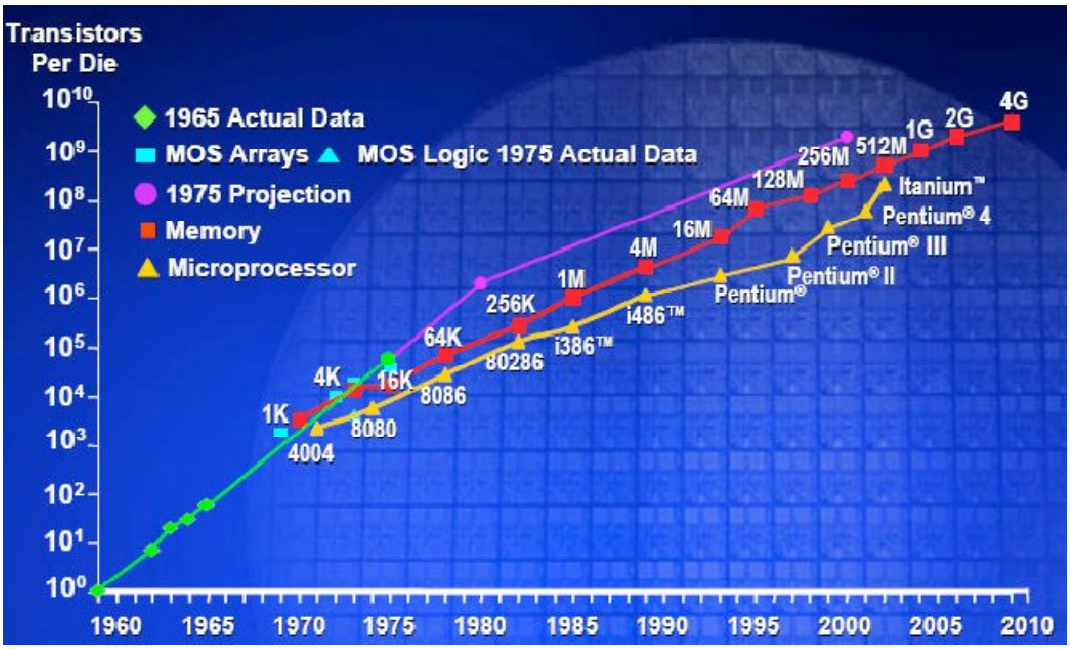


Figure 2.1. Number of transistors on a chip, as a function of the first year of production[3].

Figure 2.2. The increase in chip performance, measured in millions of instructions persecond (MIPS), as a consequence of scaling[3] .

2.2 Bulk Si-MOSFET Scaling Challenges

Figure 2.3 shows the schematic of the conventional planar bulk Si-MOSFET, the basic building block of an integrated circuit. As the gate length (*Lg*) of a MOSFET decreases, the capacitive coupling of the channel potential to the source and the drain terminals increases with respect to the capacitive coupling to the gate terminal, resulting in short channel effects (SCE), such as threshold voltage (*VTH*) roll-off? smaller *VTH* at shorter *Lg*, and drain- induced barrier lowering (DIBL)? smaller *VTH* at higher drain voltage (*VDS*) due to reduction of the source-channel potential barrier by the drain voltage. *VTH* roll-off and DIBL manifest into increased off-state transistor leakage (*Ioff*). *Ioff* is becoming a severe concern for high-performance logic technologies that may hinder CMOS scaling because of significant passive power consumption as shown in Figure

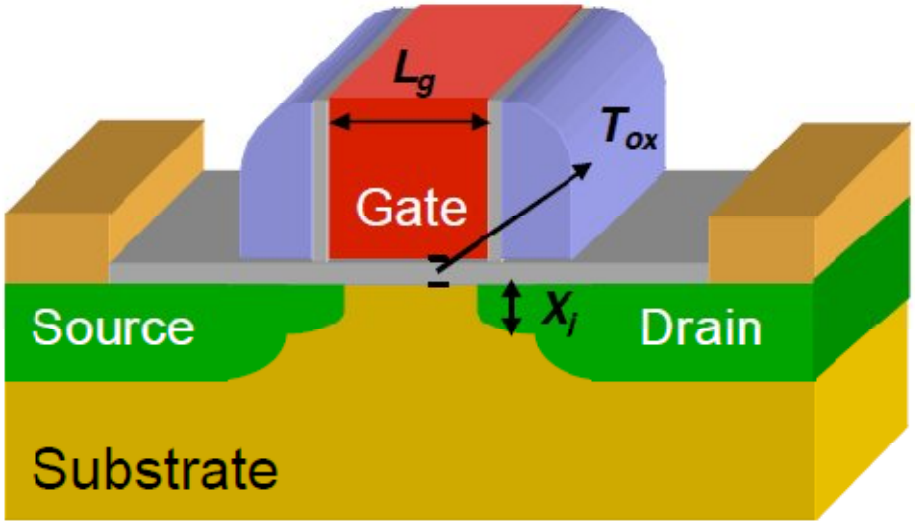


Figure 2.3. Schematic diagram of the bulk Si MOSFET[7]

Therefore, careful device design is required so that SCE do not prevent the use of a minimum *Lg* MOSFET. For bulk MOSFETs, a minimum *Lg* must be ~5*l*, where *l* is the characteristic length and is given by [4]

This scaling methodology has worked very well for several decades, but as silicon CMOS technology advances into the nanometer regime, fundamental and practical limits impede the traditional scaling of transistors as discussed next. Historically, the gate dielectric thickness has been the single most important dimension to enable device

scaling. Scaling down of the gate dielectric not only increases capacitive coupling of the gate to the channel but also leads to increased on-state transistor drive current (*Ion*).

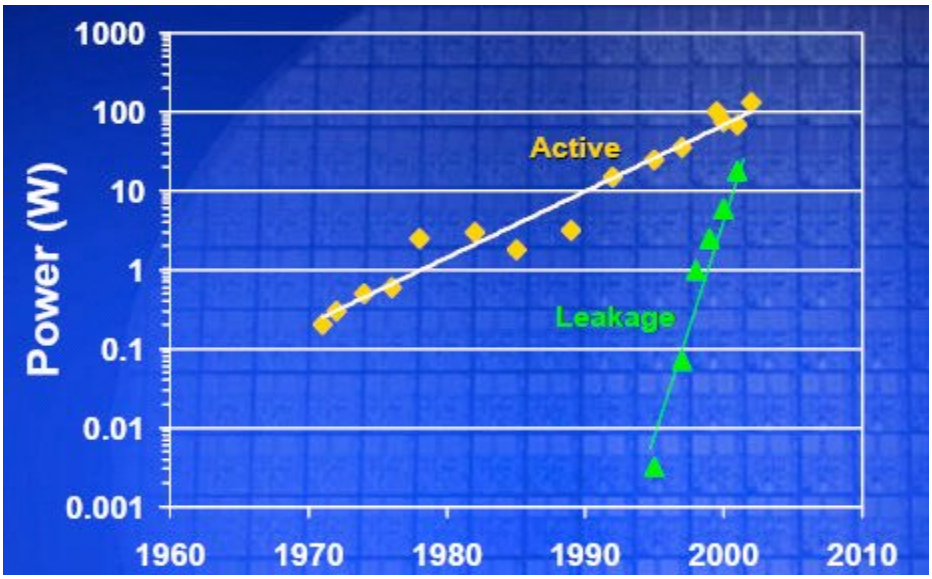


Figure 2.4. The trend in active and leakage power of microprocessors as a consequence of scaling [2]. The leakage power is approaching ~50% of the total power in a modernday microprocessor.

This scaling methodology has worked very well for several decades, but as silicon CMOS technology advances into the nanometer regime, fundamental and practical limits impede the traditional scaling of transistors as discussed next. Historically, the gate dielectric thickness has been the single most important dimension to enable device scaling. Scaling down of the gate dielectric not only increases capacitive coupling of the gate to the channel but also leads to increased on-state transistor drive current (*Ion*). However, the thickness of SiO2-based gate dielectrics is approaching physical limits (<2nm) resulting in severe gate leakage current due to quantum mechanical tunneling of carriers across the thin dielectric. To scale down *Tdep*, higher channel doping density is necessary. Reducing *Tdep* helps to eliminate leakage paths far from the dielectric/channel interface. In sub-100 nm MOSFETs, a halo implant is generally used to suppress subsurface leakage, but this increases the average doping in the channel [5]. The increase in channel doping leads to degraded carrier mobility due to higher vertical electric field and more impurity scattering. For very high channel doping near the source/drain extensions, band-to-band tunneling also becomes an issue. Furthermore, as the channel volume shrinks in ultra-scaled transistors, the statistical fluctuation of

dopant atoms causes device-to-device variations [6, 7]. Shallow *Xj* reduces the source/drain-channel coupling relative to the gate-channel coupling. However, the reduced junction depth increases parasitic source/drain resistance, resulting in degraded on-state transistor drive current.

2.3 Device Structure and Physical Operation

Device structure of MOSFET

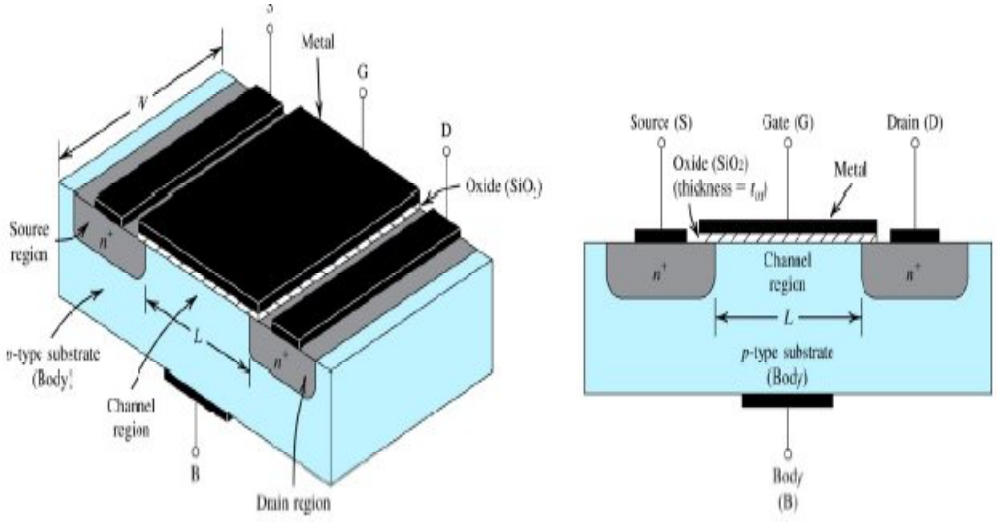


Figure 2.5 device structure of MOSFET[15]

- "MOS" ≡ metal-oxide-semiconductor structure.
- MOSFET is a four-terminal device: gate (G), source (S), drain (D) and body (B).
- The device size (channel region) is specified by channel width (*W*) and channel length (*L*).
- Two kinds of MOSFETs: *n*-channel (NMOS) and *p*-channel (PMOS) devices
- The device structure is basically symmetric in terms of drain and source.
- Source and drain terminals are specified by the operation voltage.

2.3.1 Operation with zero gate voltage

- The MOS structure form a parallel-plate plate capacitor with gate oxide layer in the middle.
- Two *pn* junctions (S-B and D-B) are connected as back to back diodes.

- The source and drain terminals are isolated by two depletion regions without conducting current.
- The operating principles will be introduced by using the *n*-channel MOSFET as an example.
- Creating a channel for current flow
- Positive charges accumulate in gate as a positive voltage applies to gate electrode.
- The electric field forms a depletion region by pushing holes in *p*-type substrate away from the surface.
- Electrons start to accumulate on the substrate surface as gate voltage exceeds a threshold voltage *V*t .
- The induced *n* forms a channel region thus for current flow from drain to source.
- The channel is created by inverting the substrate surface from *p*-type to *n*-type inversion layer.
- The field controls the amount of charge in the channel and determines the channel conductivity.

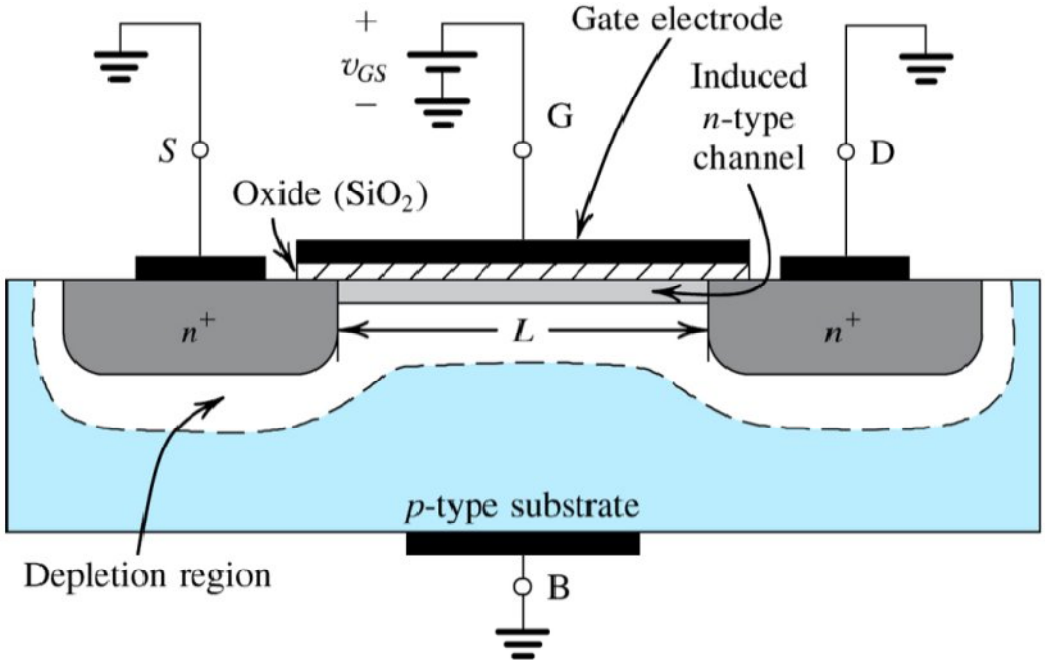


figure2.6 Operation of n-type MOSFET[11]

2.3.2Applying a small drain voltage

- A positive *Vgs* > *V*t is used to induce the channel and it is called *n*-channel enhancement-type MOSFET.

- Free electrons travel from source to drain through the induced *n*-channel due to a small *Vds*.
- The resulting current *i*D flows from drain to source (opposite to the direction of the flow of negative charge).
- The current is proportional to the number of carriers in the induced channel.
- The channel is controlled by the effective voltage or overdrive voltage: *Vov=Vgs- Vt*
- The electron charge in the channel due to the overdrive voltage: |*Q*| = *C*ox*WLv*OV
- Gate oxide capacitance *C*ox is defined as capacitance per unit area.
- MOSFET can be approximated as a linear resistor in this region with a resistance value inversely
- proportional to the excess gate voltage

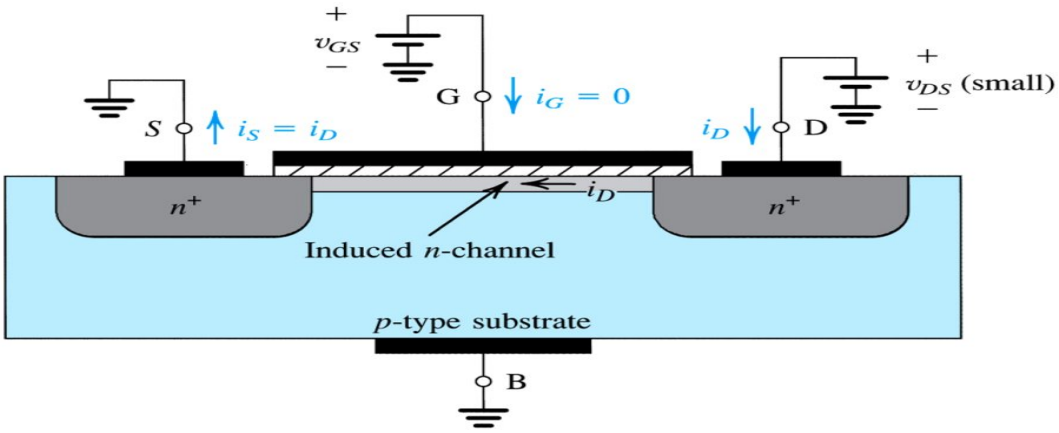


Figure2.7 N MOSFET by applying smaal +ve drain voltage[11]

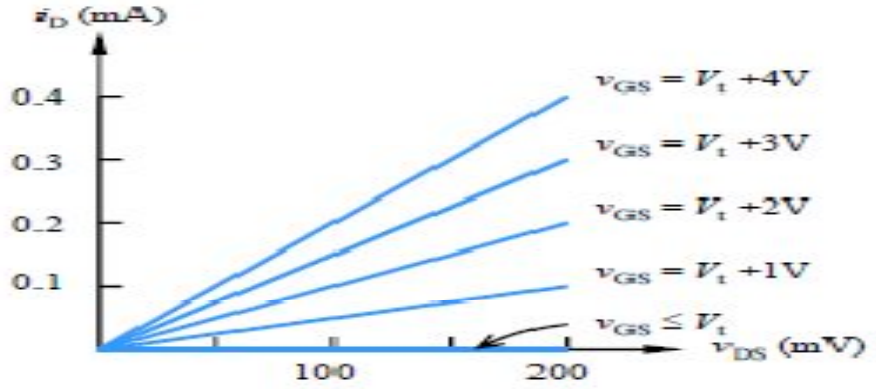


Figure 2.8 Id vs Vgs of n MOSFET at constt Vt[11]

2.3.3 Operation as increasing drain voltage

- As *Vds* increases, the voltage along the channel increases from 0 to *Vds* , and the voltage between the gate
- and the points along the channel decreases from *v*GS at the source end to (*v*GS *Vds*) at the drain end.
- Since the inversion layer depends on the voltage difference across the MOS structure, increasing *Vds* will
- result in a tapered channel.
- The resistance increases due to tapered channel and the *Id- Vds* curve does not continue as a straight line.
- At the point *Vds* sat = *Vgs* - *V*t , the channel is **pinched off** at the drain side.
- Increasing *Vds* beyond this value has little effect on the channel shape and *i*D saturates at this value.
- **Triode region**: *Vds* < *Vds* sat
- **Saturation region**: *Vds* >*Vds* sat

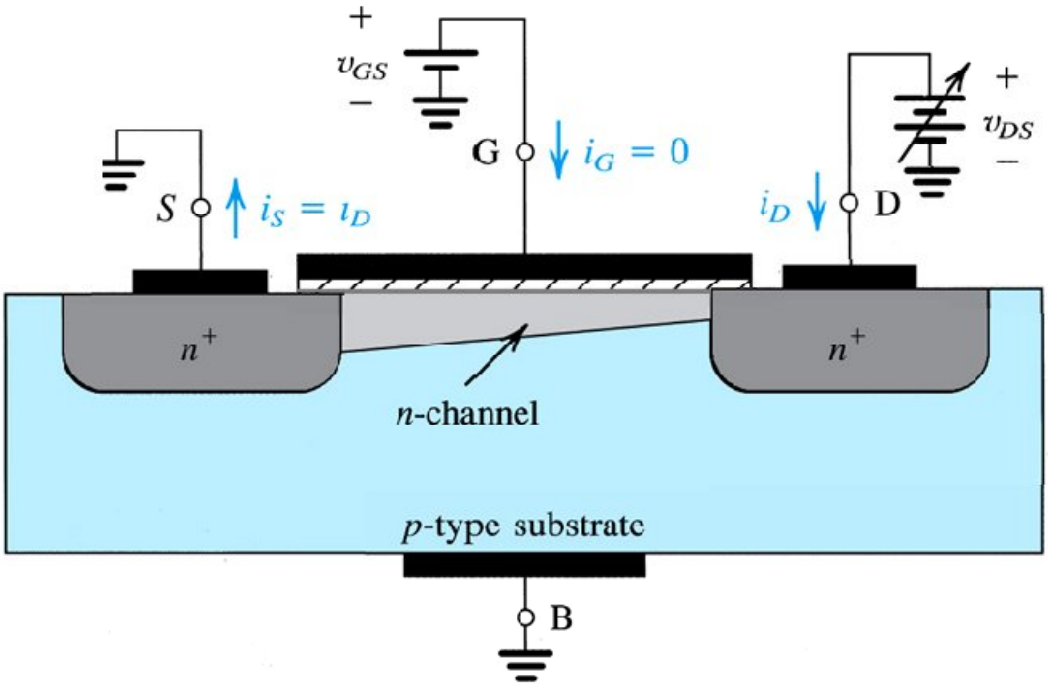


Figure 2.9 operation of n-mos by further increasing Vds[11,12]

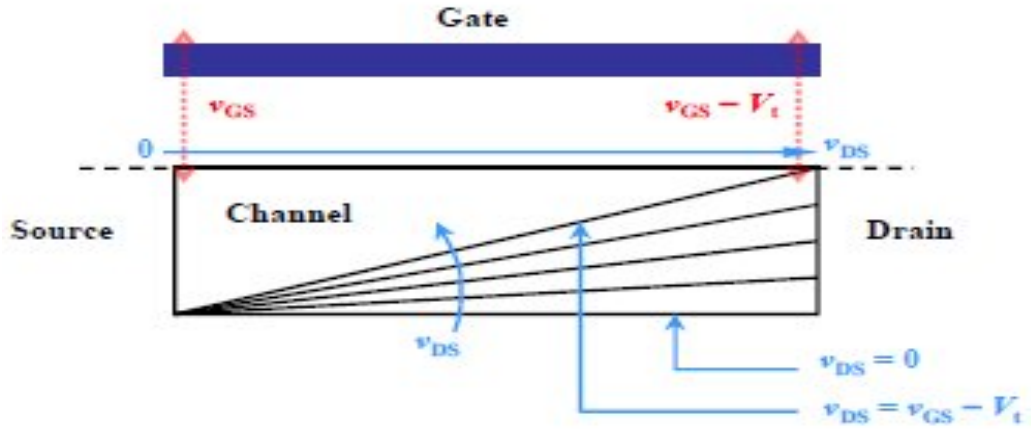


Figure 2.10 channel shape of n-mos[12]

2.3.4 The body effect

- The BS and BD junction should be reverse biased for the device to function properly.
- Normally, the body of a *n*-channel MOSFET is connected to the most negative voltage.
- The depletion region widens in BS and BD junctions and under the channel as *V*SB increases.
- **Body effect**: *V*t increases due to the excess charge in the depletion region under the channel.
- The body effect can cause considerable degradation in circuit performance.
- Threshold voltage:

2.3.5 Temperature effect

- *V*t decreases by ~2mV for every 1'C rise → *i*D increases with temperature.
- *k*'n decreases with temperature → *i*D decreases with increasing temperature.
- For a given bias voltage, the overall observed effect of a temperature increase is a decrease in *i*D .

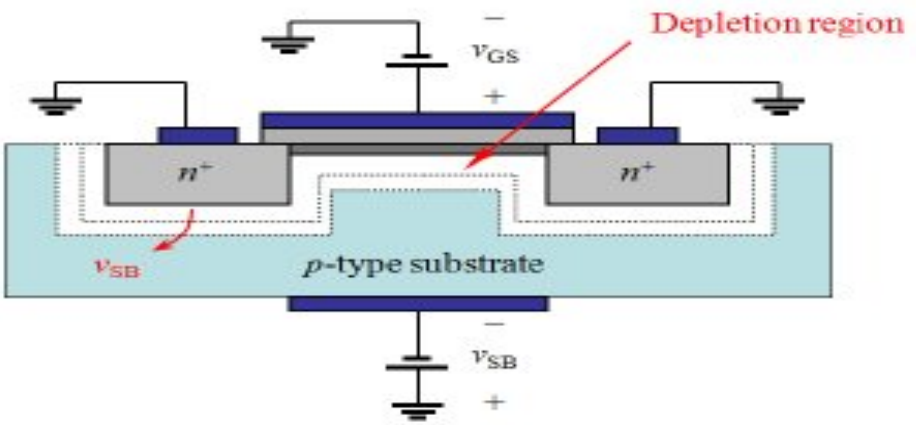


Figure 2.11 Body and temprature effet in n-mos[11]

2.4 Downscaling- Why needed

Computing power has increased dramatically over the past few decades, because of the major advancements in silicon integrated circuit (IC) technology led by the continuous miniaturization in the size of MOS transistor. The fast progress in the semiconductor industry has been driven by improved circuit working and performance together with side by side reduction in the manufacturing costs. With the invent MOS transistor its dimensions have been shrinking 30% for every 3 years, following

The main reason to make transistors smaller is to pack more and more devices in a specified chip area. This results in a chip with the same functionality in a smaller area, or chips with more functionality in the same area. Since fabrication costs for a semiconductor wafer are comparatively fixed, the cost per integrated circuits is mainly related to the number of chips that can be formed per wafer. As smaller ICs allow more chips per wafer, therefore there is a reduction in the price per chip. Reduction of the physical MOS device dimensions has improved both circuit speed and density in the following ways

- Circuit operational frequency increases with a reduction in gate length(Lg), allowing for faster circuits.
- Chip area decreases therefore enabling higher transistor density and cheaper ICs.
- Switching power density is almost constant; this allows lesser power per function or additional circuits at the same power.
- Per transistor cost decreases

The classic scaling rule is called “constant-field scaling”. It was planned by

Dennard et al. in 1974 [15]. As the name implies this method was based on keeping a constant electric field throughout the channel length of the MOSFET by means of scaling down voltages and device dimensions by a definite factor k and conversely up scaling doping concentrations (Na,Nd) by that same factor. This allowed the power consumed per area (power density) to remain constant while the circuit delay went down by factor k. As a result, the circuit speeds up by the same factor k, and the power dissipation per circuit is decreased by factor of k^2.

Basically scaling can be made in two ways: constant voltage scaling and constant field scaling. In constant voltage scaling only lateral dimensions of the MOSFET are scaled i.e. gate length and gate width which may lead to dielectric breakdown. Constant voltage scaling is a simply geometrical route. To remove this drawback constant field scaling is done. In this lateral dimensions (gate length, gate width), perpendicular dimensions (oxide thickness), and voltages are scaled along with the doping levels.

2.4.1 Gate length scaling

Gate length scaling is directly related to the MOSFET scaling. Smaller gate length yields higher currents that result in consequently higher speed circuits. Smaller gate lengths are made possible by the advanced lithographic capability and this enhancement allows operation at lower voltages. At the same time higher packaging density is also achieved, due to the ability to pattern finer structures.

2.4.2 Gate oxide scaling

Higher drive current is achieved by scaling gate oxide to produce a higher gate capacitance so that extra inversion is induced at the same gate bias. Stronger capacitive coupling allows the gate to have superior control of the potential in the channel region and thus reducing short channel effects and maintaining good subthreshold turn-off slope. Gate oxide scaling is not restricted by manufacturing control. At very low dimensions of gate length, quantum mechanical(QM) tunnelling takes place leading to a gate leakage current. This leakage current increase exponentially with the reduction in oxide thickness and this in turn increases the chip standby power.

2.4.3 Voltage scaling

Main challenges for power voltage scaling (i.e. applied drain bias) have been the non-scaling character of threshold voltage. In scaling the MOSFET, the supply voltage has to be scaled along with the physical dimensions of the transistor to maintain a constant electric field across the source and drain called “constant field scaling”. The power supply voltage is usually reduced to minimize power dissipation and because of reliability reasons.

To maintain acceptable on-state performance, the device threshold voltage must also be scaled so that it can accommodate the reduced power supply. As threshold voltage is reduced, Ioff will be increased because the channel potential barrier height is reduced. So threshold voltage scaling is a limiting issue in transistor gate scaling.

2.5 Outcome of downscaling-SCE

A MOSFET device is considered to be short when the channel length is of the same magnitude as the depletion-layer widths of the source and drain junction. As the channel length L is reduced to boost both the operation speed and the quantity of components per chip, the Short Channel Effects arise. With the Short Channel Effects many important device characteristics are related, so it affects a lot.

2.5.1 Subthreshold Leakage

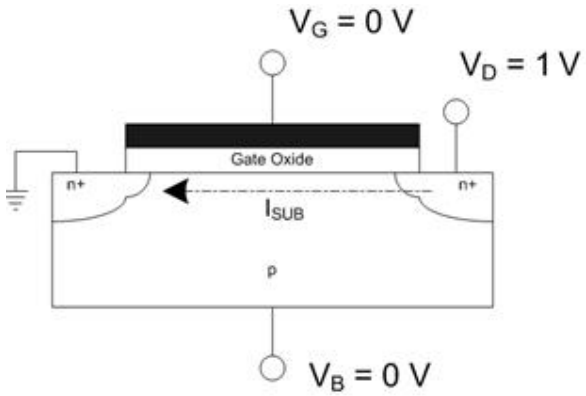


Figure 2.12 Subthreshold leakage in an nFET [16]

Subthreshold conduction or subthreshold leakage or subthreshold drain current is the current that flows between the source and drain of a MOSFET when the transistor

is in subthreshold region, or weak-inversion region i.e., for gate-to-source voltages below the threshold voltage(Vgs<VT). Ideally this state is considered as the off-state but practically it is not. In digital circuits, subthreshold conduction is usually assumed as a parasitic leakage state that would ideally have no current. The subthreshold region is often referred to as the weak inversion region. This weak inversion region is the main component of the MOSFET off-state current, Ioff. Ioff is the Id(drain current) measured at Vgs=0 and Vds=Vdd. It is important to keep Ioff as low as possible to minimize the static power that a circuit consumes when it is in the standby mode.

Subthreshold conduction is only one contributor of leakage current, other contributors are gate-oxide leakage and junction leakage. In beginning, subthreshold conduction in transistors was very small, but with downscaling of transistors, leakage from all sources increased their contribution. For a technology with threshold voltage of 0.2 V, leakage can exceed 50% of total power consumption.

The reason for the increasing importance of subthreshold conduction is that the supply voltage has continually scaled down, to reduce the dynamic power consumption of integrated circuits (the power that is consumed when the transistor is switching from an on-state to an off-state, which depends on the square of the supply voltage), and to carry on electric fields inside small devices low, to maintain device reliability. The value of subthreshold conduction is set by the threshold voltage, which sits between ground and the supply voltage, and therefore has to be reduced with the supply voltage. This reduction means less gate voltage swing below threshold to turn the device off, and as subthreshold conduction varies exponentially with gate voltage, it becomes more and more important as MOSFETs shrink in size.

At Vgs below Vt, the inversion electron concentration is small but it allow allow a small leakage current to flow between the source and the drain. For a given W and L, there are two ways to reduce leakage current. The first is to have a large Vt but this solution is not very good because a large Vt reduces Ion and which in turn increases the gate delays. The other good way is to reduce the subthreshold swing(S). S can be decreased by reducing oxide thickness(Tox). But again there is a loop in this as Tox is reduced gate leakage increases.[17]

2.5.2 Vt roll off

The threshold voltage of a long channel device is not affected by the channel

length and the drain voltage. But when channel length size is reduced becomes shorter and shorter, the threshold voltage shows a greater reliance on the channel length and the drain voltage.

This dependence of the Vt is due to the loss of control by the gate of the depletion region underneath it. The gate voltage only controls a fraction of the depletion layer. Vt is lower for transistor with shorter gate length(Lg). This Vt roll-off is typically measured in mV/nm.

For digital applications, the Vt roll-off is the most undesirable SCE. One must ensure that Vt does not become too low for the minimum Lg devices on a chip. The SCE is more prominent at higher drain bias. Vt drops with decreasing Lg. When Vt drops too much, Ioff becomes too large and that channel length is not tolerable.

The occurrence of Vt roll off can be understood as follows. In a short-channel device, the source drain distance is equal to the depletion width in the vertical direction in the channel region. The drain potential has a strong effect on the band bending over a significant fraction of the channel. Thus, the energy barrier which prevents carriers from flowing through under the "off" condition is deeply lowered by the drain field penetration. This causes a substantial increase of the subthreshold current, thus a reduced Vt. In a long-channel device, the source and drain are so far apart that their depletion regions have no effect on the energy barrier or the electric field pattern in most part of the channel. . Vertical dimensions in a MOSFET like oxide thickness, depletion width and junction depth must be reduced in order to support the reduction of gate length. To avoid threshold voltage roll-off, the substrate doping concentration should be chosen such that the minimum gate length is about 2-3 times Wdep.[18].

2.5.3 DIBl

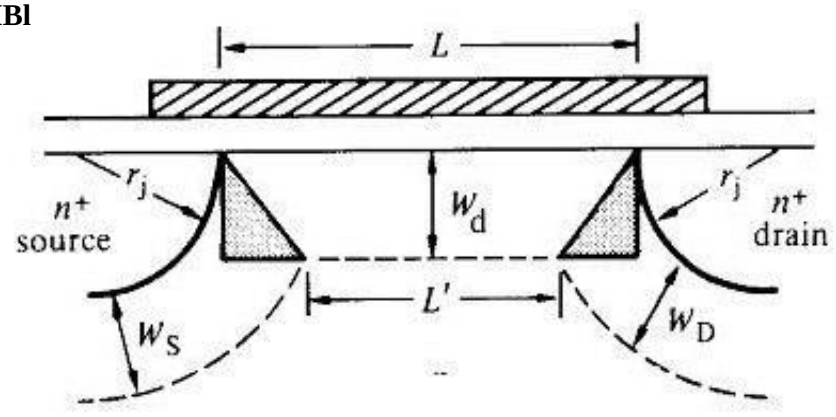


Figure 2.13 source/drain depletion region influence on the gatdepletionr egion[19].

For a SC transistor, the depletion region of the source and drain enhance significantly resulting in reduction in Vt at higher drain bias. So threshold condition can be achieved at a lower gate bias. When the depletion regions surrounding the drain moves towards the source, the two depletion layers merge and punch through occurs. Punch through can be minimized with thinner oxides, larger substrate doping, shallower junctions, and with longer channels.

The current flow in the channel depends on creating and sustaining an inversion layer on the surface. If the gate bias voltage is not sufficient to invert the surface, the charge carriers in the channel face a potential barrier that blocks the flow. Increasing the gate voltage reduces this potential barrier and, eventually, allows the flow of carriers under the influence of the channel electric field. In small-geometry MOSFETs, the potential barrier is controlled by both the gate-to-source voltage and the drain-to-source voltage. If the drain voltage is increased, the potential barrier in the channel decreases, leading to drain-induced barrier lowering (DIBL). The reduction of the potential barrier eventually allows electron flow between the source and the drain, even if the gate-to-source voltage is lower than the threshold voltage. The channel current that flows under this conditions (i.e Vgs<Vt) is called the sub-threshold current.

In other words, the SCE gives a better depletion width with an increase in surface potential, making the channel more attractive for electrons and increasing the expected current for a given gate bias.

DIBL is therefore a measure of the short channel performance of transistor and can be measured by difference in threshold voltage between small drain bias(0.1V) and high drain bias(Vdd). It should be noted that a high DIBL or big difference between Vt does not imply poor transistor performance in a circuit operation since the transistor will not be operating at low drain bias. Rather a high DIBL indicates the presence of degraded device characteristics such as strong Vt roll-off and high Ioff.

2.6 Advantages of Multi-gate MOSFETs

As the size of MOSFET decreased, it increasingly suffered from the undesirable short-channel effect. So a alternate structure was required to control short channel effect in Mosfet, which came in the form of multigate devices. In a multigate device, the channel is surrounded by several gates on multiple surfaces. As the channel is

surrounded by more than one gate and controlled electrostatically by multiple gates so there is better channel control by the gate than the conventional MOSFETs. The main advantage of the multi-gate devices is the improved short channel effects.

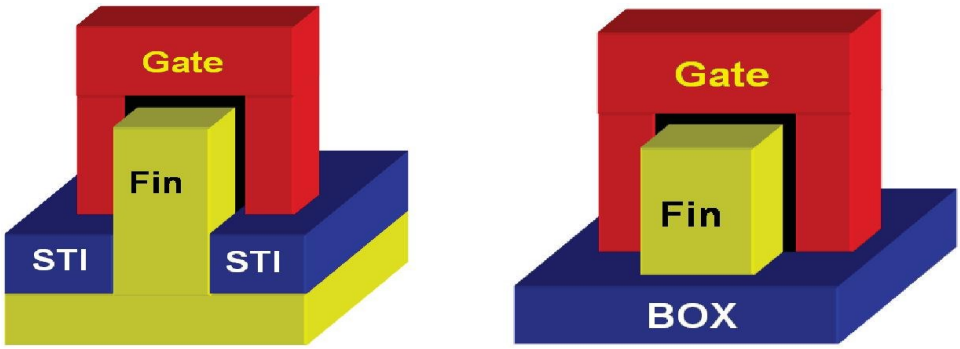
The second advantage of the multi-gate devices is the improved on-state drive current (Ion) and therefore faster circuit speed. Reduction of channel doping reduces impurity Coulombic scattering. Reduced channel doping reduces the electric field normal to the SiO_2 interface and therefore reduces the surface roughness scattering.

The third advantage is the reduced manufacturing variation.

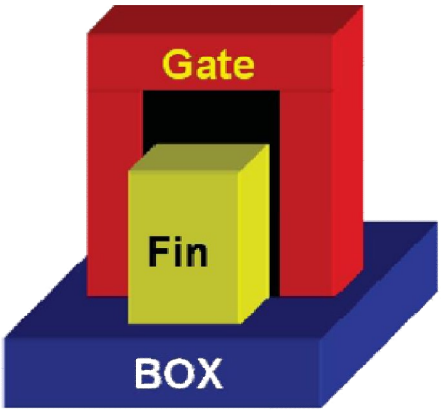
The fourth advantage is the more effective suppression of "off-state" leakage current which in turn leads to lower power consumption and improved device standby time.

Another advantage is that this technology is more compact than conventional planar transistors, improving transistor density which results to smaller overall microelectronics.

There are different types of multi-gate MOSFETs. Several examples are shown in Fig. 1. FinFETs (a type of Multigate device) can be made on either bulk or SOI substrates, forming bulk FinFET (Fig. 1(a)) or SOI FinFETs (Fig. 1(b)). (Fig. 1(c)). In double-gate FinFETs the top surface of the fin does not conduct current, whereas in triple-gate FinFETs (Figs. 1(a), (b)) the side surfaces and the top surface all conduct current. Another example of multi-gate MOSFET is the all-around gate device (Fig. 1(d)). It consists of a pillar-like body delimited by the gate dielectric and the gate. The nanowire MOSFET is one example of all-around gate devices.

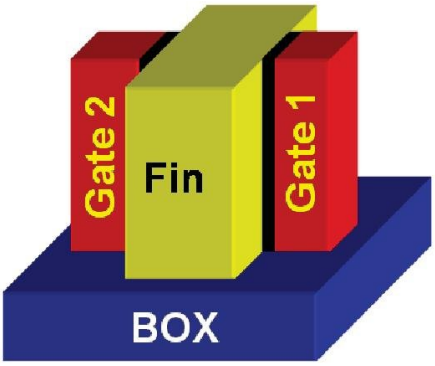


(a) Triple-gate FinFET on Bulk Si (b) Triple-gate FinFET on SOI

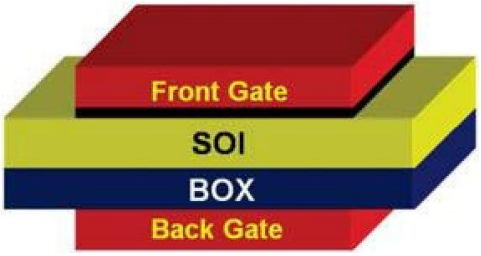


(c)Double-gate FinFET on SOI

(d) All-around Gate



(e) Independent Double-gate FinFET on SOI



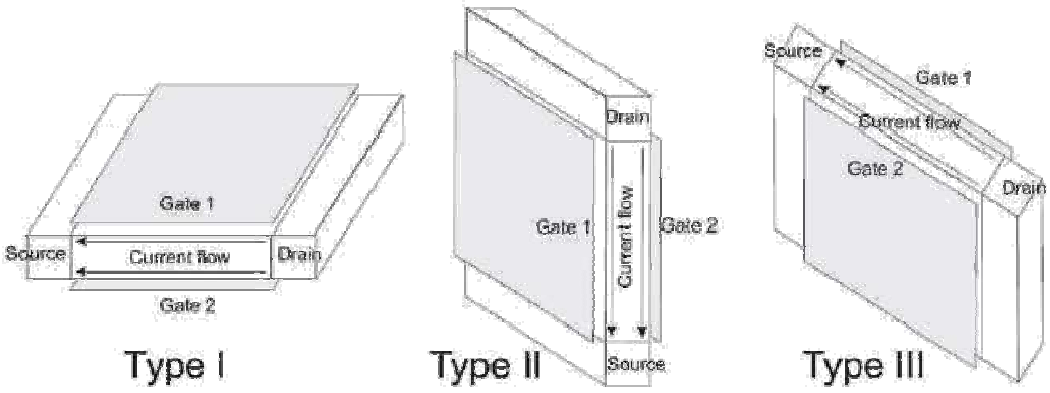
(f) Planar Double-gate SOI

Figure 2.14 Various Multi gate FETs(SOI-Semiconductor on insulator, BOX-Buried Oxide[20]

2.7 DG-MOSFET (Multi Gate Devices)

Double gate MOSFET (DG-FET) is a MOSFET that has two gates to control the channel. Its main advantage is improved gate-channel control. Because of its greater tolerance to SCE and with greater gate-channel control, the physical gate thickness can be increased (compared to planar MOSFET). Thus it also effectively controls the gate leakage current.

A DG-FET can be designed in three ways [21], labelled Types 1, 2 and 3 as shown in Fig. 3. Types 1 and 2 suffer mostly from fabrication problems, as it is hard to fabricate both gates of the same size and that too exactly aligned to each other. Also, it



Planar view Vertical view Fin

Figure 2.15: Three possible realizations of DGFETs[21]

is hard to align the source/drain regions exactly to the gate edges. More, in Type 1 DG-FETs, it is hard to provide a low-resistance, area-efficient contact at the bottom gate, as it is buried.

But the type 3 can be implemented easily and is in better position than the first two types. This type 3 led the way for double gate MOSFETs or multi-Gate MOSFETs. These type 3 structures are called FinFET.

Chapter 3

FinFET

The term FinFET was given by researchers of University of California, Berkeley(Profs. Chenming Hu, Tsu-Jae King-Liu and Jeffrey Bokor) to describe a nonplanar, double-gate transistor built on an SOI substrate, based on the earlier DELTA (single-gate) transistor design.[22] The distinguishing characteristic of the FinFET is that the conducting channel is wrapped by a thin silicon "fin", which forms the body of the device. The effective channel length of the device is depended on the thickness of the fin (measured in the direction from source to drain). It is an attractive successor of the single gate MOSFET because of its superior electrostatic properties and ease of manufacturability as compared to conventional MOSFETs.

3.1 Structure of FinFET

A Fully Depleted Lean Channel Transistor (DELTA) topology was introduced by D.Histamo in 1989. This DELTA topology was further developed for getting a better gate control. The shown DELTA structure is the predecessor of FinFET.[22]

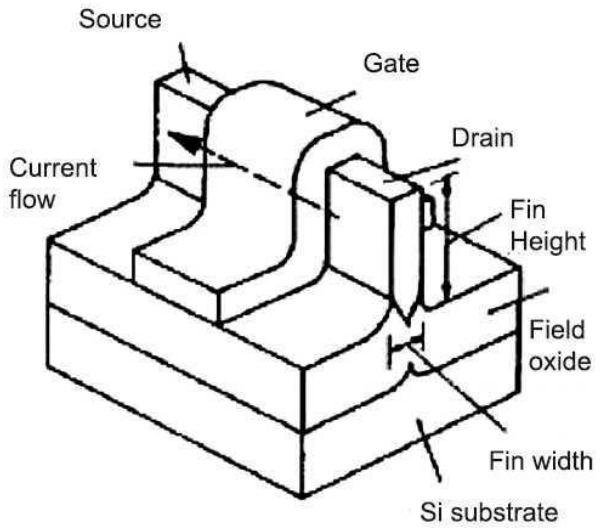


Figure 3.1: The DELTA structure[22]

The general FinFET structure is shown in Fig. 3.2. It is called so because of the thin channel region (body) stands vertically like the „fin□ of a fish between the source and drain regions. In the basic structure of the FinFET, the source, drain and fin are on a buried oxide layer(BOX). The fin is covered by dielectric material and this dielectric material is in turn covered by normally a polysilicon gate.

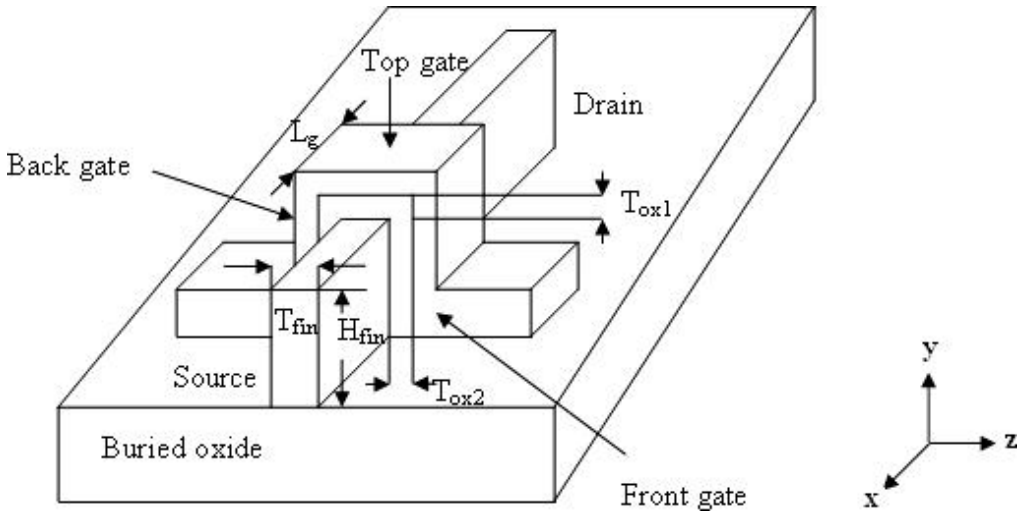


Figure 3.2 The FinFET structure[23]

The geometrical parameters of the FinFET are listed below:

(i) Gate length (*L*g): The physical gate length of FinFETs, or the printed gate length.
(ii) Fin height (*H*fin): The height of silicon fin, defined by the distance between the top gate and buried oxide layer (BOX).
(iii) Fin Width (*T*fin): The thickness of silicon fin, defined between the front and back gates. Tfin is also referred as Tsi or Wfin.
(iv) Top gate thickness (*T*ox1): The thickness of the top gate oxide.
(v) Front or back gate thickness (*T*ox2): The thickness of the front or back gate oxide.

3.2 Working of FinFET

In a FinFET the body or the fin is wrapped around by the gate in two/three sides, thus leading to higher gate-channel control and therefore reduced Short Channel

Effects. In strong inversion, conduction predominantly occurs close to the sidewalls, whereas in sub-threshold it occurs along the fin center (i.e. midway between the sidewalls). Even though current conduction is in the plane of the wafer, it is not strictly a planar device. It is rather referred to as a quasi-planar device, because its geometry in the vertical direction (viz. the fin height) also affects the behaviour of the device.

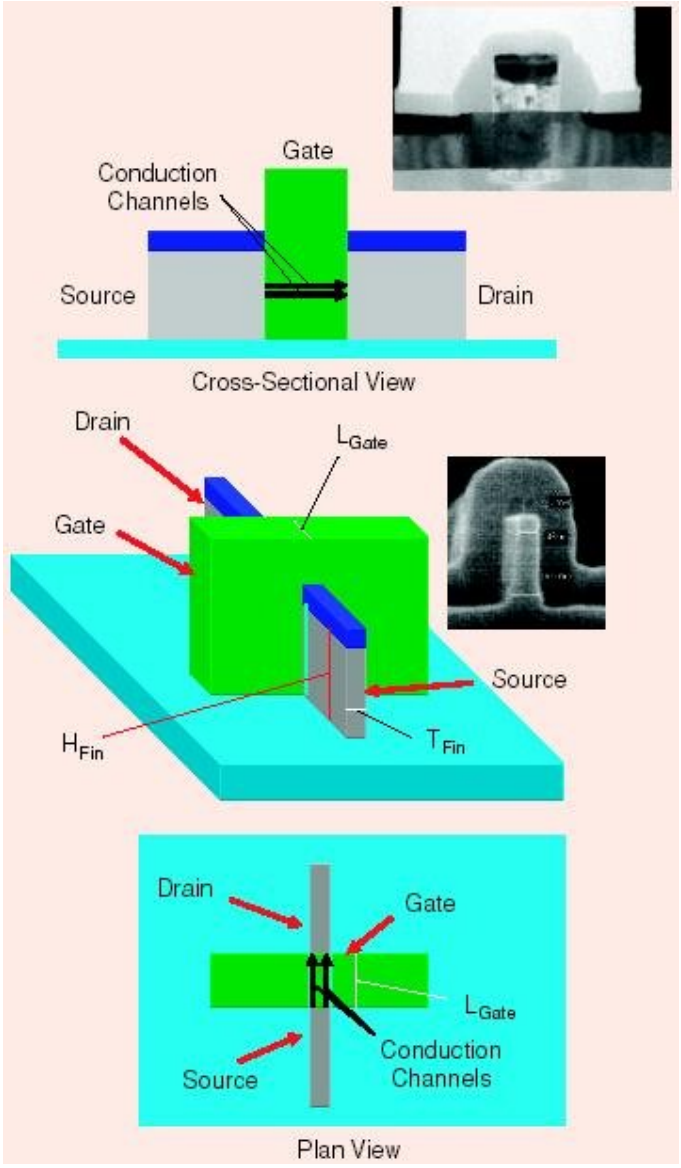


Figure 3.3 FinFET conduction path[24]

In a FinFET, the gate length L is the same as that in a conventional planar FET, whereas the device width W is quite different. W is defined as:

$$W = 2H_{fin} + T_{fin}$$

The above definition of device width is for a triple gate FinFET. If the gate above the fin is absent/ineffective, then the T_{fin} term in the above definition is taken out.

3.3 Fabrication of FinFET

The starting substrate for a FinFET is a SOI wafer with a buried oxide (BOX) thickness around 15-20 nm. The thickness of the silicon fin is about 8 nm, and the silicon is of lightly doped p-type with the dopant concentration of 1 × 10^16 cm^{-3} which ensures fully depleted device operation. The main steps in a FinFET fabrication process are those related to fin formation, gate stack formation, and source/drain extension formation. The FinFET fabrication can be done by two routes, either a "gate-first" route, or a "gate-last" route. Both routes have fabricate well working FinFETs down to 30 nm gate lengths. FinFETs are fabricated with fin widths that are typically less than one-half of the minimum gate lengths. E-beam lithography can be used to pattern the fins directly; but in this technique cost of equipment used is very high and manufacturing output is low, therefore this route is not much preferred. Hence fin patterning needs to use creative techniques in order to pattern such very small dimensions, like resist-defined fin (RDF) patterning and spacer-defined fin (SDF) patterning. These are two main techniques for fin definition which are discussed below.

Resist-defined fin (RDF) patterning

A schematic flow of the RDF process is illustrated in figure 3.4.

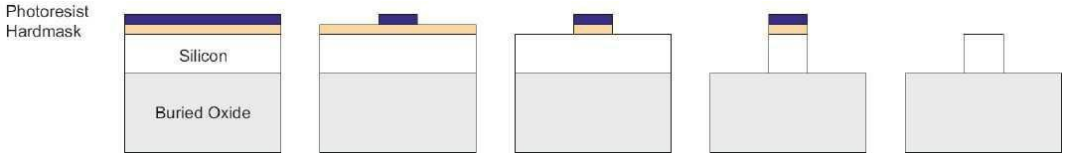


Figure 3.4 process flow for RDF Technology[25]

- First a thick hardmask is deposited on the silicon.
- Then there is deposition of positive photoresist and exposure using lithography to define the active areas.
- Unexposed areas of the photoresist are removed, which exposes the hardmask below, which is then etched using a HF-based etch process.
- Later trimming of the resist or hardmask stack is done to reduce the thickness down to the desired sublithographic dimension.
- Once again an aggressive, directional etch is done, this time etching into the silicon film, while the resist or hardmask combination serves to protect those areas that will eventually form the fins. This etch is continued till all the unprotected silicon has been etched away.
- Finally the hardmask on top of the silicon is also removed to show the fin areas.

The spacer-defined fin (SDF) patterning

A schematic of the SDF process is shown in Figure 3.5.

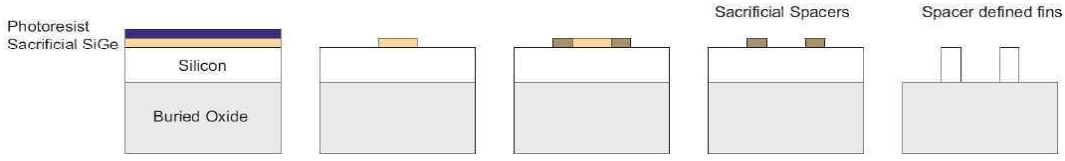


Figure 3.5 Process flow for SDF Technology[25]

- First a sacrificial SiGe film is deposited on top of the silicon film and patterned in a way that the width of the sacrificial SiGe will define the final fin-to-fin spacing.
- Then a thin nitride spacer along with the sidewalls of the SiGe is formed.
- After that SiGe film is removed, leaving behind the nitride spacers, which works as a hardmask during the subsequent etch of the silicon film.
- The thickness of the spacer turns into the resulting width of the fins.
- Depending on the process control and the desired fin widths, this process of sidewall spacer formation and etching can even be carried out one more time to result in even smaller fin widths.

- After fin width definition hydrogen annealing step takes place, to relax the stresses and defects at the surface which may have resulted due to aggressive etch chemistries employed for fin definition.

The next important section is of gate stack formation. There are two options: the "gate-first" approach and the "gate-last" approach.

- The gate-first approach:
  - First the gate dielectric is formed,
  - Then gate electrode is deposited on top.
  - Later the resist is deposited on top of this, and the stack having the gate dielectric, gate electrode, and the resist is patterned and subsequently trimmed to achieve the desired gate length.
  - Later the resist is removed.
- The gate-last approach:
  - In this source/drain is formed immediately after fin patterning.
  - Doped polysilicon or polycrystalline SiGe is deposited on the fin
  - Followed by a patterning which defines the source/drain extension regions.
  - Spacer is grown on the insides of this region, and is followed by gate stack deposition and patterning.

Using the SDF process high fin patterning densities can be obtained. The fin width is fixed in this technology, and it is not possible to use it for variable fin widths, since arbitrary fin widths are not supported in this technology.[25]

3.4 Current status of FinFET

Intel became the first company to adopt FinFET at 22 nm in 2011. The company is making its microprocessor using this new 3-D transistor.

Figure 3.6 shows a scanning electronic microscope (SEM) image of FinFET made using the new 22-nanometer manufacturing process by Intel. At a magnification of more than 100,000 times, the silicon fins are clearly visible as a series of walls projected above a flat surface.

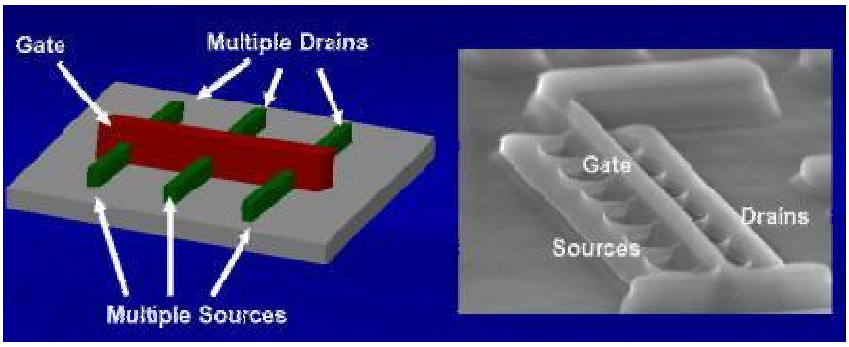


Figure 3.6 Schematic view (L) and SEM view (R) of Intel tri-gate transistors[26]

In April 2012 Intel's Ivy Bridge processors were launched which uses 22nm process technology with Intel's tri-gate FinFET. This processor incorporated 1.4 billion transistors on a die size of 160 mm^2. In this chip, at transistor level, each could produce upto 37 percent larger higher performance, while using 50 percent less power at the same performance.[26]

5nm FinFET has been demonstrated in industry fabrication and 3nm FinFET has been demonstrated in university lab.[27]

Chapter 4

Simulation

Device Simulations can give physical insight for explaining the effects observed through measurements. The simulations for this work are performed using a set of Silvaco tools, namely the Atlas Device simulator and DevEdit Device Structure Editor. The versions are 2.6.0.R for DevEdit 3D and 5.16.3.R. for Atlas 3D. Simulations are performed to know the effects of variation in fin width, fin height, oxide thickness and different materials for oxide in FinFETs. Interface effects, stress effects and quantum confinement were not taken into account.

To achieve accurate simulation results, the mesh should be denser in those regions of the device where the current density, electric field (depletion regions or interfaces) and charge generation are high. So the mesh is kept close to the Si-SiO_2 interface and the source and drain regions should be denser than other parts of the mesh. For device simulations the physical models used influence the electrical behaviour strongly. So the models should be chosen carefully. Because of the non-planar structure of FinFETs, 3D simulations are required to describe the full electric behaviour of the device. However, 3D simulations are time consuming.

4.1 Physical Parameters

The basic structure of the FinFET consists of a SiO_2 layer over which the silicon bar(Fin) and the source/drain are present. The fin is covered by a SiO_2 layer which again is covered by a polysilicon layer called the gate. The source and drain contacts are placed at the end of the source and drain junctions. The contacts source and drain are of aluminium. The temperature for simulation is set to 300 K.

Doping concentration in silicon bar is 1X16 cm^{-3} of p-type i.e. boron and the doping profile is uniform. Source and drain are heavily doped with 1X20 cm^{-3} of n-type i.e. phosphorus and the doping profile is gaussian for both the source and drain.

DEVICE DIMENSION

GATE LENGTH	30 nm
FIN HEIGTH	15 nm
FIN WIDTH	10 nm
GATE OXIDE THICKNESS	3 nm
BURIED LAYER THICKNESS	10nm
BURIED LAYER HEIGTH	20nm
GATE MATERIAL	Polysilicon
S/D CONCENTRATION	1x10e^20/cm3
CHANNEL CONCENTRATION	1x10e^16/cm3

Figure4.1 Device dimension of finfet

4.2 DESINNING THE FINFET USING ATLAS SIMULATION

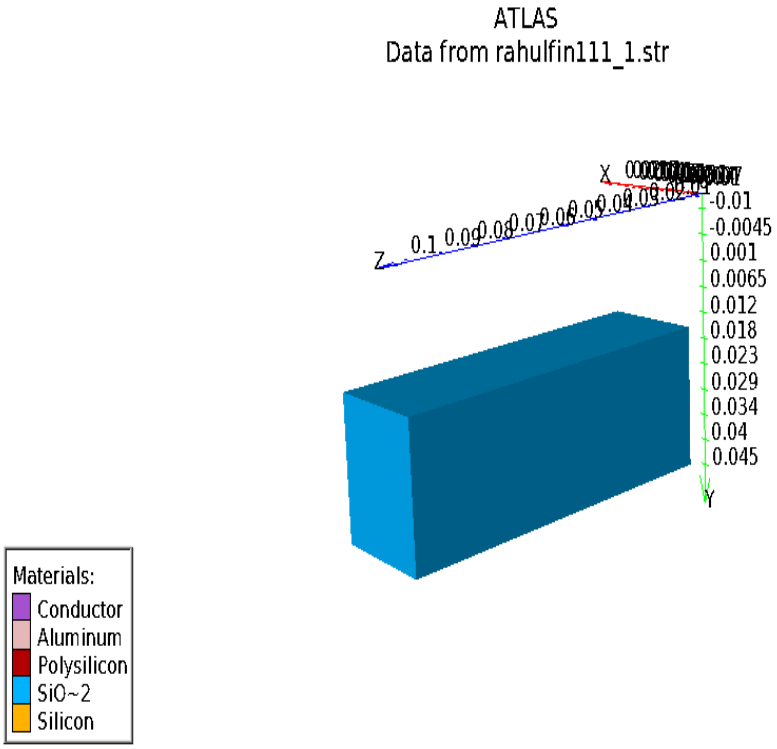


Figure4.2. Silicon substrate 100x40x20

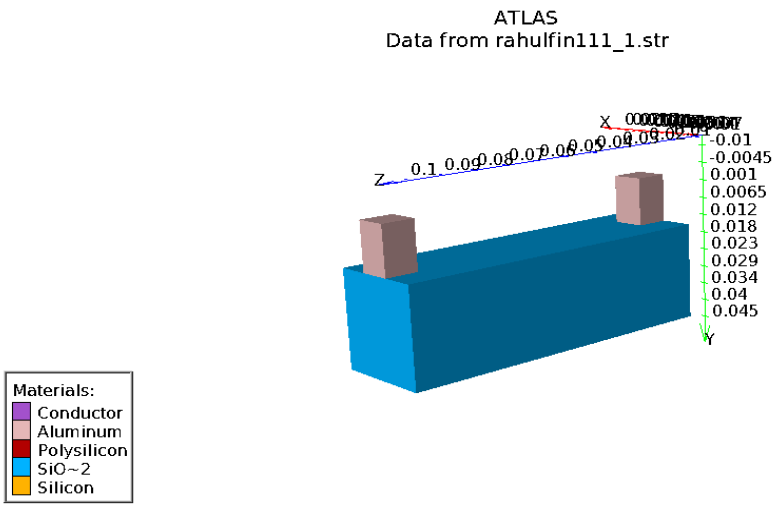


Figure4.3 Aluminium source and drain 15x15x15(nm)

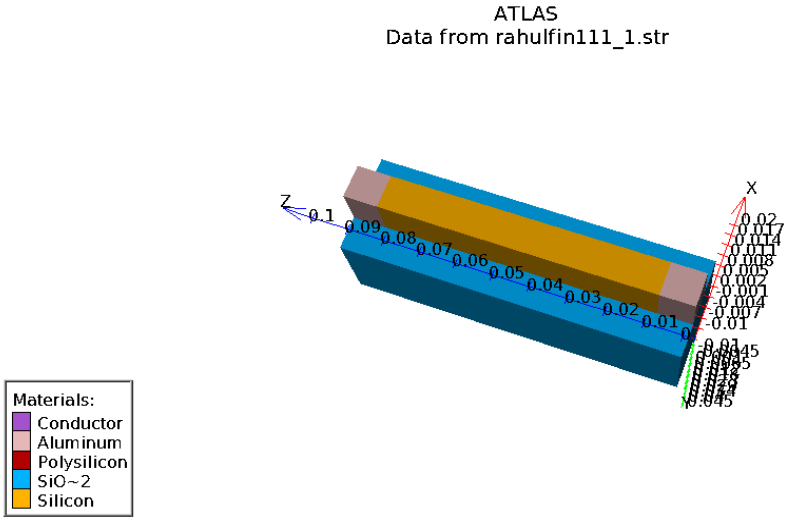


Figure4.4 Silico channel 70x15x15(nm)

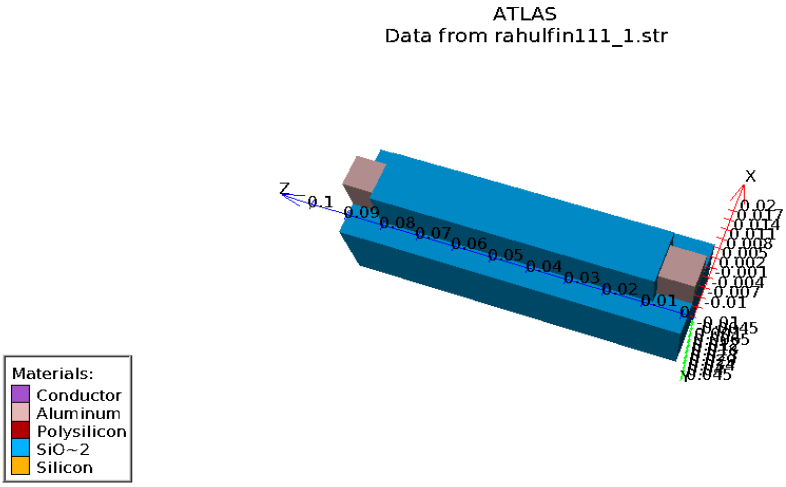


Figure 4.5 SiO2 over channel

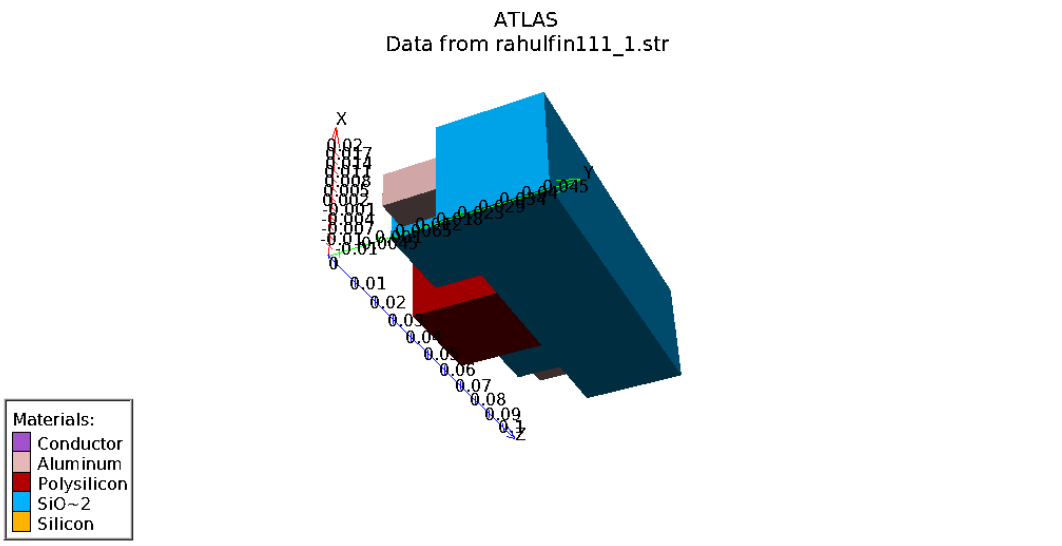


Figure4.6 Finfet 3d structure

After designing the finfet using atlas simulation , these structure are also called tony plot structure i.e these are the tony plots of finfet structure.

The basic structure of FinFET have dimension for SiO_2 Buried Oxide Layer 100nmX30nmX30nm (LXBXH) respectively. The height of the fin is 15 nm and the breadth is 10 nm. The oxide thickness is 3 nm thick at sides and 8 nm thick at top of fin making it a double gate device. The workfunction is kept about 4.60 eV. The various models used are cvt, consrh, fermi, fldmob, bgn.

4.3 SIMULATION RESULTS

The schematic structure of the device under condition is given in the Fig.. In case of the BOI FinFET , a localized insulator is introduced at the bottom of the channel region which can suppress the leakage current between the source and drain. Better heat dissipation is also expected due to the absence of insulator under Source/Drain (S/D) region. Complete 3D simulations of the devices were performed using SILVACO DevEDIT (3D), Atlas TCAD software. A self-consistent Schrodinger-Poisson with Bohm Quantum Potential model (BQP) [22] is used for the simulations. The various models used in this study are fldmob, hcte, srh, fermi and bqp. The mobility model fldmob specifies that parallel electric field is used. The conventional drift-diffusion model of charge transport neglects non-local effects, such as velocity overshoot and reduced energy dependent impact ionization. These effects are incorporated in this study by using an energy balance model, which uses a higher order approximation of

the Boltzmann Transport Equation. Since recombination effects are important, therefore, the concentration dependent Shockley–Read–Hall model (consrh) and Auger recombination model (auger) are activated in simulations. Similarly, we used Fermi-Dirac statistics for the simulation.

4.3.1 Short Channel Effects (SCEs)

The silicon fin thickness, gate oxide thickness, BOX thickness, junction depth, and channel length are the important parts of the device from an electrostatic point of view to control threshold voltage roll-off, DIBL, and subthreshold swing. The main SCEs are the threshold voltage roll-off due to charge sharing, the degradation of subthreshold swing(S), and the Drain induced barrier lowering(DIBL). These effects result in an increase in the OFF current (Ioff), decrease in threshold voltage (Vth) and the deterioration of the ON–OFF current ratio (Ion/Ioff). Electrostatic integrity relates both DIBL and threshold voltage roll-off SCE and describes the quality of electrostatic control of the channel by the gate .

4.3.2 Subthreshold Swing(S)

The subthreshold swing indicates how fast a device can react to a changing voltage level. This parameter is very important in gauging the speed of a device. Here, the variation of subthreshold swing of the simulated device against the underlap length is presented in fig. Subthreshold swing is calculated from ID-VGS plot by,

Subthreshold Swing=ΔVg(mV)/ΔlogId(decades) (1)

Where ΔVg is change in gate voltage,Δ Id is change in drain current.

As can be observed from the graph there is subthreshold swing decreases as Vds increasing.

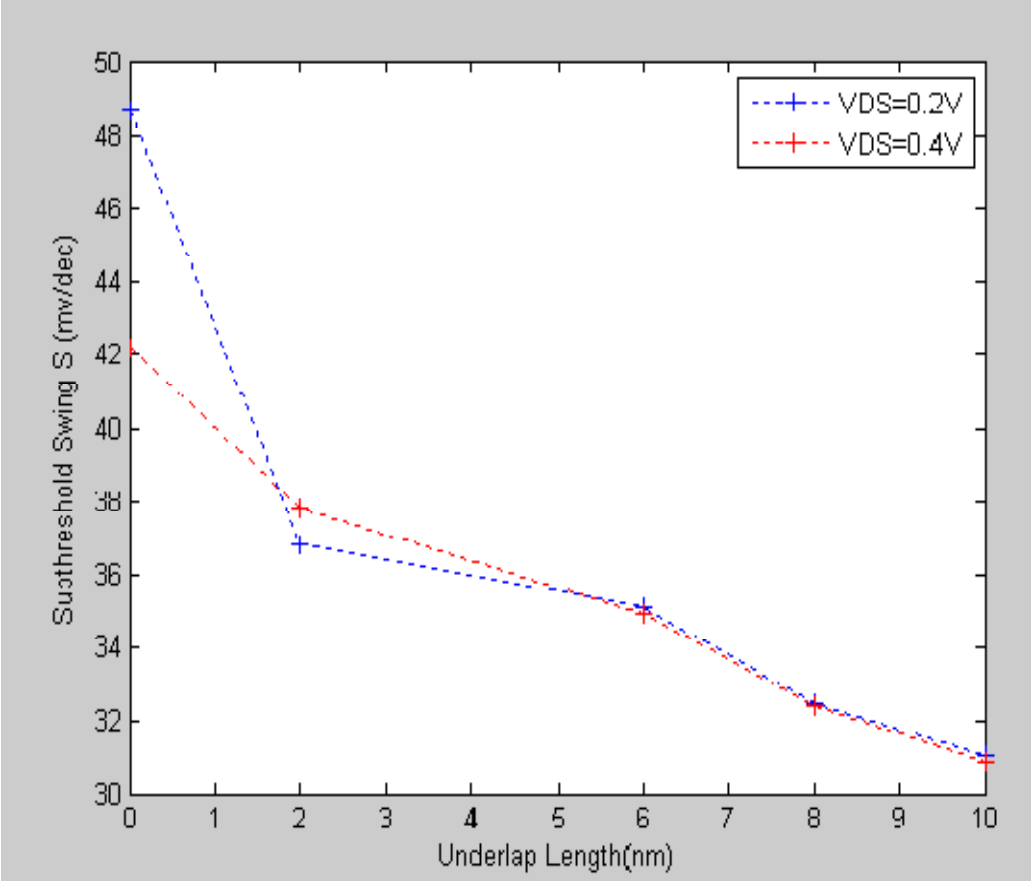


Figure4.7 subthersold swing vs length

4.3.3Threshold Voltage (Vth)

The continuation of scaling of bulk MOSFET in the nanometer range (<65 nm) has become extremely difficult as the performance of bulk MOSFET is severely degraded by short channel effects which includes threshold voltage roll off problem. As the underlap length increases control of drain over channel reduces resulting increase in threshold voltage. The variation of threshold voltage (Vth) with a change in underlap length is shown in Fig.. Hence problem of threshold voltage roll off can be resolved by changing underlap length. The required threshold voltage can be set by changing underlap Length.

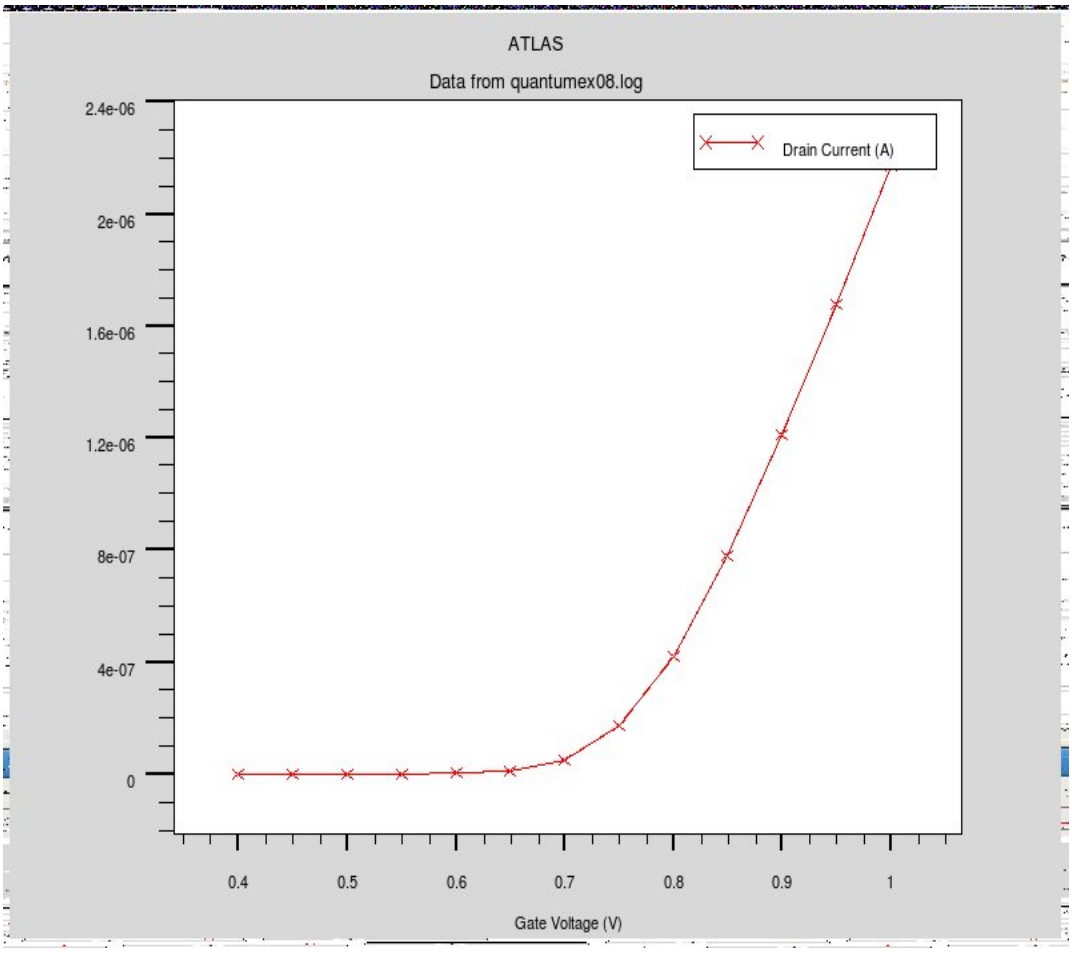


Figure 4.8 id vs vth

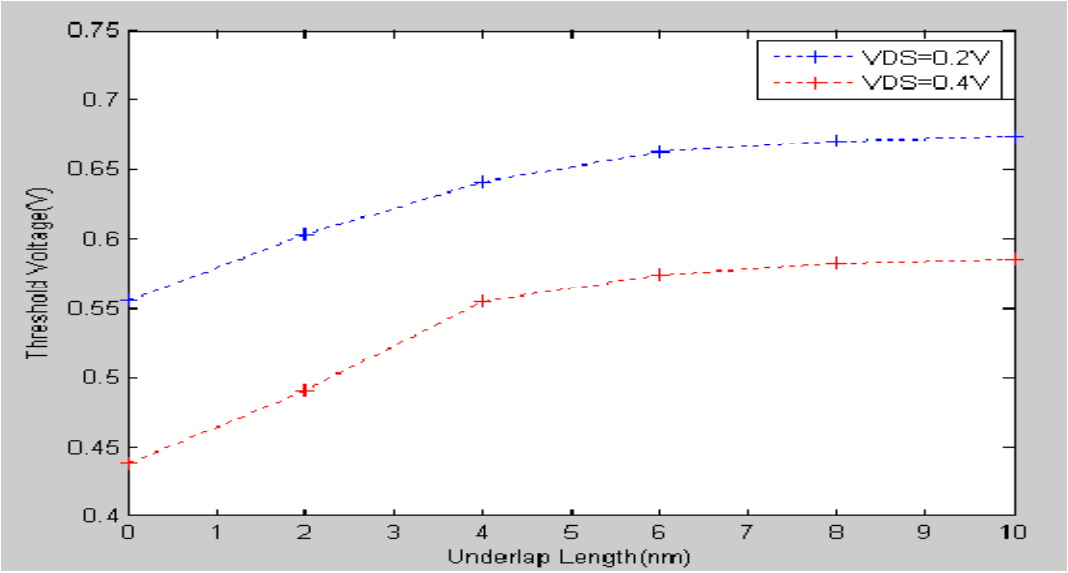


Figure4.9 Vth vs length

4.3.4 Leakage Current (IOFF)

The model for the subthreshold drain leakage current (VGS = 0) is given by [6], [7],

IOFF = μCG (W/L)(m − 1) [kBT/q]2 exp[-qVT /mKBT] (3)

where m is the ideality factor, which can be expressed as

m = 1 + γ (C/CG) (4)

Where CG is the gate-to-channel capacitance, C represents the Channel-to-bulk capacitance. Leakage current in the device increases the power dissipation unnecessarily and degrading the device lifetime. It is found that leakage current is lower for lower Vds.

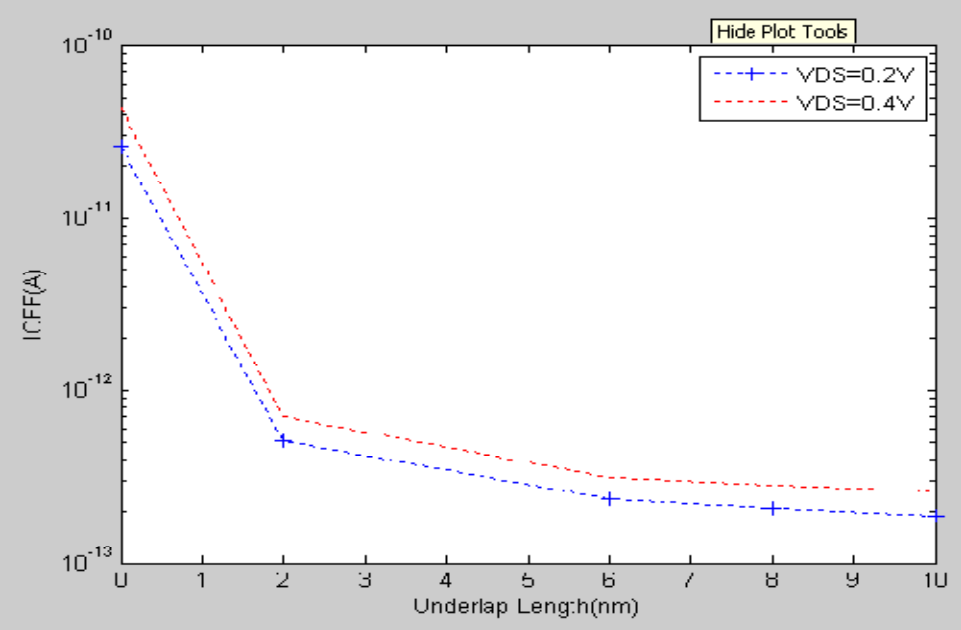


Figure4.10 Ioff vs length

4.3.5 DIBL

The fundamental electrical limitation in VLSI will be the spacing of the surface diffusions that form p-n junctions. Reverse bias on one diffused junction creates a field pattern that can lower the potential barrier separating it from an adjacent diffused junction. When this barrier lowering is large enough, the adjacent diffusion behaves as a source, resulting in an unwanted current path. But in BOI FinFET with increased underlap length DIBL is found to minimum at 4nm length

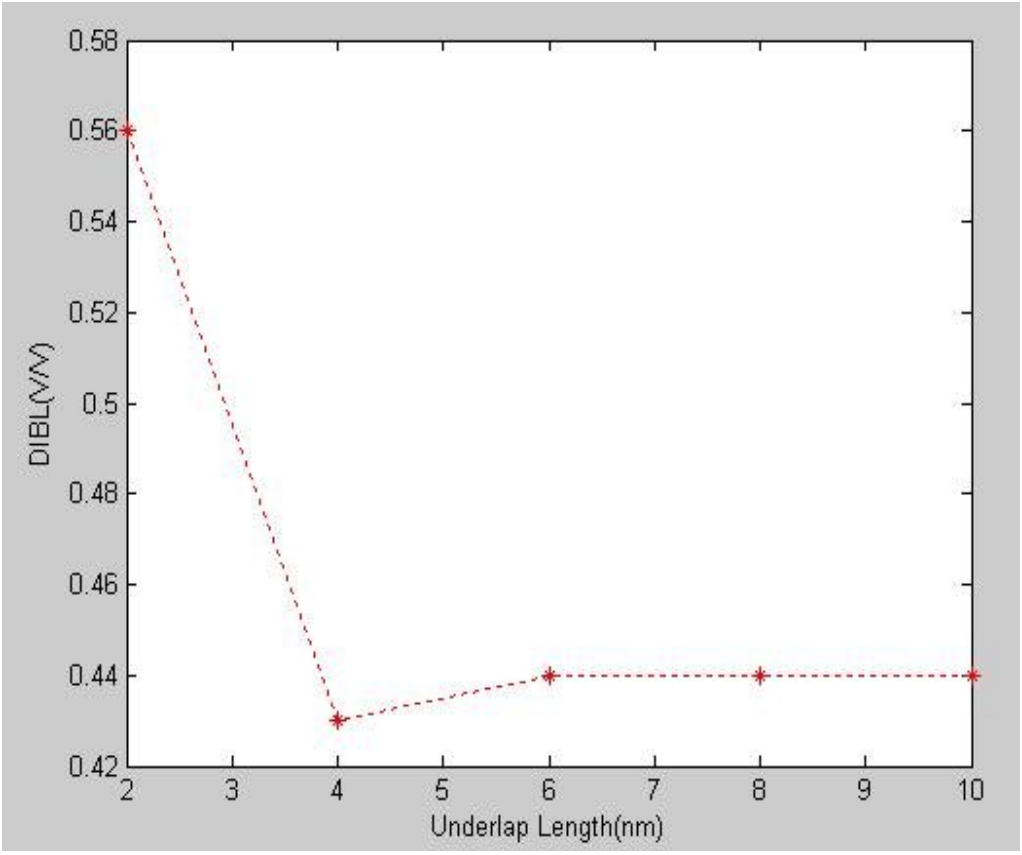


Figure4.11 Dibl vs length

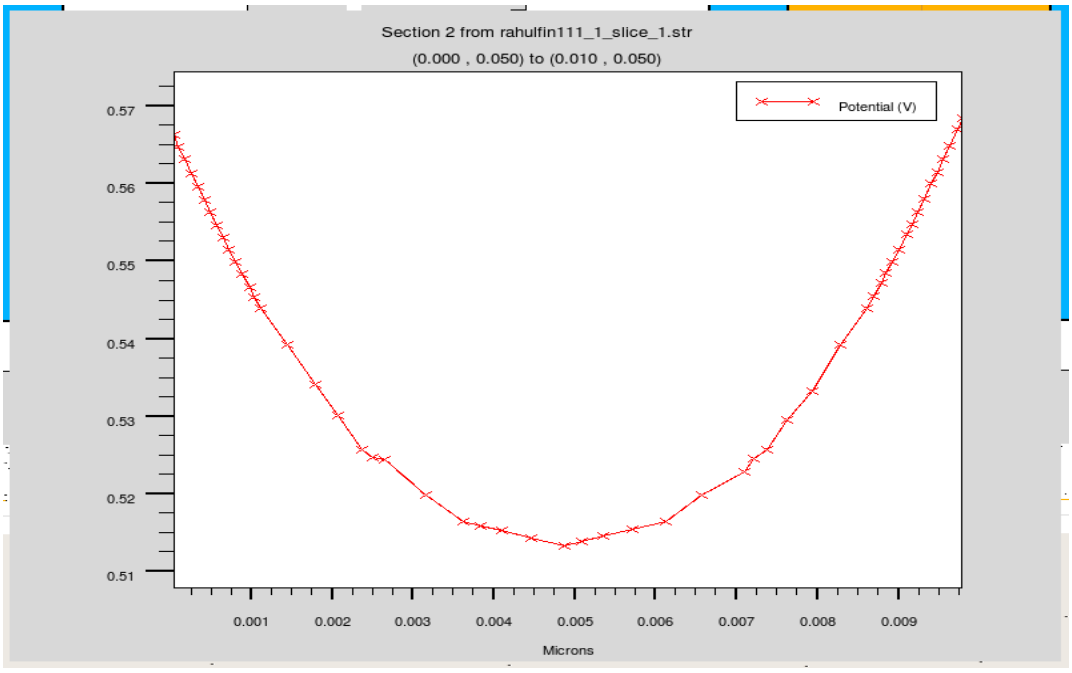


Figure4.12 Vth vs length(at Vds=0.2)

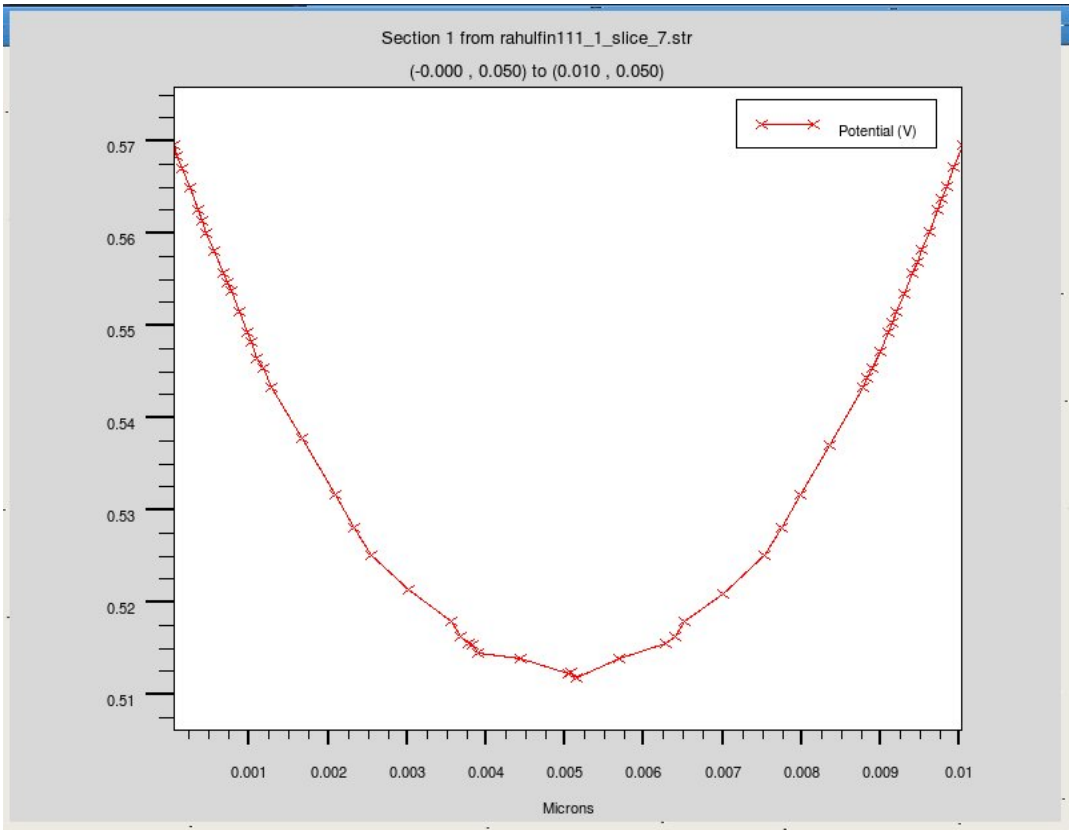


Figure4.13 Vth vs length (at Vds=0.4)

4.3.6 Drain Current (I_{ON})

Drain current is found to be lower for lower value of Vds. This drain current as high as possible the better will be the conduction of finfet, after reaching thersold value the drain current increases very fast than usual.

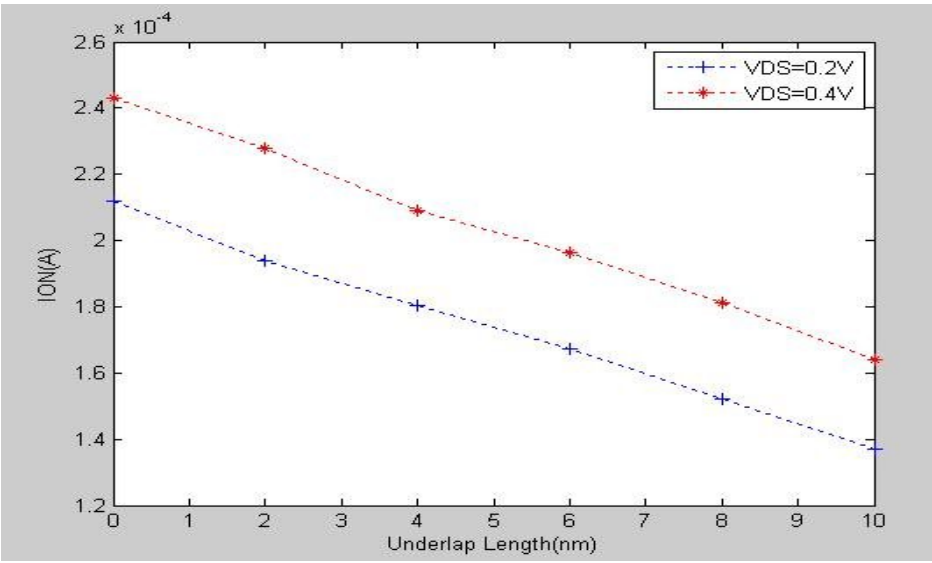


Figure4.14 Ion vs length

4.3.7 I_{ON}/I_{OFF}

The ratio ION/IOFF is also found to be increases for lower value of Vds , for same nderlap length.

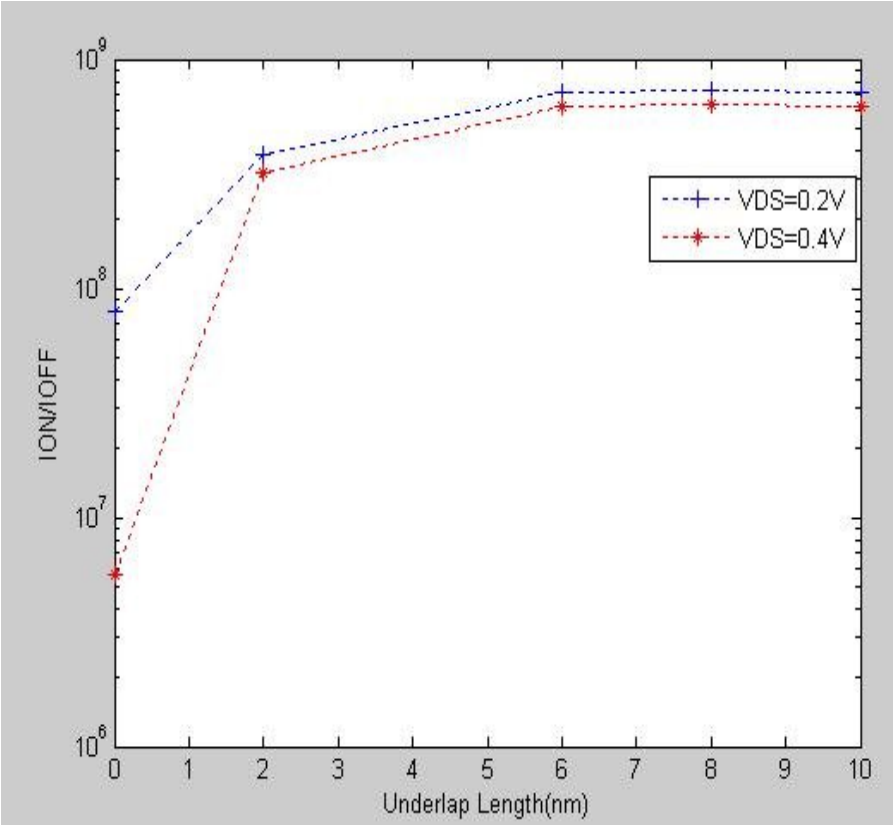


Figure 4.15 Ion/Ioff vs length

5 CONCLUSION:

A 3-D simulation of BOI triple gate FinFET device with underlap has been performed. The incorporation of underlap with BOI FinFET device has resulted in a significant improvement in SCEs, particularly DIBL reduces , leakage current reduces and ION/IOFF increases .The reduction in leakage current reduces power dissipation when device is in off condition. This avoids heating, increases lifetime and ultimately the reliability of the device.

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