

LIST OF FIGURES

Fig. No.	Description
Fig.1.1.	Active power filter connected to non-linear load
Fig.1.2.	Block Diagram of UPQC
Fig.2.1.	Schematic diagram of a solid state current limiter
Fig.2.2.	Schematic diagram of a static transfer switch
Fig.2.3.	Schematic diagram of ideal load compensation
Fig.2.4.	(a) Ideal voltage controller
Fig.2.4	(b) its practical realization
Fig.2.5.	Schematic diagram of a sensitive load protected by a DVR
Fig.2.6.	(a) Schematic diagram of a UPQC compensated system,
Fig.2.6.	(b) & (c) two alternate connections
Fig.3.1.	Left shunt UPQC
Fig.3.2.	Types of topologies of UPQC
Fig.3.3.	A typical UPQC system connected with energy storage
Fig.4.1.	Connection diagram of UPQC
Fig.4.2.	Equivalent single-phase circuit corresponding to harmonic
Fig.4.3.	Simulation scheme for hysteresis current control
Fig.4.4.	Pulse generation by hysteresis band control
Fig 5.1	Simulation model of rectifier fed RL load connected at PCC without UPQC.
Fig. 5.2.	Load Voltage and Source Current without UPQC
Fig.5.3.	THD in source current without UPQC.
Fig.5.4.	THD in Load voltage without UPQC.
Fig.5.5.	Simulation model of circuit with rectifier fed RL load using UPQC.
Fig.5.6.	Load Voltage and Source Current waveform with UPQC
Fig.5.7.	THD in Load Voltage using UPQC.
Fig.5.8.	THD in source current using UPQC.
Fig.5.9.	DC Link Voltage

LIST OF TABLES

Table 1.1	PQ Problems and their causes
Table 1.2	Power Quality (PQ) Standards
Table 5.1	System Parameters
Table 5.2	Simulation result
Table 5.3	Performance analysis of UPQC