CHAPTER 1:INTRODUCTION

1.1 MOTIVATION

Energy dissipation being an important concern in VLSI design, led engineers to think of alternative logic styles such as reversible logic gate having lower power consumption. Reversible circuits are those circuits that do not lose information as the amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation and the number of bits lost in reversible circuits is zero, so it doesn't lose energy. These circuits can generate unique output vector from each input vector, and vice versa, that is, there is a one-to-one mapping between the input and output vectors. Further, Landauer [1] has shown that for irreversible logic computations, each bit of information lost generates kTln2 joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which the computation is performed. Bennett [2] showed that kTln2 energy dissipation would not occur if a computation is carried out in a reversible way Furthermore, voltage-coded logic signals have energy of $E= ½CV^2$,and this energy gets dissipated whenever switching occurs in conventional (irreversible) logic implemented in modern CMOS technology. The important cost metrics in the design and synthesis of reversible logic circuits are the quantum cost, delay and the number of garbage outputs [3], [4]. The garbage outputs [5,6] are the unutilized outputs in reversible circuits which exist just to maintain reversibility but do not perform any useful operations. Hence, the primary goal in reversible logic design and synthesis is to minimize the quantum cost, delay and the garbage outputs [5], [6].Now a days, due to the need for low-power design and the emerging field of nanotechnology, reversible computing has become more attractive. It plays an important role in the field of low-power circuit designs and computational nanotechnology [27]. The role of computational nanotechnology and nano mechanics has become critically important in the cycle of growth and development of nanotechnology. They can also be used to design low power arithmetic and data path units for digital signal processing applications, such as the designs of low power adders, multipliers, FFT, IDCT etc, and quantum computers

1.2 Thesis Organization

In this work, a new reversible logic gate called ABCD gate is proposed. It is a 5x5 ABCD gate which provide more logic functions than available 5x5 logic gates. The thesis is organized in six chapters including the introduction chapter. In Chapter 2, the literature survey on reversibility is presented first and then available 2x2 reversible logic gates are discussed. The chapter 3 describes various 3x3 and 4x4 reversible logic gates. Thereafter a 5x5 gate namely ABCD gate is proposed in chapter 4 and is compared with existing 5x5 gates. The proposed gate can realize basic gates and universal gates, half adder, half subtractor, Decoder/ Demux, Comparator, Odd and Even parity detector, Odd and Even Parity generator and Equality Detector: In chapter 5, the simulation results of applications based on proposed gate are given. All the simulations in this thesis are carried out using **.35 µm** technology parameters. Finally the thesis is concluded in chapter 6 and scope for the future work is also given**.**

CHAPTER 2: LITERATURE SURVEY

In this chapter, the concept of reversibility in universal computing machine is discussed. The definition of reversible logic gates and the performance evaluation criterion is described briefly. The Feynman gate (a 2 x 2 reversible logic gate) is explained and its functionality is verified using SPICE simulations.

2.1 REVERSIBILITY

Conventional combinational logic circuits (irreversible hardware) dissipate heat for every bit of information that is lost during their operation and cannot be recovered in any way. However, the information can be recovered if the reversible logic gates are used to construct the circuit. In 1960s, R. Landauer [1] demonstrated that there is energy dissipation due to information loss even if an improved technology is used to construct the circuits and systems using irreversible hardware. It is shown that the loss of one bit of information dissipates **KTln2** Joules of energy where K is the Boltzmann's constant and T is the absolute temperature at which the operation is performed. Later Bennett [2], in 1973, showed that this KTln2 Joules of energy dissipation in a circuit can be avoided if it is constructed using reversible logic circuits. A reversible logic gate is an n-input, n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs but also the inputs can be uniquely recovered from the outputs. Extra inputs or outputs are added so that the number of inputs is made equal to the number of outputs whenever it is necessary. An important constraint present on the design of a reversible logic circuit is that fan-out is not allowed. A reversible circuit should be designed using minimum number of reversible gates. One key requirement to achieve optimization is that the designed circuit must produce minimum number of garbage outputs [5, 6].

Clausius demonstrated that it is not possible for a single transfer of heat from a body of lower temperature to a body of higher temperature without another connected change taking place at the exact same time. Whenever some quantity of heat Q is converted into work W, another quantity of heat must necessarily be transferred from a warmer to a colder body. The value of Q may be related to the converted work and the equivalent heat per unit of work A, and this relation is shown below:

$$Q = U + A*W$$

The value for *U* is determined by the initial and final states of the system, *W* is the work done by the system, and *A* is the equivalent heat per unit of work. In a cyclical process – meaning that the initial state and final state of a system are identical – *U* is 0, which reduces the equation to

$$Q=A*W$$

According to Clausius the rate of change of entropy of a system to be equivalent to the rate of change of heat in a system divided by the temperature function. Therefore, the change in entropy in a system is determined by

$$S=S_0 +\int (dQ/dT)$$

The value of *S* denotes the transformation content of the body, and this value is defined as the *entropy* of the body. In a reversible system, the integral is equal to zero, reducing to $S = S_0$. Resultantly, reversible systems generate zero entropy gain through their transformations.

The relationship shown below is between the number of particles *N* of an ideal gas in an isolated system, a volume *V*, constant energy *U* is as a function to determine the number of microstates of the particles in the system by relating them to the mass of an atom *m* and Planck's constant.

$$S = \Omega(U,V,N) = \left[\left(\frac{2\pi mkT}{h^2}\right)^{3/2} \frac{Ve^{5/2}}{N^{5/2}}\right] \approx e^N$$

The relationship between the gas constant and Avogadro's number, which is the numerical constant representing the proportion between the logarithm of the microstates came to be known as Boltzmann's constant, *k*.

$$S= k \ln (U,V,N)$$

$$S= k \ln (W)$$

where, W is the number of possible energy states in the system:

Reversibility in a Universal Computing Machine

Turing presented the notion of a *universal computing machine* in as a single automatic machine where its operation is completely determined by its configuration, prints either a 0 or a 1, and is able to compute any computable sequence. Feynman noted in that both natural laws and rules for computing are reversible, which allows for a computer to utilize quantum mechanics in order to produce computations without producing any entropy gain. Landauer raised the possibility in that it was not possible to design a computer that is physically reversible. He described a simple binary device as consisting of a particle in a bistable potential well, where the particle may either be at state '0' or state'1'. Using the bistable potential well, he described an irreversible operation called "restore to one," where the particle's output state was '1' regardless of the input state, meaning that the bijectivity of the device is lost, and it is not physically reversible. Since the input states and output states are discrete, and a binary computing device may only reach a state of '0' or '1', then the total number of probabilities for each input line is 2. Therefore, the maximum number of probabilities for N inputs is 2^N.Landauer substituted this quantity for W in Boltzmann's equation to relate these probabilities to the entropy change for each computing cycle. As an example, he presented a three-input, three-output device that had eight possible input states and only four possible output states, as shown in Table 2.1.

The probability of each input state – the values of A, B and C - occurring is 1/8.However, the probabilities of each output state – the values of P, Q and C - are different. The probability of (0; 0; 0) and (0; 1; 1) are 3/8 each, and the probability of (0; 0; 1) and (1; 1; 1) are both 1/8

Table 2.1 : Table presented by Landauer

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	0	0	0
0	1	1	0	1	1
1	0	0	0	0	0
1	0	1	0	1	1
1	1	0	0	0	1
1	1	1	1	1	1

Heat generation Q per computing cycle

K ln(2^{Nout}) – K ln(2^{Nin}) = $\iint_{Nin}^{Nout} \frac{dQ}{T}$

K Nout ln(2) – k Nin ln(2)= $\int_{Nin}^{Nout} \frac{dQ}{T}$

K ln (2) (Nout – Nin)= $\int_{Nin}^{Nout} \frac{dQ}{T}$

Q= kT ln(2)

K($\sum Pout$ * ln(Pout) –$\sum Pin$ * ln(Pin))

K((2*$\frac{3}{8}$*ln$\frac{3}{8}$ + 2*$\frac{1}{8}$*ln$\frac{1}{8}$) –(8*$\frac{1}{8}$*ln$\frac{1}{8}$))

$\frac{3}{2}$ K ln(2)

2.2BASIC REVERSIBLE LOGIC GATES

2.2.1 Reversible logic gate

It is an n-input n-output logic function in which there is a one-to-one correspondence between the inputs and the outputs. The input vector can be uniquely determined from the output vector due to bijective mapping. This prevents the loss of information which is the root cause of power dissipation in irreversible logic circuits. In the design of reversible logic circuits the following points must be considered to achieve an optimized circuit. They are

- Fan-out is not permitted.
- Garbage outputs must be minimum [5] [6]
- Minimum delay
- Minimum quantum cost.

Some of the important basic reversible logic gates are, Feynman gate[7],Toffoli gate[8], Fredkin gate[10] Peres gate[12] , R- gate[14], URG gate[15], TR gate[17], NFT gate[17], new BJN gate[17], SCL gate[17], MCL gate[17], MKG gate [18], DPG gate [19] ,BVF gate[20] etc. The reversible logic gates are classified on the basis of number of inputs and number of outputs they have, and the classification is as follows:

(i) 2 X 2 Gates {two inputs and two outputs} [7]

(ii) 3 X 3 Gates {three inputs and three outputs} [8], [10], [12], [17]

(iii) 4 X 4 Gates {four inputs and four outputs} [18], [19], [20],[21]

(iv) 5 X 5 Gates {five inputs and five outputs} [21],[18],[22]

The Feynman gate is explained in the following section.

2.2.2 Feynman / CNOT Gate:

The Feynman gate [7] is a 2x2 reversible gate and used in reversible logic synthesis. The block diagram of the gate is shown in Fig 2.1. It has two inputs A, B and two outputs P, Q. The input output relationship is given as

$$P=A \tag{2.1}$$

$$Q=A \oplus B \tag{2.2}$$

The Quantum cost of the gate is one. To verify the functionality of the gate, (2.1) – (2.2) are implemented using transmission gates and SPICE simulations are carried out using 0.35 μm CMOS technology parameters

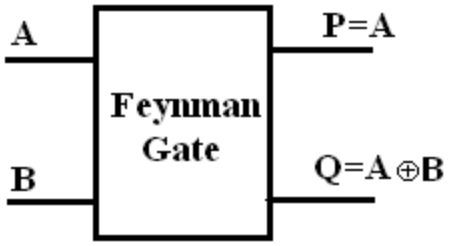

Fig 2.1 Feynman Gate – 2x2 gate

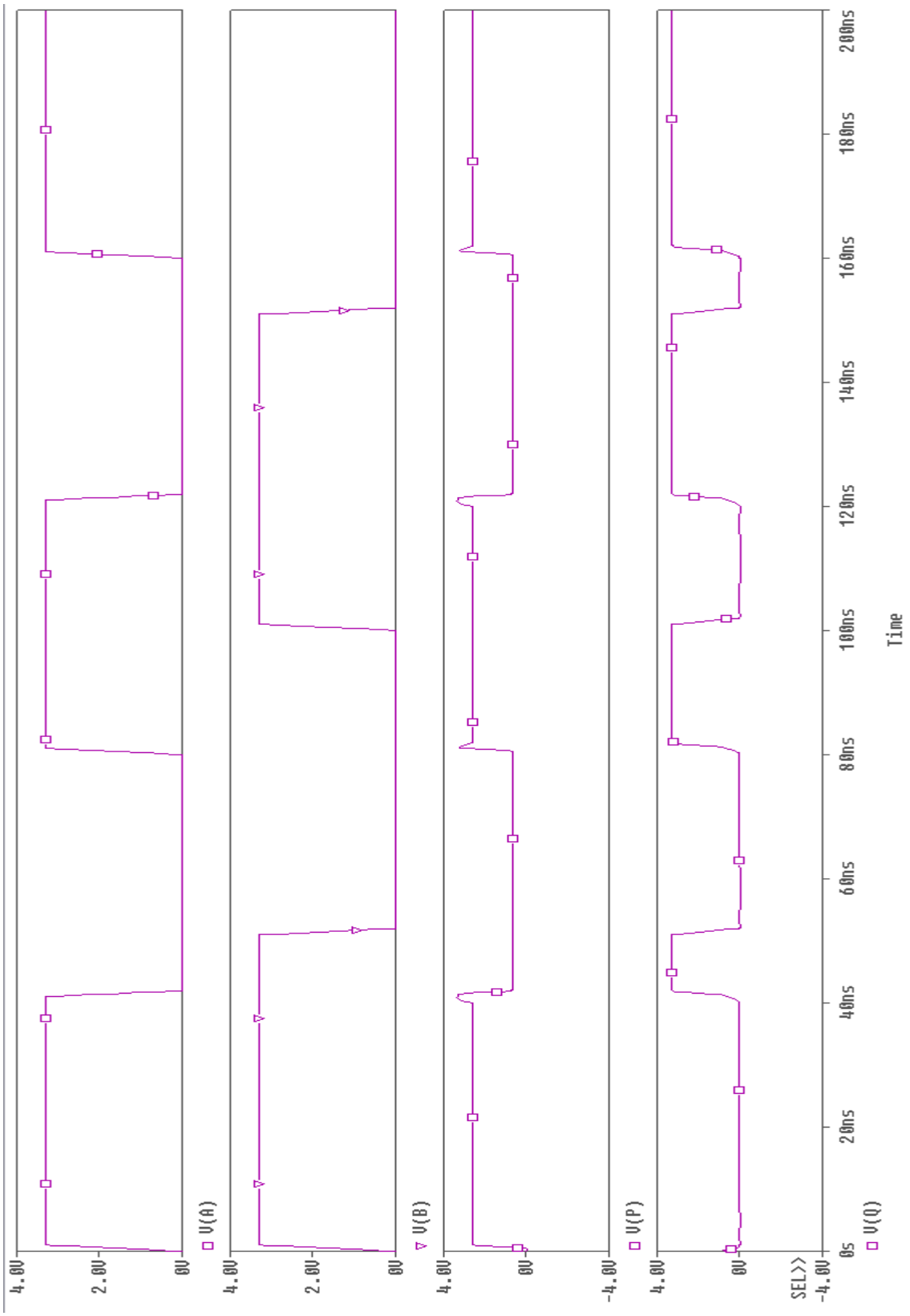

Fig 2.2 Input output waveform of Feynman Gate – 2x2 gate

CHAPTER 3: "3 X 3 AND 4X4 REVERSIBLE LOGIC GATES"

A wide variety of 3 x 3 and 4 x 4 reversible logic gates are available in the literature. In this chapter the functionality of Toffoli gate [8], Fredkin gate [10], Peres gate [12], R-gate [14], URG gate [15], new Reversible BJN gate [17], MCL gate [17], MKG gate [18], DPG Gate[19], BVF Gate[20],etc are discussed and their functionality is verified using SPICE simulations.

3.1: 3 X 3 GATES:

3.1.1 Toffoli Gate:

The Toffoli gate [8] is a 3x3 reversible gate used in reversible logic synthesis. The block diagram of the gate and its circuit implementation is shown in Fig 3.1(a) and Fig 3.1(b). It has three inputs A, B and C; and three outputs P, Q and R. The input output relationship is given as

$P=A$ (3.1)

$Q=B$ (3.2)

$R=AB\oplus C$ (3.3)

The Quantum cost of the gate is five. The truth table of the Toffoli Gate is given in Table 3.1. To verify the functionality of the gate, (3.1) – (3.3) are implemented using transmission gates and SPICE simulations are carried out using 0.35 μm CMOS technology parameters. The simulation results are shown in Fig. 3.2.Toffoli gate is used to implement reversible binary coded decimal adder [9].

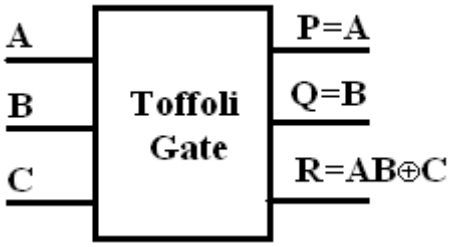

Fig 3.1(a) Toffoli Gate

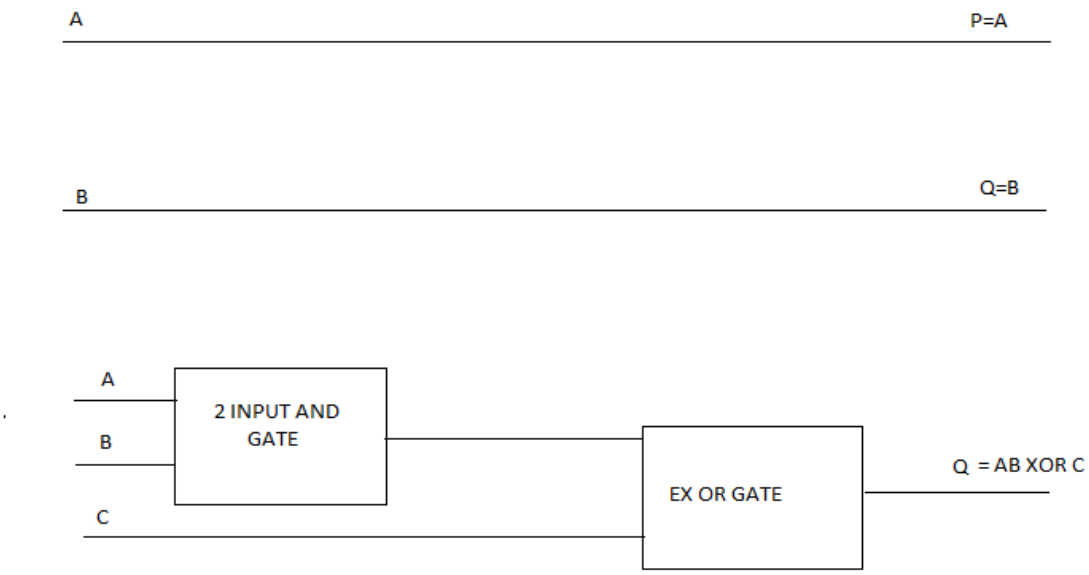

Fig 3.1(b) Circuit diagram of Toffoli gate

Table 3.1: Truth table of Toffoli

A	**B**	**C**	**P**	**Q**	**R**
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

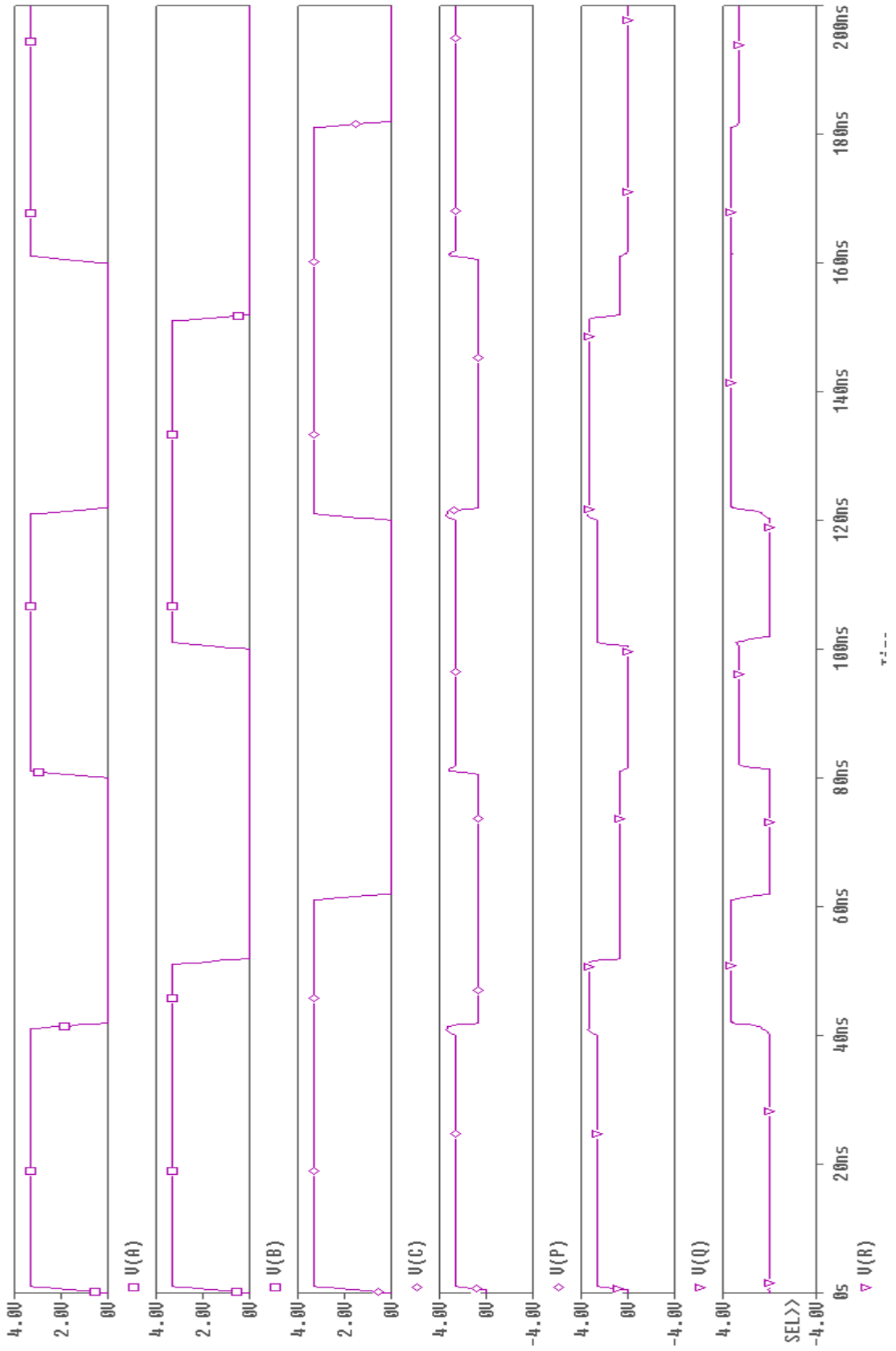

Fig 3.2 Input output waveform of Toffoli Gate

3.1.2 Fredkin Gate:

The Fredkin gate [10] is a 3x3 reversible gate used in reversible logic synthesis. The block diagram of the gate and its circuit implementation is as shown in Fig 3.3(a) and Fig 3.3(b) respectively. It has three inputs A, B and C; and three outputs P, Q and R. The input output relationship is given as

P=A (3.4)

Q=A'B+AC (3.5)

R= AB+A'C (3.6)

The Quantum cost of the gate is five. The truth table of the Fredkin Gate is given in Table 3.2. To verify the functionality of the gate, (3.4) – (3.6) are implemented using transmission gates and SPICE simulations are carried out using 0.35 μm CMOS technology parameters. The simulation results are shown in Fig. 3.4. It provides two output functions in contrast to one in Toffoli Gate. Further it may be noted that the inputs B and C are routed to exchanged or same output port depending upon the value of input A. Moreover this gate is used to design reversible PLA [11].

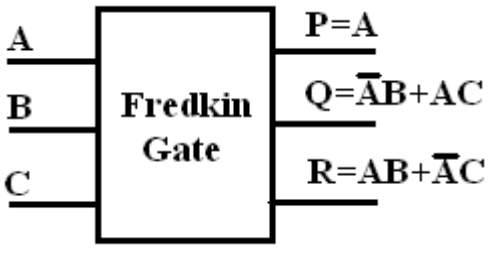

Fig 3.3(a) Fredkin gate

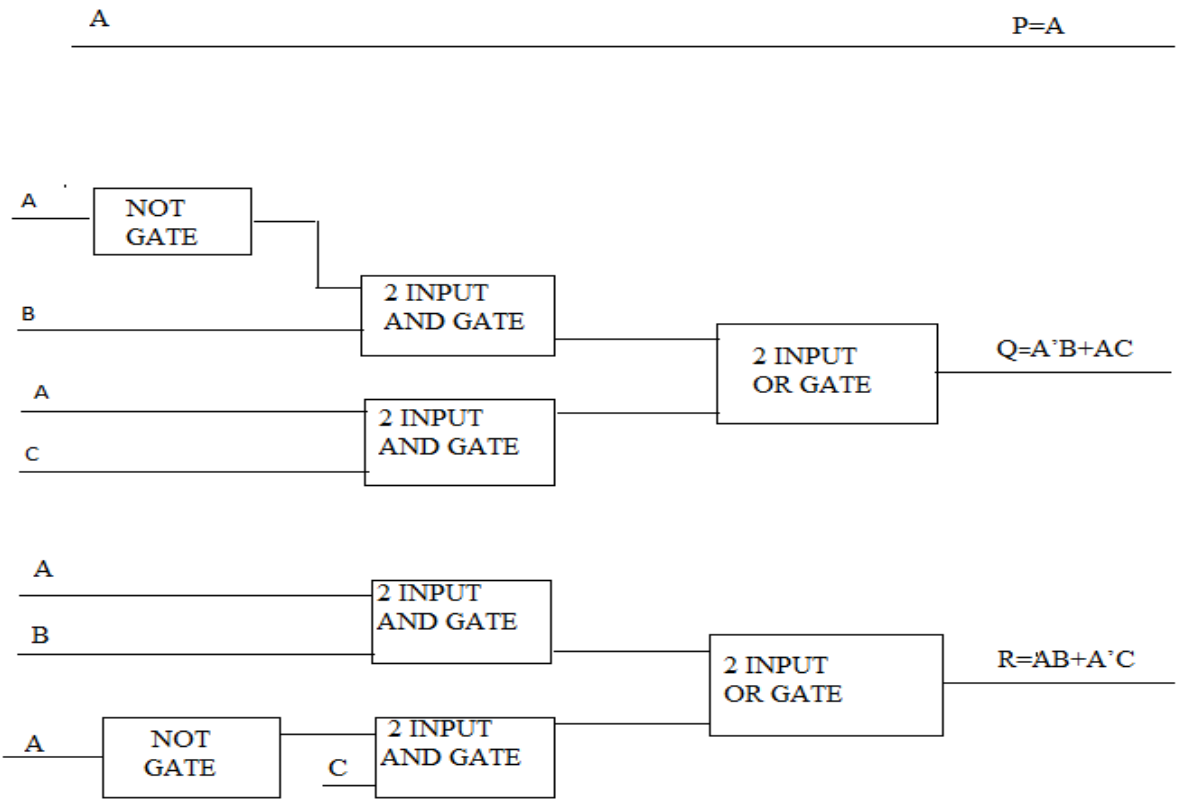

Fig 3.2 (b) Circuit diagram of Fredkin gate

Table 3.2: Truth table of Fredkin gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

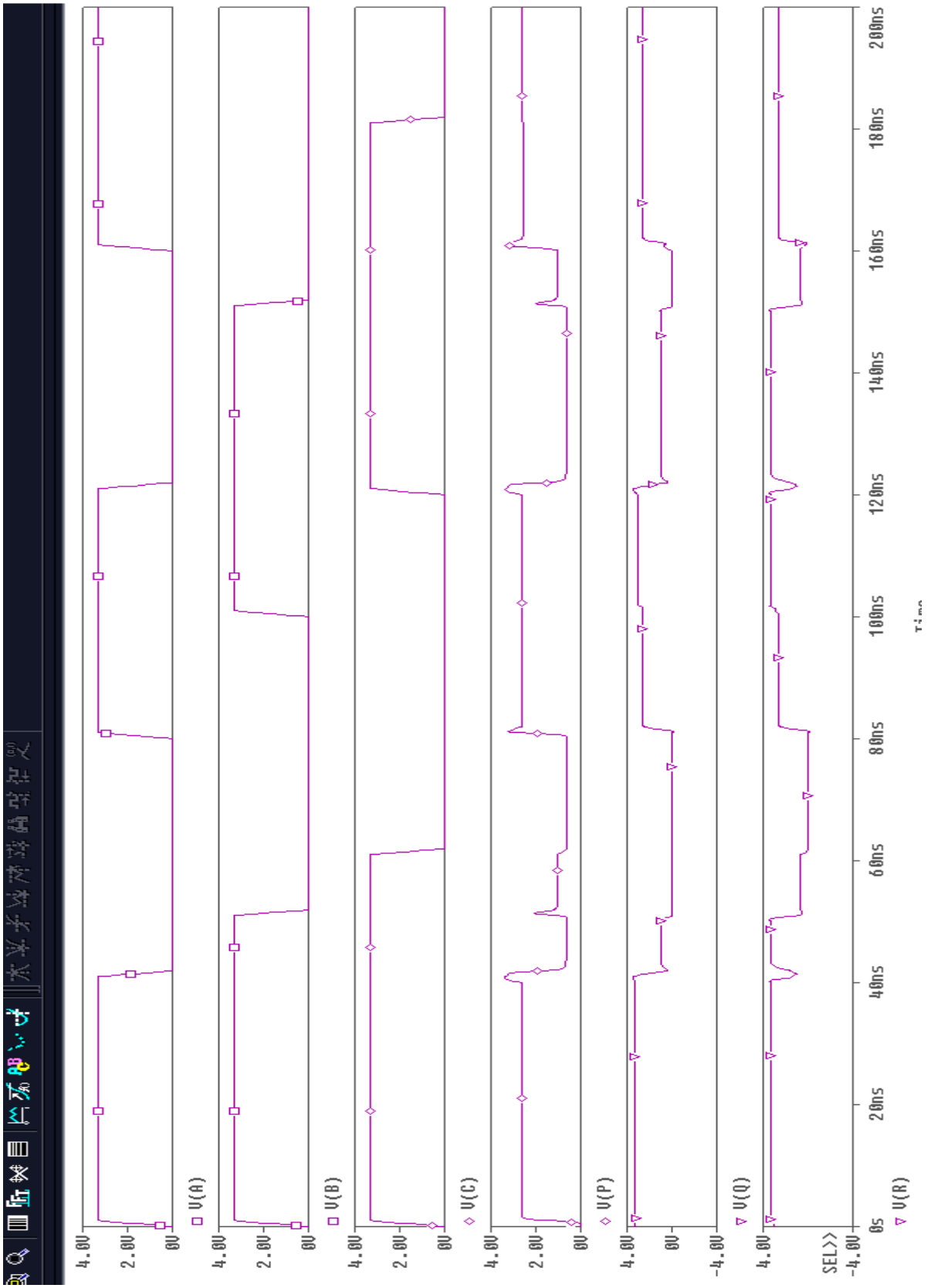

Fig 3.4 Input output waveform of Fredkin Gate

3.1.3 Peres Gate:

The Peres gate [12] is a 3x3 reversible gate used in reversible logic synthesis. The block diagram of the gate is shown in Fig 3.5. It has three inputs A, B and C; and three outputs P, Q and R. The input output relationship is given as

$P=A$ (3.7)

$Q=A \oplus B$ (3.8)

$R= AB \oplus C$ (3.9)

The Quantum cost of the gate is five. The truth table of the Peres Gate is given in Table 3.3. To verify the functionality of the gate, (3.7) – (3.9) are implemented using transmission gates and SPICE simulations are carried out using 0.35 µm CMOS technology parameters. To implement this gate two EX-OR and two AND gate are required. The simulation results are shown in Fig. 3.6.This gate is used to design reversible multiplier circuit [13].

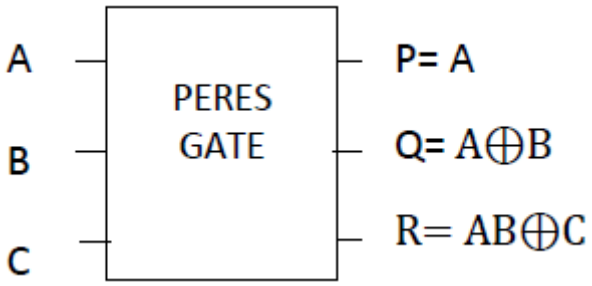

Fig 3.5Peres gate

Table 3.3: Truth table of Peres gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

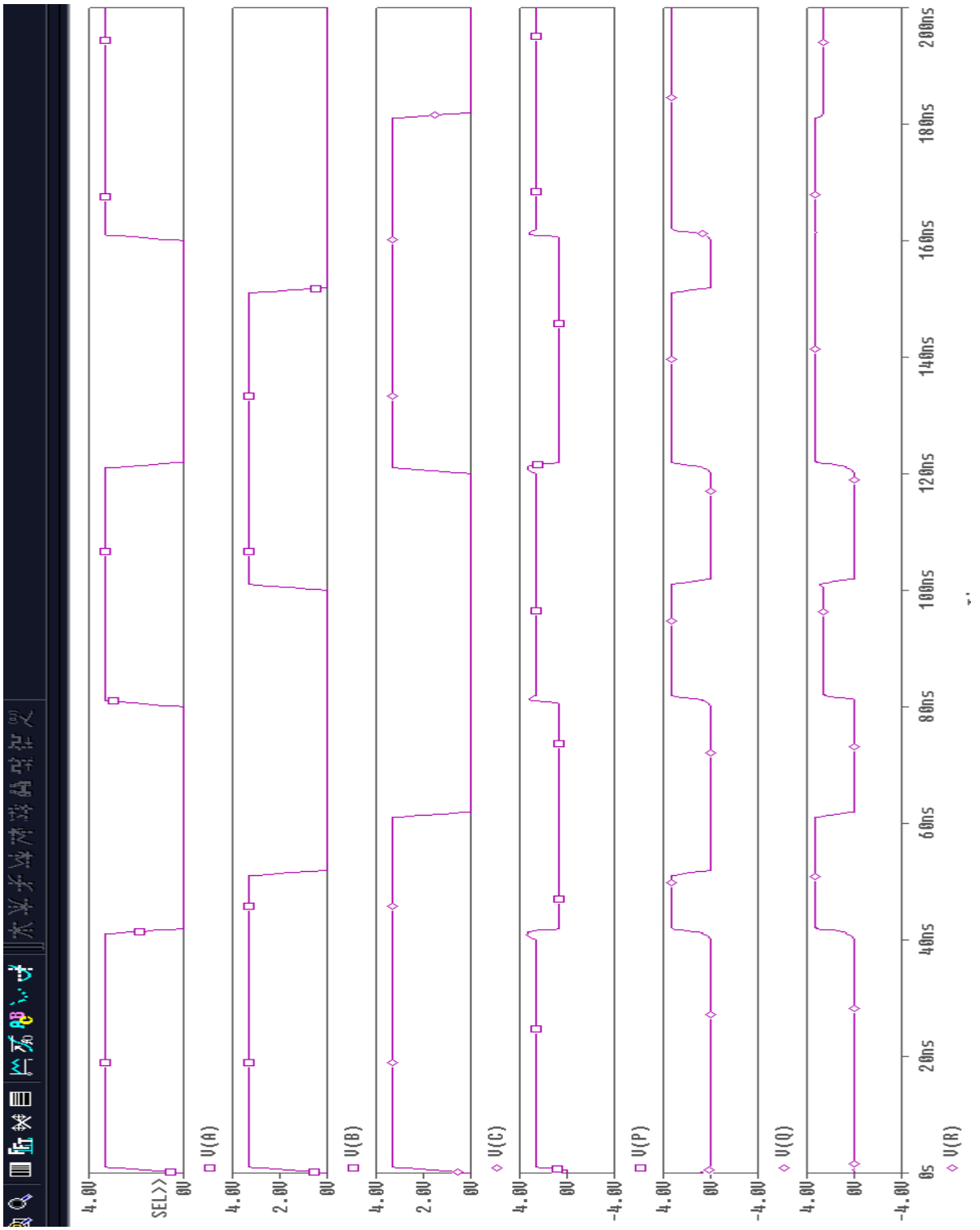

Fig 3.6 Input output waveform of Peres Gate

3.1.4 R Gate:

The R gate [14] is a 3x3 reversible gate used in reversible logic synthesis. The block diagram of the gate is shown in Fig 3.7. It has three inputs A, B and C; and three outputs P, Q and R. The input output relationship is given as

$$P=A\oplus B \quad (3.8)$$

$$Q=A \quad (3.9)$$

$$R=C'\oplus AB \quad (3.10)$$

The Quantum cost of the gate is not mentioned by author. The truth table of the R Gate is given in Table 3.4. To verify the functionality of the gate, (3.8) – (3.10) are implemented using transmission gates and SPICE simulations are carried out using 0.35 μm CMOS technology parameters. To implement this gate two EX-OR, one AND gate and three NOT gate are required. The simulation results are shown in Fig. 3.8

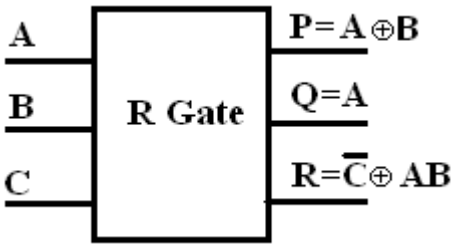

Fig 3.7 R Gate

Table 3.4: Truth table of R gate

A	B	C	P	Q	R
0	0	0	0	0	1
0	0	1	0	0	0
0	1	0	1	0	1
0	1	1	1	0	0
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	0	1	0
1	1	1	0	1	1

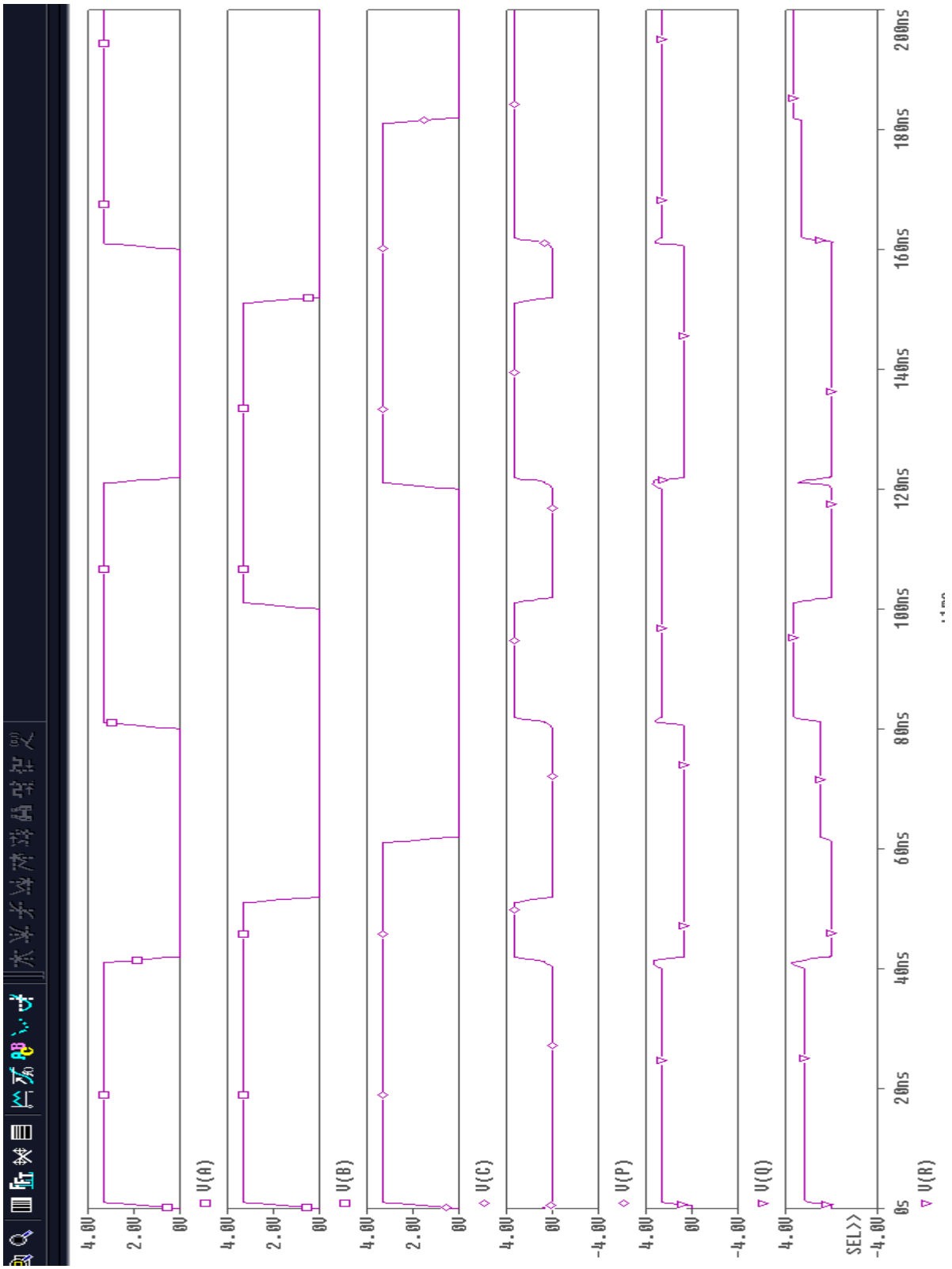

Fig 3.8 Input output waveform of R Gate

3.1.5 URG Gate: The URG gate [15] is a 3x3 reversible gate used in reversible logic synthesis. The block diagram of the gate is shown in Fig 3.9. It has three inputs A, B and C; and three outputs P, Q and R. The input output relationship is given as

$$P = (A+B) \oplus C \quad (3.13)$$

$$Q = B \quad (3.14)$$

$$R = AB \oplus C \quad (3.15)$$

The Quantum cost of the gate is not mentioned by author. The truth table of the URG Gate is given in Table 3.5. To verify the functionality of the gate, (3.13) – (3.15) are implemented using transmission gates and SPICE simulations are carried out using 0.35 μm CMOS technology parameters. To implement this gate two EX-OR, one AND gate, two NOT gate and one OR gate are required. The simulation results are shown in Fig. 3.10.This gate is used to design low power adder circuit [16].

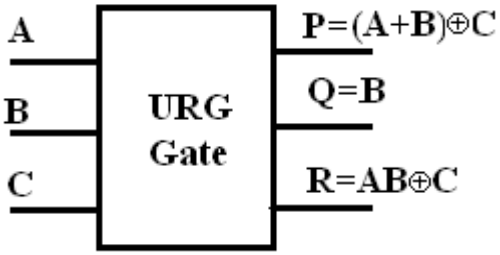

Fig 3.9 URG Gate

Table 3.5: Truth table of URG gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	1	0	1
0	1	0	1	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	0	0	1
1	1	0	1	1	1
1	1	1	0	1	0

Fig 3.10 Input output waveform of URG Gate

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3.1.6 TR Gate:

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The TR gate [17] is a 3x3 reversible gate used in reversible logic synthesis. The block diagram is shown in Fig. 3.12. It is a 3x3 gate with A, B and C as input and outputs P, Q and R. The input output relationship is given as

$P=A$ (3.16)

$Q=A \oplus B$ (3.17)

$R=AB' \oplus C$ (3.18)

The Quantum cost of the gate is six. The truth table of the TR Gate is given in Table 3.6. To verify the functionality of the gate, (3.16) – (3.18) are implemented using transmission gates and SPICE simulations are carried out using 0.35 μm CMOS technology parameters. To implement this gate two EX-OR, one AND gate and two NOT gate are required The simulation results are shown in Fig. 3.12

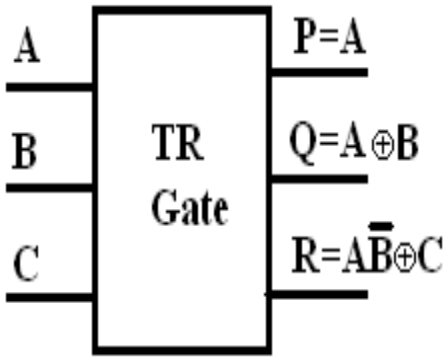

Fig 3.12 TR Gate

Table 3.6: Truth table of TR gate

A	B	C	P	Q	R
0	0	0	0	0	1
0	0	1	0	0	0
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	1	0	1

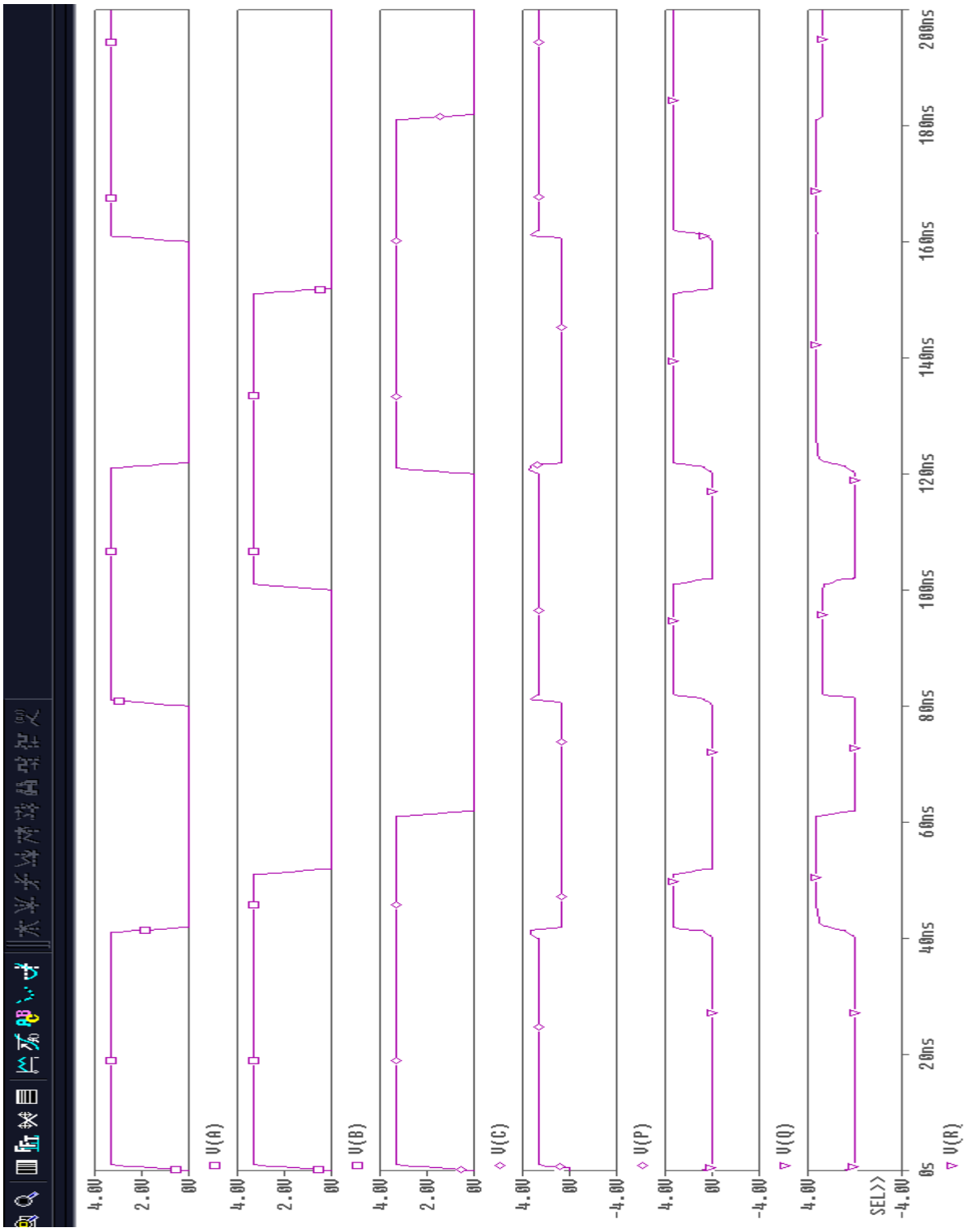

Fig 3.12 Input output waveform of TR Gate

3.1.7 New BJN Gate:

The BJN gate [17] is a 3x3 reversible gate used in reversible logic synthesis. The block diagram of the gate is shown in Fig 3.13. It has three inputs A, B and C; and three outputs P, Q and R. The input output relationship is given as

$P=A$ (3.19)

$Q=B$ (3.20)

$R=(A+B)\oplus C$ (3.21)

The Quantum cost of the gate is five. The truth table of the URG Gate is given in Table 3.7. To verify the functionality of the gate, (3.19) – (3.21) are implemented using transmission gates and SPICE simulations are carried out using 0.35 μm CMOS technology parameters. To implement this gate one EX-OR, four NOT gate and one OR gate are required. The simulation results are shown in Fig. 3.14.This gate is used to design low power comparator circuit.

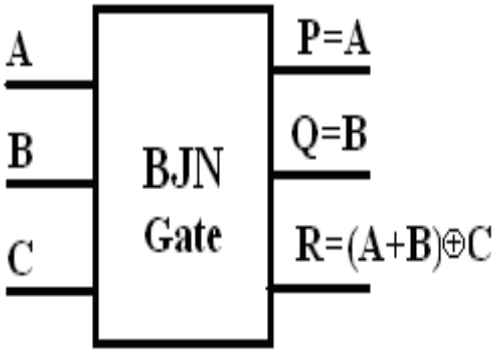

Fig 3.13 BJN Gate

Table 3.7: Truth table of BJN gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	1	0	0

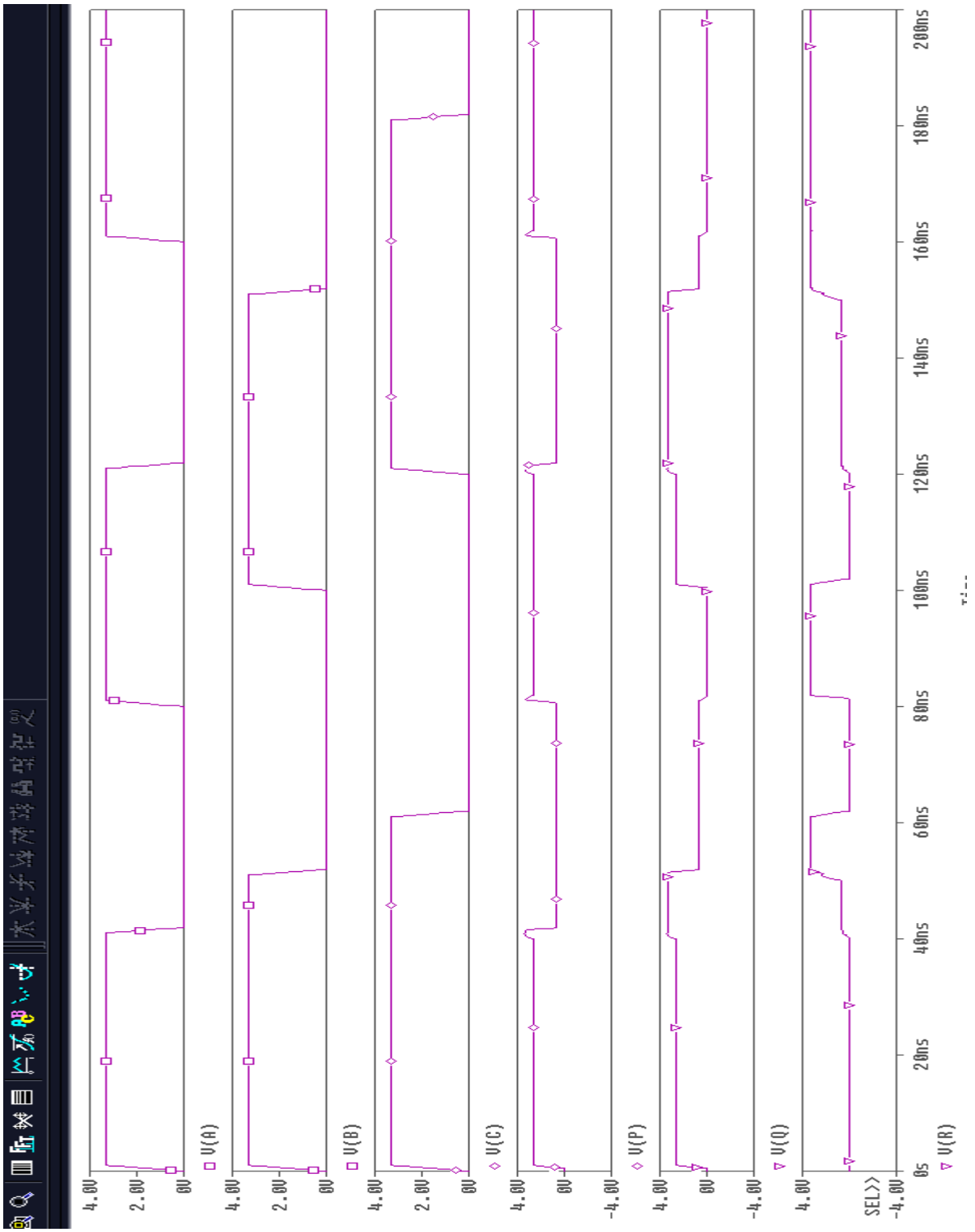

Fig 3.14 Input output waveform of BJN Gate

3.1.8 NFT Gate:

The NFT gate [17] is a 3x3 reversible gate used in reversible logic synthesis. The block diagram of the gate is shown in Fig 3.15. It has three inputs A, B and C; and three outputs P, Q and R. The input output relationship is given as

$P=A \oplus B$ (3.22)

$Q=B'C \oplus AC'$ (3.23)

$R=BC \oplus AC'$ (3.24)

The Quantum cost of the gate is five. The truth table of the URG Gate is given in Table 3.8. To verify the functionality of the gate, (3.22) – (3.24) are implemented using transmission gates and SPICE simulations are carried out using 0.35 μm CMOS technology parameters. To implement this gate four EX-OR, two NOT gate and three AND gate are required. The simulation results are shown in Fig. 3.16.

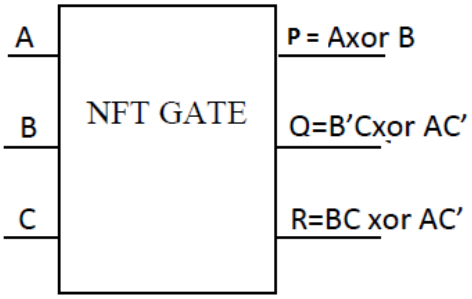

Fig 3.15 NFT Gate

Table 3.8: Truth table of NFT gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	1	0	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	0	1	1
1	1	1	0	0	1

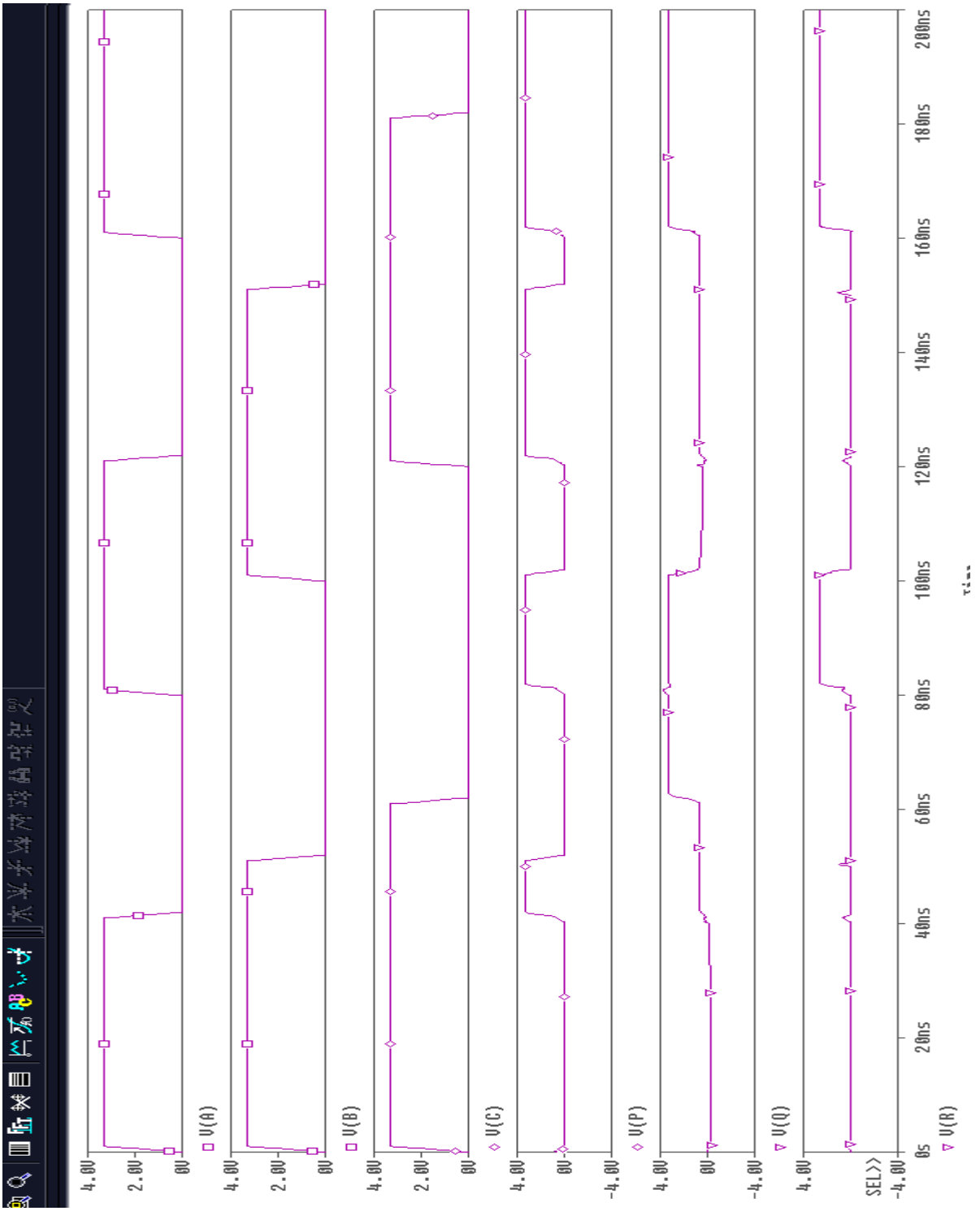

Fig 3.16 Input output waveform of NFT Gate

3.1.9 MCL gate:

The MCL gate [17] is a 3x3 reversible gate used in reversible logic synthesis. The block diagram of the gate is shown in Fig 3.17. It has three inputs A, B and C; and three outputs P, Q and R. The input output relationship is given as

P=B'C' (3.25)

Q=A'B' (3.26)

R=A (3.27)

The Quantum cost of the gate is not described by the author. The truth table of the URG Gate is given in Table 3.9. To verify the functionality of the gate, (3.25) – (3.27) are implemented using transmission gates and SPICE simulations are carried out using 0.35 μm CMOS technology parameters. To implement this gate six NOT gate and two AND gate are required. The simulation results are shown in Fig. 3.18.

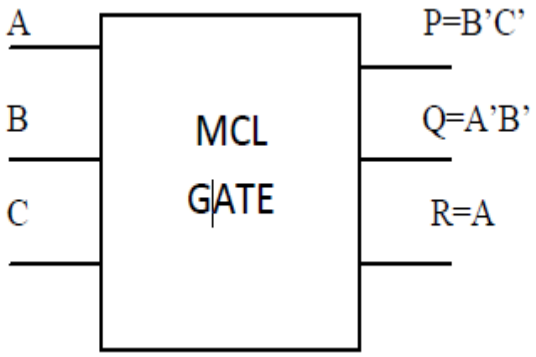

Fig 3.17 MCL Gate

Table 3.9: Truth table of MCL gate

A	B	C	P	Q	R
0	0	0	1	1	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	1	0	1
1	0	1	0	0	1
1	1	0	0	0	1
1	1	1	0	0	1

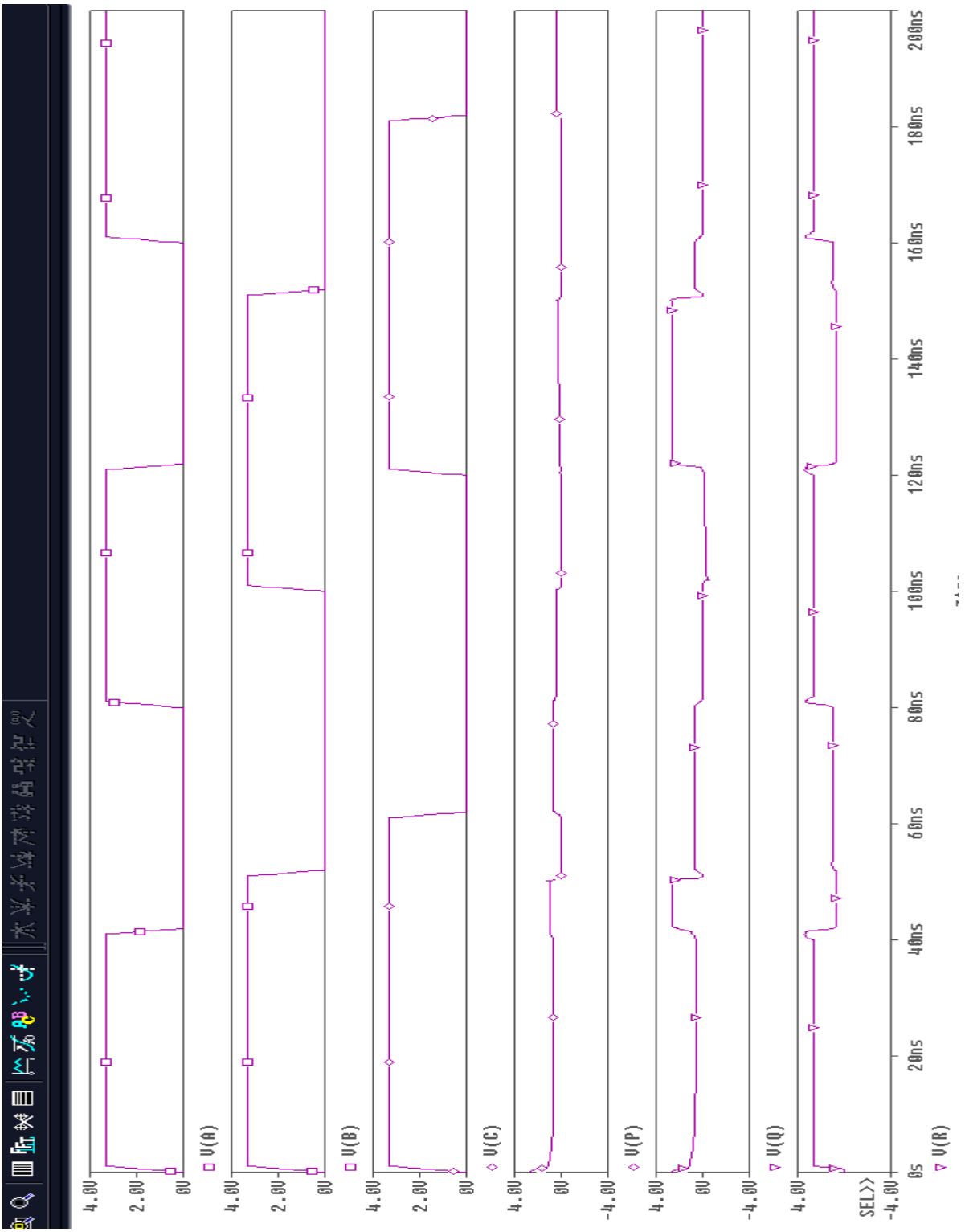

Fig 3.18 Input output waveform of MCL Gate

3.2: 4 x 4 gates

To increase the functional implementations various 4x4 gates such as SCL gate [17], MKG gate [18], DPG gate [19],BVF gate [20],etc were suggested.

3.2.1. SCL Gate:

The SCL gate [17] is a 4x4 reversible gate used in reversible logic synthesis. The block diagram of the gate is shown in Fig 3.19. It has four inputs A, B,C and D; and four outputs P, Q, R and S. The input output relationship is given as

$$P=A \tag{3.28}$$

$$Q=B \tag{3.29}$$

$$R=C \tag{3.30}$$

$$S=A\,(B+C) \oplus D \tag{3.31}$$

The Quantum cost of the gate is not described by the author. The truth table of the SCL Gate is given in Table 3.10. To verify the functionality of the gate, (3.28) – (3.31) are implemented using transmission gates and SPICE simulations are carried out using 0.35 μm CMOS technology parameters. To implement this gate six NOT gate, one AND gate, one OR gate and one XOR gate are required. The simulation results are shown in Fig. 3.20.This gate is used in clock data and recovery circuit.

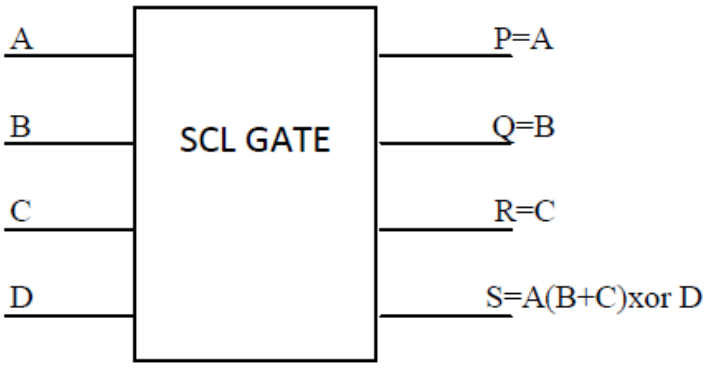

Fig 3.19 SCL Gate

Table 3.10: Truth table of SCL gate

A	B	C	D	P	Q	R	S
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	1
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1

Fig 3.20 Input output waveform of SCL Gate

3.2.2. MKG Gate:

The MKG gate [18] is a 4x4 reversible gate used in reversible logic synthesis. The block diagram of the gate is shown in Fig 3.21. It has four inputs A, B, C and D; and four outputs P, Q, R and S. The input output relationship is given as

$$P=A \tag{3.32}$$

$$Q=C \tag{3.33}$$

$$R= (A'D'\oplus B') \oplus C \tag{3.34}$$

$$S=(A'D'\oplus B')\ C\oplus(AB\oplus D) \tag{3.35}$$

The Quantum cost of the gate is not described by the author. The truth table of the MKG Gate is given in Table 3.11. To verify the functionality of the gate, (3.32) – (3.35) are implemented using transmission gates and SPICE simulations are carried out using 0.35 μm CMOS technology parameters. To implement this gate seven NOT gate, three AND gate and four XOR gate are required. The simulation results are shown in Fig. 3.20.

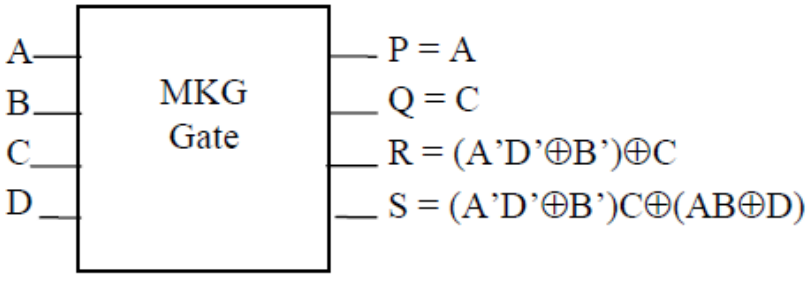

Fig 3.21 MKG Gate

Table 3.11: Truth table of MKG gate

A	B	C	D	P	Q	R	S
0	1	0	0	0	0	1	0
0	1	0	1	0	0	0	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	1	0
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	1
0	0	1	0	0	1	1	0
0	0	1	1	0	1	0	1

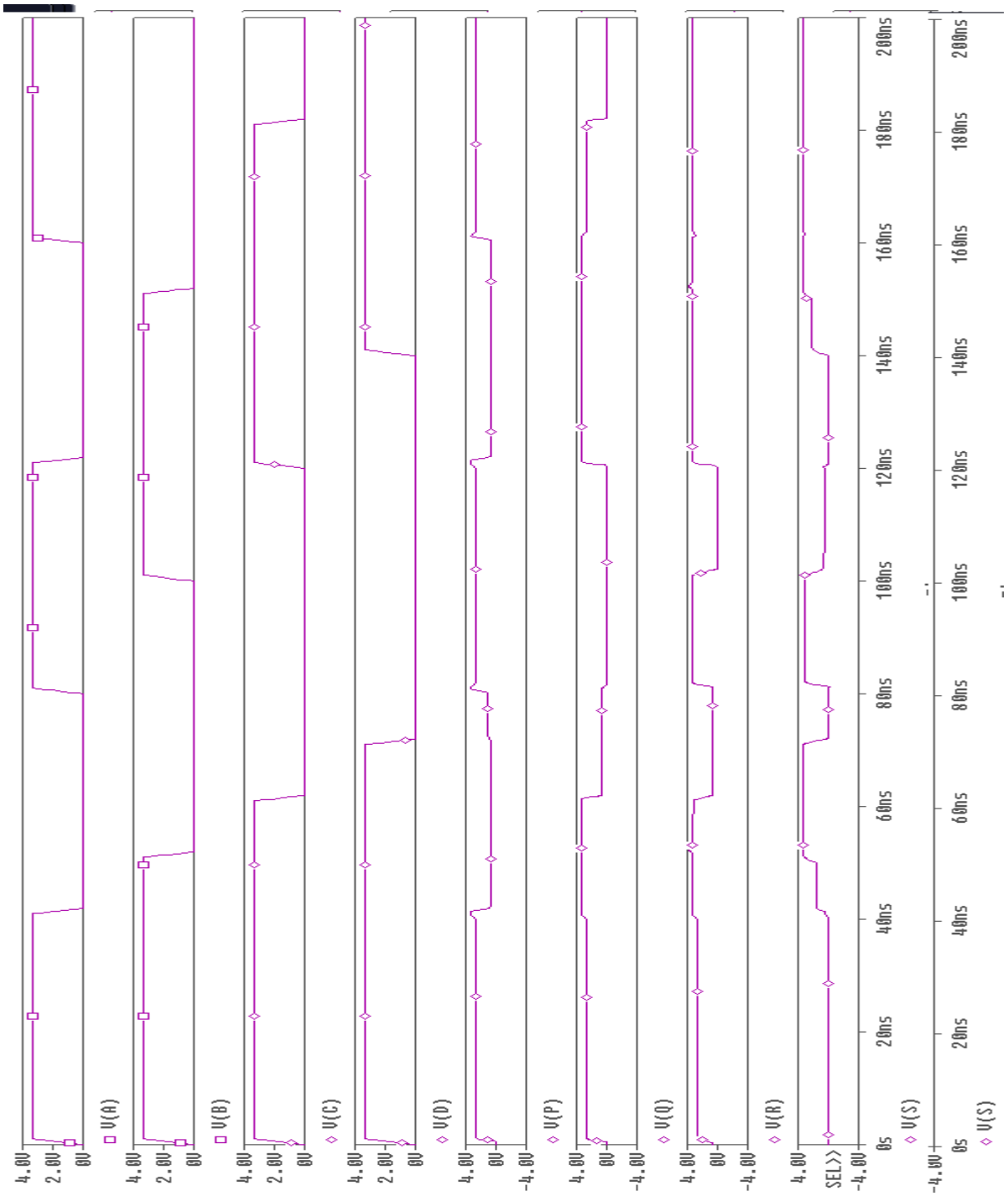

Fig 3.22 Input output waveform of MKG Gate

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3.2.3 DPG Gate: The DPG gate [19] is a 4x4 reversible gate used in reversible logic synthesis. The block diagram of the gate is shown in Fig 3.23. It has four inputs A, B, C and D; and four outputs P, Q, R and S. The input output relationship is given as

$$P=A \quad (3.36)$$

$$Q=A \oplus B \quad (3.37)$$

$$R= (A \oplus B) \oplus D \quad (3.38)$$

$$S= (A \oplus B)\ C \oplus AB \oplus C \quad (3.39)$$

The Quantum cost of the gate is not described by the author. The truth table of the MKG Gate is given in Table 3.12. To verify the functionality of the gate, (3.36) – (3.39) are implemented using transmission gates and SPICE simulations are carried out using 0.35 μm CMOS technology parameters. To implement this gate two NOT gate, two AND gate and three XOR gate are required. The simulation results are shown in Fig. 3.24.

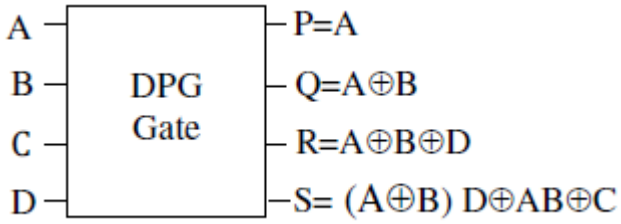


Fig 3.23 DPG Gate

Table 3.12: Truth table of DPG gate

A	B	C	D	P	Q	R	S
0	1	0	0	0	1	1	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	1
0	1	1	1	0	1	0	0
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	1	1

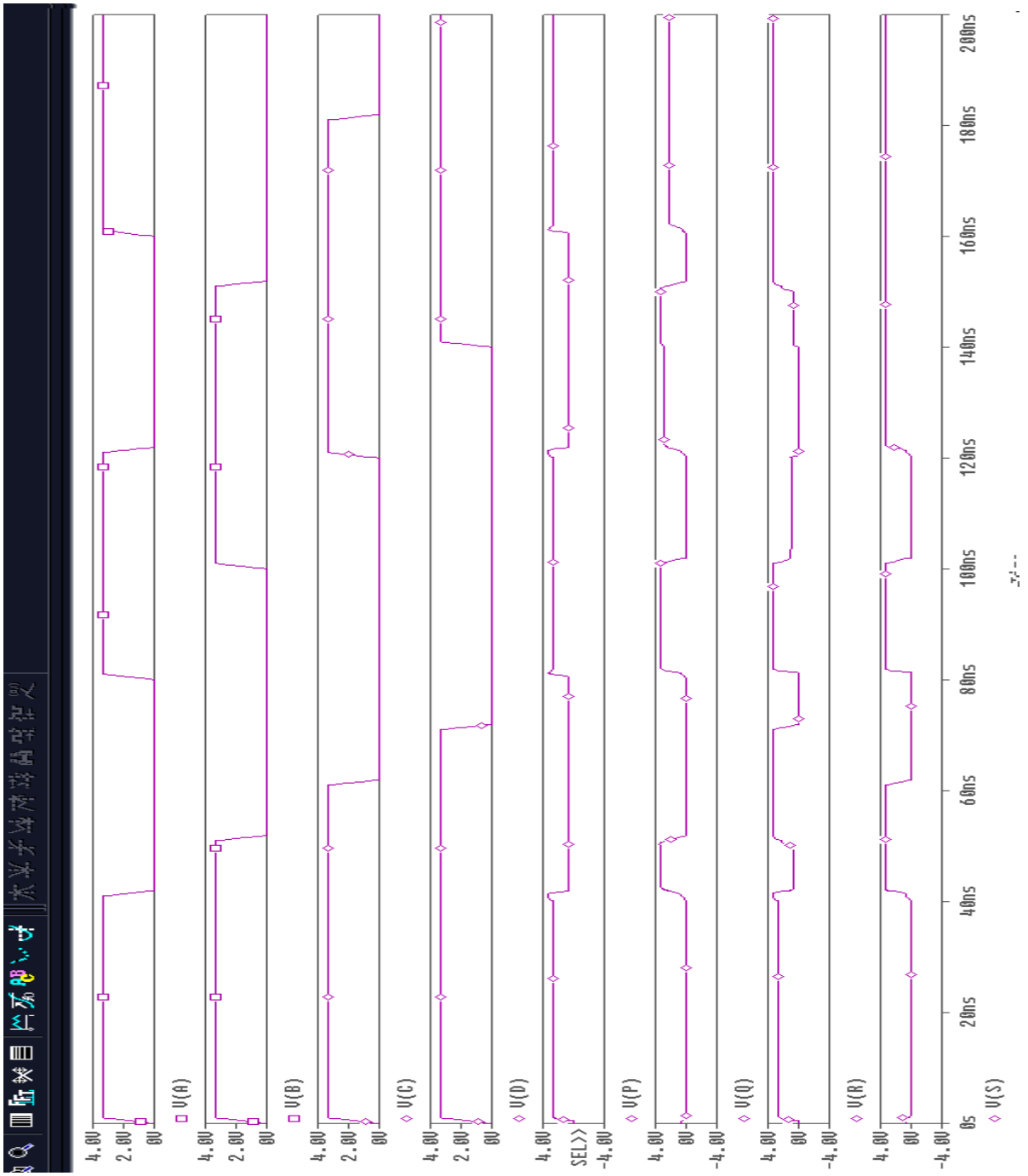


Fig 3.24 Input output waveform of DPG Gate

3.2.4 BVF Gate

The BVF gate [20] is a 4x4 reversible gate used in reversible logic synthesis. This is a reversible double XOR gate and can be used for duplication of the required inputs to meet the fan-out requirements. The block diagram of the gate is shown in Fig 3.25. It has four inputs A, B, C and D; and four outputs P, Q, R and S. The input output relationship is given as

$$P=A \tag{3.40}$$

$$Q=C \tag{3.41}$$

$$R= (A'D'\oplus B') \oplus C \tag{3.42}$$

$$S=(A'D'\oplus B')\ C\oplus(AB\oplus D) \tag{3.43}$$

The Quantum cost of the gate is not described by the author. The truth table of the MKG Gate is given in Table 3.13. To verify the functionality of the gate, (3.40) – (3.43) are implemented using transmission gates and SPICE simulations are carried out using 0.35 μm CMOS technology parameters. To implement this gate four NOT gate and two XOR gate are required. The simulation results are shown in Fig. 3.26

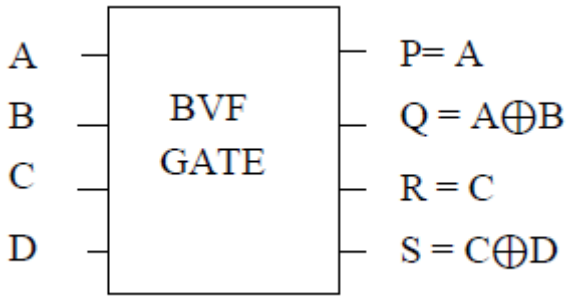


Fig 3.25 BVF Gate

Table 3.13: Truth table of BVF gate

A	B	C	D	P	Q	R	S
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	1
0	1	1	1	0	1	1	0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	1

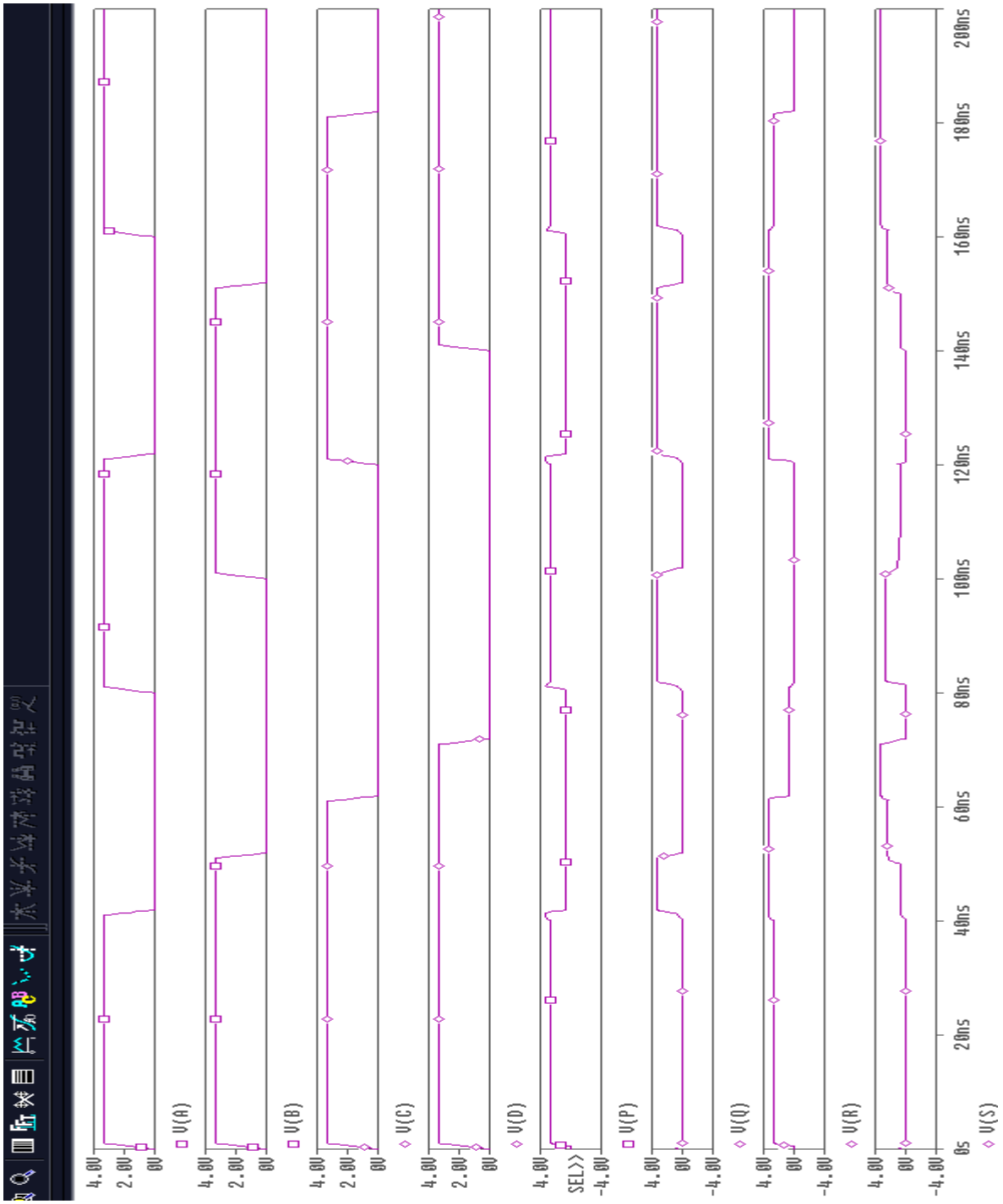


Fig 3.26 Input output waveform of BVF Gate

CHAPTER 4:

PROPOSED GATE AND COMPARISION WITH EXISTING 5 X 5 GATES

The 2 x2, 3 x 3 and 4 x 4 reversible logic gates described in chapter 2 and 3 have limited functionality. The gate can be made versatile by increasing the number of inputs and outputs. Therefore, this chapter put forwards available 5x5 reversible logic gates such as PPPG gate[21], SBV gate [18] and BVPPG gate [22]. A new 5x5 reversible logic gate is also proposed and is compared with the existing 5x5 gates.

4.1 EXISTING 5X5 GATES:

In this section the operation of available 5 x5 gates is explained and their functional verification using spice is given.

4.1.1 PPPG GATE

This is a new 5x5 parity preserving reversible gate, PPPG [21], depicted in Figure 4.1. When one of the input variables also acts as output then the gate is called one-through. This gate is a one-through gate. The input pattern corresponding to particular output pattern is uniquely determined from the truth table. The proposed reversible PPPG is parity preserving. This is readily verified by comparing the parity of the input to the parity of the output that is A B C D E and P Q R S T. It has five inputs A, B, C D and E; and five outputs P, Q, R, S and T. The input output relationship is given as

$$P=A \quad (4.1)$$

$$Q=A'C'\oplus B' \quad (4.2)$$

$$R= (A'C'\oplus B')\oplus D \quad (4.3)$$

$$S= (A'C'\oplus B').D \oplus (AB\oplus C) \quad (4.4)$$

$$T= BE(A+D)+A'D(C\oplus E) +B'D(A+E) \quad (4.5)$$

The truth table of the MKG Gate is given in Table 4.1. To verify the functionality of the gate, (4.1) – (4.5) are implemented using transmission gates and SPICE simulations are carried out using 0.35 μm CMOS technology parameters. To implement this gate eleven NOT gate , ten AND gate , seven XOR gate and two OR gate are required The simulation results are shown in Fig. 4.3.This gate is universal in the sense that it can be used for implementing any arbitrary Boolean functions. e.g. A B C D E = (A 1 1 D 1) P Q R S T (A 0 D A' A+D)

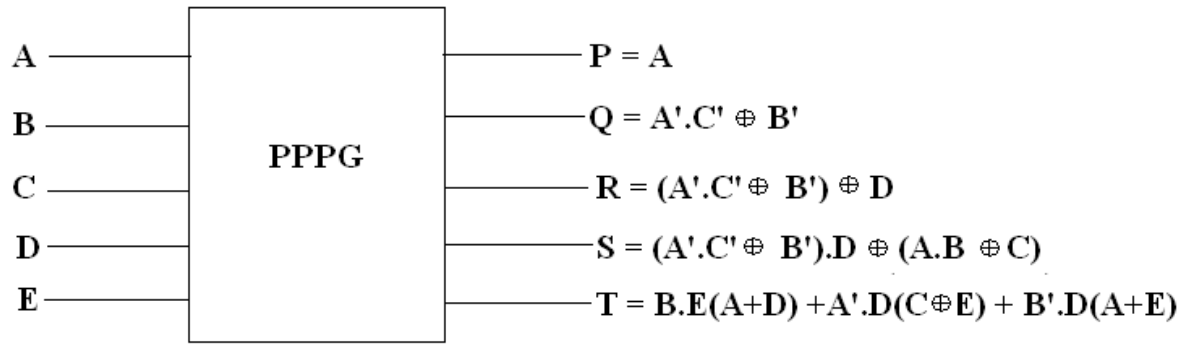


Fig 4.1 PPPG gate

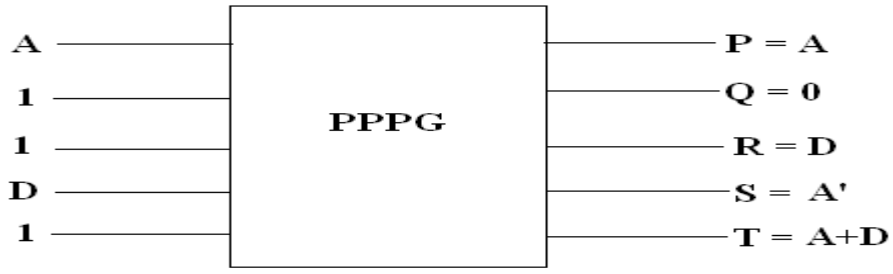


Fig 4.2 PPPG as NOT and OR

Table 4.1: Truth table of PPPG gate

A	B	C	D	E	P	Q	R	S	T
0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	0	1	1	0
0	0	0	1	1	0	0	1	1	1
0	0	1	0	0	0	1	1	0	0
0	0	1	0	1	0	1	1	0	1
0	0	1	1	0	0	1	0	1	0
0	0	1	1	1	0	1	0	1	1
0	1	0	0	0	0	1	1	0	1
0	1	0	0	1	0	1	1	0	1
0	1	0	1	0	0	1	0	1	0
0	1	0	1	1	0	1	0	1	0
0	1	1	0	0	0	0	0	0	1
0	1	1	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	1	1
0	1	1	1	1	0	0	1	1	0
1	0	0	0	0	1	1	1	0	1
1	0	0	0	1	1	1	1	0	0
1	0	0	1	0	1	1	0	1	1
1	0	0	1	1	1	1	0	1	0
1	0	1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1	0	0
1	0	1	1	0	1	1	0	1	1
1	0	1	1	1	1	1	0	1	0
1	1	0	0	0	1	0	0	1	0
1	1	0	0	1	1	0	0	1	1
1	1	0	1	0	1	0	1	0	0
1	1	0	1	1	1	0	1	0	1
1	1	1	0	0	1	0	0	1	0
1	1	1	0	1	1	0	0	1	1

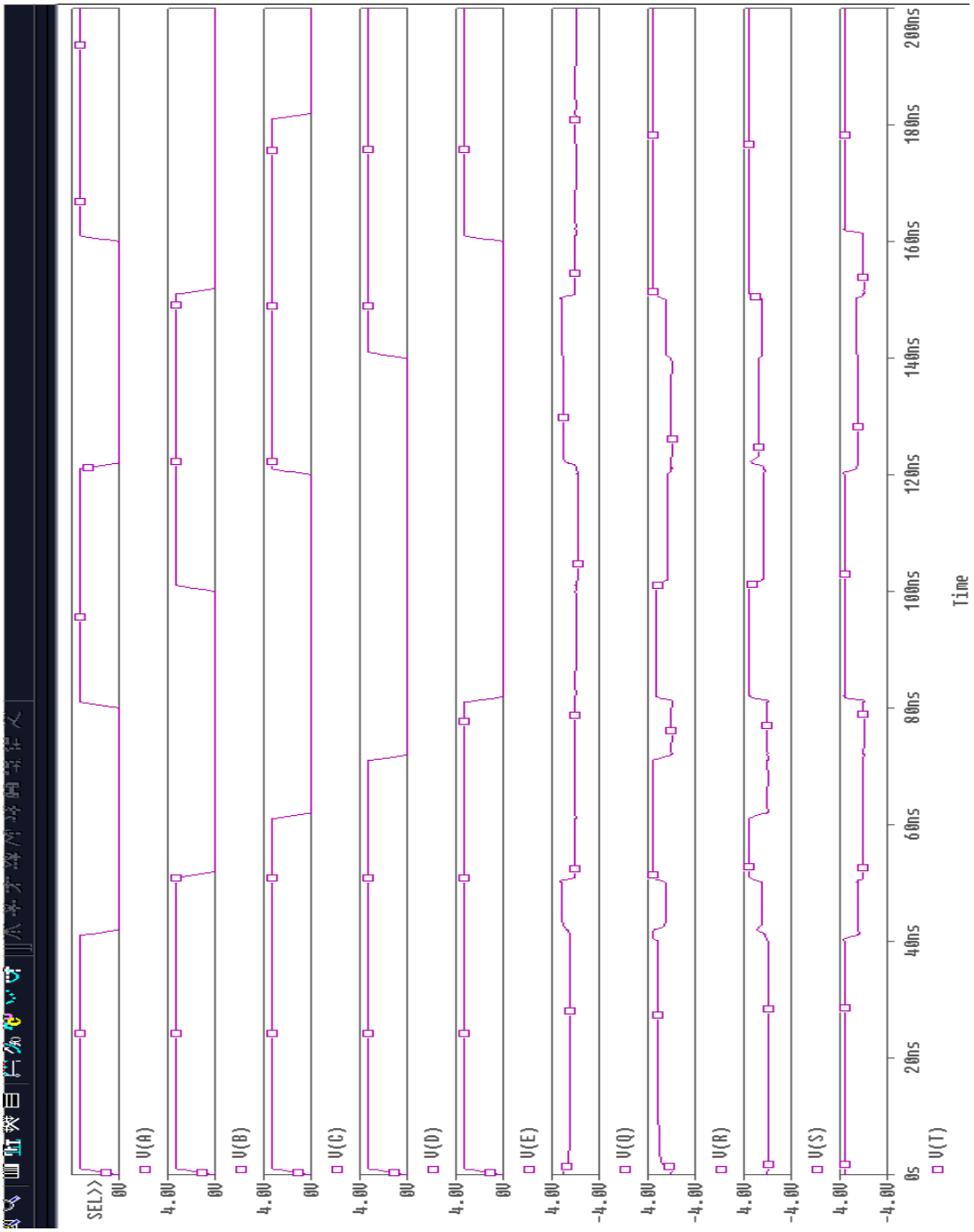


Fig 4.3 Input output waveform of PPPG gate

4.1.2 SBV Gate:

The SBV gate [18] is a 5x5 reversible gate used in reversible logic synthesis. The block diagram of the gate is shown in Fig 4.4(a). It has five inputs A, B, C, D and E; and five outputs P, Q, R, S and T. The input output relationship is given as

$$P=(B'C'A')\oplus E \quad (4.6)$$

$$Q=B\oplus C \quad (4.7)$$

$$R= C \quad (4.8)$$

$$S=D' \quad (4.9)$$

$$T=B' \quad (4.10)$$

To verify the functionality of the gate, (4.6) – (4.10) are implemented using transmission gates and SPICE simulations are carried out using 0.35 μm CMOS technology parameters. To implement this gate five NOT gate, two AND gate and two XOR gate are required The simulation results are shown in Fig. 4.4(b). This gate can individually work as a nines complementer with one garbage output.

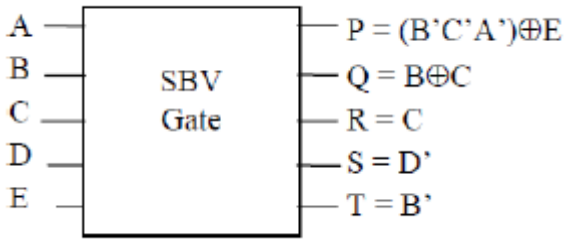


Fig 4.4(a) SBV gate

Fig 4.4(b) Input output waveform of SBV Gate

4.1.3 BVPPG gate

BVPPG gate [22] is a 5 x 5 reversible gate and its block diagram is as shown in figure 4.5. Its quantum cost is 10. The truth table of BVPPG is as shown in the Table 4.2. It has five inputs A, B, C, D and E; and five outputs P, Q, R, S and T. The input output relationship is given as

$$P=A \tag{3.40}$$

$$Q=B \tag{3.41}$$

$$R= (AB) \oplus C \tag{3.42}$$

$$S=D \tag{3.43}$$

$$T= AD \oplus E$$

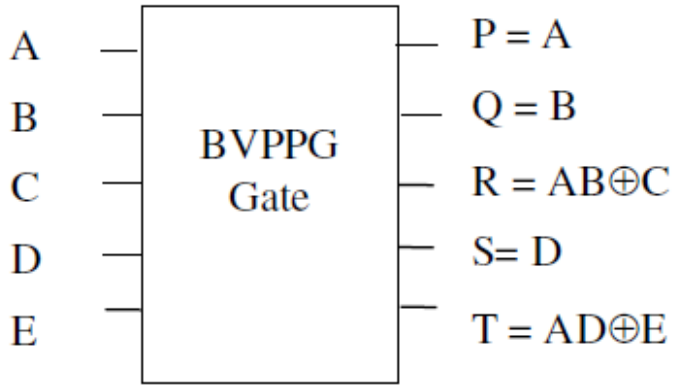


Fig 4.5 BVPGG Gate

To verify the functionality of the gate, (3.40) – (3.43) are implemented using transmission gates and SPICE simulations are carried out using 0.35 μm CMOS technology parameters. To implement this gate two AND and two XOR gate are required. The simulation results are shown in Fig.4.7.The BVPPG gate [22] is used to construct the partial product generator which has least number of gates and least number of garbage outputs. The two product terms are available at the outputs R and T of the BVPPG gate with C and E inputs maintained constant at 0. The other outputs namely P, Q and S are used for fan-out of the multiplier operands as shown in figure 4.6. This reduces the number of external fan-out gates to zero this design, which is main design feature.

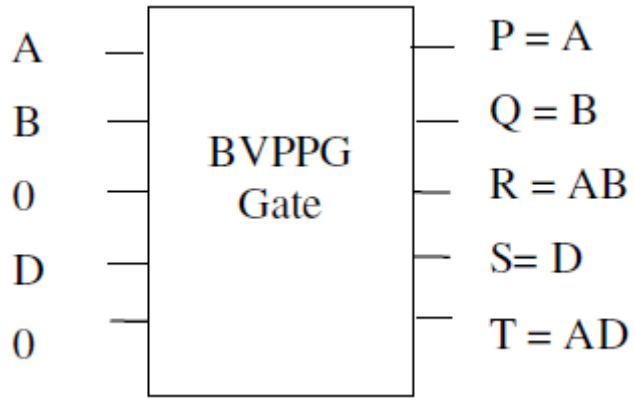


Fig4.6 BVPPG gate producing product terms and duplication of the inputs.

Table 4.2: Truth table of BVPGG gate

A	B	C	D	E	P	Q	R	S	T
0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	0	0	1	1
0	0	0	1	1	0	0	0	1	1
0	0	1	0	0	0	0	1	0	0
0	0	1	0	1	0	0	1	0	1
0	0	1	1	0	0	0	1	1	0
0	0	1	1	1	0	0	1	1	1
0	1	0	0	0	0	1	0	0	1
0	1	0	0	1	0	1	0	0	1
0	1	0	1	0	0	1	1	1	0
0	1	0	1	1	0	1	1	1	0
0	1	1	0	0	0	1	1	0	1
0	1	1	0	1	0	1	1	0	0
0	1	1	1	0	0	1	1	1	1
0	1	1	1	1	0	1	1	1	0
1	0	0	0	0	1	0	0	0	1
1	0	0	0	1	1	0	0	0	0
1	0	0	1	0	1	0	0	1	1
1	0	0	1	1	1	0	0	1	0
1	0	1	0	0	1	0	0	0	1
1	0	1	0	1	1	0	0	0	0

Fig 4.7 Input output waveform of BVPGG Gate

4.2 PROPOSED GATE

The ABCD gate is a 5x5 reversible gate and used in reversible logic synthesis. The block diagram of the gate is shown in Fig 4.8. It has five inputs A, B , C ,D and E; and five outputs P, Q, R, S and T. The input output relationship is given as

$$P=(A+B)\oplus C \quad (4.11)$$

$$Q=(A'B)\oplus D \quad (4.12)$$

$$R=(AB')\oplus D \quad (4.13)$$

$$S=AB\oplus D \quad (4.14)$$

$$T=A\oplus B\oplus E \quad (4.15)$$

The truth table of the MKG Gate is given in Table 4.3. To verify the functionality of the gate, (4.11) – (4.15) are implemented using transmission gates and SPICE simulations are carried out using 0.35 μm CMOS technology parameters. The simulation results are shown in Fig. 4.9.

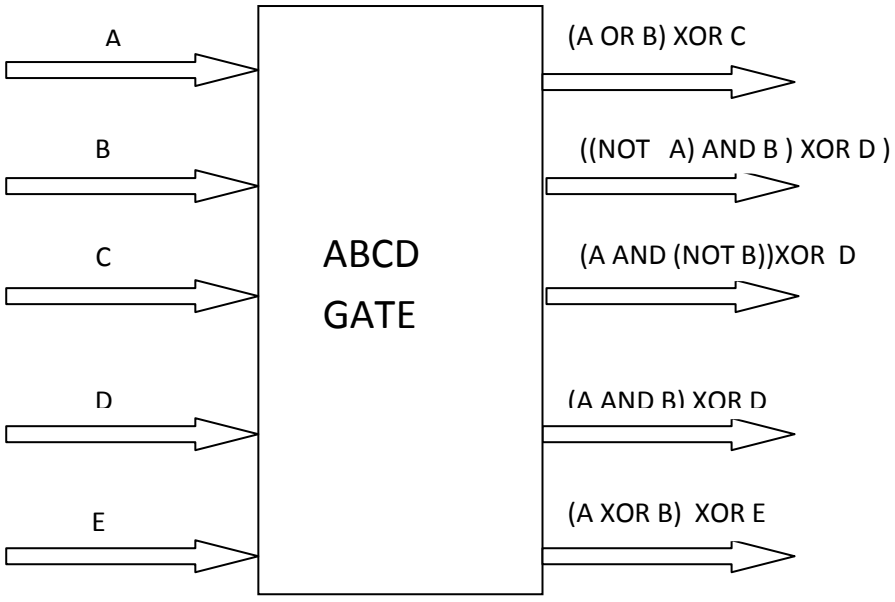


Fig 4.8 ABCD Gate

Table 4.3: Truth table of ABCD Gate

A	B	C	D	E	P	Q	R	S	T
0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	1	1	1	0
0	0	0	1	1	0	1	1	1	1
0	0	1	0	0	1	0	0	0	0
0	0	1	0	1	1	0	0	0	1
0	0	1	1	0	1	1	1	1	0
0	0	1	1	1	1	1	1	1	1
0	1	0	0	0	1	1	0	0	1
0	1	0	0	1	1	1	0	0	1
0	1	0	1	0	1	0	1	1	0
0	1	0	1	1	1	0	1	1	0
0	1	1	0	0	0	1	0	0	1
0	1	1	0	1	0	1	0	0	0
0	1	1	1	0	0	0	1	1	1
0	1	1	1	1	0	0	0	1	0
1	0	0	0	0	1	0	1	0	1
1	0	0	0	1	1	0	1	0	0
1	0	0	1	0	1	1	0	1	1
1	0	0	1	1	1	1	0	1	0
1	0	1	0	0	0	0	1	0	1
1	0	1	0	1	0	0	1	0	0
1	0	1	1	0	0	1	0	1	1
1	0	1	1	1	0	1	0	1	0
1	1	0	0	0	1	0	0	1	0
1	1	0	0	1	1	0	0	1	1
1	1	0	1	0	1	1	1	0	0
1	1	0	1	1	1	1	1	0	1
1	1	1	0	0	0	0	0	1	0
1	1	1	0	1	0	0	0	1	1

Fig 4.9 Input output waveform of ABCD Gate

4.3 COMAPRISION WITH EXISTING 5 X 5 GATES

Parameter	NCG Gate	PPPG Gate	BVPGG Gate	SBV Gate	ABCD Gate
Parity Preserve	NA	YES	YES	YES	YES
Garbage Outputs	NA	11	NA	NA	0
Constant Inputs	Dependent on application	NA	NA	NA	3
Total Delay	4α+2β+0d+2γ	7α+11β+11d+2γ	2α+2β+0d+0γ	2α+2β+5d+0γ	6α+3β+2d+1γ
Applications	Overflow detection	Fault tolerant adder	Partial product generation	Nines complementer	Universal gate.

Table 4.4 Comparison Table

Garbage output: The number of unused outputs required just to maintain the reversibility of the logic gate.

Constant Input: The number of inputs which are kept at a constant level always [23].

Circuit complexity: Circuit complexity [24][25] is defined in terms of :

α = A two input EXOR gate calculation

β = A two input AND gate calculation

δ = A NOT gate calculation

d= A OR gate calculation

T = Total logical calculation

CHAPTER 5:SIMULATION

In this chapter various applications of proposed ABCD gate are mentioned and its functional verification is done using SPICE.

5.5 ABCD Gate and its application:

5.5.1 NAND Gate: To verify the functionality SPICE simulations are carried out using 0.35 µm CMOS technology parameters. The simulation results are shown in Fig.5.1.NAND gate can be made using ABCD gate with output at S for constant input C=0,D=1.E=0 and the Simulation results are found to be in accordance with theory.

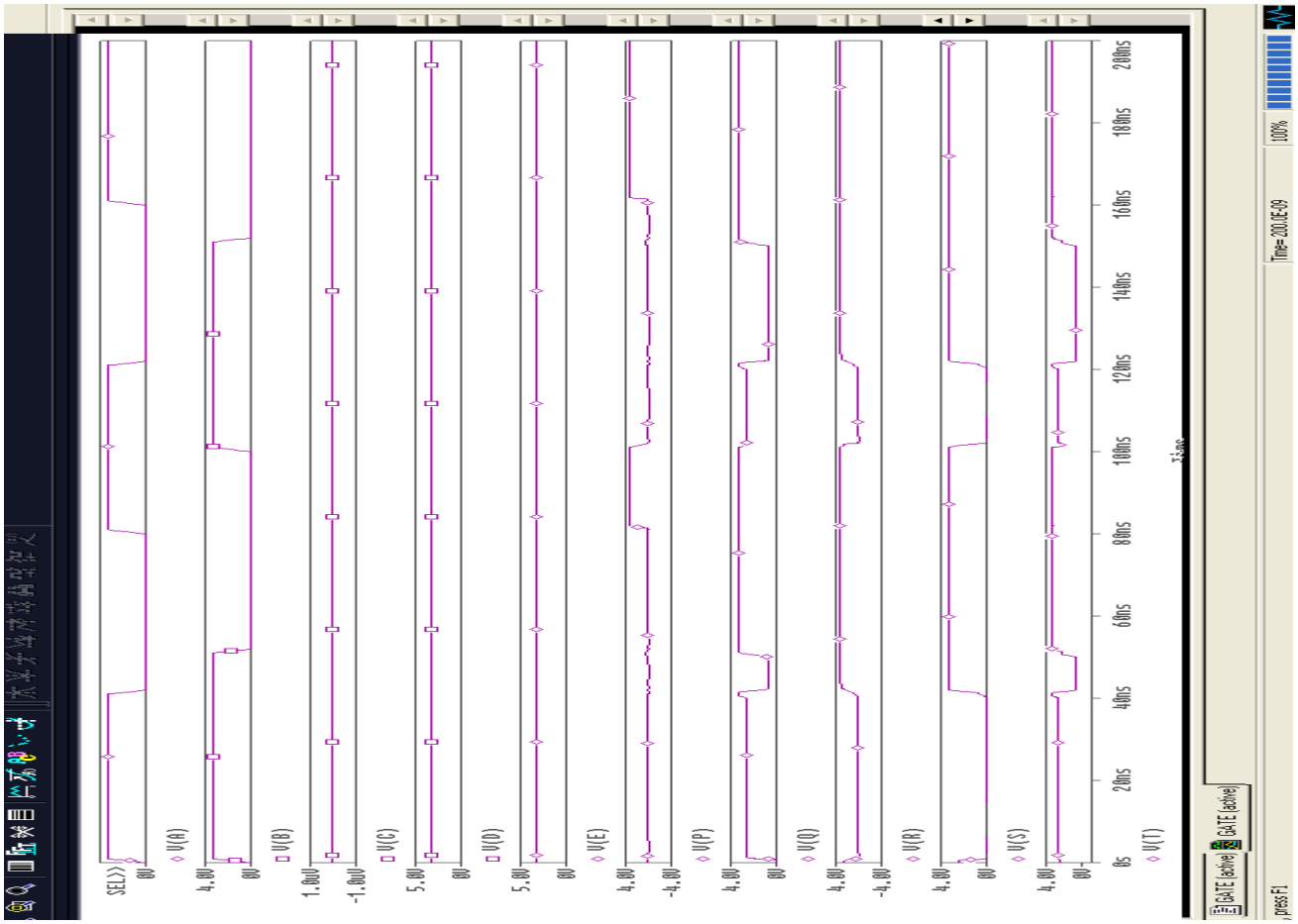


Fig 5.1 Input Output waveform of NAND gate with output at S for constant input C=0,D=1.E=0

5.5.2 NOR Gate: To verify the functionality SPICE simulations are carried out using 0.35 µm CMOS technology parameters. The simulation results are shown in Fig.5.2. NOR gate can be made using ABCD gate with output at P for constant input C=1,D=0.E=0 and the Simulation results are found to be in accordance with theory.

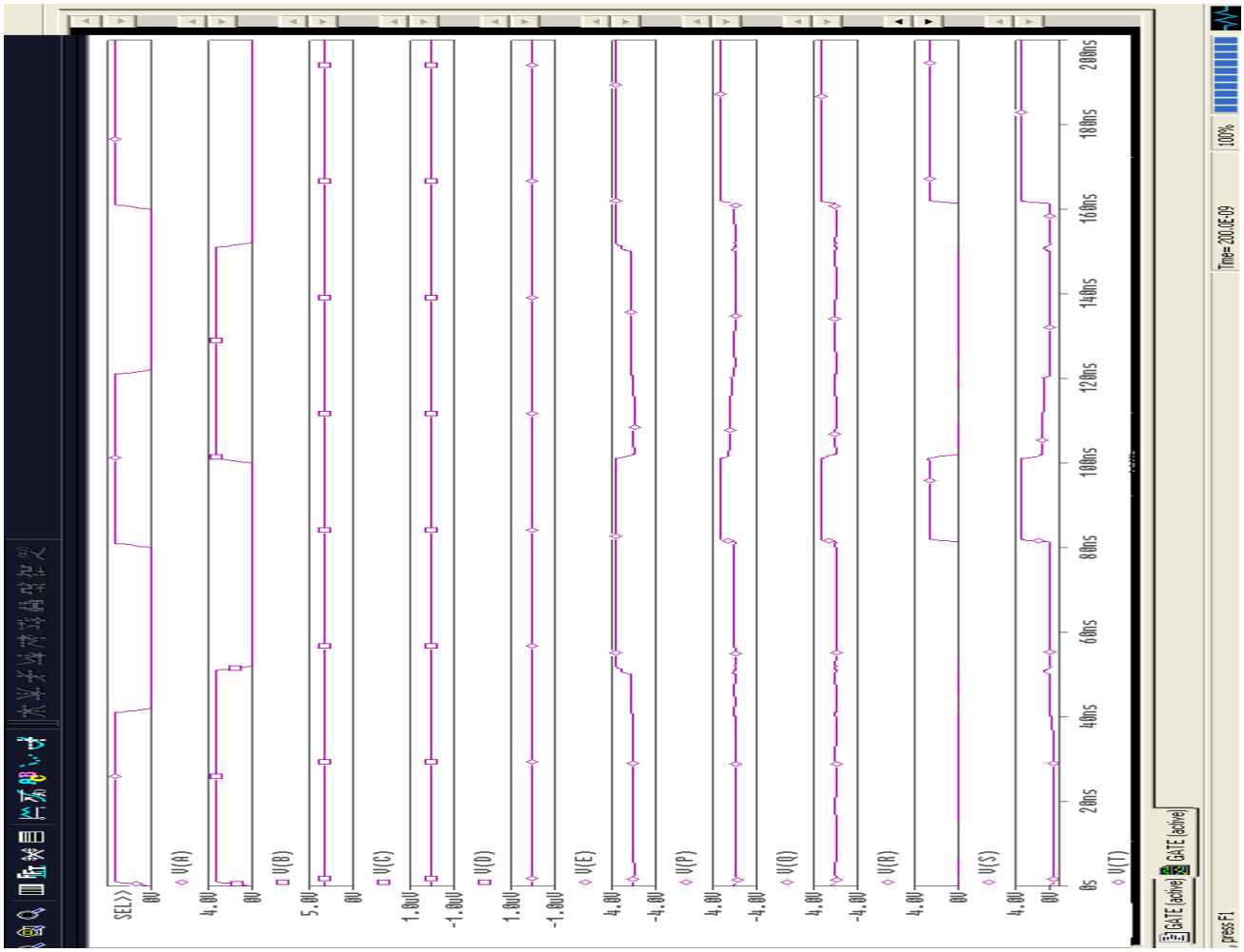
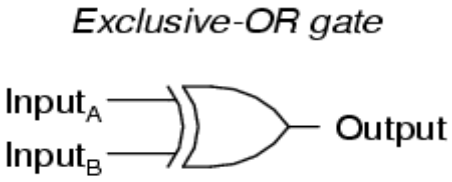


Fig 5.2 Input Output waveform of NOR gate with output at P for constant input C=1,D=0.E=0

5.5.3 EX OR Gate:



A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0

Fig 5.3 EX OR gate

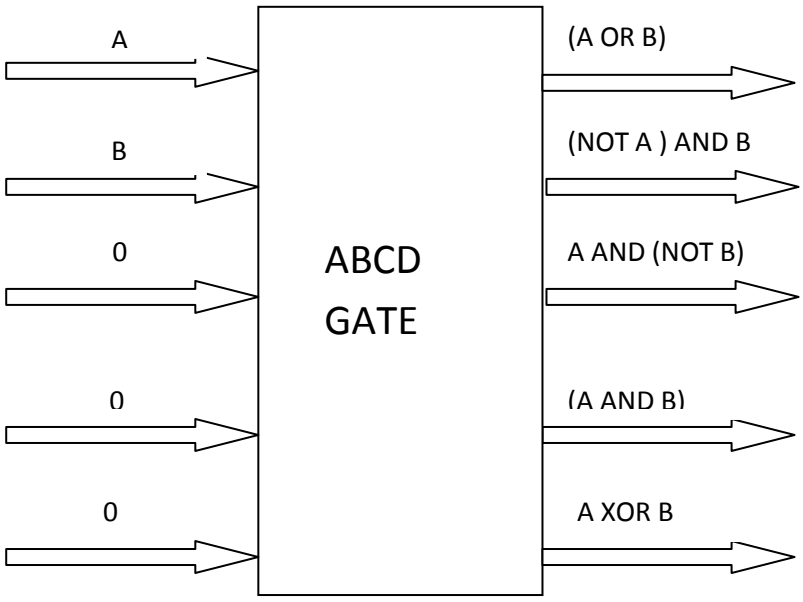


Fig 5.4 EX OR gate using ABCD Gate

To verify the functionality SPICE simulations are carried out using 0.35 µm CMOS technology parameters. The simulation results are shown in Fig.5.5. EX OR gate can be made using ABCD gate with output at T for constant input C=1,D=0.E=0 and the Simulation results are found to be in accordance with theory.

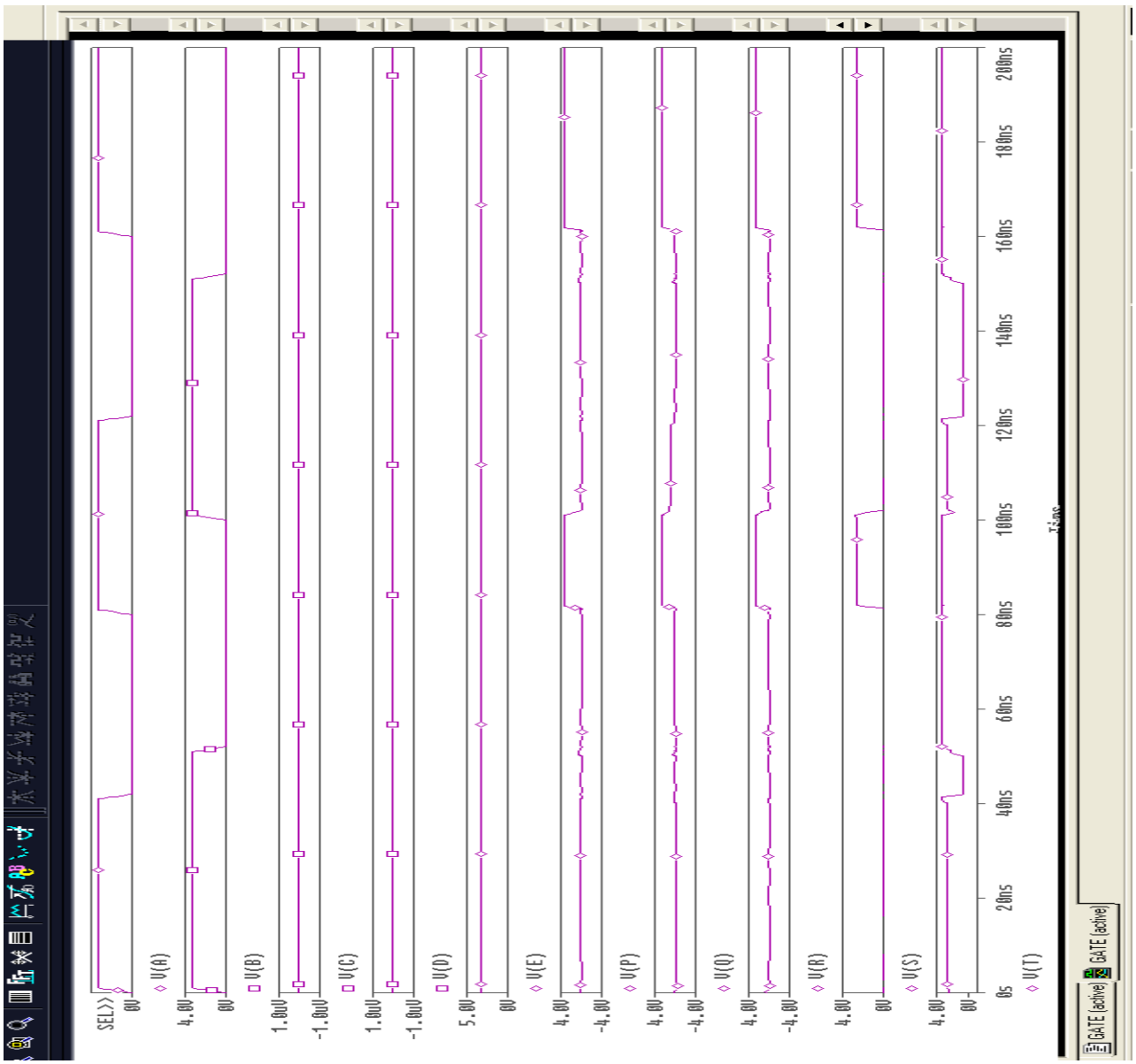


Fig 5.5 Input Output waveform of EX OR gate using ABCD gate with output at T for constant input C=1,D=0.E=0

5.5.4 EX NOR Gate

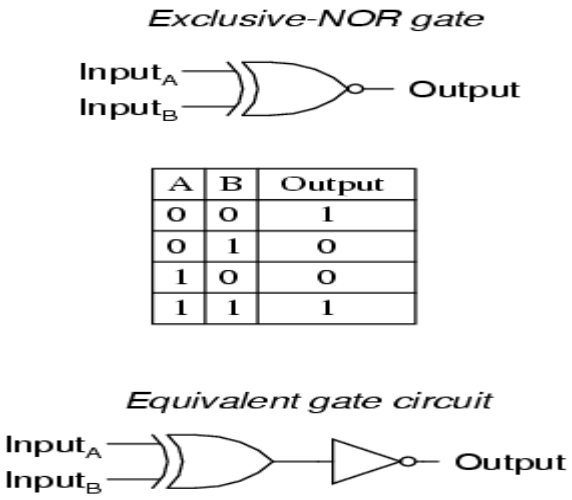


Fig 5.6 EX NOR Gate

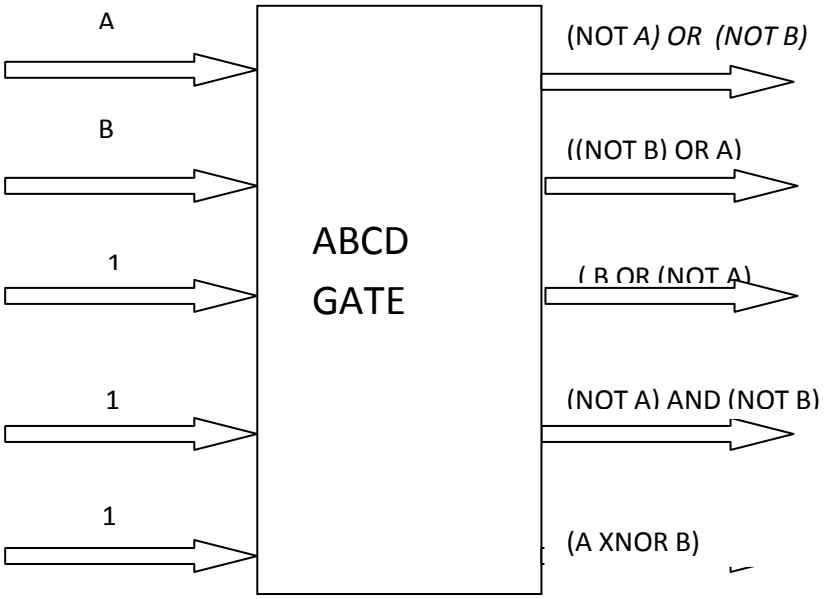


Fig 5.7 EX NOR gate using ABCD Gate

To verify the functionality SPICE simulations are carried out using 0.35 µm CMOS technology parameters. The simulation results are shown in fig 5.8. EX NOR gate can be made using ABCD gate with output at T for constant input C=1,D=1.E=1 and the Simulation results are found to be in accordance with theory.

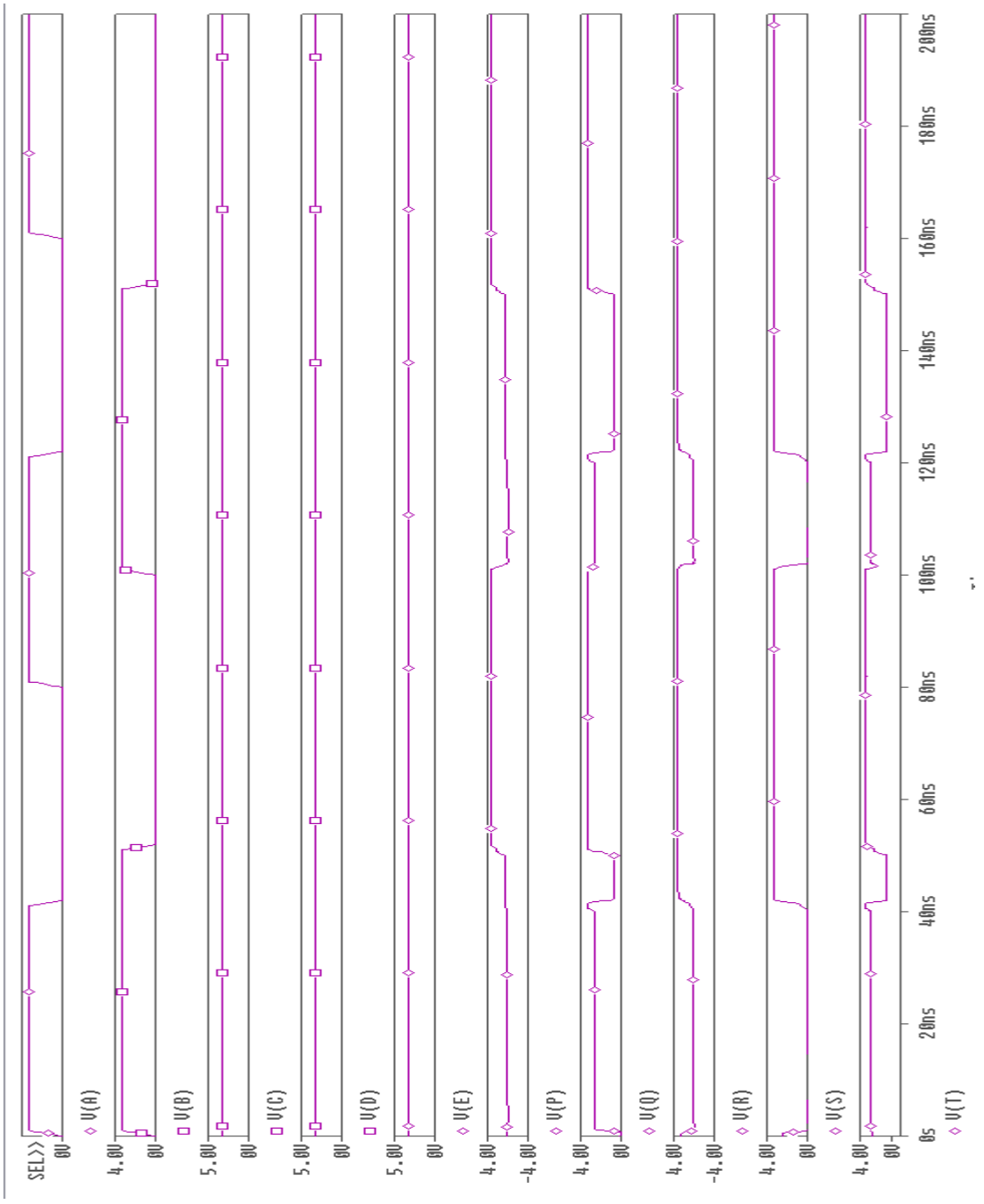


Fig 5.8 Input Output waveform of EX NOR gate using ABCD gate with output at T for constant input C=1,D=1.E=1

5.5.5 3 X 8 Decoder

Inputs			Outputs							
X	Y	Z	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	**1**	0	0	0	0	0	0	0
0	0	1	0	**1**	0	0	0	0	0	0
0	1	0	0	0	**1**	0	0	0	0	0
0	1	1	0	0	0	**1**	0	0	0	0
1	0	0	0	0	0	0	**1**	0	0	0
1	0	1	0	0	0	0	0	**1**	0	0
1	1	0	0	0	0	0	0	0	**1**	0
1	1	1	0	0	0	0	0	0	0	**1**

Table 5.1: Truth table of 3X8 decoder

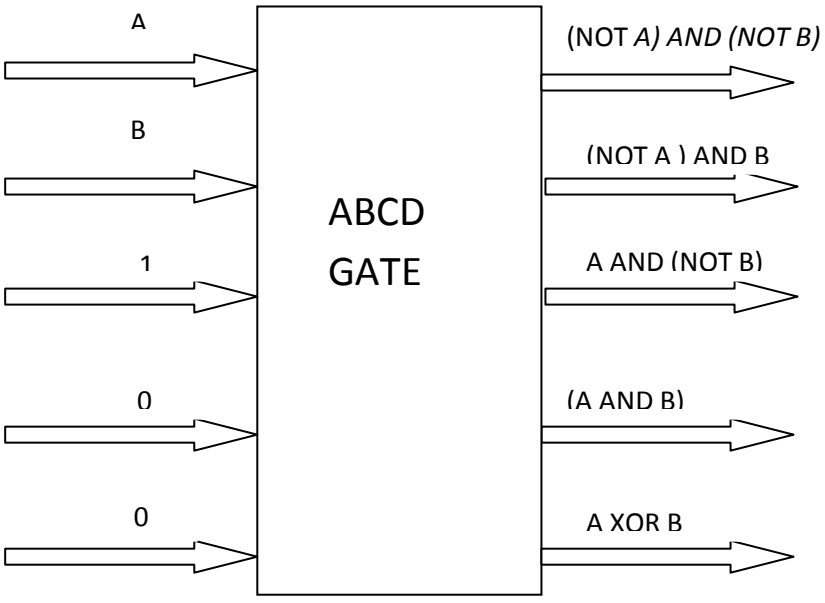


Fig 5.9 3 X 8 decoder using ABCD Gate

To verify the functionality SPICE simulations are carried out using 0.35 µm CMOS technology parameters. The simulation results are shown in Fig.5.10. 3X8 decoder can be made using ABCD gate with output at PQRS for constant input C=1,D=0.E=0 and the Simulation results are found to be in accordance with theory.

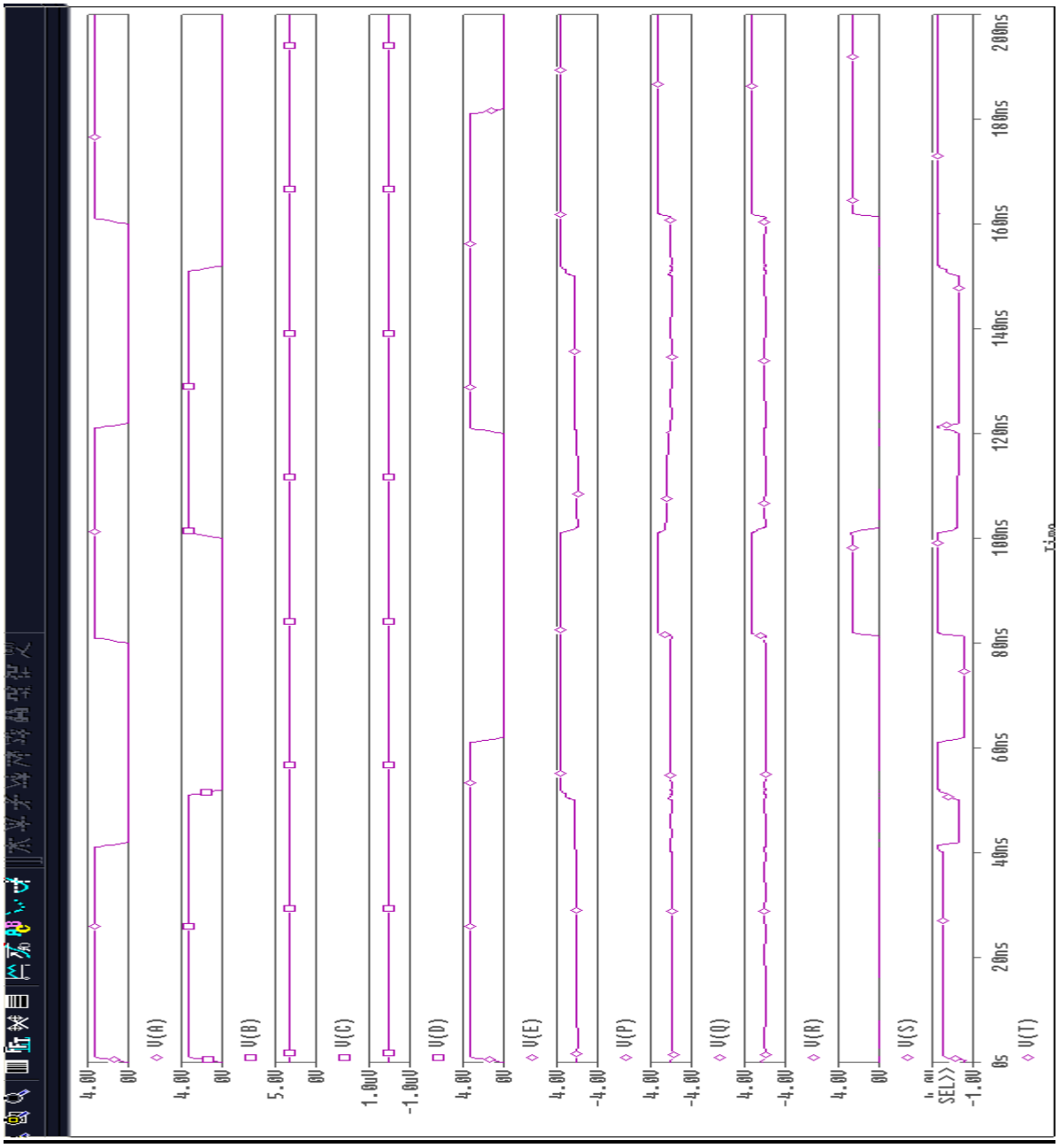


Fig 5.10 Input Output waveform of Decoder using ABCD gate with output at P,Q,R,S for constant input C=1,D=0.E=0

5.5.6. Half Adder:

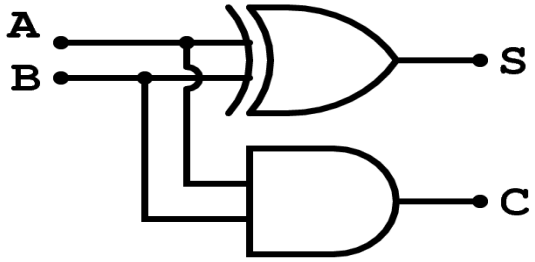


Fig 5.11 Half Adder

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Table 5.2: Truth table of Half Adder

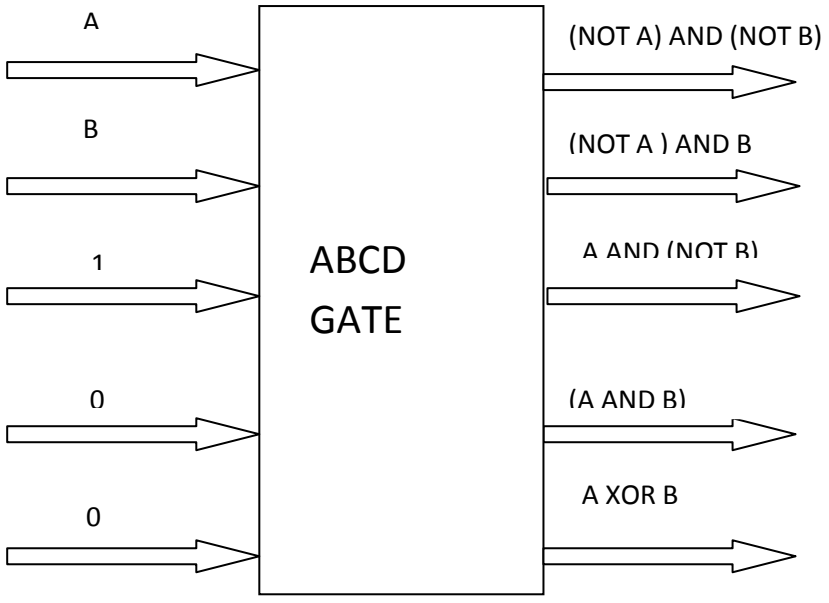


Fig 5.12 Half Adder using ABCD Gate

To verify the functionality SPICE simulations are carried out using 0.35 µm CMOS technology parameters. The simulation results are shown in Fig.5.13. Half adder can be made using ABCD gate with output at T and S for constant input C=0,D=0.E=0 and the Simulation results are found to be in accordance with theory.

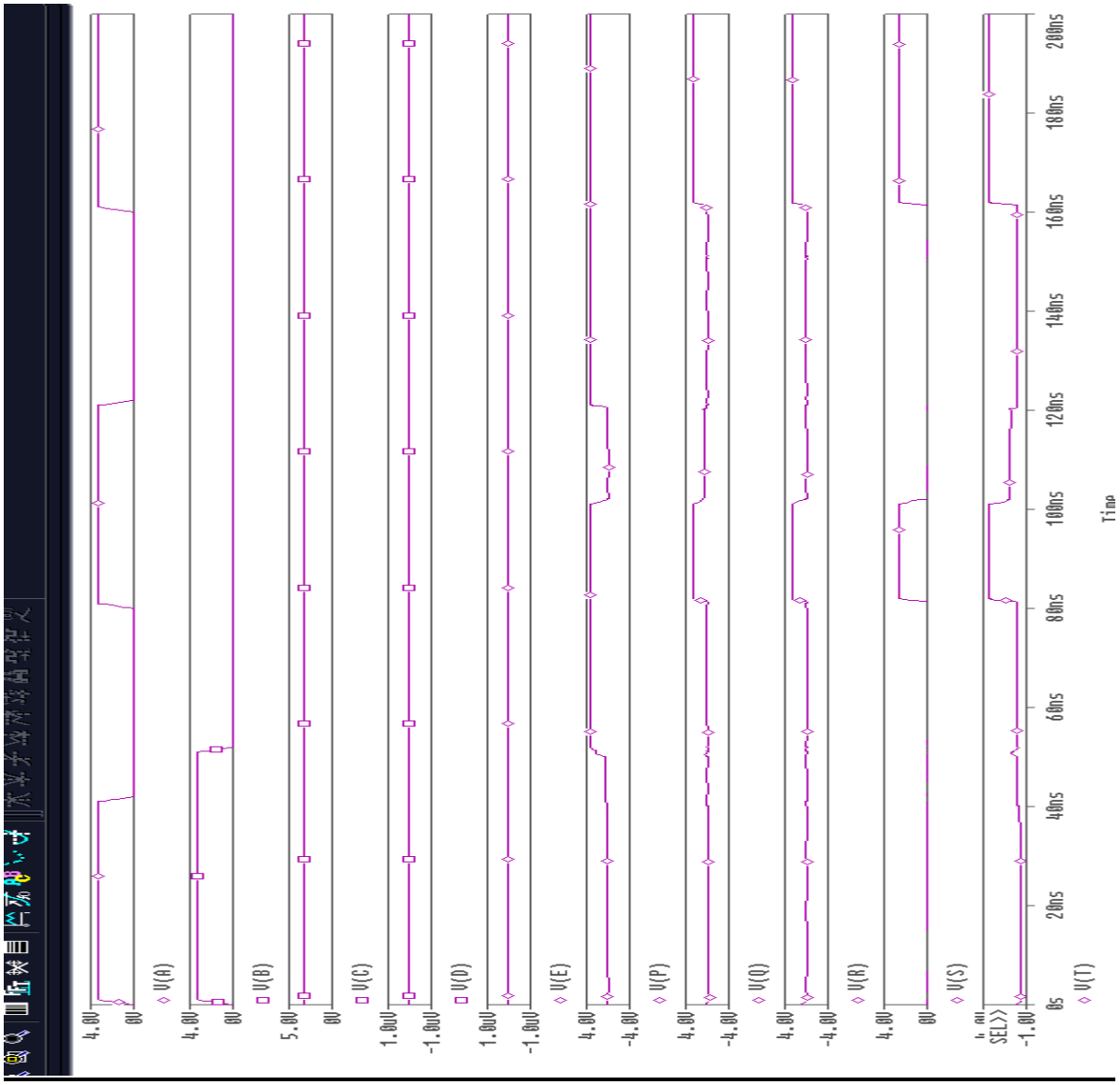


Fig 5.13 Input Output waveform of Half Adder using ABCD gate with output at T and S for constant input C=0,D=0.E=0

5.5.7. Half Subtractor :

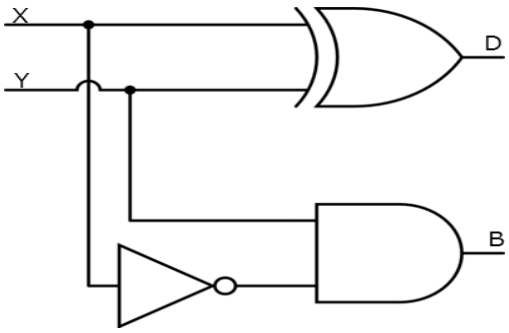


Fig 5.14 Half Subtractor

A	B	DIFFERENCE	BORROW
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Table 5.3: Truth table of Half Subtractor

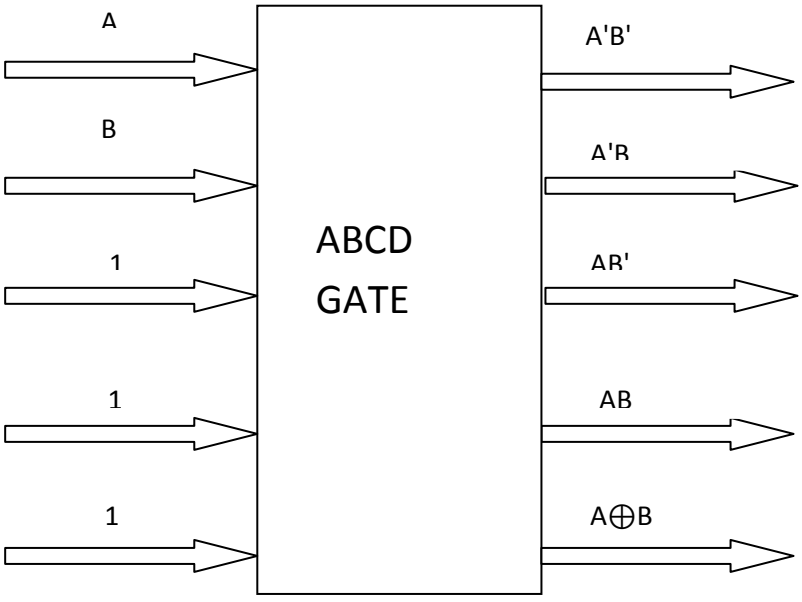


Fig 5.15 Half Subtractor using ABCD Gate

To verify the functionality SPICE simulations are carried out using 0.35 µm CMOS technology parameters. The simulation results are shown in Fig.5.16. Half subtractor can be made using ABCD gate with output at T and S for constant input C=1,D=0.E=0 and the Simulation results are found to be in accordance with theory.

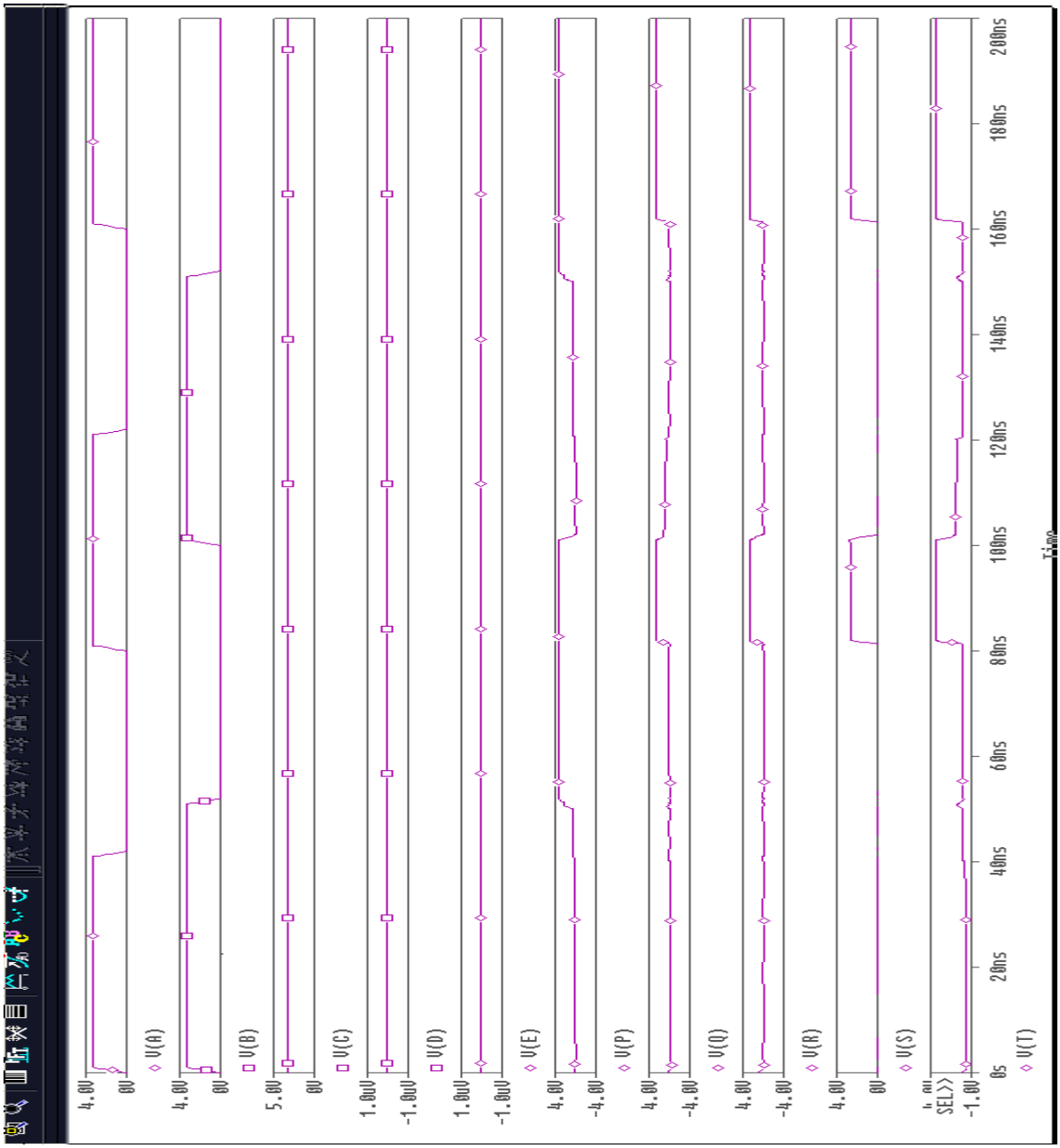


Fig 5.16 Input Output waveform of Half Subtractor using ABCD gate with output at T and S for constant input C=1,D=0.E=0

5.5.7 ONE BIT COMPARATOR:

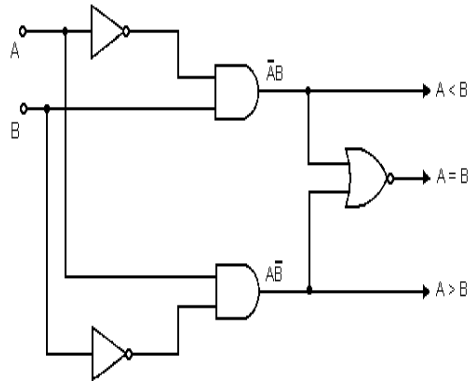


Fig 5.17 Comparator

A	B	A>B	A<B	A=B
0	0	0	0	1
0	1	0	1	0
1	0	1	0	0
1	1	0	0	1

Table 5.4: Truth table of comparator

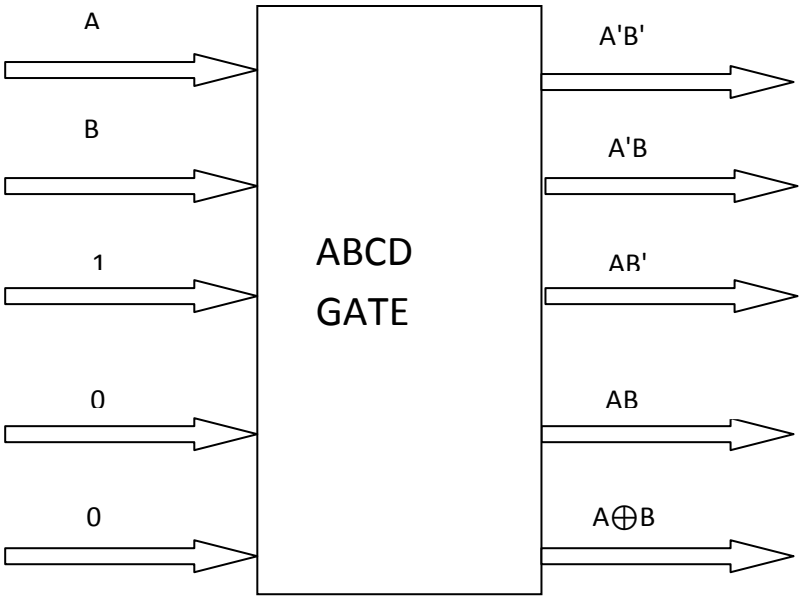


Fig 5.18 One bit comparator using ABCD Gate

To verify the functionality SPICE simulations are carried out using 0.35 μm CMOS technology parameters. The simulation results are shown in Fig.5.19. One bit comparator can be made using ABCD gate with output at PQRS for constant input C=1,D=0.E=0 and the Simulation results are found to be in accordance with theory.

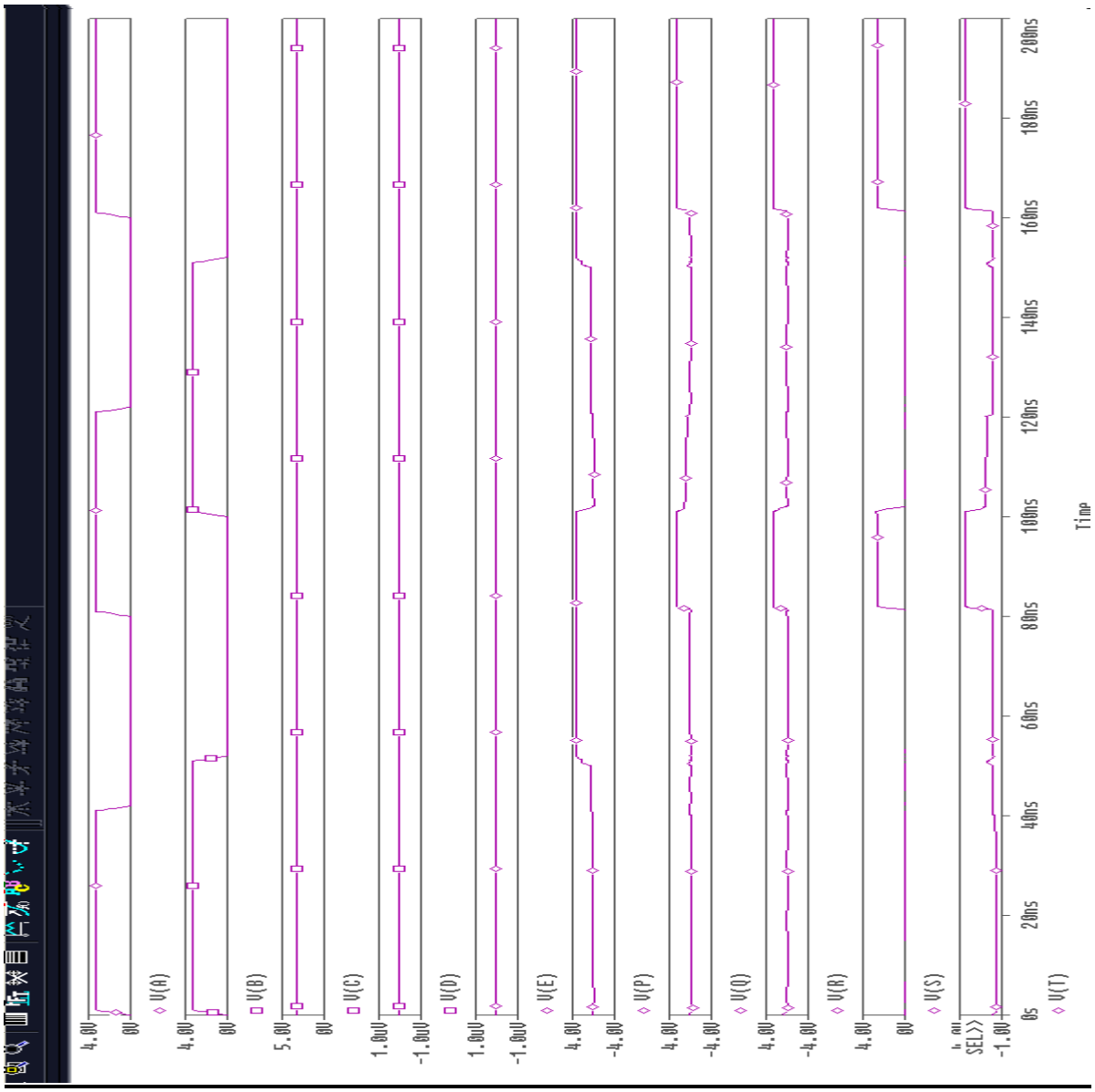


Fig 5.19 Input Output waveform of Comparator using ABCD gate with output at P,Q, Rand S for constant input C=1,D=0.E=0

5.5.7 Even Parity Detector:

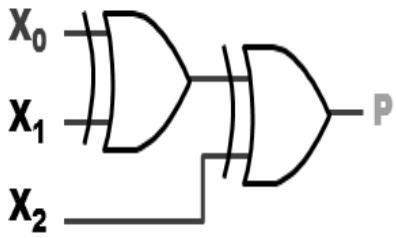


Fig 5.20 Even Parity Detector

D1	D2	D3	Even-Parity
0	0	0	True
0	0	1	False
0	1	0	False
0	1	1	True
1	0	0	False
1	0	1	True
1	1	0	True
1	1	1	False

Table 5.5: Truth table even parity detector

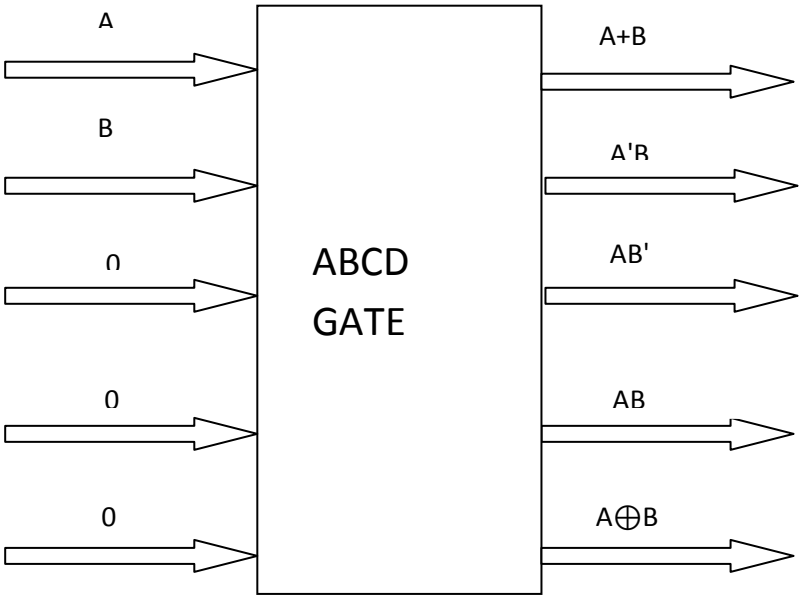


Fig 5.21 Even parity detector using ABCD Gate

To verify the functionality SPICE simulations are carried out using 0.35 µm CMOS technology parameters. The simulation results are shown in Fig.5.22. Even parity detector can be made using ABCD gate with output at T, for constant input C=0,D=0.E=0 and the Simulation results are found to be in accordance with theory.

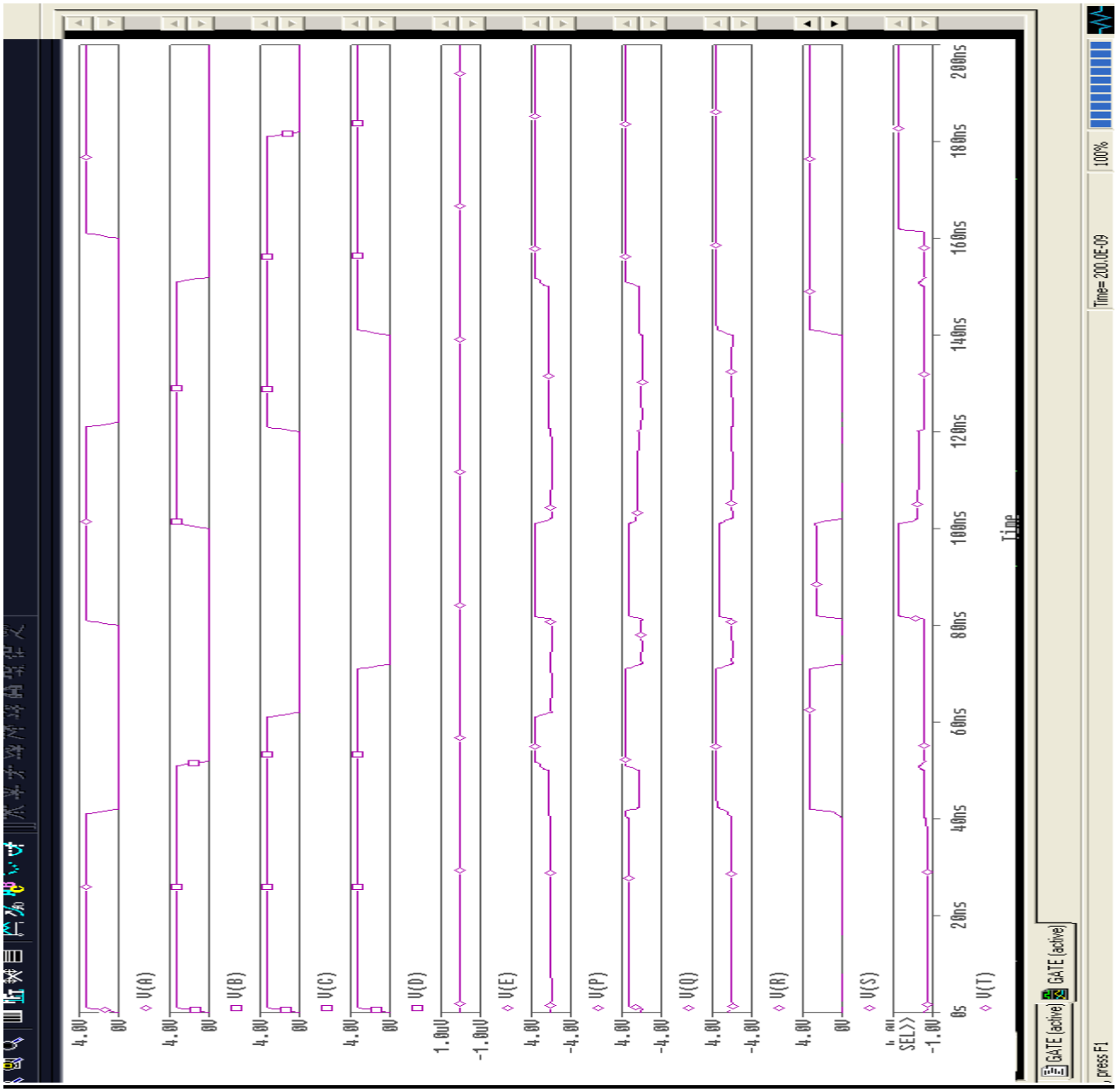


Fig 5.22 Input Output waveform of Even parity detector using ABCD gate with output at T for constant input C=0,D=0.E=0

To verify the functionality SPICE simulations are carried out using 0.35 µm CMOS technology parameters. The simulation results are shown in Fig.5.23. Even parity generator can be made using ABCD gate with output at T for constant input C=1,D=0.E=1 and the Simulation results are found to be in accordance with theory.

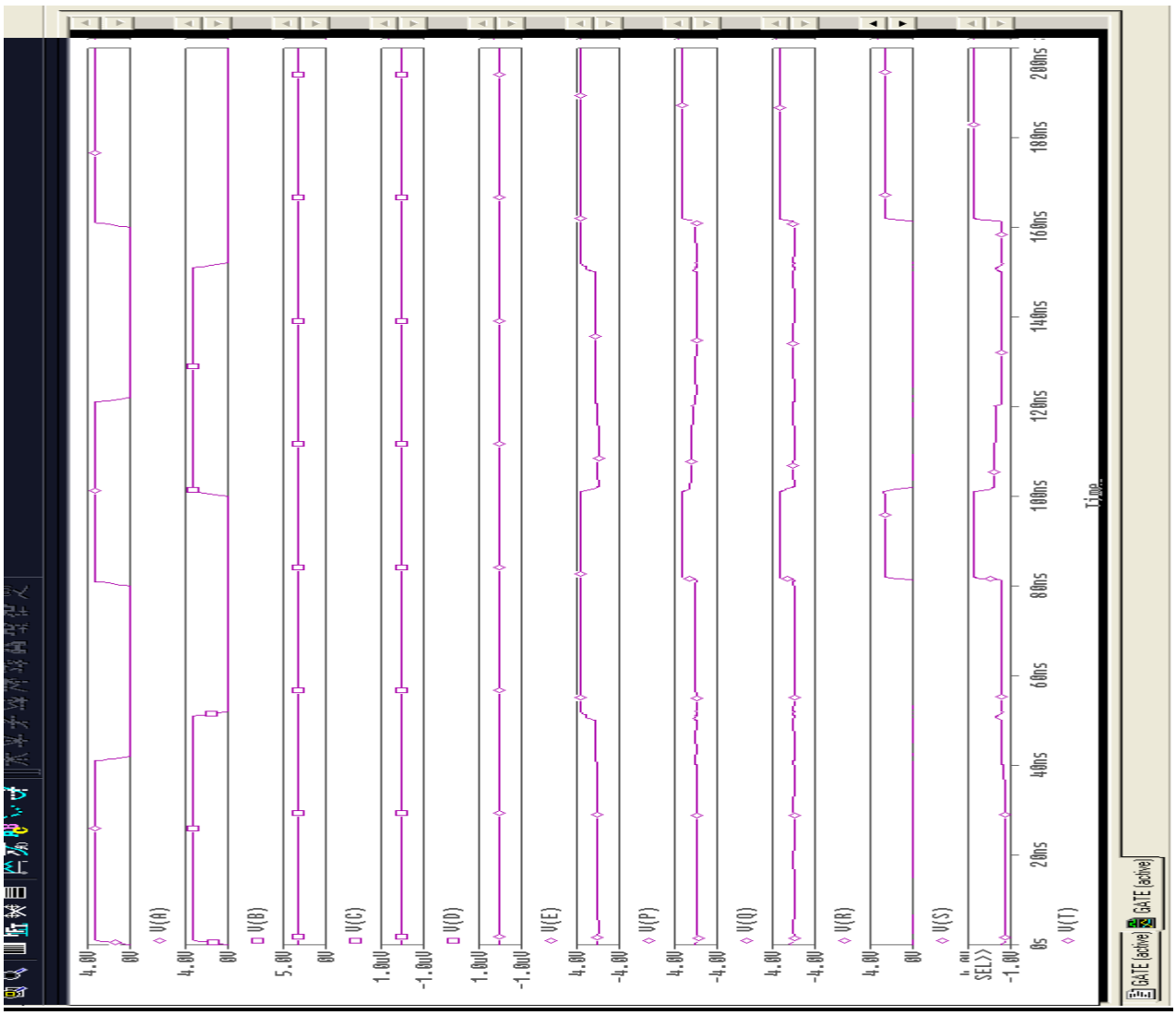


Fig 5.23 Input Output waveform of Even parity generator using ABCD gate with output at T for constant input C=1,D=0.E=1

To verify the functionality SPICE simulations are carried out using 0.35 µm CMOS technology parameters. The simulation results are shown in Fig.5.24. Odd parity detector can be made using ABCD gate with output at T for constant input C=1, D=0.E=1 and the Simulation results are found to be in accordance with theory.

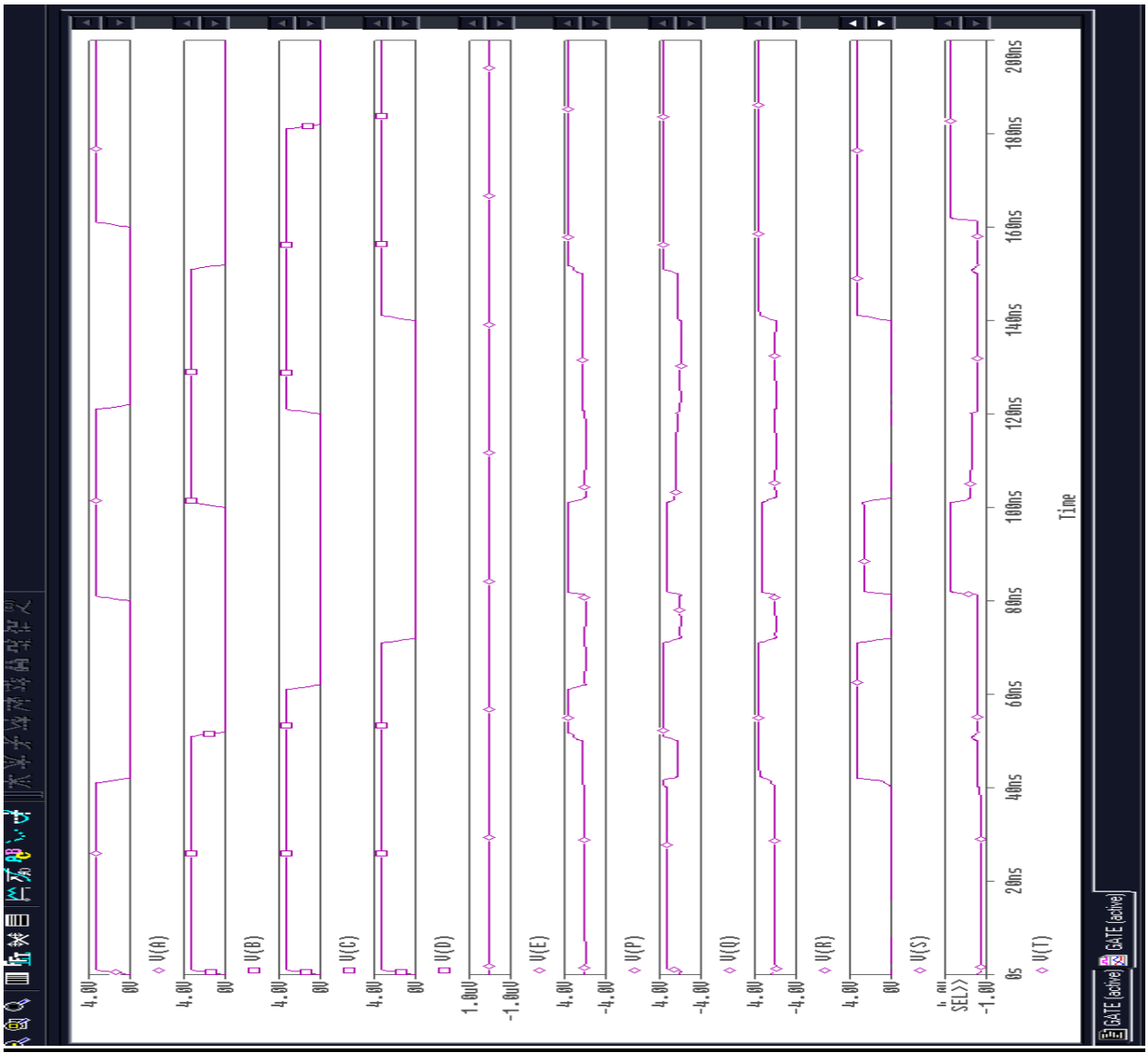


Fig 5.24 Input Output waveform of Odd parity detector using ABCD gate with output at T for constant input C=1,D=0.E=1

To verify the functionality SPICE simulations are carried out using 0.35 µm CMOS technology parameters. The simulation results are shown in Fig.5.25. Odd parity generator can be made using ABCD gate with output at T for constant input C=1, D=1.E=1 and the Simulation results are found to be in accordance with theory.

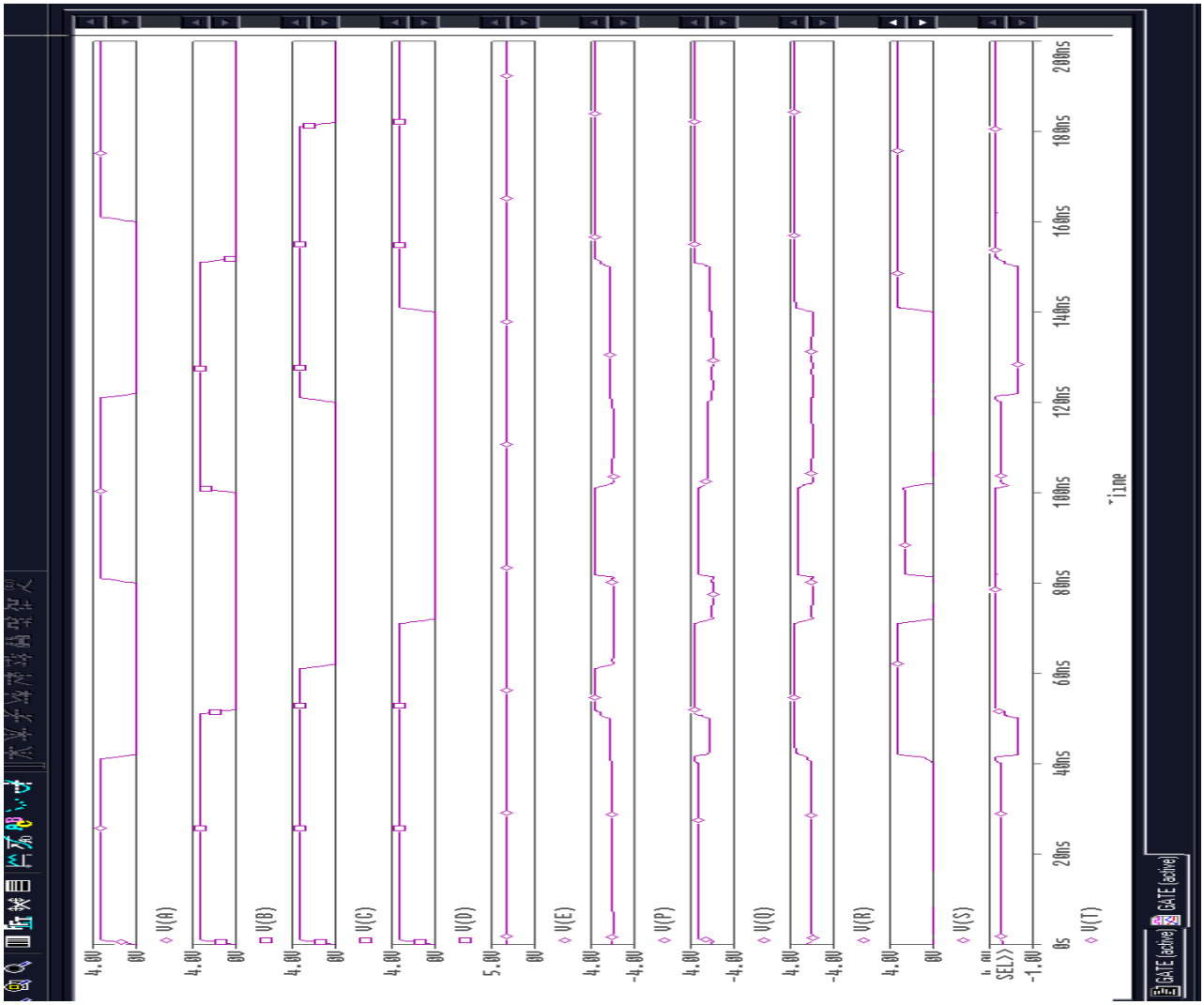


Fig 5.25 Input Output waveform of Odd parity generator using ABCD gate with output at T for constant input C=1,D=1.E=1

CHAPTER 6:

CONCLUSION

The focus of this work is the application of a reversible logic gate for implementing multiple functions like universal gate, decoder/DMUX. comparator, half adder, half subtractor, even/odd parity detector which are of importance in VLSI communication systems and other significant applications areas like such as quantum computing, nano-technology and optical computing. In the present proposal an attempt is made to design a multifunction reversible logic gate keeping in view the optimization factors of the reversible circuits.

This work also aims at minimising the parameters like number of garbage outputs, number of constant inputs, number of reversible gates and their levels. The proposed logic gate is highly optimized as it does not yield the garbage output and at the same time it is highly flexible as it produces important basic functions used in logic circuit design. The future work includes applying concept of reversible logic to build different combinational circuits using new flexible reversible gate.

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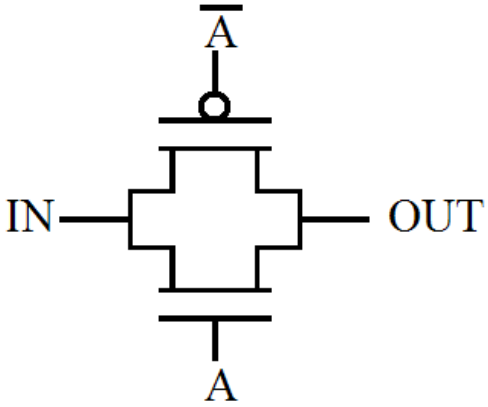
APPENDIX:

Transmission Gates

Basically, a transmission gate made up of two field effect transistors , in which - in contrast to conventional discrete field effect transistor - the substrate terminal (Bulk) is connected internally to the source terminal. The two transistors, an n-channel MOSFET and a p-channel MOSFET are thereby connected in parallel , but only the source and drain terminals of the two transistors are connected together. The gates are in a transmission gate via a NOT gate connected with each other (inverter), thereby a resulting control terminal is formed. However, since a transmission gate to block flow in either direction, must be to the substrate terminals of each power supply potential is connected to ensure that the substrate diode is always in the reverse direction to operate. The substrate terminal of the n-channel MOSFET is thus connected to the negative supply voltage potential and the substrate terminal of the p-channel MOSFETs connected to the positive supply voltage potential. The control input is a logic zero (negative power supply potential) is applied to the gate of the n-channel MOSFET is also at a negative supply voltage potential. The gate of the p-channel MOSFETs is located, due to the inverter at the positive supply voltage potential. Regardless of on which switching terminal of the transmission gate (A or B) a voltage is applied (within the permissible range), the gate-source voltage of the n-channel MOSFETs of the p-channel MOSFETs is always negative, always positive be. Thus, neither of the two transistors will conduct, and the transmission gate locks. Is located at the control input a logic one , so and the gate terminal of the n-channel MOSFETs is located at a positive supply voltage potential. By the inverter, the gate terminal of the p-channel MOSFETs is now at a negative supply voltage potential. Since the substrate of the transistors is not connected to the source terminal, the drain and source terminals are almost equal and the transistors begin at a voltage difference between the gate terminal and a channel of the two terminals to conduct. If now one of the switching terminals of the transmission gate to a voltage near the negative supply voltage potential, so is most n-channel MOSFET has a positive gate-source voltage (gate-drain voltage), and the transistor begins to conduct : The transmission gate passes. The voltage at one of the switching terminals of the transmission gate is now raised continuously up to the positive supply voltage potential, and then the gate-source voltage is decreased (gate-drain) voltage of the n-channel MOSFETs, and begins to turn off. At the same time, however, the p-channel MOSFET has a negative gate-source voltage (gate-drain) voltage

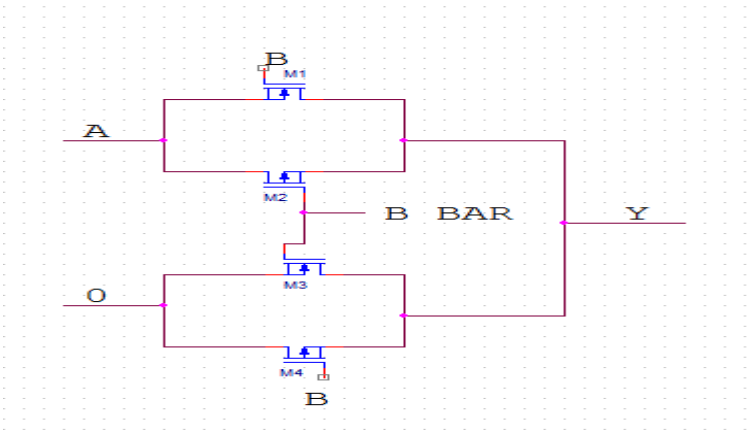
built up which this transistor starts to conduct and the transmission gate turns on further. Thereby it is achieved that the transmission gate passes over the entire voltage range



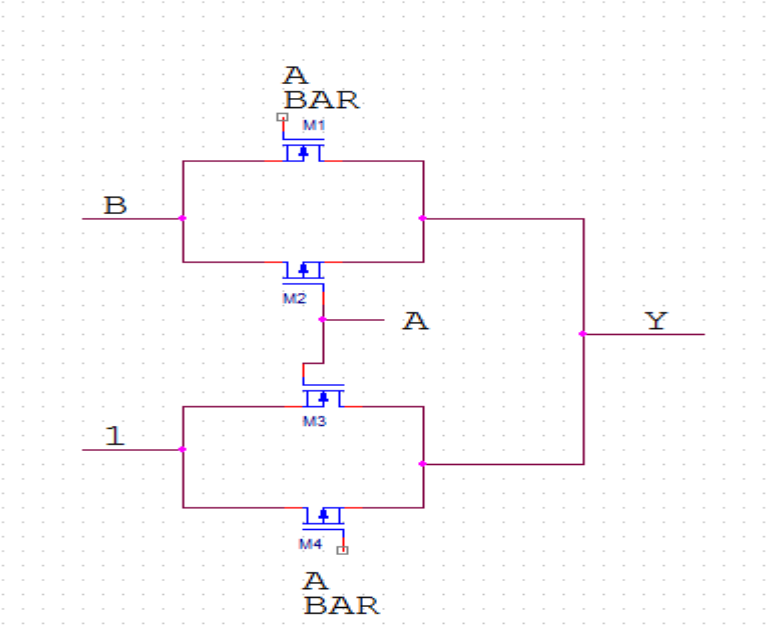
CONTROL		INPUT	OUTPUT
PMOS	NMOS	IN	OUT
0	1	0	0
0	1	1	1
1	0	0	HIGH IMPEDANCE
1	0	0	HIGH IMPEDANCE

.Fig 2.13 Transmission Gates

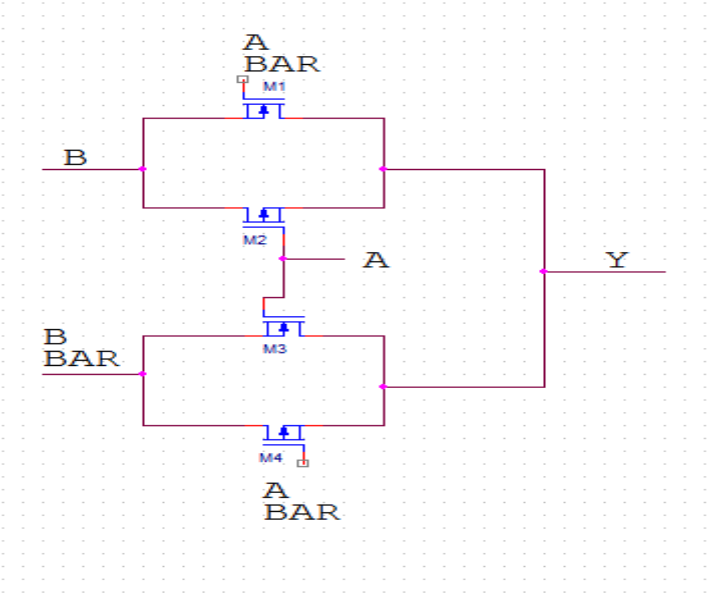
AND GATE USING TRANSMISSION GATE LOGIC:



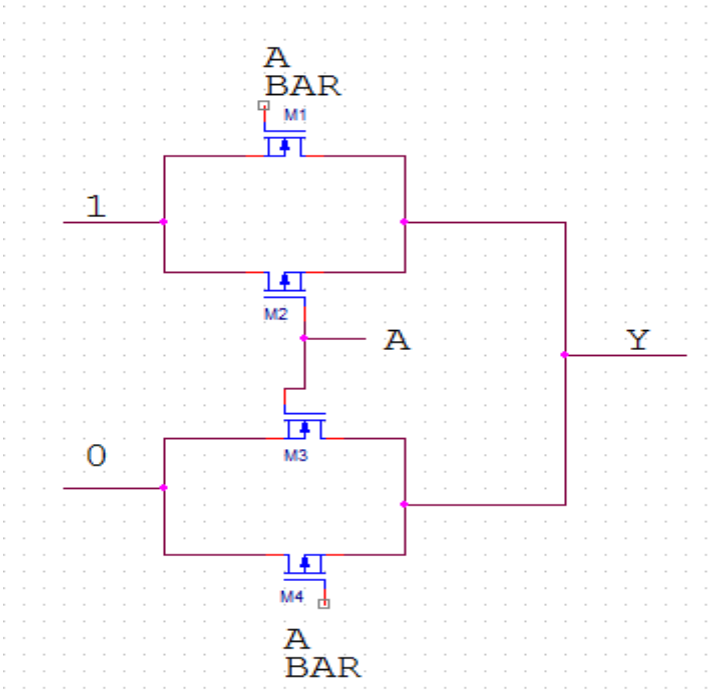
OR GATE USING TRANSMISSION GATE LOGIC:



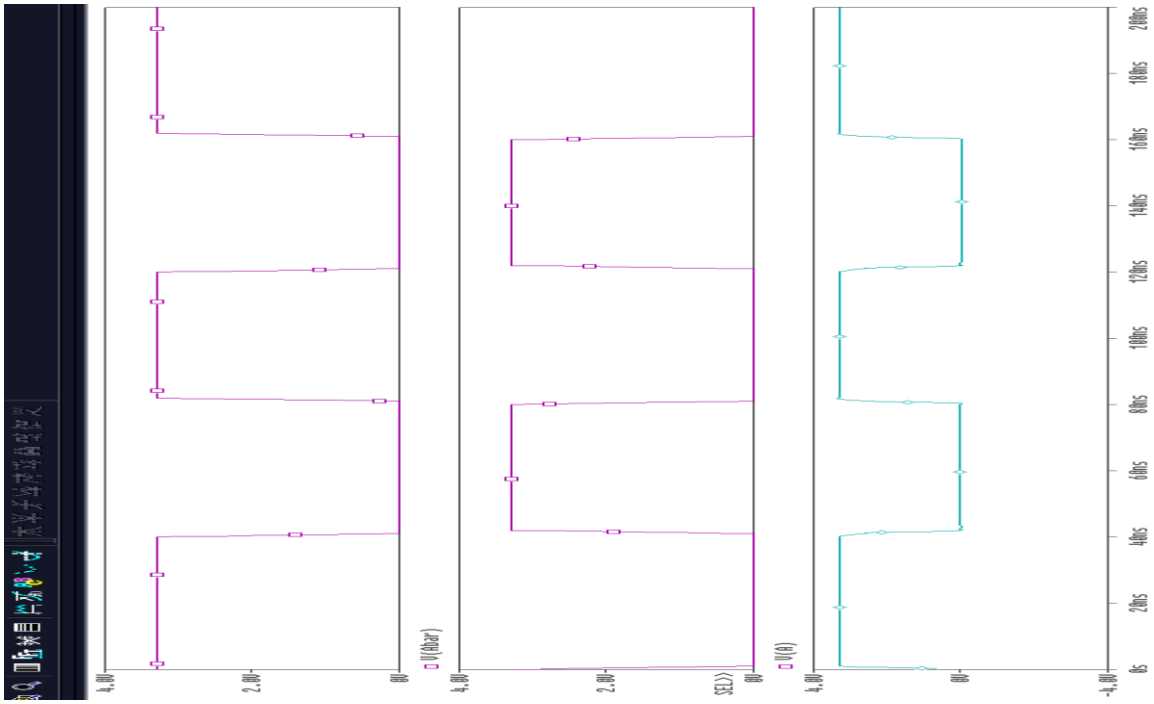
XOR GATE USING TRANSMISSION GATE LOGIC:



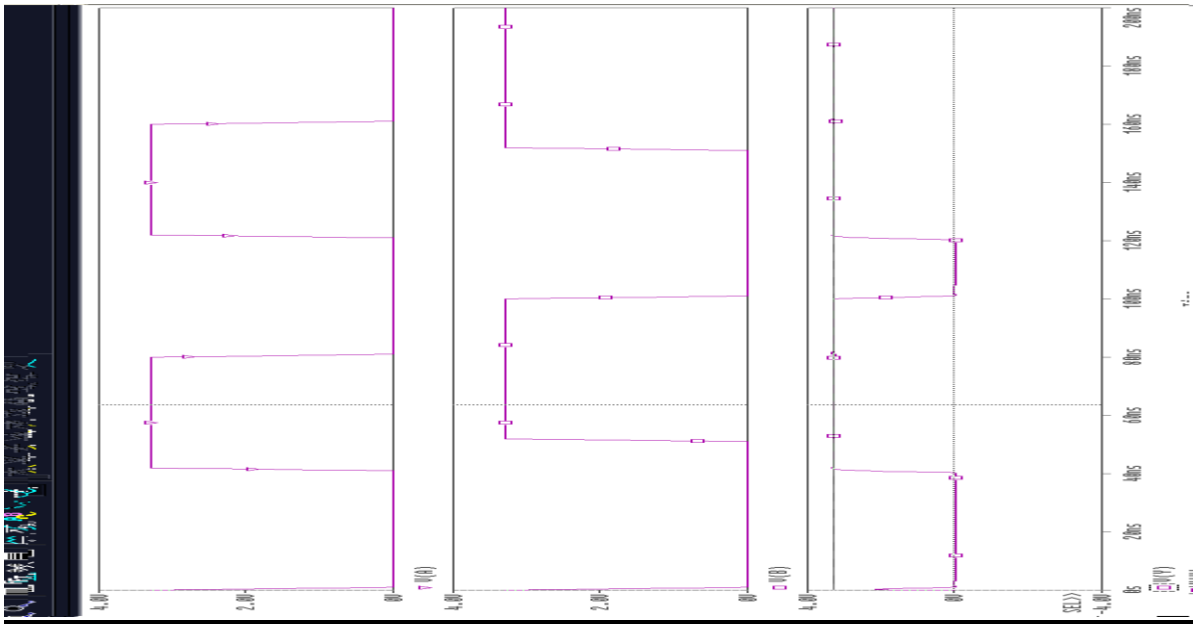
NOT GATE USING TRANSMISSION GATE LOGIC:



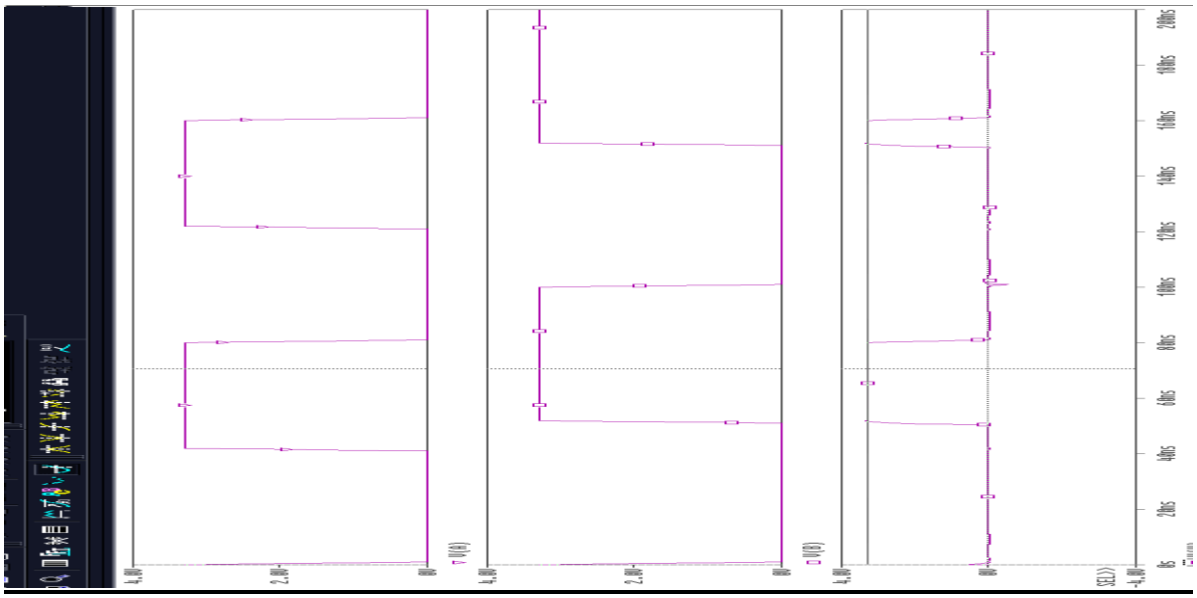
NOT Gate using transmission gate:



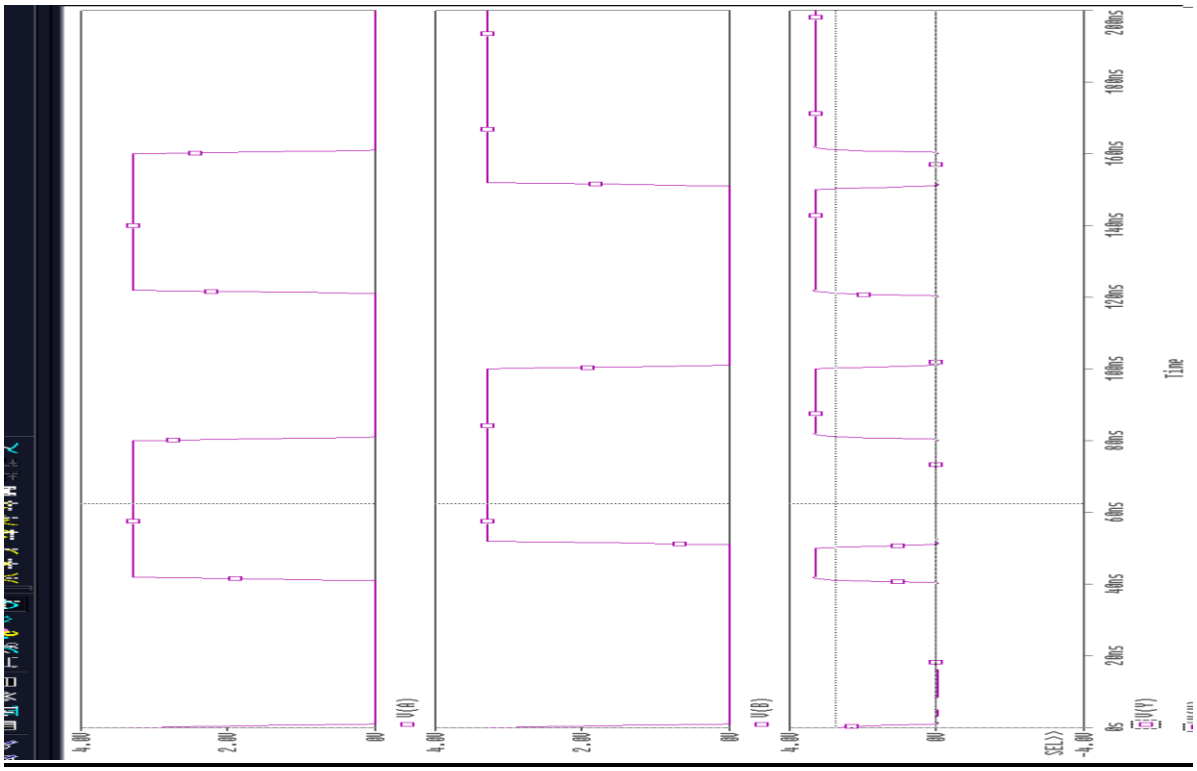
OR Gate using transmission gate:



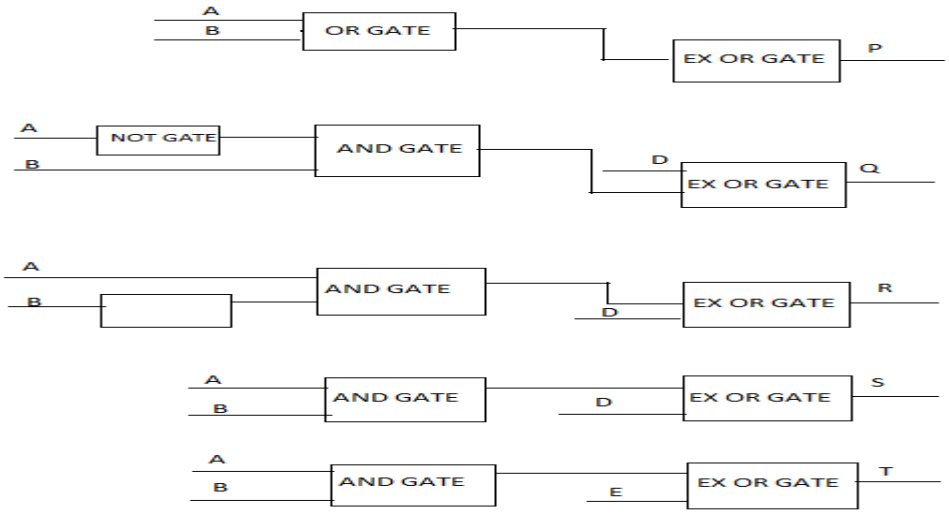
AND Gate using transmission gate:



EX OR Gate using transmission gate:



CIRCUIT IMPLEMENTATION OF ABCD GATE:


A
B
OR GATE
EX OR GATE
P
A
NOT GATE
B
AND GATE
D
EX OR GATE
Q
A
B
AND GATE
D
EX OR GATE
R
A
B
AND GATE
D
EX OR GATE
S
A
B
AND GATE
E
EX OR GATE
T

MODEL PARAMETERS:

.MODEL NMOS NMOS (LEVEL = 3, TOX = 7.9E-9, NSUB = 1E17,
+GAMMA=0.5827871, PHI=0.7, VTO=0.5445549, DELTA=0,
+UO = 436.256147, ETA = 0, THETA = 0.1749684,
+KP =2.055786E-4, VMAX=8.309444E4, KAPPA=0.2574081,
+RSH = 0.0559398, NFS = 1E12, TPG = 1, XJ = 3E-7,
+LD=3.162278E-11, WD=7.046724E-8, CGDO=2.82E-10,
+CGSO = 2.82E-10, CGBO = 1E-10, CJ = 1E-3, PB = 0.9758533,
+MJ =0.3448504, CJSW=3.777852E-10, MJSW=0.3508721)

.MODEL PMOS PMOS
+ (LEVEL = 3, TOX = 7.9E-9, NSUB = 1E17,
+GAMMA=0.4083894, PHI=0.7, VTO=-0.7140674, DELTA=0,
+UO =212.2319801, ETA=9.999762E-4, THETA=0.2020774,
+KP = 6.733755E-5, VMAX = 1.181551E5, KAPPA = 1.5,
+RSH = 30.0712458, NFS = 1E12, TPG=-1, XJ = 2E-7,
+LD=5.000001E-13, WD=1.249872E-7, CGDO=3.09E-10,
+CGSO = 3.09E-10, CGBO = 1E-10, CJ = 1.419508E-3,
+PB=0.8152753, MJ=0.5, CJSW=4.813504E-10, MJSW=0.5)