A Dissertation work on

DESIGN OF ANALOG GILBERT CELL MULTIPLIER USING CMOS TECHNOLOGY

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by

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DEDICATION

I would like to dedicate my work to my Father, Sh. Dharamvir Singh and my family members. I believe that I have made it possible merely due to the prayers and great moral support from my parents throughout my studies. Specially, my Father has been a source of great inspiration throughout this course work. My parents and family members have been always around to cheer me up and were always willing to partake in my sporadic study breaks.

As it is well said 'In every conceivable manner, the family is link to our past, bridge to our future.'

CERTIFICATE

This is to certify that the work contained in this dissertation entitled "**Design of Analog Gilbert Cell Multiplier Using CMOS Technology"** submitted by Jagdish Prasad (11/E&C/09) of Delhi College of Engineering in partial fulfilment of the requirement for the degree of Master of Engineering in Electronics & Communication is a bonafide work carried out under my guidance and supervision in the academic year 2009-11.

The work embodied in this dissertation has not been submitted for the award of any other degree to the best of my knowledge.

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Chapter 1

Introduction

Analog multiplier is one of the fundamental building blocks in analog circuit design. Particularly the multiplier is important in communication and signal processing circuits where they are commonly used for modulation, mixing, phase detection, and adaptive filtering. Advancements in biomedical devices and increasing portability of signal measurement equipment, low power multipliers for portable battery power applications are also becoming increasingly important. For cost effectiveness, low power multiplier solutions are needed. In bipolar technology, most multiplier architectures were originally developed where signal distortion can be kept low across a wide range of frequencies [2]. As digital design has advanced, the ability to build analog and digital circuits with a single technology has become increasingly important. Development of CMOS multiplier architectures has evolved to meet mixed signal and low power needs. Due to its low processing cost and low power consumption CMOS technology is better suited for digital circuits than bipolar technology. However, reaching the level of nonlinear error that bipolar multipliers can achieve is difficult in CMOS technology.

The variable transconductance Gilbert cell multiplier architecture [2], which is the most common bipolar multiplier architecture, allows for linear operation due to the exponential **I-V** relationship of the BJT. Most CMOS multiplier architectures are biased in the active region of strong inversion, where the MOSFET **I-V** relationship is a square-law relationship. Due to the different **I-V** relationship between bipolar and CMOS,

traditional architectures used for bipolar multipliers cannot easily be implemented in CMOS.

Although difficult to build, and limited in their performance, many CMOS square-law multipliers have been built based on the bipolar Gilbert cell architecture [18]- [20]. To do this, various linearization techniques are used to compensate for the square-law nonlinearities. Other square-law CMOS multiplier architectures use floating gates [21], signal attenuation [17] [18], and other forms of variable transconductance [12] [22], to achieve linearity. There are also CMOS architectures that implement bipolar characteristics, using lateral bipolar transistors [23], or the subthreshold region [24]. All of these architectures deviate from the traditional Gilbert cell architecture in implementation to achieve linear operation. This thesis will present CMOS multiplier architectures that more closely match the traditional bipolar Gilbert cell architecture. By doing so, some of the benefits of this architecture, such as low nonlinear error and higher bandwidths, can be taken advantage of.To evaluate analog multipliers it is important to understand some fundamental concepts. The function of a multiplier is just as its name implies, it multiplies two signals together. Ideal multipliers satisfy the fundamental multiplication expression.

$$Z = (A_0)\ XY, \qquad (1.1)$$

where output Z is the product of input signals X and Y, and A_0 , the multiplier gain constant.

A key multiplier specification is linearity. The level of nonlinearity that is allowed is dependent on the multiplier application. An example of this is in audio communications,
where signal distortion introduced by the multiplier is very undesirable. Another application where linearity is important is in precision signal

measurement equipment. A standard of less than 1 % nonlinear error is set for most bipolar analog multipliers [2].

Linearity is typically quantified by measuring the nonlinear error of the transfer function at unity gain. The % nonlinear error is defined by [12]

$$\% \, NLerror = \frac{Z-X}{Z_{FS}}.100 \qquad (1.2)$$

Referring to Equation (1.1), to measure the linearity on input X, input Y and the gain constant Ao, are set such that their product is equal to one (Ao·Y = 1). Then the difference between output Z and input X is taken across the full input range of X. This defines the nonlinear error, Z - X, which is the numerator of Equation 1.2. The % nonlinear error is then determined by dividing the nonlinear error by ZFS, which is the full scale output range when the multiplier is set at unity gain. This method of measuring linearity quantifies the output signal deviation from the ideal linear output signal characteristic when an input is swept across its full range. The same method is used to measure the multiplier linearity with regards to the Y input, where Ao·X = 1, and Y is swept and compared to Z.

Other key multiplier parameters are total harmonic distortion (THD), dynamic input range, bandwidth, DC offset and noise immunity. As with nonlinear error, the importance of each of these specifications depends on the application. All of these parameters, with exception of noise immunity, will be considered in this thesis.

Most multipliers can be classified as single-quadrant, two-quadrant, or fourquadrant

multipliers, depending on the possible polarities of the input signals. Single quadrant multipliers only allow positive input signals. Two-quadrant multipliers allow one signal to swing both positive and

negative. In four-quadrant multipliers, both input signals can be negative or positive.

The bipolar Gilbert cell multiplier architecture referred to above is also referred to as a "translinear" multiplier [5]. It is a fully differential four-quadrant current multiplier. Multiplying currents rather than voltages can offer better bandwidth performance, lower power operation and better noise immunity.

CMOS versions of the four-quadrant Gilbert cell multiplier is presented in this thesis.With a focus fully differential current-mode multipliers will be developed on linearity. High frequency operation (compared to other CMOS multiplier architecture) will also be addressed. All data is collected from Matlab, Mathcad and Cadence Spectre Spice simulations of circuits built in an AMIS *O.35-J.lm* process, with the exception of data presented in test results chapter (Chapter 6), where results from silicon are presented.

1.1 Contributions

Contributions of this thesis are as follows:

• Developed design methods for multiplier circuits biased in weak and moderate inversion.

• Fabricated and tested three CMOS multiplier circuits biased in weak and moderate inversion. The correlation between simulation and silicon is shown.

• Developed a highly linear, low power CMOS multiplier circuit.

• Developed an analysis method to identify the contributions of distortion from ideality factor mismatch in a CMOS weak inversion Gilbert cell multiplier.

• Proposed distortion cancellation methods to improve CMOS Gilbert cell multiplier linearity in weak and moderate inversion.

Chapter 2

Background: The Bipolar Gilbert Cell Multiplier

2.1 Introduction

The bipolar Gilbert cell was introduced by Barrie Gilbert in 1968. He started by developing a wide-band amplifier which consisted of a differential pair with diode connected I-V converters connected to each base terminal [1]. This wide-band amplifier configuration has a very linear transfer characteristic. The amplifier was then implemented into a four-quadrant multiplier configuration [2].

A block diagram of the Gilbert cell architecture is shown in Figure 2.1. $I_{T1} - I_{T2}$ and $I_{D1} - I_{D2}$ create the differential inputs, I_{Tin} and I_{Din}, respectively. These inputs are named with reference to their function, I_{T1} and I_{T2} being tail currents to differ-

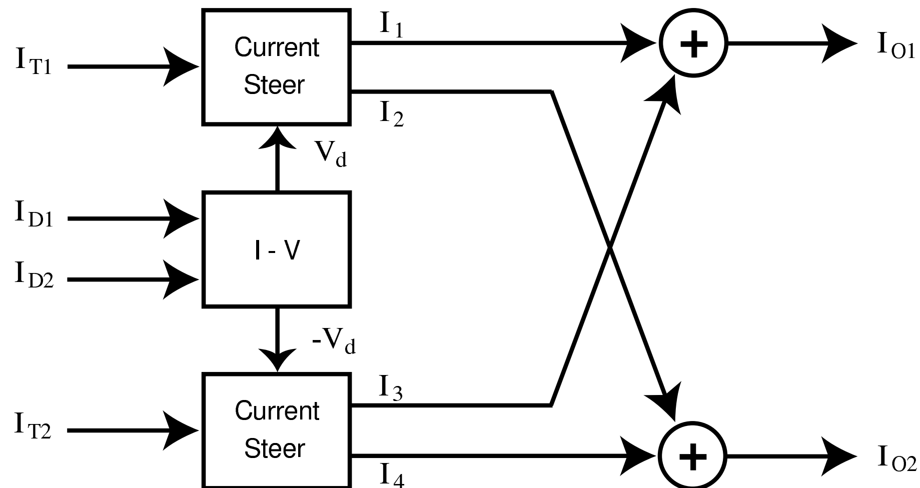


Figure 2.1: Gilbert cell architecture block diagram.

entially coupled devices, and I_{D1} and I_{D2} being input currents to current-to-voltage converting diode connected devices. The diode input currents (I_{D1} and I_{D2}) are first converted to voltages V_{D1} and V_{D2}. The difference of these voltages, V_d, is then applied to current steering devices, differentially controlling how tail input currents, I_{T1} and I_{T2}, are being split between currents I_1 and I_2, and I_3 and I_4, respectively. These currents are then cross-coupled and added. The output currents are $I_{O1} = I_1 + I_3$, and $I_{O2} = I_2 + I_4$. The final differential output current is then $I_{out} = I_{O1} - I_{O2}$.

If the full differential diode input current range is used at either positive or negative polarity, all of the tail currents will be steered to one output of each current steering block. This results in the full differential of the I_{Tin} input at the output, providing the maximum differential output current. Diode input currents that are smaller than the maximum will steer some of the tail current to the opposite output. Tail currents steered to the opposite output become common at the differential outputs and end up canceling when the final differential output current is taken. Thus, at $[I_{Din}]_{min}$, tail currents are divided equally, causing all current to be common at the output, and making $I_{out} = 0$.

An important point to note here is that the differential output current, I_{out}, can get no larger than the differential tail input current, I_{Tin}. This results in a maximum multiplier gain of unity. Based on this criterion, the gain constant, A_o, of the ideal multiplier expression (1.1) then becomes inverted maximum of one of the inputs, as shown in Equation (2.1),

$$Z = \left(\frac{1}{Y_{max}}\right) XY. \tag{2.1}$$

In the following sections, the design of the four-quadrant Gilbert cell multiplier will be evaluated by first analyzing the bipolar differential pair behavior. The effects of adding diode-connected devices to the inputs of the differential pair will then be evaluated. This configuration makes up a linear wide-band current amplifier, as discussed in [1]. Finally, two amplifiers will be combined into the multiplier configuration. This will result in a transfer characteristic that satisfies the ideal linear multiplier expression of Equation (2.1), where Z, X, and Y are differential signals.

2.2 Bipolar Differential Pair

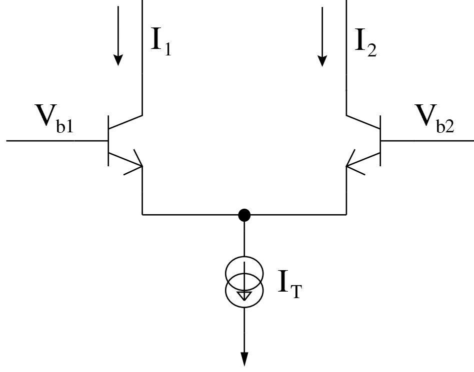


Figure 2.2: Bipolar differential pair.

To evaluate bipolar linear multiplication, the single differential pair of Figure 2.2 is first evaluated. The exponential I-V relationship applied to each transistor may be written

$$I_c = I_S e^{V_{be}/V_T}, \tag{2.2}$$

where I_c is the collector current, I_S is the saturation current, V_T is the thermal voltage, and V_{be} is the base to emitter voltage. The differential relationship between the two transistors introduces the additional constraint

$$I_1 + I_2 = \alpha I_T. \tag{2.3}$$

Combining equations (2.2) and (2.3) gives [3]

$$I_1 = \frac{\alpha I_T}{1 + e^{(V_{b2}-V_{b1})/V_T}}, \tag{2.4}$$

$$I_2 = \frac{\alpha I_T}{1 + e^{(V_{b1}-V_{b2})/V_T}}. \tag{2.5}$$

For the differential input voltage, $V_d = V_{b1} - V_{b2}$, the differential output current $I_{out} = I_1 - I_2$ is

$$I_{out} = \alpha I_T \left(\frac{e^{V_d/V_T} - e^{-V_d/V_T}}{2 + e^{-V_d/V_T} + e^{V_d/V_T}} \right). \tag{2.6}$$

The transfer characteristics are shown in Figure 2.3. There is a small linear range around the middle of each characteristic that is typically used for linear amplification of small signals.

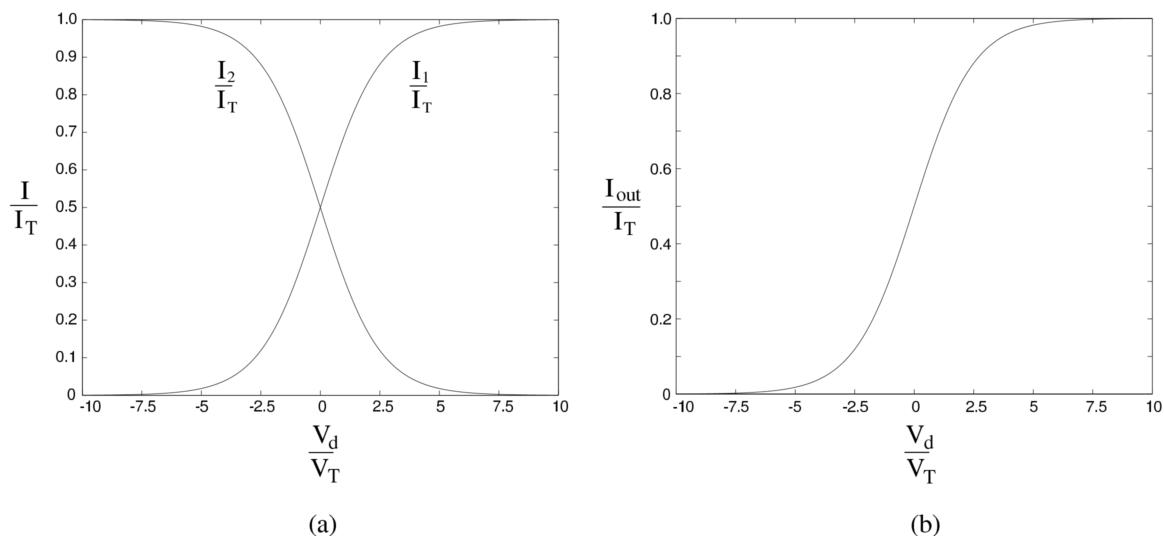


Figure 2.3: Bipolar differential pair transfer characteristics.

2.3 Bipolar Current-mode Amplifier

To increase the linear input range, diode connected devices can be added to the base terminals of the differential pair in the manner shown in Figure 2.4. If an input current is forced into the diode-connected devices, the input voltage from base to emitter becomes

$$V_{be} = V_T \ln\left(\frac{I_D}{I_s}\right). \tag{2.7}$$

The differential input voltage to the differential pair devices is now

$$V_d = V_{be1} - V_{be2} = V_T\left(\ln\left(\frac{I_{D1}}{I_s}\right) - \ln\left(\frac{I_{D2}}{I_s}\right)\right). \tag{2.8}$$

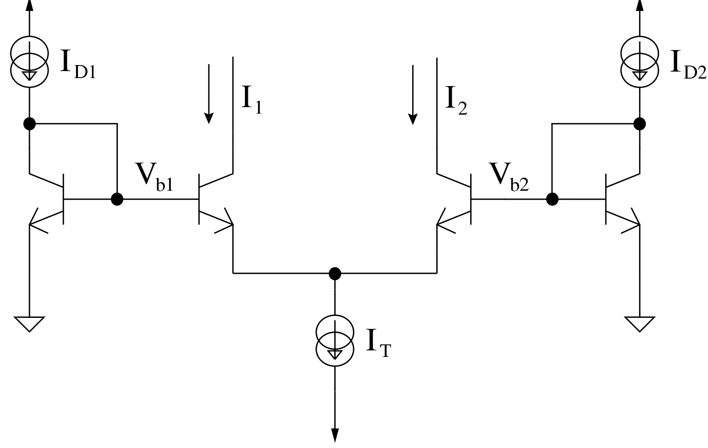


Figure 2.4: Bipolar current-mode amplifier.

Replacing $V_{b1} - V_{b2}$ in equations (2.4) and (2.5) with V_d from Equation (2.8) and evaluating the exponential term, the logarithmic terms in V_d cancel the exponential terms,

$$e^{V_d/V_T} = e^{\frac{V_T[\ln(I_{D1}/I_s) - \ln(I_{D2}/I_s)]}{V_T}} = \frac{e^{\ln(I_{D1}/I_s)}}{e^{\ln(I_{D2}/I_s)}} = \frac{I_{D1}}{I_{D2}}. \tag{2.9}$$

The collector currents then become

$$I_1 = \alpha I_T \left(\frac{I_{D2}}{I_{D1} + I_{D2}} \right), \tag{2.10}$$

$$I_2 = \alpha I_T \left(\frac{I_{D1}}{I_{D1} + I_{D2}} \right). \tag{2.11}$$

I_{out} now becomes

$$I_{out} = \alpha I_T \left(\frac{I_{D2} - I_{D1}}{I_{D1} + I_{D2}} \right). \tag{2.12}$$

Plots of equations (2.10), (2.11), and (2.12) are shown in Figure 2.5.

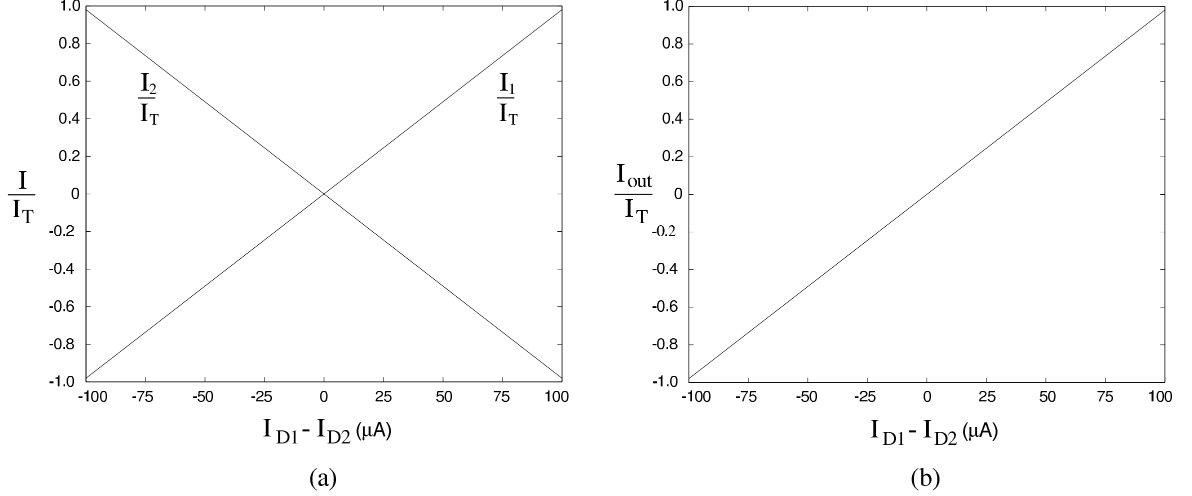


Figure 2.5: Bipolar current-mode amplifier, linear transfer characteristics.

The amplifier input current is defined as the difference between I_{D1} and I_{D2}. I_{D1} and I_{D2} function differentially according to

$$I_{D1} = I_Q + \Delta I, \tag{2.13}$$

$$I_{D2} = I_Q - \Delta I, \tag{2.14}$$

where I_Q is a quiescent midpoint of the maximum input swing, and ΔI is the deviation from that midpoint, having opposite polarity between I_{D1} and I_{D2}. For fully differential inputs,

$$\left[\frac{I_{D2} - I_{D1}}{I_{D1} + I_{D2}}\right]_{max} = 1. \tag{2.15}$$

Therefore, combining equations (2.12) and (2.15),

$$[I_{out}]_{max} = \alpha I_T. \tag{2.16}$$

It can be seen from the plots and equations that the linear input range has been increased to span the entire range of I_T. Due to the ratio in Equation (2.15), any differential input range can be used as long as all devices stay in the active region.

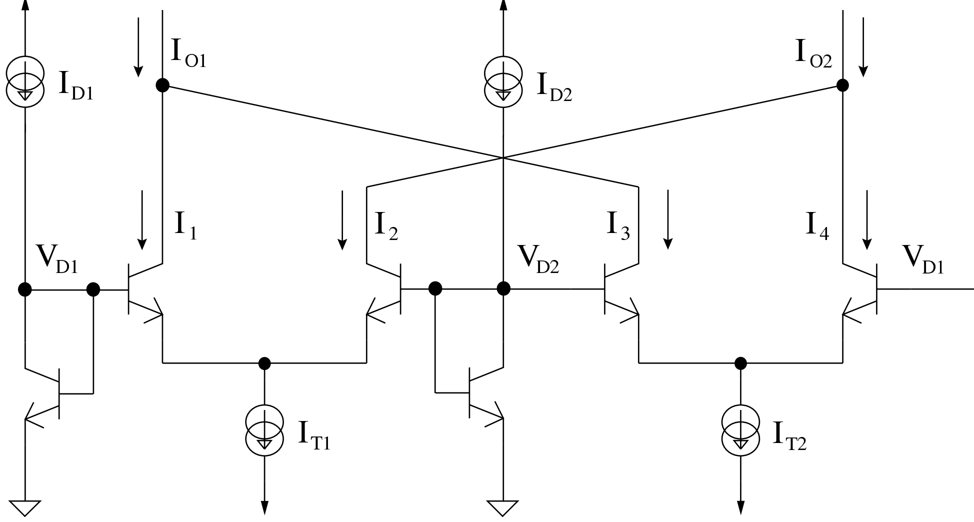


Figure 2.6: Bipolar Gilbert cell multiplier.

2.4 Bipolar Gilbert Cell Multiplier

Combining two current-mode amplifiers as shown in Figure 2.6 creates the Gilbert cell current-mode multiplier. Comparing Figure 2.6 to the block diagram of Figure 2.1, each differential pair acts as a current steering device. Each diode-connected device acts as an I-V converter. Also, each device port matches the naming conventions at each block port in the block diagram.

The Gilbert cell collector currents can be defined as

$$\mathrm{I_1} = \frac{\alpha \mathrm{I_{T1}}}{1 + \mathrm{e}^{-\mathrm{V_d}/\mathrm{V_T}}}, \tag{2.17}$$

$$\mathrm{I_2} = \frac{\alpha \mathrm{I_{T1}}}{1 + \mathrm{e}^{\mathrm{V_d}/\mathrm{V_T}}}, \tag{2.18}$$

$$\mathrm{I_3} = \frac{\alpha \mathrm{I_{T2}}}{1 + \mathrm{e}^{\mathrm{V_d}/\mathrm{V_T}}}, \tag{2.19}$$

$$\mathrm{I_4} = \frac{\alpha \mathrm{I_{T2}}}{1 + \mathrm{e}^{-\mathrm{V_d}/\mathrm{V_T}}}. \tag{2.20}$$

Combining collector currents according to $I_{O1} = I_1 + I_3$ and $I_{O2} = I_2 + I_4$, the differential output current, $I_{out} = I_{O1} - I_{O2}$, results in

$$I_{out} = \frac{\alpha(I_{T1} - I_{T2})(e^{V_d/V_T} - e^{-V_d/V_T})}{2 + e^{-V_d/V_T} + e^{V_d/V_T}}. \quad (2.21)$$

Plugging V_d from (2.8) into (2.21) gives

$$I_{out} = \frac{\alpha(I_{T1} - I_{T2})(I_{D2}/I_{D1} - I_{D1}/I_{D2})}{2 + I_{D2}/I_{D1} + I_{D1}/I_{D2}}. \quad (2.22)$$

Simplifying Equation (2.22) results in

$$I_{out} = \frac{\alpha}{(I_{D1} + I_{D2})}(I_{T1} - I_{T2})(I_{D2} - I_{D1}). \quad (2.23)$$

Comparing Equation (2.23) to the ideal multiplier expression (2.1), $I_{out} = Z$, $I_{D2} - I_{D1} = X$, and $I_{T1} - I_{T2} = Y$. Multiplying the common-base current gain, α, to the right side, Equation (2.23) matches the ideal linear multiplier expression (2.1). This is only true with fully differential inputs.

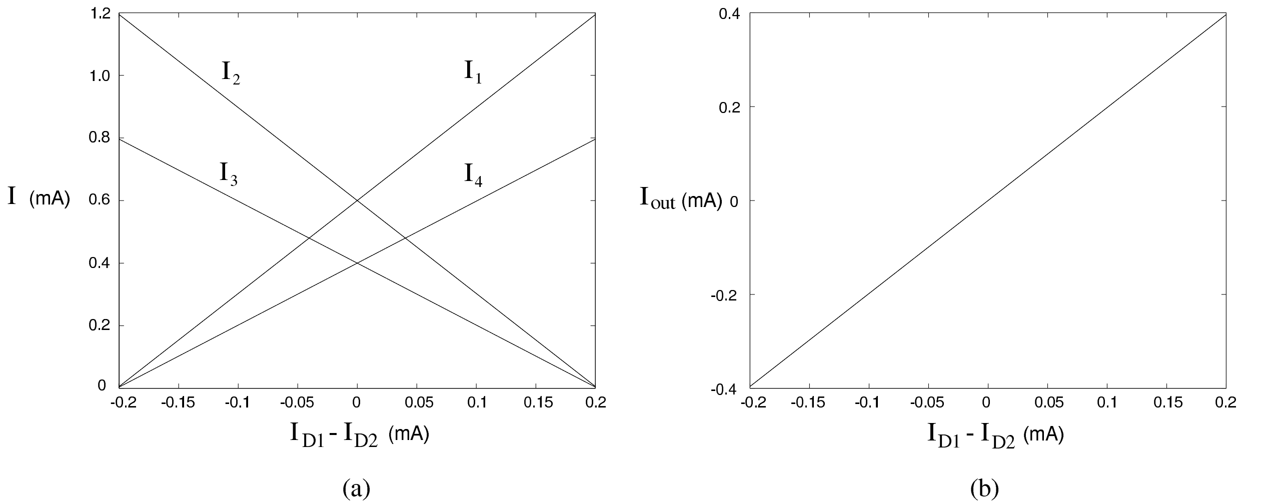


Figure 2.7: Bipolar Gilbert cell multiplier linear transfer characteristics.

Figure 2.7 shows the individual linear collector currents as well as the linear differential output current, I_{out}. Slightly different than the current-mode amplifier,

where the maximum output current is the whole range of I_T, the maximum multiplier output, I_{out}, is the maximum difference between tail currents, $I_{T1} - I_{T2}$. If Equation (2.23) is re-written as

$$I_{out} = \alpha(I_{T1} - I_{T2})\frac{(I_{D2} - I_{D1})}{(I_{D1} + I_{D2})}, \tag{2.24}$$

and for fully differential inputs,

$$\left[\frac{I_{D2} - I_{D1}}{I_{D1} + I_{D2}}\right]_{max} = 1, \tag{2.25}$$

combining equations (2.24) and (2.25) results in

$$[I_{out}]_{max} = \alpha[I_{T1} - I_{T2}]_{max}. \tag{2.26}$$

Regardless of input range used, the entire differential range of the tail current is utilized, maximizing input range. This ideal first order behavior neglects some higher order effects such as ohmic emitter resistance, finite beta, and device mismatch, which introduce some nonlinear effects. However, steps can be taken to minimize these effects [1][2].

Chapter 3

The CMOS Gilbert Cell Multiplier in Strong Inversion

3.1 Introduction

The basic function of a CMOS Gilbert cell is the same as its bipolar equivalent. However, creating a linear CMOS multiplier is not nearly as straight forward due to the difference in bipolar and CMOS technologies. The fundamental I-V characteristic for a BJT is modeled by an exponential function. The fundamental I-V characteristic for a MOSFET is modeled by the square law. As will be shown in the following sections, this difference creates a significant challenge to linearizing the CMOS Gilbert cell. Simply adding a diode connected device to the gate terminals will not result in a linear Gilbert cell multiplier.

In the following sections, the CMOS Gilbert cell will be evaluated in the same manner as was done in Chapter 2, where the single differential pair is evaluated first, then the current-mode amplifier is presented, and finally the whole Gilbert cell is addressed. First order analysis will be used initially, then higher order effects of strong inversion will be considered.

3.2 CMOS Differential Pair

For a single MOSFET operating in the active region, the first order I-V characteristic behaves according to the square-law relationship

$$\mathrm{I_d} = \frac{\mu \mathrm{C_{OX}}}{2}\frac{\mathrm{W}}{\mathrm{L}}(\mathrm{V_{gs}} - \mathrm{V_t})^2, \tag{3.1}$$

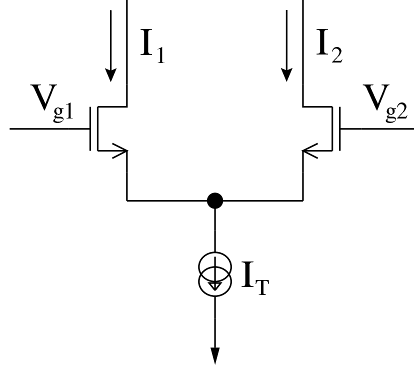


Figure 3.1: CMOS differential pair.

where I_d is the drain current, μ is the mobility constant, C_{OX} is the oxide capacitance, W is the device channel width, L is the channel length, V_t is the threshold voltage, and V_{gs} is the gate to source voltage.

For a MOSFET differential pair, as shown in Figure 3.1, the devices share the tail current according to

$$I_1 + I_2 = I_T. \tag{3.2}$$

Combining equations (3.1) and (3.2), drain currents become

$$I_1 = \frac{I_T}{2} + \sqrt{2KI_T}\left(\frac{V_d}{2}\right)\sqrt{1 - \frac{(V_d/2)^2}{(I_T/2K)}}, \tag{3.3}$$

$$I_2 = \frac{I_T}{2} - \sqrt{2KI_T}\left(\frac{V_d}{2}\right)\sqrt{1 - \frac{(V_d/2)^2}{(I_T/2K)}}, \tag{3.4}$$

where $K = \frac{\mu C_{ox}}{2}\frac{W}{L}$ and $V_d = V_{g1} - V_{g2}$, and V_{g1} and V_{g2} swing differentially [3]. This can also be written as

$$I_1 = \frac{I_T}{2} + \frac{V_d}{2}\sqrt{K(2I_T - KV_d^2)}, \tag{3.5}$$

$$I_2 = \frac{I_T}{2} - \frac{V_d}{2}\sqrt{K(2I_T - KV_d^2)}. \tag{3.6}$$

It can be seen from equations (3.5) and (3.6) that each drain current is centered around $\frac{I_T}{2}$. Within a range, as V_d increases, each drain current ramps up or down from $\frac{I_T}{2}$. Figure 3.2(a) is a plot of equations (3.5) and (3.6).

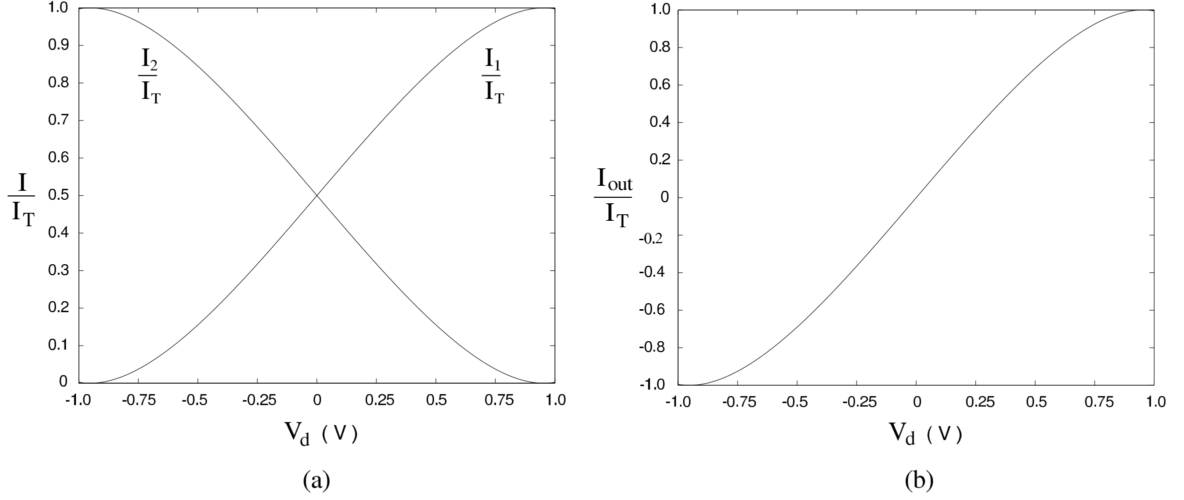


Figure 3.2: CMOS differential pair transfer characteristics.

The differential output current, $I_1 - I_2$, is

$$I_{out} = V_d\sqrt{K(2I_T - KV_d^2)}. \tag{3.7}$$

This results in the nonlinear differential output current shown in Figure 3.2(b). When $KV_d^2 << 2I_T$, the KV_d^2 term under the square root can be neglected and the drain currents ramp linearly. This is the region where small signal gain is achieved in traditional closed-loop amplifiers using differential pair inputs. As V_d gets larger, the KV_d^2 term becomes significant and the drain currents round off. Thus, the differential output current of the differential pair can be considered linear only over a small input range of a few tenths of a volt [4].

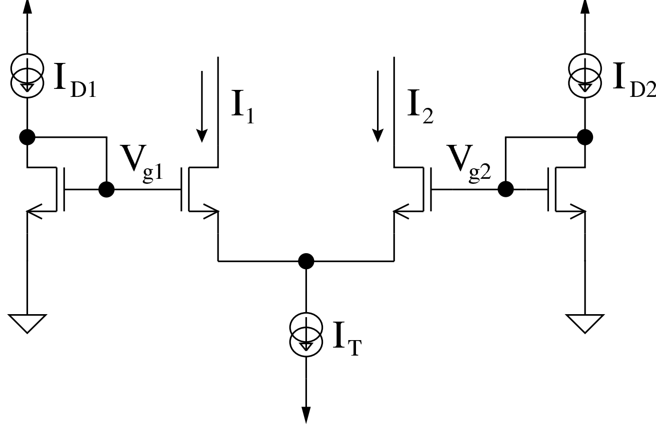


Figure 3.3: CMOS current-mode amplifier.

3.3 CMOS Current-mode Amplifier

If a diode-connected device is added to each gate of the differential pair, as shown in Figure 3.3, a highly linear current-mode amplifier can be created. Linearity can be achieved across the full differential input range. The gate voltages are controlled by the currents forced across the diode connected devices according to

$$V_{gs} = \sqrt{\frac{I_D}{K}} + V_t. \tag{3.8}$$

Comparing to the single differential pair, the differential input voltage, V_d, now becomes

$$V_d = \sqrt{\frac{I_{D1}}{K}} - \sqrt{\frac{I_{D2}}{K}}. \tag{3.9}$$

Adding the diodes and current sources creates a new equation for I_{out},

$$I_{out} = \left(\sqrt{\frac{I_{D1}}{K}} - \sqrt{\frac{I_{D2}}{K}}\right)\sqrt{K\left(2I_T - K\left(\sqrt{\frac{I_{D1}}{K}} - \sqrt{\frac{I_{D2}}{K}}\right)^2\right)}. \tag{3.10}$$

This equation can be reduced to show how the linear input range can be increased. Squaring both sides to remove the radical, and combining terms results in

$$I_{out}^2 = 2KI_T\left(\sqrt{\frac{I_{D1}}{K}} - \sqrt{\frac{I_{D2}}{K}}\right)^2 - K^2\left(\sqrt{\frac{I_{D1}}{K}} - \sqrt{\frac{I_{D2}}{K}}\right)^4. \tag{3.11}$$

If K matches between the diode-connected and differential pair devices, K can be removed to simplify to

$$I_{out}^2 = 2I_T\left(\sqrt{I_{D1}} - \sqrt{I_{D2}}\right)^2 - \left(\sqrt{I_{D1}} - \sqrt{I_{D2}}\right)^4. \tag{3.12}$$

Expanding terms, the second and fourth order terms on the right hand side of Equation (3.12) become

$$\left(\sqrt{I_{D1}} - \sqrt{I_{D2}}\right)^2 = I_{D1} - 2\sqrt{I_{D1}I_{D2}} + I_{D2}, \tag{3.13}$$

$$\left(\sqrt{I_{D1}} - \sqrt{I_{D2}}\right)^4 = I_{D1}^2 + I_{D2}^2 + 6I_{D1}I_{D2} - 4I_{D1}\sqrt{I_{D1}I_{D2}} - 4I_{D2}\sqrt{I_{D1}I_{D2}}. \tag{3.14}$$

To reduce to linear form, Equation (3.12) should take the form $I_{out}^2 = (\text{linear terms})^2$. This requires that the linear input range $I_{D1} + I_{D2}$ be equal to I_T. Substituting $I_{D1} + I_{D2}$ for I_T, and expanding equations (3.12), (3.13), and (3.14), the square root terms drop out resulting in

$$I_{out}^2 = I_{D1}^2 - 2I_{D1}I_{D2} + I_{D2}^2 = \left(I_{D1} - I_{D2}\right)^2. \tag{3.15}$$

Taking the square root of both sides

$$I_{out} = \pm(I_{D1} - I_{D2}). \tag{3.16}$$

Equation (3.16) shows the linear relationship between the differential input currents, I_{D1} and I_{D2}, and the differential output current, I_{out}. A plot of this linear characteristic is shown in Figure 3.4. It should be noted that this linear relationship occurs only when the input currents I_{D1} and I_{D2} are fully differential, and while $I_{D1} + I_{D2} = I_T$.

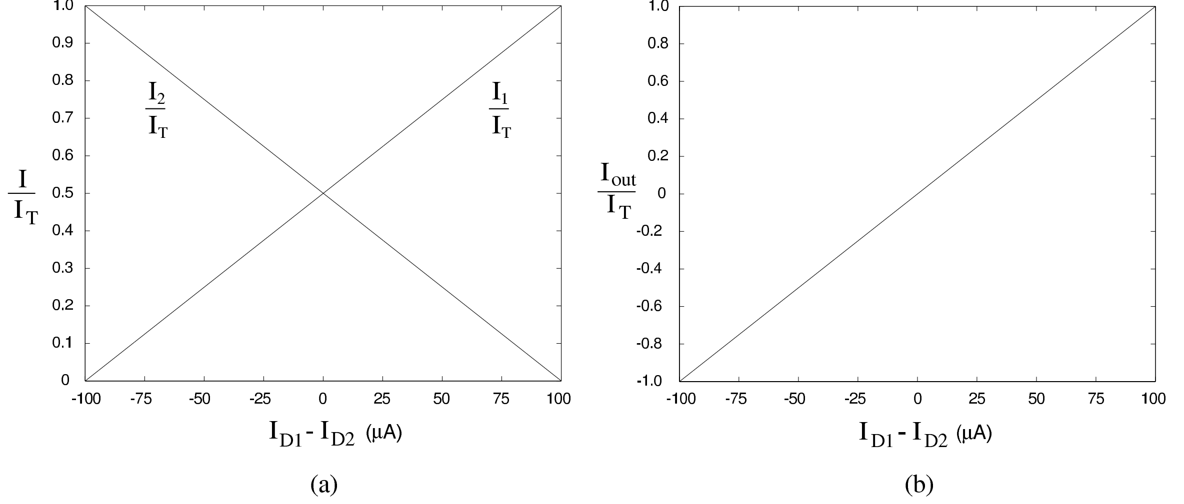


Figure 3.4: CMOS current-mode amplifier, linear transfer characteristics.

3.4 CMOS Gilbert Cell Multiplier

Combining two CMOS current-mode amplifiers, as shown in Figure 3.5, creates the CMOS Gilbert cell multiplier. Defining the CMOS multiplier drain currents

$$I_1 = \frac{I_{T1}}{2} + \frac{V_d}{2}\sqrt{K(2I_{T1} - KV_d^2)}, \tag{3.17}$$

$$I_2 = \frac{I_{T1}}{2} - \frac{V_d}{2}\sqrt{K(2I_{T1} - KV_d^2)}, \tag{3.18}$$

$$I_3 = \frac{I_{T2}}{2} - \frac{V_d}{2}\sqrt{K(2I_{T2} - KV_d^2)}, \tag{3.19}$$

$$I_4 = \frac{I_{T2}}{2} + \frac{V_d}{2}\sqrt{K(2I_{T2} - KV_d^2)}, \tag{3.20}$$

where all transistors are the same size (same K) and $V_d = V_{D1} - V_{D2}$. Currents sum at the outputs according to $I_{O1} = I_1 + I_3$ and $I_{O2} = I_2 + I_4$. The differential output

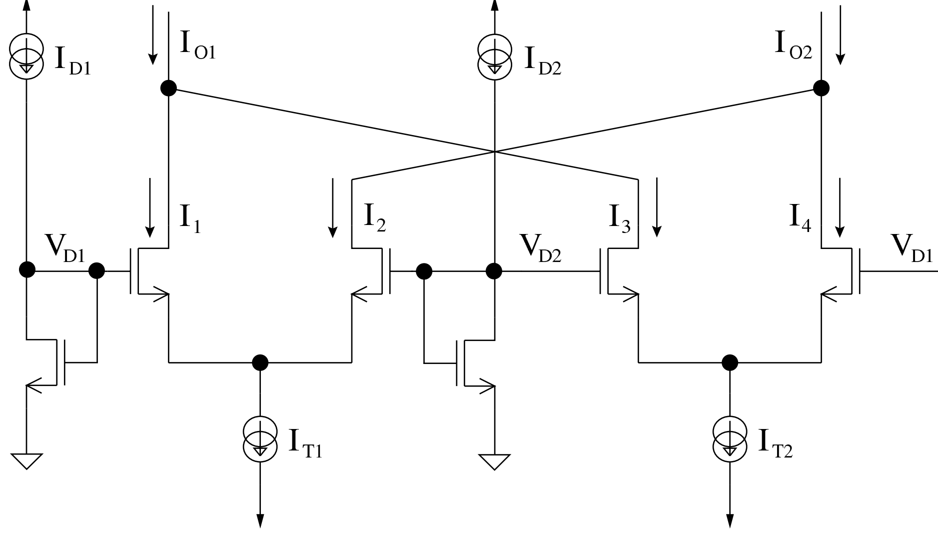


Figure 3.5: CMOS Gilbert cell multiplier.

current is $I_{out} = I_{O1} - I_{O2}$. Combining (3.17) through (3.20) and simplifying, the $\frac{I_{T1}}{2}$ and $\frac{I_{T2}}{2}$ terms cancel leaving

$$I_{out} = V_d\left(\sqrt{K(2I_{T1} - KV_d^2)} - \sqrt{K(2I_{T2} - KV_d^2)}\right). \tag{3.21}$$

Adding the equation for V_d (3.9) to Equation (3.21), results in a complex algebraic expression for I_{out},

$$I_{out} = \left(\sqrt{\frac{I_{D1}}{K}} - \sqrt{\frac{I_{D2}}{K}}\right) \times \left[\sqrt{K\left(2I_{T1} - K\left(\sqrt{\frac{I_{D1}}{K}} - \sqrt{\frac{I_{D2}}{K}}\right)^2\right)} - \sqrt{K\left(2I_{T2} - K\left(\sqrt{\frac{I_{D1}}{K}} - \sqrt{\frac{I_{D2}}{K}}\right)^2\right)}\right]. \tag{3.22}$$

Breaking down this equation mathematically would be very difficult. However, linearity can be evaluated by examining the behavior of the CMOS current-mode amplifier. Section 3.3 showed how to create a linear transfer characteristic across the full differential input range of the amplifier. This is only possible if the criteria $I_{D1} + I_{D2} = I_T$ is met. The Gilbert cell configuration is basically just two current-mode amplifiers combined such that they share their diode connected devices. Now that the amplifiers

share their diode connected devices, the criteria $I_{D1} + I_{D2} = I_T$ cannot be met. The multiplier configuration requires $I_{T1} \neq I_{T2}$ to form the tail differential input. Therefore, at least one set of drain currents will be nonlinear. This is shown in Figure 3.6, where one differential pair has linear drain current characteristics, and the other has nonlinear characteristics.

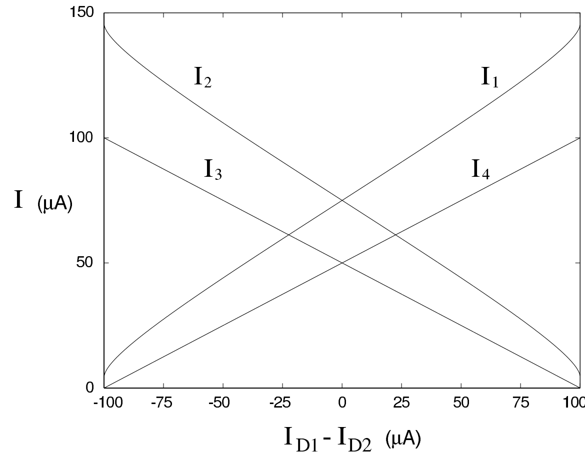


Figure 3.6: Linear and nonlinear drain current characteristics.

Summation and subtraction of the device currents shown in Figure 3.6 results in the differential output current characteristic shown in Figure 3.7. This result is true for all combinations of $I_{D1} + I_{D2}$ vs. I_{T1} and I_{T2}. Since the signal content is fully differential, even small nonlinearities in the drain current characteristics create significant nonlinearities in the differential output current, I_{out}.

In summary, the CMOS Gilbert cell multiplier linearity is dependent on the criterion, $I_{D1} + I_{D2} = I_T$. Since this criterion cannot be met, the CMOS multiplier architecture by itself is nonlinear.

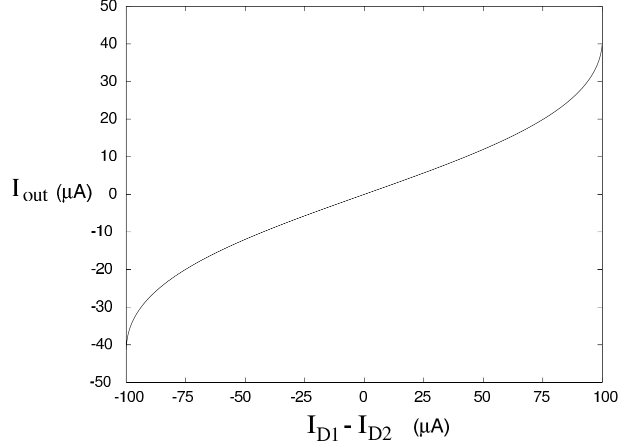


Figure 3.7: CMOS Gilbert cell multiplier transfer characteristic.

3.5 Higher Order Effects

The conclusions drawn in Section 3.4 are based on first order analysis. Final conclusions cannot be made until higher order effects in strong inversion are addressed. Short channel effects and channel length modulation should be considered.

As gate length decreases, short channel effects change the first order MOSFET I-V characteristic. This is due to the effects of velocity saturation [13] [14]. If this effect is added to the first order drain current equation, the MOSFET drain current equation can be re-written as

$$I_d = \frac{\mu C_{OX} W}{2L\left(1 + \frac{V_{gs} - V_t}{\varepsilon_C L}\right)} (V_{gs} - V_t)^2, \tag{3.23}$$

where ε_C is the critical electric field. As ε_C gets large the additional term drops out, resulting in the first order equation for I_d. However, for short channel devices, ε_C is limited, making the new term significant. The result is an I-V relationship where

$$I_d = \frac{\mu C_{OX}}{2} \frac{W}{L} (V_{gs} - V_t)^x. \tag{3.24}$$

Here x is larger than one and smaller than two. The final result is a less aggressive slope for the characteristic relative to a purely square law device, as V_{gs} increases. This effect actually improves linearity in the multiplier configuration, reducing the curvature of Figure 3.7.

As the drain to source voltage, V_{ds}, increases, channel length modulation becomes significant and the first order Equation (3.1) changes to

$$I_d = \frac{\mu C_{OX}}{2} \frac{W}{L} (V_{gs} - V_t)^2 (1 + \lambda V_{ds}), \tag{3.25}$$

where λ is a process parameter. Different than short channel effects, the additional term added for channel length modulation creates a more aggressive slope on the I-V characteristic, as V_{ds} now becomes significant. This translates into degraded linearity in the multiplier as the curvature of Figure 3.7 increases. Although moderate in its effects due to small λ values, channel length modulation effects should be considered when evaluating multiplier linearity.

Chapter 4

The CMOS Gilbert Cell Multiplier in Subthreshold

4.1 Introduction

There is a CMOS region of operation where the I-V device characteristic is modeled similar to the bipolar model. The subthreshold region is defined as the region of device operation where V_{gs} is biased below the threshold voltage, V_t. In this region, exponential diffusion currents dominate, as drift currents have fallen off due to the reduction of channel inversion. The first order model for MOSFET diffusion current is

$$I_{ds} = I_o(\frac{W}{L})e^{V_{gs}/nV_T}, \tag{4.1}$$

where V_T is the thermal voltage defined by

$$V_T = \frac{kT}{q}. \tag{4.2}$$

Also, n is the ideality factor, and I_o is a constant that is primarily process dependent [5].

Notice that the MOSFET drain current model in subthreshold is very similar to the bipolar model of Equation (2.2). Using the same technique as in Chapter 2, and substituting Equation (4.1) for Equation (2.2), the subthreshold differential output current for the CMOS Gilbert cell configuration shown in Figure 3.5 is

$$I_{out} = (I_{T1} - I_{T2})\frac{(I_{D2} - I_{D1})}{(I_{D1} + I_{D2})}. \tag{4.3}$$

This chapter will explore the biasing and higher order effects of the subthreshold region that introduce nonlinearities into Equation (4.3). Based on these effects,

solutions to minimize multiplier output distortion will be discussed. Finally, theory from this chapter, along with the theory from Chapter 3, will provide the basis for a method describing how to build linear CMOS multipliers biased in the weak and moderate inversion regions.

4.2 Subthreshold Biasing

The multiplier output current reduces to Equation (4.3) only when the voltage-current relationship is purely exponential, such as in deep subthreshold, where primarily diffusion current is present [6]. Addition of drift currents will cause nonlinear behavior of I_{out}. Figure 4.1 [9], shows the relationship between the diffusion and drift currents within the total drain current of a MOSFET. Here the regions where the diffusion and drift currents dominate can be seen relative to V_{gs} and V_t.

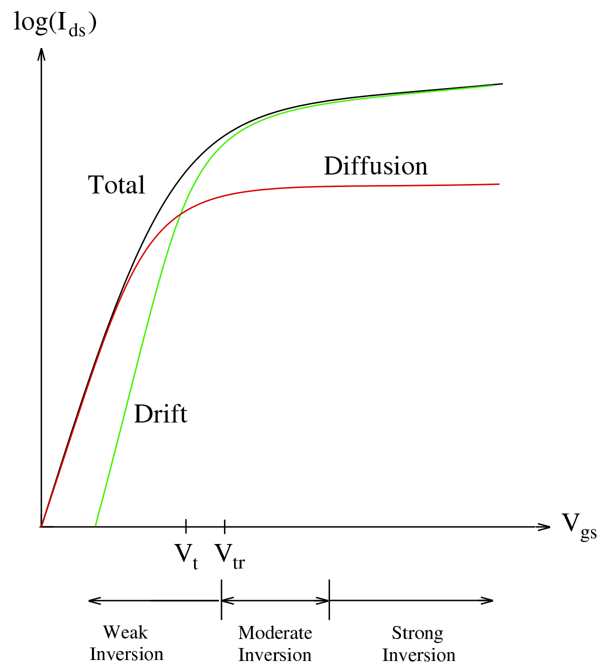


Figure 4.1: Diffusion and drift components of the total device current.

To identify the bias points where the diffusion current dominates enough to validate Equation (4.3), some relationships can be defined. Foty [6] defines a bias point where the diffusion current becomes nearly constant at

$$\mathrm{V_{tr}} = \mathrm{V_t} + 3\mathrm{V_T}, \tag{4.4}$$

where $\mathrm{V_T} = \mathrm{kT/q}$. $\mathrm{V_{tr}}$ is shown relative to $\mathrm{V_t}$ in Figure 4.1. Substituting (4.4) into the strong inversion current Equation (3.1) gives an upper limit of the diffusion current

$$\mathrm{I_{limit}} = 9\mathrm{K}\left(\mathrm{V_T}\right)^2, \tag{4.5}$$

where

$$\mathrm{K} = \frac{\mu \mathrm{C_{OX}}}{2}\left(\frac{\mathrm{W}}{\mathrm{L}}\right). \tag{4.6}$$

Since $\mathrm{I_{limit}}$ is defined as the maximum diffusion current [6], $\mathrm{I_{limit}}$ can then be used to estimate the weak inversion current, which is a combination of diffusion and drift currents, neither of these currents dominating in this region. The weak inversion drain current, $\mathrm{I_{weak}}$, can be estimated empirically by [6]

$$\mathrm{I_{weak}} = \frac{\mathrm{I_{exp}}\mathrm{I_{limit}}}{\mathrm{I_{exp}} + \mathrm{I_{limit}}}, \tag{4.7}$$

where $\mathrm{I_{exp}}$ is the exponential diffusion current. In deep subthreshold, $\mathrm{I_{exp}} << \mathrm{I_{limit}}$, and Equation (4.7) reduces to $\mathrm{I_{weak}} = \mathrm{I_{exp}}$. Now, using Equation (4.7), maximum $\mathrm{I_{exp}}$ for a given device size can be estimated. If 1 % is chosen as the maximum deviation of $\mathrm{I_{weak}}$ from $\mathrm{I_{exp}}$ before $\mathrm{I_{weak}}$ becomes nonexponential, then maximum $\mathrm{I_{exp}}$ can be

Table 4.1: Subthreshold current range

W/L	$\mathrm{I_{limit}}$	$[\mathrm{I_{exp}}]_{\mathrm{max}}$
0.1	47.7nA	0.482nA
1	477nA	4.82nA
10	4.77uA	48.2nA
100	47.7uA	482nA
1000	477uA	4.82uA

derived by setting $I_{weak} = (1.01)I_{exp}$, and solving for I_{exp} at any given device size (W/L) and using the associated I_{limit} value.

Table 4.1 shows I_{limit} and $[I_{exp}]_{max}$ values for a typical range of device sizes. Parameters from an AMIS 0.35-μm process are used and V_T is assumed to be 26 mV at room temperature.

Here it can be seen that for most W/L ratios, I_{exp} can be assumed to be less than 1 μA. So for most ranges of device sizes, Equation (4.3) is only valid (multiplying exponential currents only), for device currents less than 1 μA.

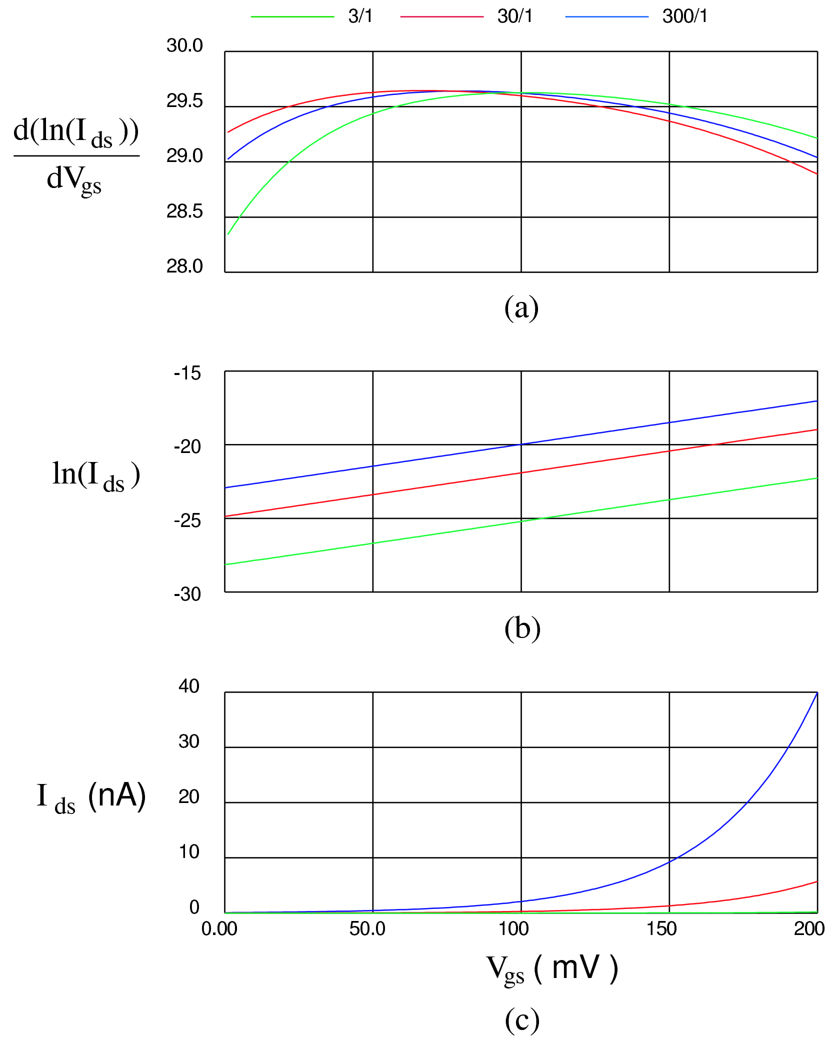


Figure 4.2: I_{exp} range.

Simulation of an NMOS device shows even tighter constraints on the range of exponential current. If the logarithm of Equation (4.1) is taken, then

$$\ln(I_{ds}) = \ln\left(I_o \frac{W}{L}\right) + \frac{1}{nV_T} \cdot V_{gs}. \tag{4.8}$$

This results in a linear relationship between $\ln(I_{ds})$ and V_{gs}. The other parameters are constants, only causing offset and scaling of the linear curve.

Figure 4.2 shows the I_{exp} range for typical values of W/L. Figure 4.2(c) is plot of the drain current of an NMOS device as V_{gs} is swept. Figure 4.2(b) is a plot of the log of I_{ds}. Here the linear relationship between $\ln(I_{ds})$ and V_{gs} over a range of V_{gs} can be seen. Deviations from the linear relationship shown in Figure 4.2(b) represent contributions of nonexponential currents (i.e. drift currents). In 4.2(a), the derivative of $\ln(I_{ds})$ is taken to see the linear range of the slope of $\ln(I_{ds})$. For $V_{gs} < 200$ mV, the percent change in the slope of $\ln(I_{ds})$ is less than five percent. This corresponds to $[I_{ds}]_{max}$ of about 40 nA at W/L = 300/1.

The simulated values of maximum exponential drain current are compared to I_{limit} and the empirical values of I_{exp} in Table 4.2. From simulation results, for a gate length of 1 μm, and typical device widths, it can be concluded that to have an exponential current to within five percent, an operating range of $V_{gs} < 0.2$ V and $I_{ds} < 40$ nA should be used. This will allow the math of Equation (4.3) to be valid. Decreasing the gate length allows for a larger exponential drain current. However, for the given process, exponential currents are not expected to exceed 1 μA.

Table 4.2: Empirical versus simulated exponential current range.

W/L	I_{limit}	Empirical I_{exp}	Simulated I_{exp}
1	477nA	4.82nA	0.2nA
10	4.77uA	48.2nA	8nA
100	47.7uA	482nA	40nA

4.3 The Inversion Coefficient

A useful way to identify the operating region of a MOSFET is to quantify the inversion level of the transistor. The inversion coefficient (IC) is a parameter that can measure the inversion level. The inversion coefficient is defined by [15]

$$\mathrm{IC} = \frac{\mathrm{I_{ds}}}{2\mathrm{n}\mu_0\mathrm{C_{OX}}(\mathrm{W/L})\mathrm{V_T}^2} = \frac{\mathrm{I_{ds}}}{\mathrm{I_0}(\mathrm{W/L})}, \tag{4.9}$$

where $\mathrm{I_{ds}}$ is the device drain current, n is the ideality factor, μ_0 is the low field mobility, $\mathrm{C_{OX}}$ is the gate oxide capacitance, $\mathrm{V_T}$ is the thermal voltage (kT/q), and W and L are the device width and length, respectively. $\mathrm{I_0}$ is a process dependent current equal to $2\mathrm{n}\mu_0\mathrm{C_{ox}}\mathrm{V_T}^2$.

The device inversion is classified into three inversion regions - weak, moderate, and strong inversion. Table 4.3 shows each region relative to the inversion coefficient. The inversion coefficient is less than 0.1 for weak inversion, greater than 10 for strong inversion, and in between 0.1 and 10 for moderate inversion. The inversion coefficient will be used later to classify the operating regions of various multiplier circuits.

Table 4.3: Inversion regions versus inversion coefficient (IC).

Weak	Moderate	Strong
$\mathrm{IC} < 0.1$	$0.1 < \mathrm{IC} < 10$	$\mathrm{IC} > 10$

4.4 Higher Order Effects

Some higher order effects must be considered when biasing devices in weak inversion. One way to understand higher order effects in subthreshold is to examine process modeling. BSIM models are widely used to model CMOS processes. The BSIM3v3 model is the latest widely used revision of BSIM models. In the following sections, various levels of BSIM models will be used to explain higher order effects in the subthreshold region. Data for all parameters is taken from an AMIS 0.35-μm process.

4.4.1 V_{ds} Term

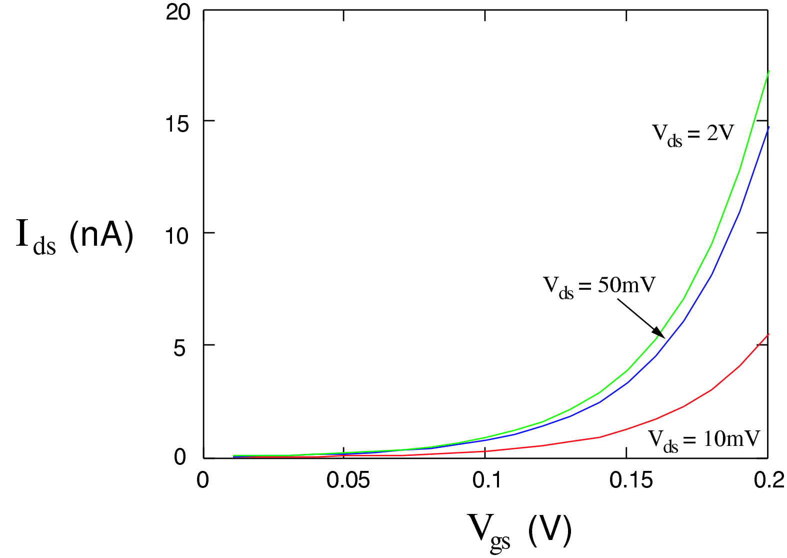


Figure 4.3: V_{ds} term effect on I_{ds}.

Using the BSIM model, the subthreshold drain current can be defined as [6]:

$$I_{ds} = I_0 e^{\frac{V_{gs}-V_t}{nV_T}} \left(1 - e^{\frac{-V_{ds}}{V_T}}\right), \tag{4.10}$$

where

$$I_0 = \frac{\mu_v C_{ox} W_{eff}}{L_{eff}} \cdot {V_T}^2 \cdot e^{1.8}. \tag{4.11}$$

An additional term with respect to V_{ds} has been added to the first order model of Equation (4.1), as well as reference to the threshold voltage, V_t (the addition of V_t will be discussed later). The V_{ds} term becomes significant at small values of V_{ds}. If one percent variation on I_{ds} is defined as significant, then the point where $e^{-V_{ds}/V_T} = 0.01$ should be defined. Solving for V_{ds} at ambient temperature, the term becomes significant at $V_{ds} = 120$ mV. Therefore, for $V_{ds} > 120$ mV, the $1 - e^{-V_{ds}/V_T}$ term will change I_{ds} by less than 1 %. For $V_{ds} < 120$ mV, the device moves out of saturation, causing I_{ds} to drop off by greater than 1 %.

Figure 4.3 plots Equation (4.10) at $V_{gs} << V_t$ for various V_{ds} values. It can be seen that I_{ds} drops off only after V_{ds} gets very small.

4.4.2 Ideality Factor

Another important term in Equation (4.10) is the ideality factor, n. The ideality factor models how "ideally" a MOSFET drain current matches the voltage-to-current characteristic of the ideal Shockley diode equation [6],

$$I = I_O e^{\frac{V_d}{V_T}}. \tag{4.12}$$

Here I_O is a constant and V_d is the voltage across the diode. When $n = 1$, the exponent of Equation (4.10) closely matches the Shockley diode expression. n is also sometimes called the slope factor.

The "nonidealities" that n models are caused by the difference between a MOSFET conduction channel and the simple pn junction that is modeled by the Shockley diode equation. To model n, small signal capacitances under the MOS gate are examined.

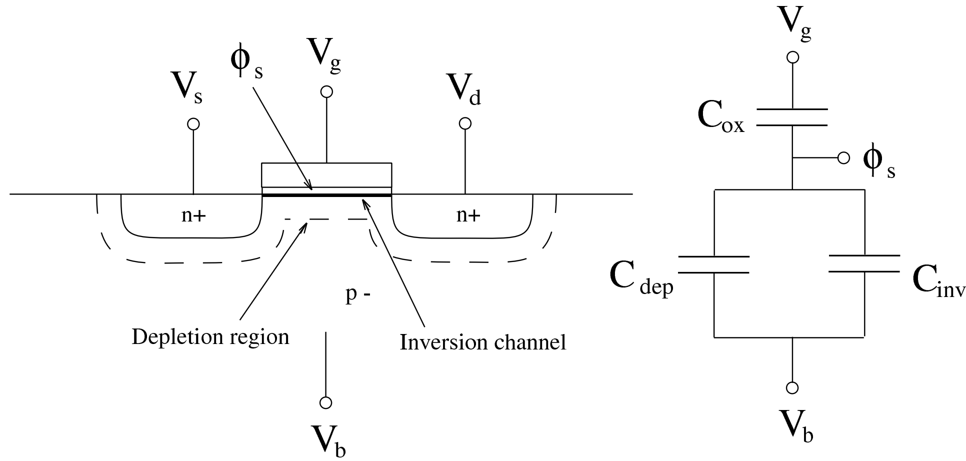


Figure 4.4: Capacitive divider.

Figure 4.4 shows an NMOS cross-section and the associated capacitive divider between the oxide capacitance, and the parallel depletion and inversion capacitances.

Here ϕ_s is the surface potential between the oxide and the silicon. The inverse of the total capacitance, C_{gb}, is defined as

$$\frac{1}{C_{gb}} = \frac{1}{C_{ox}} + \frac{1}{C_{depl} + C_{inv}}. \tag{4.13}$$

In Figure 4.4, the gate voltage, V_g, acts as the mechanism to create "charge injection" for the diffusion currents, somewhat similar to a bipolar device. Therefore, it is important to model the gate coupling. n can be defined by evaluating the total gate coupling capacitance, C_{gb}, versus C_{ox}, C_{dep}, and C_{inv} [7]. Contributions of each MOS coupling capacitance to the total coupling capacitance are shown in Figure 4.5.

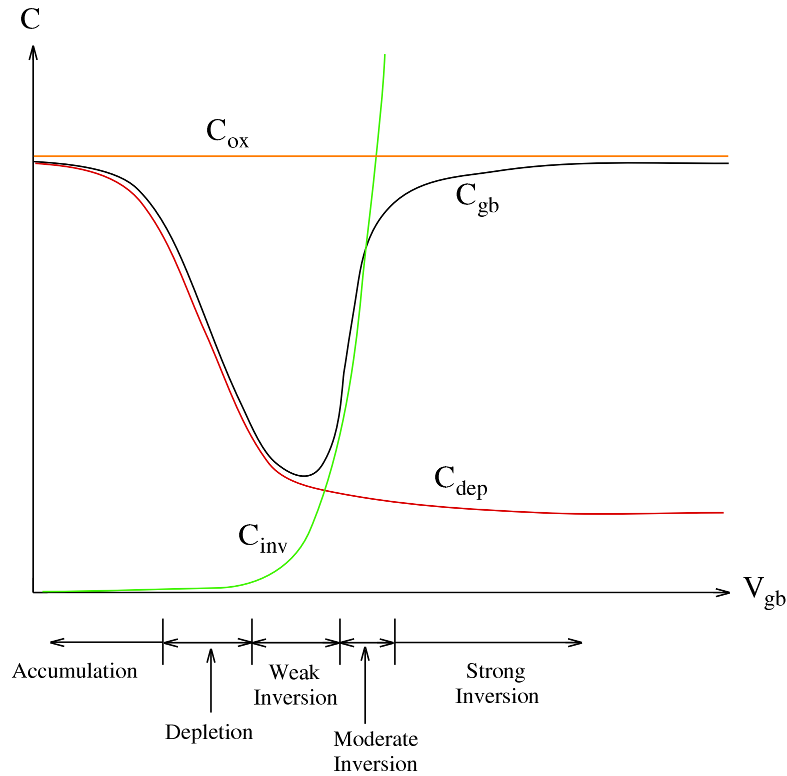


Figure 4.5: MOSFET coupling capacitances.

Decreasing V_g toward the depletion and accumulation modes, the physical depletion region decreases in width, and positive charge accumulates under the gate,

causing an effective bottom plate to C_{gb}. This effect causes C_{dep} to become large, resulting in $C_{gb} \rightarrow C_{ox}$. Increasing V_g toward moderate and strong inversion, C_{inv} increases as an inversion channel of negative charge builds up under the gate. This inversion charge shields the depletion region, preventing any further widening of the depletion region. The inversion channel also creates an effective bottom plate of C_{gb}. As C_{inv} becomes large, $C_{gb} \rightarrow C_{ox}$. In weak inversion, C_{dep} and C_{inv} are comparable in size, causing the capacitive divider to reduce C_{gb} below C_{ox}.

The ideality factor tracks this gate coupling behavior, and is thus also referred to as the "gate coupling coefficient" [8]. A first order approximation of n is [6]

$$n = 1 + \frac{C_{depl}}{C_{inv}}. \tag{4.14}$$

Referring to Figure 4.5, as the device moves toward depletion mode, C_{dep} increases, while C_{inv} decreases, causing n to increase. Moving toward moderate inversion, as charge builds up in the inversion channel, C_{inv} increases, while C_{dep} effectively decreases due to inversion channel shielding, causing n to decrease. Thus, n models how strongly the charge on the gate couples to the charge in the channel.

Typical values of n range from 1.2 to 1.6 in modern processing [8]. Even though the ideality factor is mostly determined by processing, there are some design parameters that cause moderate variations in n. BSIM3 defines n as [6]

$$\begin{aligned} n = 1 + \mathrm{NFACTOR} \cdot \frac{C_{dep}}{C_{ox}} + \frac{1}{C_{ox}} \cdot (\mathrm{CDSC} + \mathrm{CDSCB} \cdot V_{bsx} + \mathrm{CDSCD} \cdot V_{ds}) \\ \times \left[e^{-\frac{\mathrm{DVT1} \cdot L_{eff}}{2 \cdot L_t}} + 2 \cdot e^{-\frac{\mathrm{DVT1} \cdot L_{eff}}{L_t}} \right] + \frac{C_{it}}{C_{ox}}, \end{aligned} \tag{4.15}$$

where

$$C_{dep} = \frac{\epsilon_{Si}}{x_d}, \tag{4.16}$$

$$x_d = \left(\frac{2\epsilon_{Si} (\phi_S - V_{bsx})}{q \cdot \mathrm{NCH}} \right)^{\frac{1}{2}}, \tag{4.17}$$

and

$$L_t = \left(\frac{\epsilon_{Si} \cdot x_d}{C_{ox}} \right)^{\frac{1}{2}} \cdot (1 + \mathrm{DVT2} \cdot V_{bsx}). \tag{4.18}$$

In these equations, V_{bsx} is an auxiliary substrate bias expression which tracks V_{bs} almost exactly except at large values of V_{bs}. V_{bs}, V_{ds}, and L_{eff} are the design parameters that can be used to modify n. The remaining parameters are process dependent or physical constants.

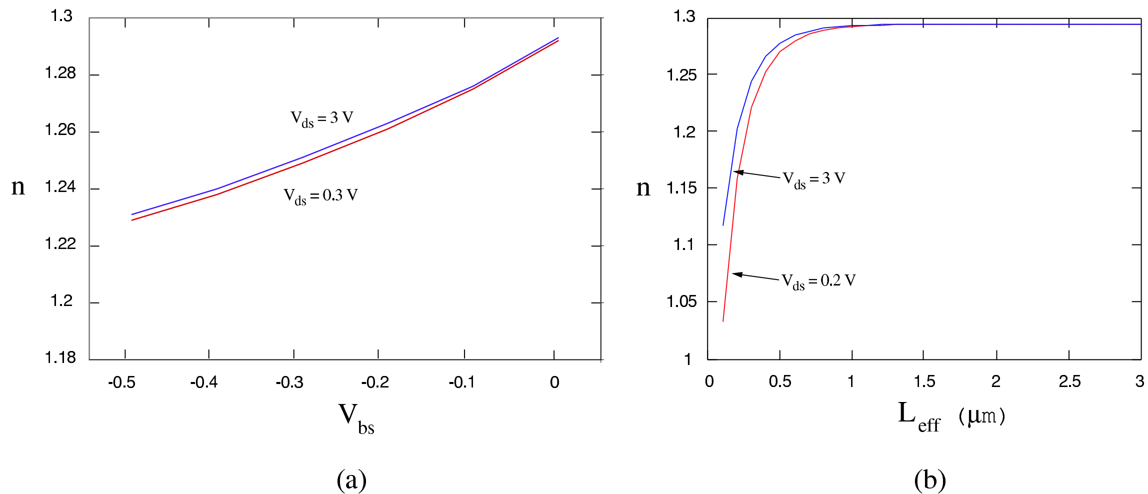


Figure 4.6: Ideality factor, n, versus V_{bs}, V_{ds}, and L_{eff}.

Figure 4.6 plots n versus V_{bs}, V_{ds}, and L_{eff}. As shown, increasing the body effect slightly decreases the ideality factor. Also, increasing V_{ds} increases n, but is almost negligible for most ranges of V_{ds}. Figure 4.6 also shows that short channel effects cause n to drop off below $L_{eff} = 1\mu m$. Above this value, n is basically constant. Consistent with short channel theory, at small gate lengths, n becomes sensitive to V_{ds}. Increasing V_{ds} proportionally increases n in short channel devices.

To evaluate the effects of n on I_{ds} in weak inversion, BSIM Equation (4.10) is used again. This model is similar to the BSIM2 model, and much easier to evaluate than the BSIM3 model, which uses extensive empirical data to model I_{ds}. The addition of V_t to the BSIM model creates a different relationship between n and I_{ds} at V_{gs}, above and below V_t.

Figure 4.7 plots I_{ds} at V_{gs} around V_t, for $n = 1.2$ and 1.3. It can be seen that for $V_{gs} > V_t$, n is inversely proportional to I_{ds}. Increasing n, decreases I_{ds}. For

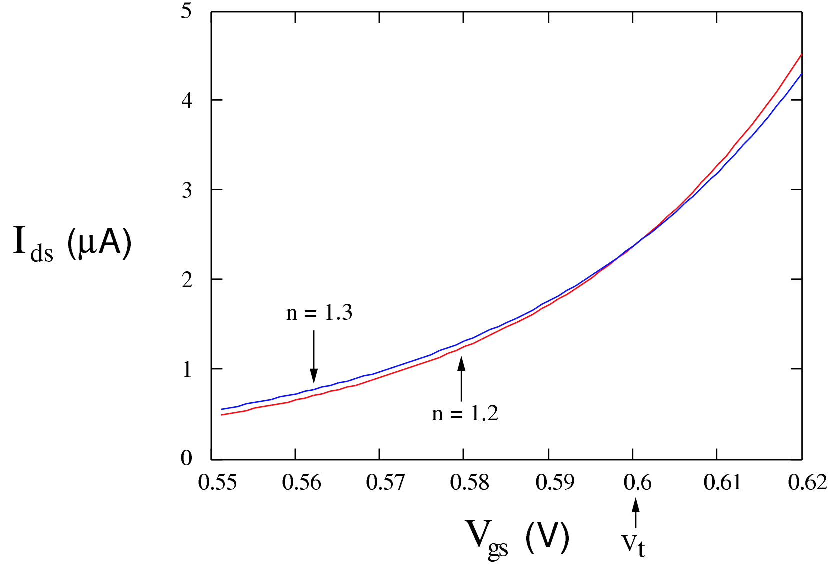


Figure 4.7: n versus I_{ds} around $V_{gs} = V_t$.

$V_{gs} < V_t$, n and I_{ds} become directly proportional, and increasing n will increase I_{ds}. In contrast, in the basic subthreshold current Equation (4.1), n is always inversely proportional to I_{ds}.

Plotting Equation (4.10) at $V_{gs} << V_t$, the effects of n on I_{ds} can be seen. Figure 4.8 shows I_{ds} at n = 1.2, 1.3, and 1.4. Here I_{ds} increases with n. Comparing Figures 4.6 and 4.8, the effects of V_{bs} and L_{eff} relating to n can be extrapolated. These relationships are shown in Table 4.4, which defines the effects of individual changes in V_{bs} and L_{eff} on n, and consequently, on I_{ds}.

Table 4.4: $|V_{bs}|$, L_{eff}, n relationship to I_{ds}

$\|V_{bs}\|$	L_{eff}	n
inverse	direct	direct

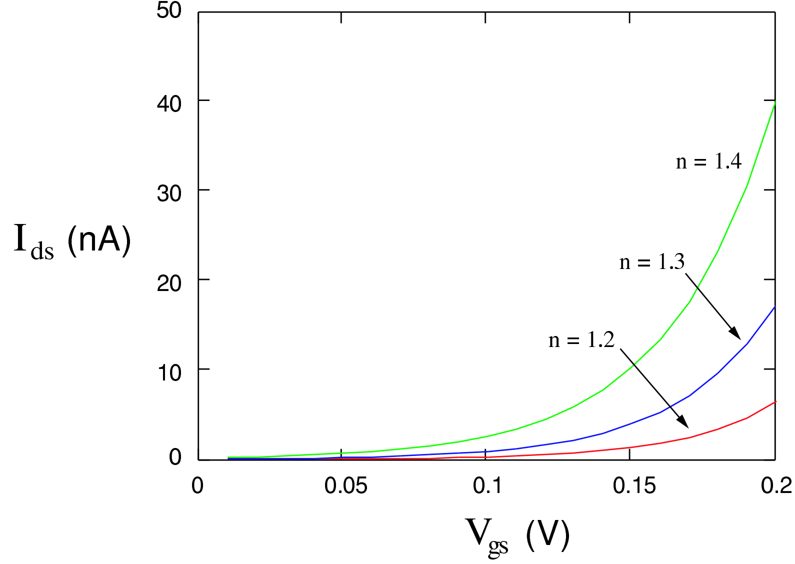


Figure 4.8: n versus I_{ds}.

4.4.3 Threshold Voltage

Understanding high order effects on the voltage threshold, V_t, will also help explain some of the behavior of subthreshold currents. BSIM3 defines the threshold voltage as [6]

$$V_t = VTH0 + K1 \cdot \left[(\phi_s - V_{bsx})^{\frac{1}{2}} - \phi_s^{\frac{1}{2}}\right] - K2 \cdot V_{bsx} + V_{LND} - V_{SCE} + V_{NCE}, \quad (4.19)$$

where V_{LND} is the lateral nonuniform doping voltage, V_{SCE} is the short channel effect voltage, and V_{NCE} is the narrow channel effect voltage. These voltages are defined as

$$V_{LND} = K1 \cdot \left[\left(1 + \frac{NLX}{L_{eff}}\right)^{\frac{1}{2}} - 1\right] \cdot \phi_s^{\frac{1}{2}}, \quad (4.20)$$

$$V_{SCE} = \Theta_t \cdot \left[2 \cdot (V_{bi} - \phi_s) + V_{ds}\right], \quad (4.21)$$

$$V_{NCE} = (K3 + K3B \cdot V_{bsx}) \cdot \frac{t_{ox}}{W_{eff} + W0} \cdot \phi_s. \quad (4.22)$$

In Equation (4.21), Θ_t is defined as

$$\Theta_t = e^{\left(-\frac{L_{eff}}{2 \cdot L_{t,SCE}}\right)} + 2 \cdot e^{\left(-\frac{L_{eff}}{L_{t,SCE}}\right)}, \quad (4.23)$$

where $L_{t,SCE}$ is a characteristic length.

Considering equations (4.19) - (4.23), V_{bs}, V_{ds}, W_{eff}, and L_{eff} are all parameters of V_t that can be modified by design. The other parameters are primarily process dependent.

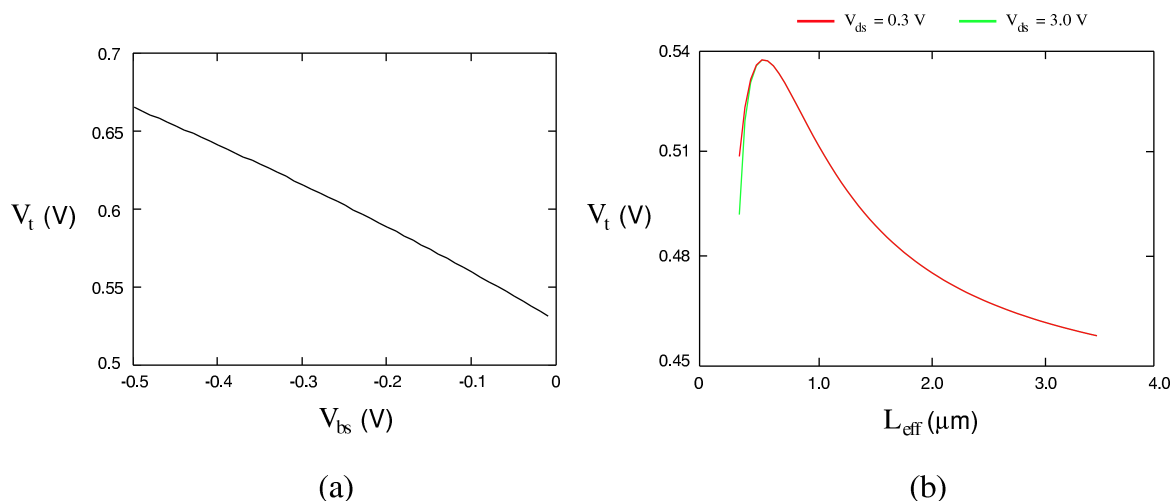


Figure 4.9: V_t, versus V_{bs} and L_{eff}.

Figure 4.9 is a plot of changes in V_t at different values of V_{bs} and L_{eff}. 4.9(a) shows that V_t increases with body effect as V_{bs} causes widening of the depletion region. Increased body effect causes the device to turn on slower as V_{gs} ramps.

Figure 4.9(b) shows V_t "roll-up" at smaller L_{eff} sizes. This is caused by reverse short channel effects (RSCE). Classic theory predicts that V_t will roll-off (decrease) as L_{eff} decreases due to short channel effects (SCE). As gate lengths have decreased to submicron lengths, "localized pileup of channel dopants near the source and drain ends" [10] of a device channel causes an increase in the threshold voltage as L_{eff} decreases. This nonuniform lateral doping causes RSCE, which overcomes SCE, even causing peaking in V_t [11]. Ideally, V_t would be constant across the full range of L_{eff}.

BSIM3 models of the AMIS 0.35-μm process show RSCE behavior for both NMOS and PMOS devices. 4.9(b) shows a plot of a simulation of an NMOS device, biased in subthreshold (V_{gs} = 0.2 V) at V_{ds} = 0.3 V and 3.0 V. V_{ds} only affects V_t at the shortest channel lengths, as can be seen in Figure 4.9. Here V_t peaks at a

maximum value around $L_{eff} = 0.6\ \mu m$. SCE then overcomes RSCE, creating a roll-off of V_t down to then minimum L_{eff}. Variations across typical values of W_{eff} causes negligible changes in V_t.

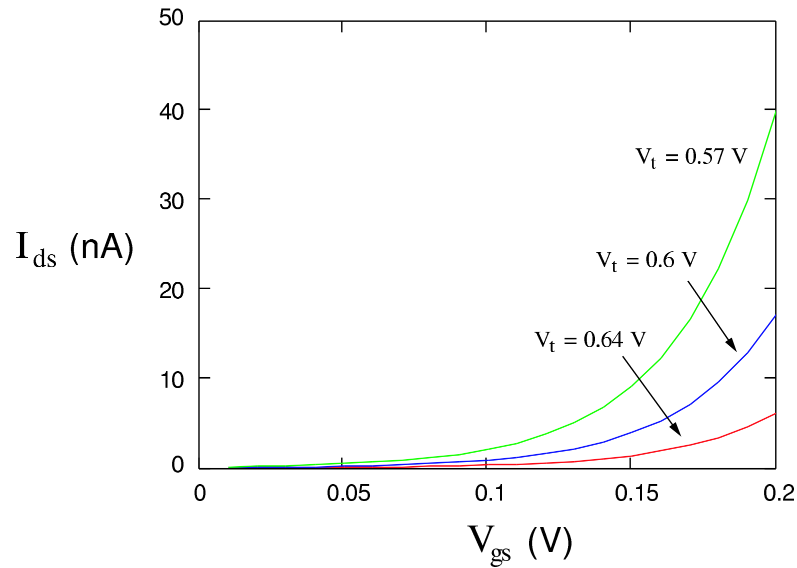


Figure 4.10: V_t versus I_{ds}.

Figure 4.10 shows the effects of variations in V_t on I_{ds} of Equation (4.10) at $V_{gs} << V_t$. Here I_{ds} is inversely proportional to V_t. As with the ideality factor, body effect and short channel effects are the main variants to V_t. Table 4.5 shows the relationship the design parameters have to I_{ds} when included as parameters to V_t. It should be noted that beyond the peak of V_t, that is caused by RSCE, a reverse relationship between L_{eff} and V_t to that shown in Table 4.5 is expected, as V_t rolls-off due to SCE.

Table 4.5: $|V_{bs}|$, L_{eff}, and V_t relationship to I_{ds}

$\|V_{bs}\|$	L_{eff}	V_t
inverse	direct	inverse

4.4.4 Ideality Factor versus Threshold Voltage

If figures 4.8 and 4.10 are compared, it can be seen that the only difference between the effects of n and V_t on I_{ds} are the scale and that they have inverse effects. Examining Equation (4.10) with $V_{gs} < V_t$ (subthreshold bias), this inverse relationship between n and V_t can also be seen.

Referring to the capacitive divider in Figure 4.4, the physical relationship between n and V_t becomes apparent. V_t is defined as the gate-source voltage, V_{gs}, where the concentration of electrons under the gate is equal to the concentration of holes in the substrate far from the gate [5]. In essence, it is the gate voltage where an inversion channel is established. This inversion channel has an associated inversion capacitance, C_{inv}. Therefore, a correlation exists between V_t and C_{inv}. Widening of the depletion region through body effect, and reverse short channel effects, change the level of C_{inv} for any given value of V_{gs}. V_t tracks with C_{inv}, just as n tracks gate coupling.

Combining tables 4.4.2 and 4.4.3, a summary of the body effect and short channel effects on n, V_t, and I_{ds} is compiled. Table 4.6 shows that variations in $|V_{bs}|$ and L_{eff} affect n and V_t inversely, when devices are biased in subthreshold. This is consistent with Equation (4.10), meaning that changes in n and V_t with respect to V_{bs} and L_{eff} reinforce each other.

Table 4.6: $|V_{bs}|$, L_{eff}, n, and V_t relationship to I_{ds}

$\|V_{bs}\|$	L_{eff}	n	V_t
inverse	direct	direct	inverse

4.5 Biasing and Higher Order Effects on the Gilbert Cell Multiplier

As was mentioned in Section 4.2, to represent the multiplier differential output current by Equation (4.3), all device currents must be exponential. To achieve this exponential current-voltage relationship, device drain currents and gate-source

voltages must be small. This section will address the effects that biasing devices in deep subthreshold range has on the Gilbert Cell multiplier architecture. Also, the impact of subthreshold higher order effects will be discussed.

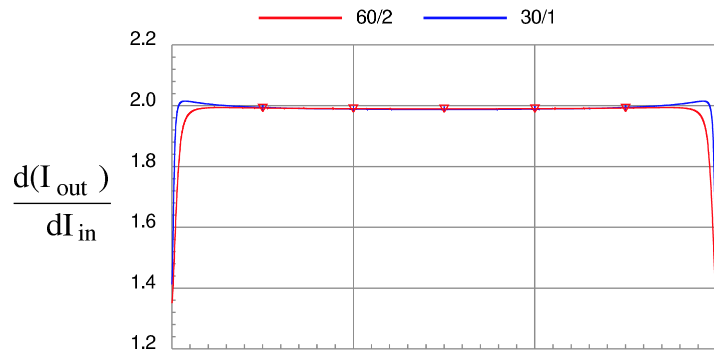
As each effect is analyzed, the slope of the multiplier transfer characteristic will be examined as a qualitative measure of linearity. Evaluating the slope provides a visual measurement of small changes in the linearity, providing an intuition of how each higher order effect changes the output characteristic. A perfectly linear transfer characteristic would have a constant slope across the whole input range.

4.5.1 The V_{ds} Term versus the Diode-connected Devices

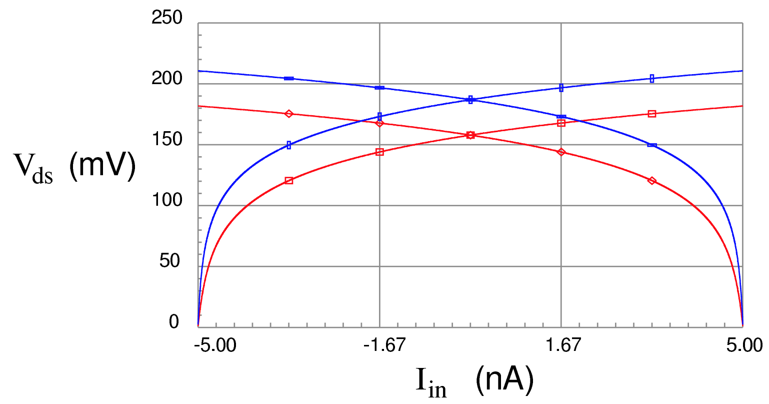
At small V_{gs} values, the diode connected devices in the multiplier become sensitive to the $\left(1 - e^{-V_{ds}/V_T}\right)$ term in Equation (4.10). Since the gate is tied to the drain, $V_{ds} = V_{gs}$. As the input current gets small, V_{ds} also gets small, causing the V_{ds} term to become significant.

Figure 4.11(b) shows a plot of V_{ds} versus the differential input current, I_{in}. This plot is from simulation of an NMOS multiplier in subthreshold. It can be seen that V_{ds}, for at least one of the diode-connected inputs, gets very small at each input current rail. The slope of the multiplier transfer characteristic is plotted in Figure 4.11(a). As V_{ds} gets small, the V_{ds} term causes the gain to drop off in the diode connected devices. This causes the slope to decrease at the rails of I_{out}. The effect on I_{out} is to round off the rails. The V_{ds} term generally does not become significant until V_{ds} is very small.

The impact of the V_{ds} term on linearity changes with the device size (W/L). This is mainly because V_t and r_{ds} change with device size. Larger devices become more sensitive as V_t and r_{ds} decrease, shifting the V_{ds} curve downward. This makes the V_{ds} term more significant for larger ranges of I_{out}. This can be seen in Figure 4.11(a).



(a)



(b)

Figure 4.11: Effects of the V_{ds} term on linearity.

4.5.2 Ideality Factor Mismatch

Considering the influence of the ideality factor, n, in the Gilbert cell multiplier architecture, it is important that n match between all devices. This allows the cancellation of n, in the final I_{out} equation. Differences in n between devices introduces terms in the final I_{out} equation that cause distortion.

The most significant distortion is caused by mismatches between the ideality factor of the diode-connected devices and the source-coupled devices. To evaluate this distortion, these n factors are annotated in the subthreshold drain current equations. For the diode- connected devices

$$I_{ds} = I_o \frac{W}{L} e^{V_{gs}/n_{diode} V_T}, \tag{4.24}$$

and for the differentially paired devices,

$$I_{ds} = I_o \frac{W}{L} e^{V_{gs}/n_{diff} V_T}. \tag{4.25}$$

The V_{ds} term is left out to simplify the math.

Solving for $I_{out} = (I_1 + I_3) - (I_2 + I_4)$, as done in Chapter 2, the n terms are retained in the differential current and voltage equations,

$$I_1 = I_2 e^{V_d/n_{diff} V_T}, \tag{4.26}$$

$$I_2 = I_1 e^{-V_d/n_{diff} V_T}, \tag{4.27}$$

$$I_3 = I_4 e^{-V_d/n_{diff} V_T}, \tag{4.28}$$

$$I_4 = I_3 e^{V_d/n_{diff} V_T}, \tag{4.29}$$

$$V_d = n_{diode} V_T \left[\ln\left(\frac{I_{D1}}{K_{diode}}\right) - \ln\left(\frac{I_{D2}}{K_{diode}}\right) \right]. \tag{4.30}$$

Applying $I_{T1} = I_1 + I_2$ and $I_{T2} = I_3 + I_4$ to equations (4.26) - (4.29),

$$I_1 = \frac{I_{T1}}{1 + e^{-V_d/n_{diff} V_T}}, \tag{4.31}$$

$$I_2 = \frac{I_{T1}}{1 + e^{V_d/n_{diff} V_T}}, \tag{4.32}$$

$$I_3 = \frac{I_{T2}}{1 + e^{V_d/n_{diff}V_T}}, \tag{4.33}$$

$$I_4 = \frac{I_{T2}}{1 + e^{-V_d/n_{diff}V_T}}. \tag{4.34}$$

Adding Equation (4.30) to equations (4.31) - (4.34), and reducing the exponent,

$$e^{\frac{n_{diode}}{n_{diff}}\left[\ln\left(\frac{I_{D2}}{K_{diode}}\right)-\ln\left(\frac{I_{D1}}{K_{diode}}\right)\right]} = \frac{e^{\frac{n_{diode}}{n_{diff}}\ln\left(\frac{I_{D2}}{K_{diode}}\right)}}{e^{\frac{n_{diode}}{n_{diff}}\ln\left(\frac{I_{D1}}{K_{diode}}\right)}} = \frac{\left(\frac{I_{D2}}{K_{diode}}\right)^{\frac{n_{diode}}{n_{diff}}}}{\left(\frac{I_{D1}}{K_{diode}}\right)^{\frac{n_{diode}}{n_{diff}}}} = \frac{(I_{D2})^{\frac{n_{diode}}{n_{diff}}}}{(I_{D1})^{\frac{n_{diode}}{n_{diff}}}}, \tag{4.35}$$

the new drain current equations become

$$I_1 = \frac{I_{T1}\,(I_{D1})^{\frac{n_{diode}}{n_{diff}}}}{(I_{D1})^{\frac{n_{diode}}{n_{diff}}} + (I_{D2})^{\frac{n_{diode}}{n_{diff}}}}, \tag{4.36}$$

$$I_2 = \frac{I_{T1}\,(I_{D2})^{\frac{n_{diode}}{n_{diff}}}}{(I_{D1})^{\frac{n_{diode}}{n_{diff}}} + (I_{D2})^{\frac{n_{diode}}{n_{diff}}}}, \tag{4.37}$$

$$I_3 = \frac{I_{T2}\,(I_{D2})^{\frac{n_{diode}}{n_{diff}}}}{(I_{D1})^{\frac{n_{diode}}{n_{diff}}} + (I_{D2})^{\frac{n_{diode}}{n_{diff}}}}, \tag{4.38}$$

$$I_4 = \frac{I_{T2}\,(I_{D1})^{\frac{n_{diode}}{n_{diff}}}}{(I_{D1})^{\frac{n_{diode}}{n_{diff}}} + (I_{D2})^{\frac{n_{diode}}{n_{diff}}}}. \tag{4.39}$$

The final differential output current is then

$$I_{out} = \frac{\left[(I_{D2})^{\frac{n_{diode}}{n_{diff}}} - (I_{D1})^{\frac{n_{diode}}{n_{diff}}}\right](I_{T1} - I_{T2})}{\left[(I_{D1})^{\frac{n_{diode}}{n_{diff}}} + (I_{D2})^{\frac{n_{diode}}{n_{diff}}}\right]}. \tag{4.40}$$

The ratio of n terms in the exponent of each I_D input causes the distortion. Figure 4.12 is a plot of Equation (4.40) for three cases: $n_{diode} > n_{diff}$, $n_{diode} < n_{diff}$, and $n_{diode} = n_{diff}$. For $n_{diode} = n_{diff}$, the exponential terms disappear, and Equation (4.40) becomes the same as Equation (4.3). The multiplier has a linear function. Mismatches in n cause change in slope, which introduces distortion, making the multiplier nonlinear.

If the slope of I_{out} is taken for each case, distortion can be analyzed. Figure 4.13 shows the slope of I_{out} relative to the input currents, for each of the cases outlined above. For $n_{diode} < n_{diff}$, the distortion can be defined as "concave slope distortion",

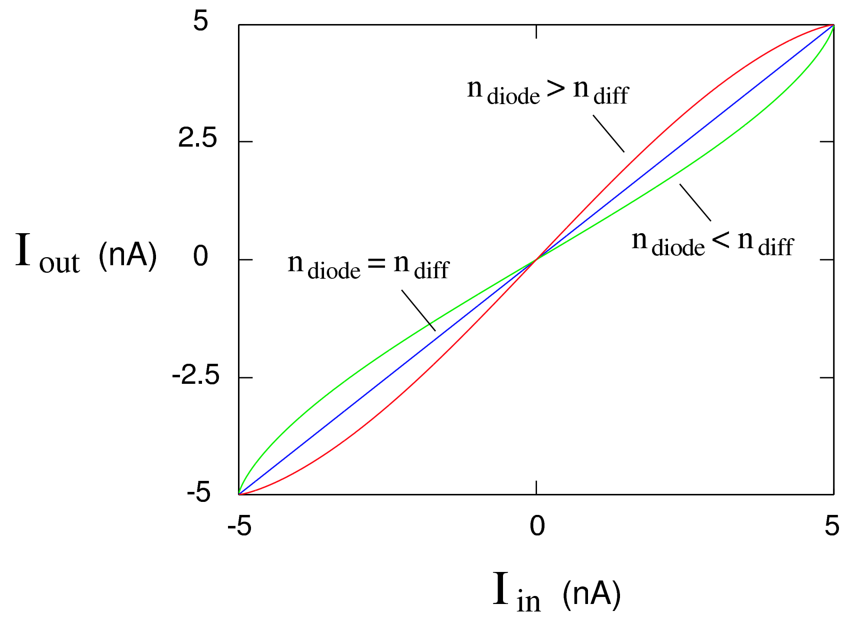


Figure 4.12: Effects of n on I_{out}.

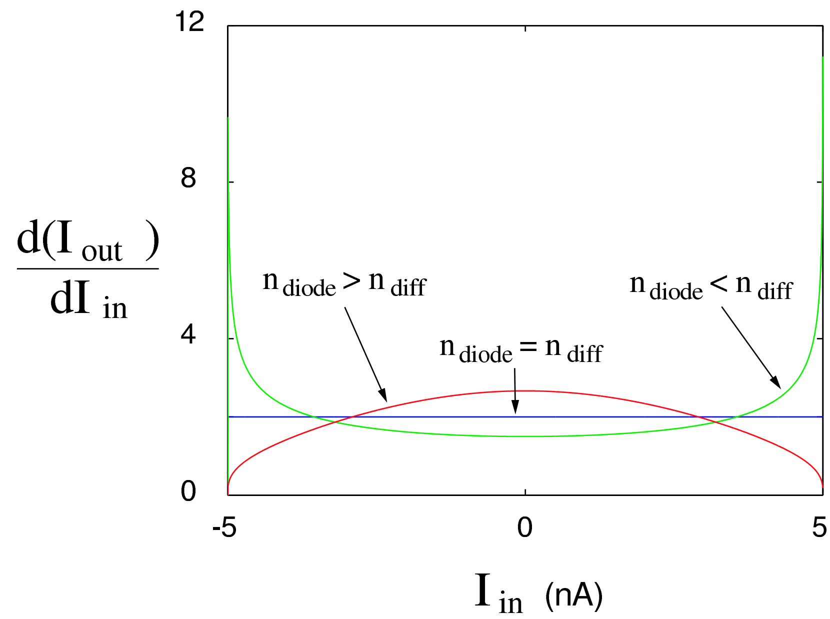


Figure 4.13: Effects of n on the slope of I_{out}.

due to the concave shape of the slope of I_{out} across the input range. For $n_{diode} > n_{diff}$, the distortion can be defined as "convex slope distortion", due to the convex shape. When $n_{diode} = n_{diff}$, there is no change in slope and the transfer characteristic is defined as "linear."

Section 4.4.2 identified the effects of V_{bs}, and L_{eff}, on the ideality factor. These effects can be carried over to the multiplier linearity. Section 4.4.2 defined an inverse relationship between V_{bs} and n, and a direct relationship between L_{eff} and n. Table 4.7 defines the relationships of V_{bs}, L_{eff}, and n to the type of slope distortion.

Table 4.7: V_{bs}, Leff, and n effects on slope distortion

$\lvert V_{bsdiode}\rvert > \lvert V_{bsdiff}\rvert$	$L_{effdiode} < L_{effdiff}$	$n_{diode} < n_{diff}$	concave slope distortion
$\lvert V_{bsdiode}\rvert < \lvert V_{bsdiff}\rvert$	$L_{effdiode} > L_{effdiff}$	$n_{diode} > n_{diff}$	convex slope distortion

4.5.3 Threshold Voltage Mismatch

Similar to the ideality factor, if the threshold voltages for all devices match across the input range, the threshold terms drop out of the final differential output current equation. However, due to the different large signal behavior between the differential and diode connected pairs, V_t's do not match, and must be retained. This results in a very large and complex final output current equation, which is not included here.

Evaluating the relationship between V_t and Leff, V_t mismatch effects can be seen in simulation. In simulations of the Gilbert cell architecture, for NMOS devices with longer gate lengths, the threshold voltages of each differential pair and the diode connected pair match. However, for short channel devices, this is not the case. The differential pair thresholds still match, but the diode connected device thresholds start to differ across the input range. This is shown in Figure 4.14 where

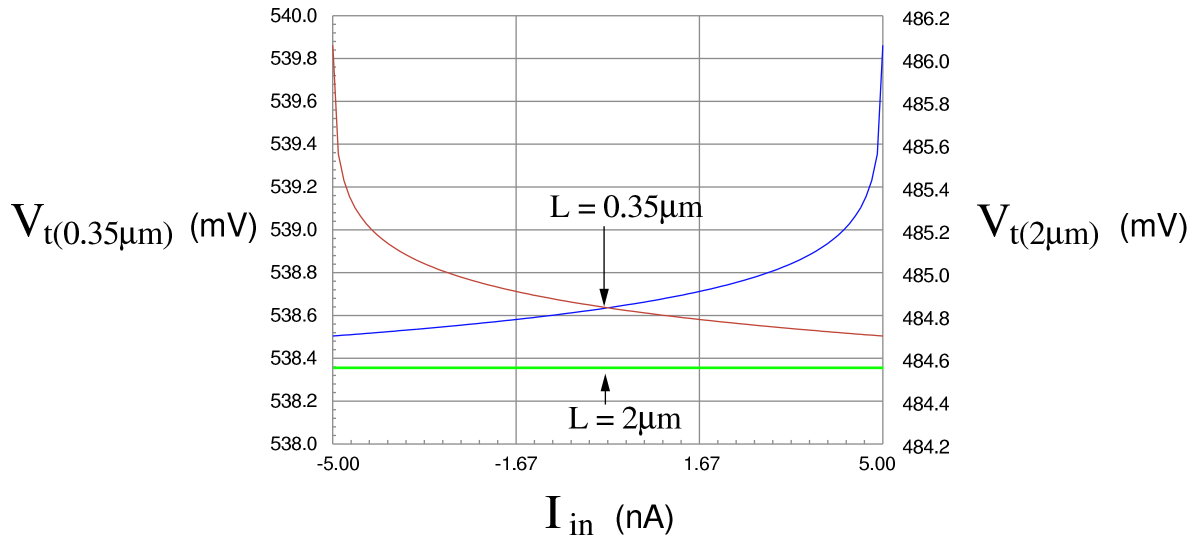


Figure 4.14: Simulated V_t values for L = 0.35 μm and 2 μm.

the diode-connected V_t's are shown for L = 0.35 μm and 2 μm. While the L = 2 μm thresholds stay constant at about 484.6 mV, and both thresholds match closely, at L_{eff} = 0.35 μm the curve looks like an inverted V_{ds} curve for a diode connected pair. This is due to the inverse relationship between V_t and V_{ds}, which can be extrapolated from Equations (4.19) and (4.21).

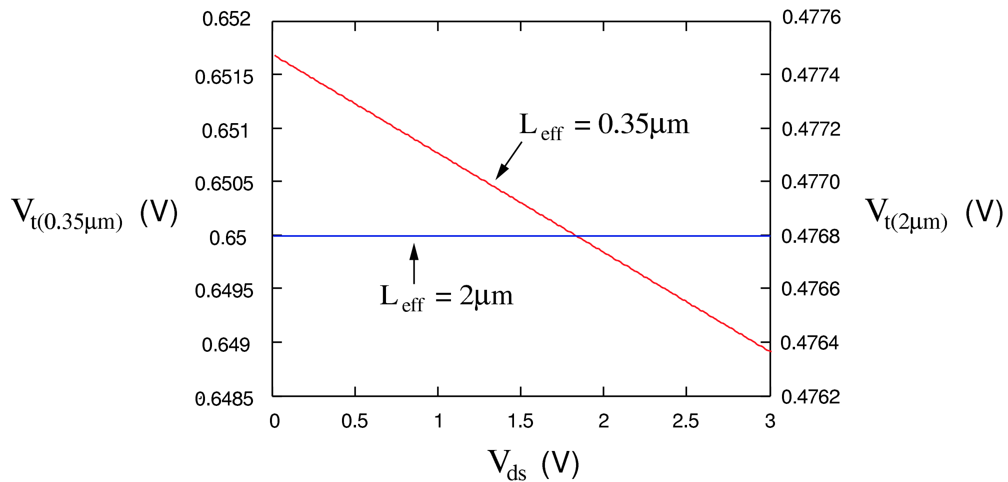


Figure 4.15: Inverse relationship between V_t and V_{ds} for Leff = 0.35 μm and 2 μm.

Figure 4.15 plots V_t versus V_{ds} for $L_{eff} = 0.35\,\mu$m and $2\,\mu$m. In the BSIM3 V_t equations (4.19) - (4.23), V_{ds} is effectively multiplied by the exponent of the ratio of L_{eff} and the characteristic length, $L_{t,SCE}$. Due to the relationship between L_{eff} and the characteristic length, the inverse relationship between L_{eff} and V_{ds} becomes significant only for short gate lengths.

Figure 4.16 shows the slope of the transfer characteristic at $L = 0.35\,\mu$m and $2\,\mu$m. Here the sensitivity to V_t mismatch on the multiplier can be seen. Even for small V_t mismatches like those shown in Figure 4.15 for $L_{eff} = 0.35\,\mu$m, the effect on the Gilbert cell causes significant concave distortion.

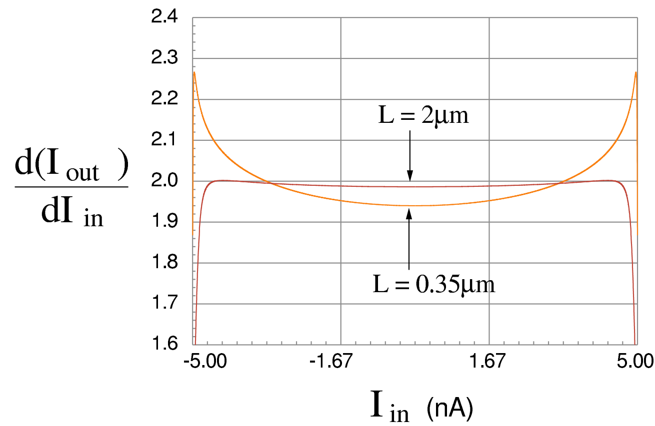


Figure 4.16: Slope of I_{out} for $L = 0.35\,\mu$m and $2\,\mu$m.

It is important to note here that isolating all sources of distortion in a simulation environment can be very difficult. Also, plotting BSIM models can become very tedious when working with complex equations and multiple empirical parameters. Therefore, some of the distortion in Figure 4.16 may be caused by other unknown sources. However, consistencies between Cadence and Mathcad simulations indicate that a substantial portion of the distortion is caused by V_t mismatch.

Also, the similarities between the behavior of the ideality factor, n, and V_t, shown in the last few sections should be noted. Data collected in this chapter, and the trends in BSIM modeling suggests that these parameters are closely related in

subthreshold. Their common relationship to C_{inv} would also suggest this. Therefore, data presented in Sections 4.5.2 and 4.5.3 may contain some crossover between the two parameters.

4.5.4 Charging Parasitic Capacitances with Small Device Currents

Section 4.2 defined the maximum device current levels to assure exponential (diffusion) currents, and allow I_{out} to be characterized by Equation (4.3). Small device currents must be used for linear multiplier function. However, these small device currents themselves can cause distortion under certain conditions. In addition to the V_{ds} effects (see Section 4.5.1) caused by small currents in the diode connected devices, small device currents also limit the operating frequency of the Gilbert cell multiplier. This is due to the time it takes to charge device parasitic capacitances.

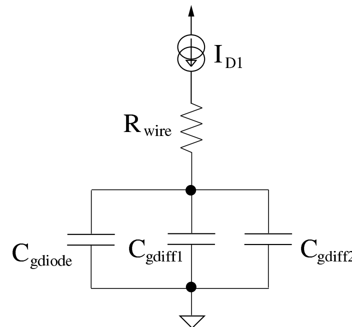


Figure 4.17: RC circuit from gate capacitors.

Looking into the inputs on the diode connected side (I_D) of the multiplier, the input can be modeled by the RC circuit shown in Figure 4.17. R_{wire} represents series resistance in the wires (which should be small), and the capacitors represent parasitic gate capacitances of devices on one side of each differential pair and the diode pair. Since the device currents are so small, it takes time to charge these capacitances. Increasing the device sizes increases parasitic capacitances, further increasing the time required to charge the capacitors.

Current used to charge the parasitic capacitances is then diverted from the device drain input until the capacitances are charged. This causes a "droop" in the drain current, as it starts to ramp. This droop converts directly into a droop in V_{gs} on one side of each differential pair, and on one of the diode connected devices. The final result is a droop in the differential output current, causing distortion. These effects are plotted in Figure 4.18. This plot shows significant distortion on I_{out}. Here devices at a maximum of 5 nA is used, with devices sizes of 10 μm/0.35 μm. For less than 10 percent distortion across the full input range, maximum frequencies are around 10 KHz, for this circuit.

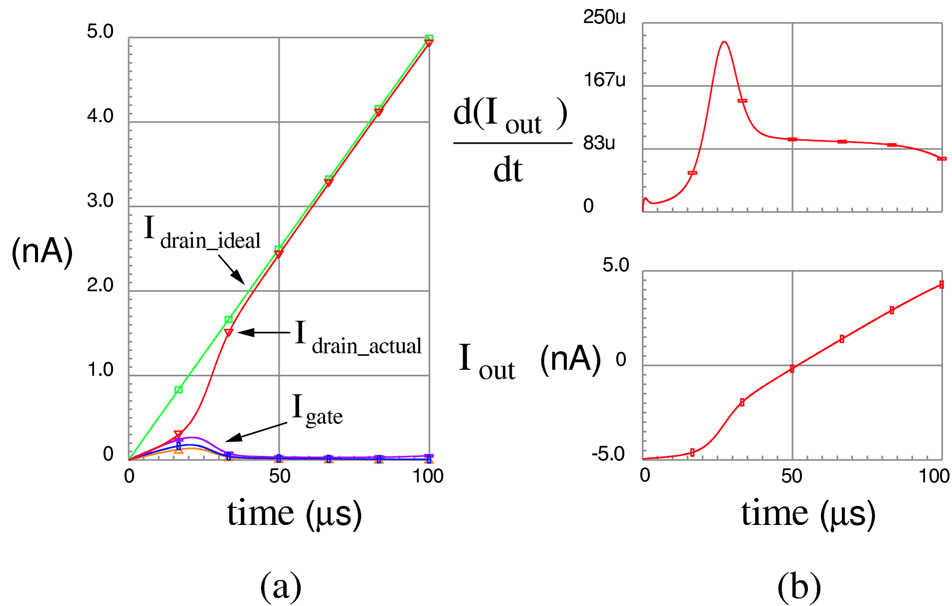


Figure 4.18: Charging gate capacitor effects on linearity.

Increasing device currents will improve AC performance. However, operating frequency will only increase up to the limit set by the RC time constant of the circuit modeled above. Also, increasing device currents introduces drift currents components to the differential output current, Equation (4.3), causing distortion.

Chapter 5

CMOS Weak and Moderate Inversion Gilbert Cell Multiplier Circuits

5.1 Introduction

Chapters 3 and 4 present the behavior of the CMOS Gilbert cell architecture biased in strong inversion and subthreshold, respectively. Based on the data and theory presented, four-quadrant multiplier circuits can be built biased in the weak and moderate inversion regions, that have low distortion and high performance levels, relative to many other CMOS multiplier architectures. This chapter will present three multiplier circuit configurations biased across the weak and moderate inversion, where effects from both drift and diffusion currents are present. Circuit performance will be evaluated, and tradeoffs will be identified, based on simulation results.

5.2 Deep Subthreshold Multiplier Circuit

Chapter 4 outlined biasing and higher order effects on the Gilbert cell architecture in subthreshold. Both of these effects can cause variations to the ideal diode expression of Equation (4.12), that introduces distortion to the final multiplier differential output current, Equation (4.3). Applying the concepts presented, a linear deep subthreshold multiplier can be built by minimizing the distortion caused by V_{ds}, the ideality factor, drift current components, and parasitic capacitances.

The first two multiplier circuits presented in Chapter 5 are based on the PMOS Gilbert cell architecture shown in Figure 5.1. The deep subthreshold circuit is designed such that all possible sources of distortion are minimized. PMOS devices are

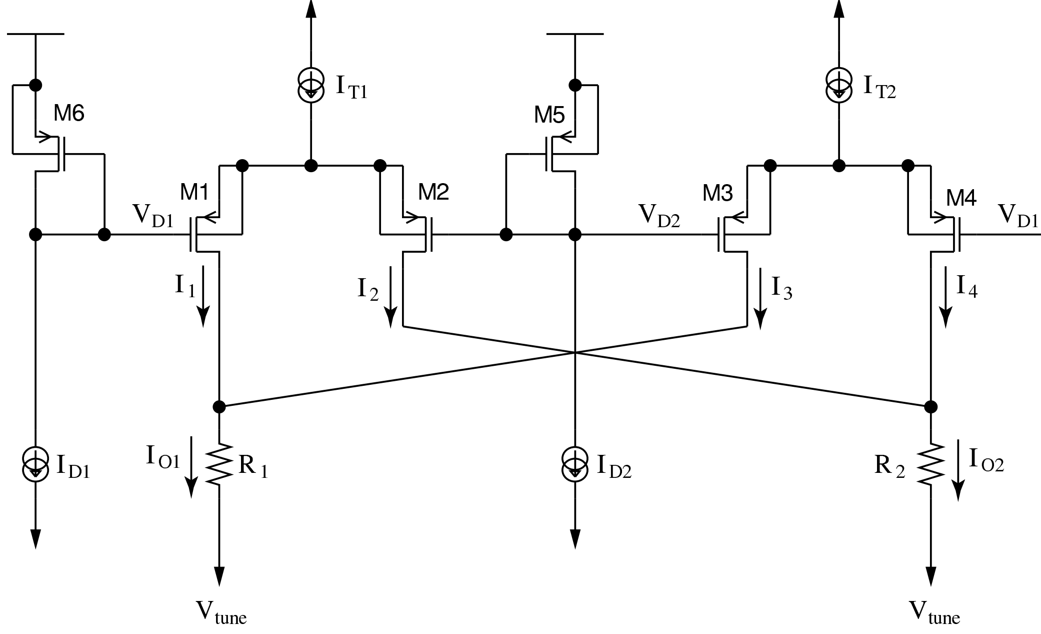


Figure 5.1: PMOS Gilbert cell multiplier circuit.

used so that in the n-well only $0.35 - \mu$m AMIS process, the bulk can be tied to the source. This eliminates body effect on all the devices. This also requires layout of each pair of devices in separate n-wells. Since the final multiplier output current Equation (4.3) requires that all device sizes match to build a linear multiplier, all device widths are 10 μm, and all device lengths are 2 μm. Device widths are kept small to minimize the parasitic capacitances that cause long charging times. Longer gate lengths are chosen to reduce short channel effects and improve device channel length matching. Dynamic input currents are chosen to be less than 5 nA to assure that the resulting gate-to-source voltages are small enough to keep the devices biased deep into subthreshold. This minimizes any effects of drift currents. At $|V_t| = 0.56$V, $|V_{gs}|$ across the dynamic input range of each device is less than 0.4V. Also, the drains of the differentially paired devices are tied to 0.3 V through a 1MΩ resistor (for test purposes) to help optimize the linearity. The circuit was initially simulated with 1kΩ resistors tied to ground. The linearity and performance are almost identical to the 1kΩ case, but the small resistors made measuring the output voltage across the resistors difficult, so 1MΩ resistors are used.

At these small input currents, this circuit is biased deep into weak inversion. This is shown when calculating the inversion coefficient. For a PMOS device in the AMIS 0.35-μm process, the process current $I_0 = 0.07382\,\mu A$. At device size 10μm/2μm and device currents less than 5 nA, IC $<$ 0.0135. This is well below the upper weak inversion IC limit of 0.1.

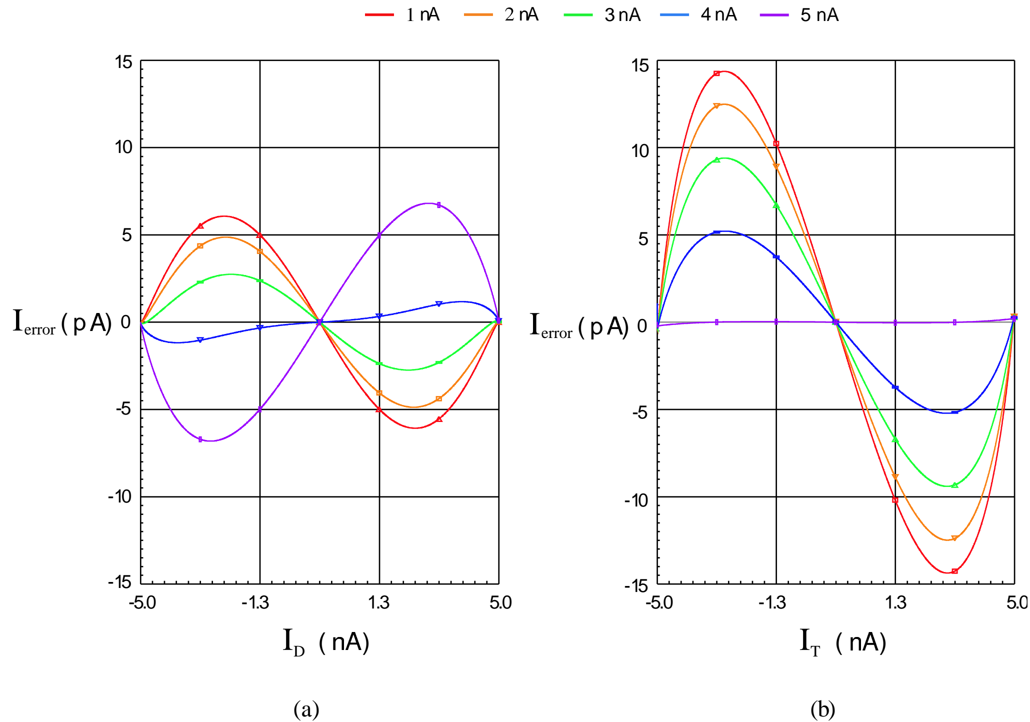


Figure 5.2: Deep subthreshold DC linearity: NL_{error} across input ranges.

The DC linearity can be found by sweeping the full range of one differential input current, while biasing the other differential input current at a fixed differential range. For example, for the maximum output current simulation, $I_{D1} = 0 \rightarrow 5$ nA, $I_{D2} = 5 \rightarrow 0$ nA, $I_{T1} = 5$ nA, and $I_{T2} = 0$ nA. Figure 5.2 shows the DC NL_{error} sweeping the full range of each differential input, while the other differential input is at 1nA, 2nA, 3nA, 4nA, and 5nA. This is necessary to assess the total multiplier linearity across both input ranges.

In Figure 5.2, I_{error} (which is NL_{error}) is less than 7 pA when sweeping the I_D input, and less than 15 pA when sweeping the I_T input. Referring to the output current slope to qualitatively examine the linearity versus higher order effects, the plots of 5.2(b) are representative of concave slope distortion. Here the simulated output current exceeds the ideal output current when the differential input current I_T is negative, and it is less than the ideal output current when I_T is positive. The plots of 5.2(a) show some amounts of both convex and concave slope distortion. It can be seen that even though most sources of body and short channel effects are removed, there still remains some distortion due to the different large signal biasing of each device. Adjusting the V_{ds} of the differential devices helps tune the circuit to minimize the remaining distortion.

Table 5.1: Deep subthreshold circuit, DC output nonlinearity.

Opposite $I_{D/T}$ range	% NL Error, I_D Sweep	% NL Error, I_T Sweep
5nA	0.068	0.002
4nA	0.012	0.052
3nA	0.027	0.094
2nA	0.049	0.125
1nA	0.061	0.144

The final % NL_{error} is reported in Table 5.1. Less than 0.068 % nonlinearity can be achieved across the whole range of I_D. I_T is a little more sensitive to the biasing effects. There is up to 0.144 % nonlinearity across 100 % of the I_T range for small values of I_D. The DC differential output currents are shown in Figure 5.3, for a full range of differential input currents. Since the DC output current plots are virtually identical for both I_D and I_T, this figure represent current sweeps on both inputs.

The AC performance is limited by the small currents used in deep subthreshold. The bandwidth is limited to 48 kHz on the I_D input, and 130 kHz on the I_T input. The bandwidth is measured with a full scale sinusoid on the measured input, while the other input is at DC full scale (0 nA and 5 nA). Since this is a current mode

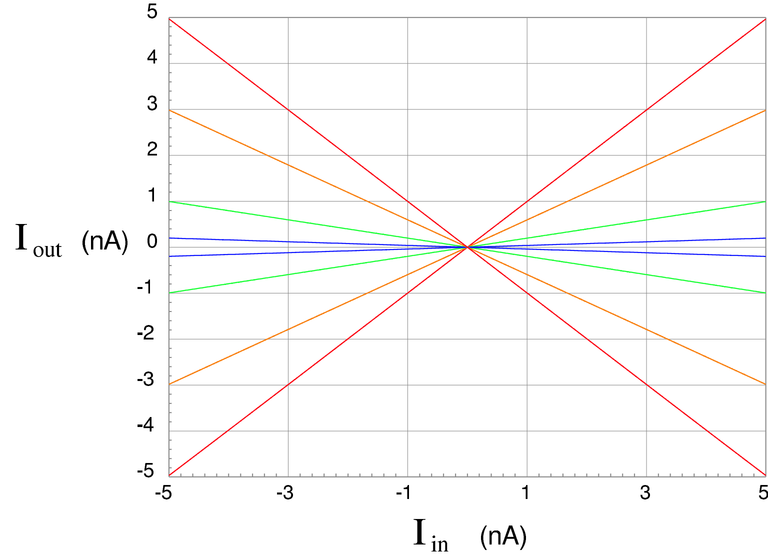


Figure 5.3: I_{out} DC linearity across full range of input currents.

circuit, the gain is close to unity for both inputs. However, some gain attenuation exists as leakage currents are more significant at the very small deep subthreshold current levels.

To measure transient linearity, total harmonic distortion (THD) is measured across the dynamic input range and operating frequency range. THD data is plotted in Figure 5.4. At low frequencies, full scale input distortion is comparable to DC distortion levels. As the frequency increases, the parasitic RC effects described in Section 4.5.4 increase output distortion.

Examining the plots, significant distortion at the full scale input range starts to occur above 1 kHz. Higher frequencies can be reached by sacrificing input range. Note the cross over in 5.4(b), where the 100 kHz curve drops in distortion level below the 10 kHz curve. This happens when nearing the 3 db bandwidth, as the gain starts to fall off, and the reduced current range due to gain loss reduces the distortion.

Even though the bandwidths of the deep subthreshold multiplier are as high as 130 kHz, the distortion due to parasitic capacitances limits the operating frequency of the circuit to a few kHz.

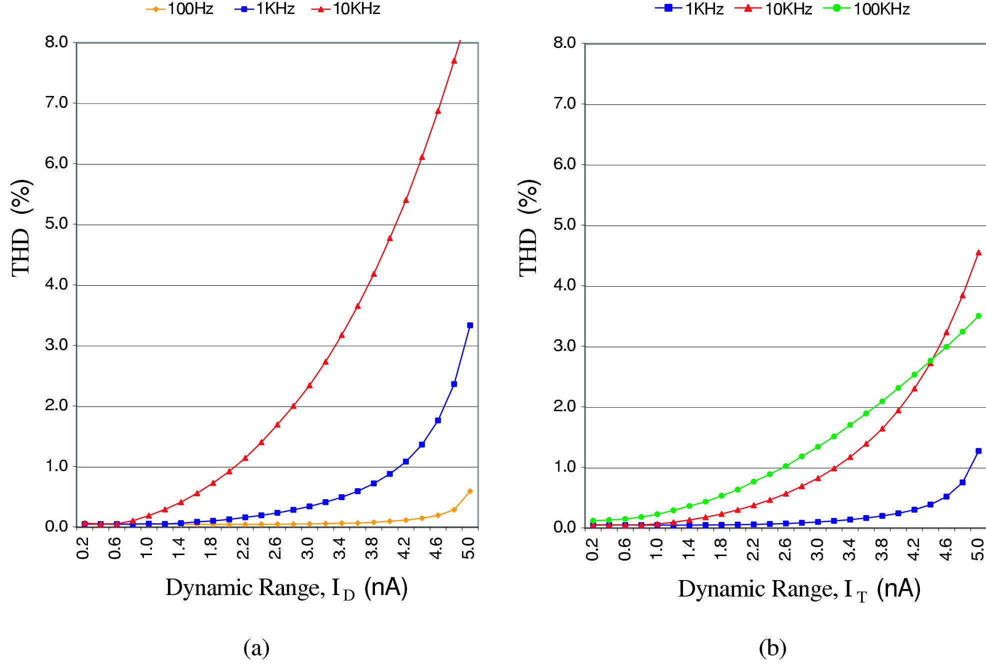


Figure 5.4: THD for deep subthreshold circuit with distortion removed.

5.3 Shallow Subthreshold Multiplier Circuit

To improve the AC performance of the multiplier, input currents can be increased to help charge the parasitic capacitances. However, as input currents are increased, linearity suffers due to increased drift currents, as the device is biased closer to the threshold voltage, and an inversion channel starts to develop. To minimize drift current components, a larger W/L ratio can be used to reduce gate-to-source voltages, moving the device further into subthreshold (see Section 4.2). The tradeoff is that as the device width increases, so does the parasitic gate capacitances, decreasing the AC performance. Therefore, a minimum gate length should be used first to increase the W/L ratio. The minimum sized gate length will increase the threshold voltage due to RSCE (as explained in Section 4.4.3), as well as decrease V_{gs}, limiting the inversion channel and reducing drift currents.

To build the "shallow" subthreshold multiplier circuit, the PMOS architecture shown in Figure 5.1 is used again with different device sizes and current levels. Device sizes of $60\mu m/0.35\mu m$ are used for all devices, with $V_L = 1.75$ V and $R_L = 1$ KΩ.

Minimum gate length devices not only improve AC performance, but the short channel effects cause convex slope distortion, which helps cancel some of the concave slope distortion introduced by drift currents, as the devices are biased closer to the threshold voltage. As with the deep subthreshold circuit, V_L (which is the same as V_{tune} in Figure 5.1) tunes the linearity, adjusting V_{ds} to take further advantage of short channel effects. The input current range is chosen at $0\,\mu A - 1\,\mu A$, which is the maximum estimation for exponential device currents, extrapolated from Table 4.2. PMOS devices are used once again to eliminate body effect, tying the source to the substrate. When sweeping the input currents, $|V_{gs}| < 0.4\,V$ for all inputs, at $|V_{tmin}| = 0.45\,V$.

With these device sizes and currents, the inversion coefficient is less than 0.079. This classifies the shallow subthreshold circuit at the high end of weak inversion. This is consistent with the maximum exponential current estimates of Table 4.2. At $I_{ds} \sim 1\,\mu A$ drift currents are starting to become significant.

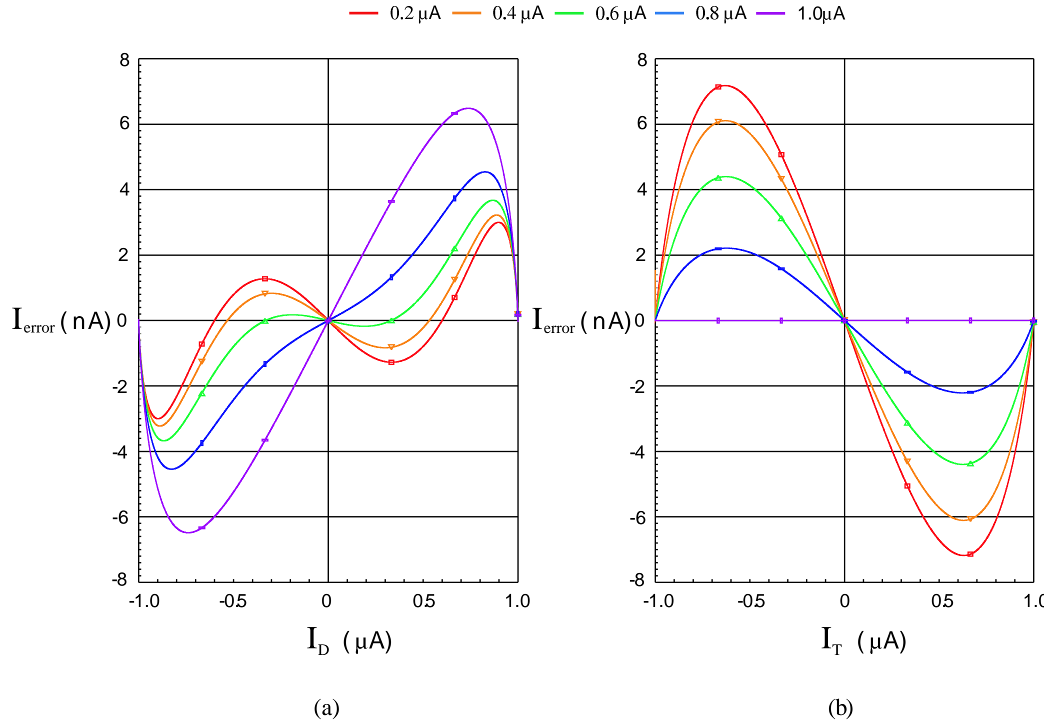


Figure 5.5: Shallow subthreshold DC linearity: NL_{error} across input ranges.

Evaluating the DC linearity, Figure 5.5 shows the linearity across the input range of both inputs, I_D and I_T. Less than 0.359 % nonlinearity can be achieved across 100 % of the dynamic input range for both inputs. This is reported in Table 5.2. Reducing the large V_{ds} across the devices by increasing V_L to 1.75 V helps reduce the convex slope distortion shown in Figure 5.5(a). However, this also increases the concave slope distortion in Figure 5.5(b). This concave distortion is primarily caused by drift current components, since $|V_{gs}|$ of each diode-connected device is largest at the minimum differential input current ranges. The concave slope distortion shown in Figure 5.5(b) is consistent with the theory presented in Chapter 3, and shown in Figure 3.7.

Table 5.2: Shallow subthreshold circuit, DC output nonlinearity.

Opposite $I_{D/T}$ range	% NL Error, I_D Sweep	% NL Error, I_T Sweep
1.0uA	0.324	8.9e-5
0.8uA	0.227	0.111
0.6uA	0.184	0.220
0.4uA	0.161	0.305
0.2uA	0.150	0.359

Increasing the current dramatically improves the AC performance of the multiplier, compared to the deep subthreshold circuits. The resulting 3 db bandwidths are 8.3 MHz and 11.4 MHz for I_D and I_T, respectively. The current gain is very close to unity, since leakage currents are less significant compared to the larger signal currents (relative to the deep subthreshold signal currents).

With the increased input currents, the device is able to charge parasitic capacitances much quicker, allowing for lower total harmonic distortion at higher frequencies. Figure 5.6 shows that for full input ranges, THD is less than 3 % for up to 100 kHz.

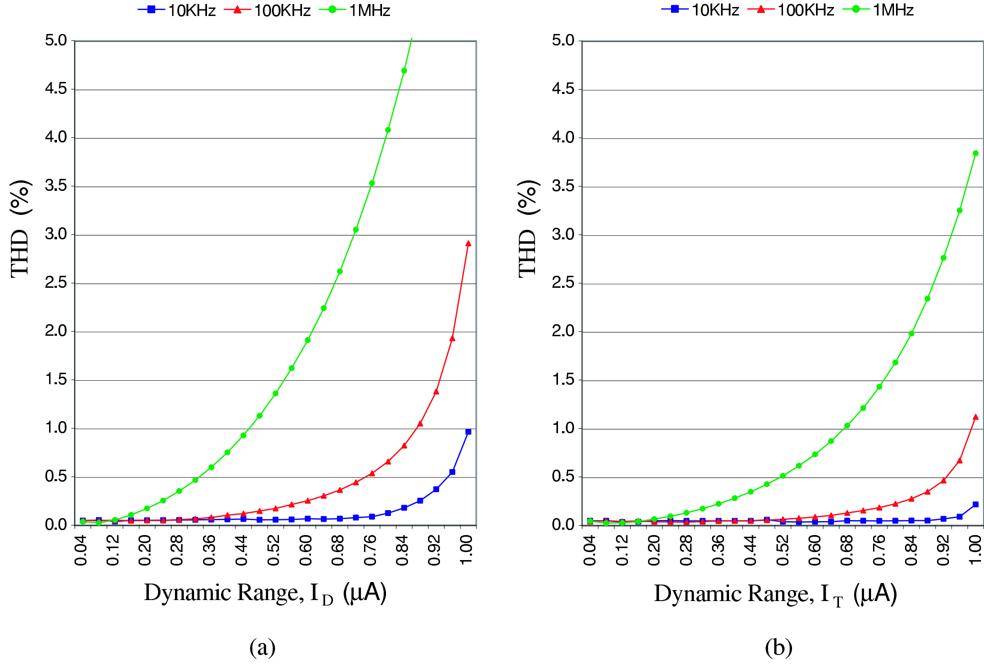


Figure 5.6: THD for shallow subthreshold circuit.

Increasing the device currents sacrifices some linearity for speed. Processing sensitivities are small, but matching devices is critical, since this architecture is sensitive to device mismatch, particularly in the differential pairs, and the diode pair. Common centroid layout can be used on the differential pair to improve matching.

5.4 Superthreshold Multiplier Circuit

As with the shallow subthreshold multiplier, further increase in device current causes a larger drift current component of the total device current. If input currents cause gate-to-source voltages to exceed the threshold voltage, by definition, an inversion channel will be established well enough that the drift current components will be very significant. The concave slope distortion created by the drift currents will be large enough that subthreshold linearizing techniques alone will not be sufficient to linearize the multiplier to less than one percent distortion. Additional techniques are needed to compensate for significant drift current distortion.

Section 3.4 defined a limiting factor for building a CMOS Gilbert cell multiplier in strong inversion. For a single differential pair with diode-connected devices connected to the gates, if the criteria $I_{D1} + I_{D2} = I_T$ is met, a linear differential output current between the two drain currents of the differential pair can be achieved. However, it was shown that when applied to the Gilbert cell architecture with two differential pair sharing the diode devices, the equilibrium condition, $I_{D1} + I_{D2} = I_T$, could not be met for both I_T inputs.

This sensitivity can be reduced by adding a DC offset to the tail current inputs. For differential input ranges of the same size on I_D and I_T, if the I_D range is $0 \rightarrow 20\,\mu A$, then the I_T range should be $10\,\mu A \rightarrow 30\,\mu A$. This will center the I_T differential range around the equilibrium value of $I_{D1} + I_{D2} = 20\,\mu A$. This minimizes the maximum distortion. The result is I_T extreme input current levels at $10\,\mu A$ and $30\,\mu A$, rather than $0\,\mu A$ and $20\,\mu A$. This gives the worst case condition, $I_{D1} + I_{D2} - I_T = 10\,\mu A$, rather than $20\,\mu A$.

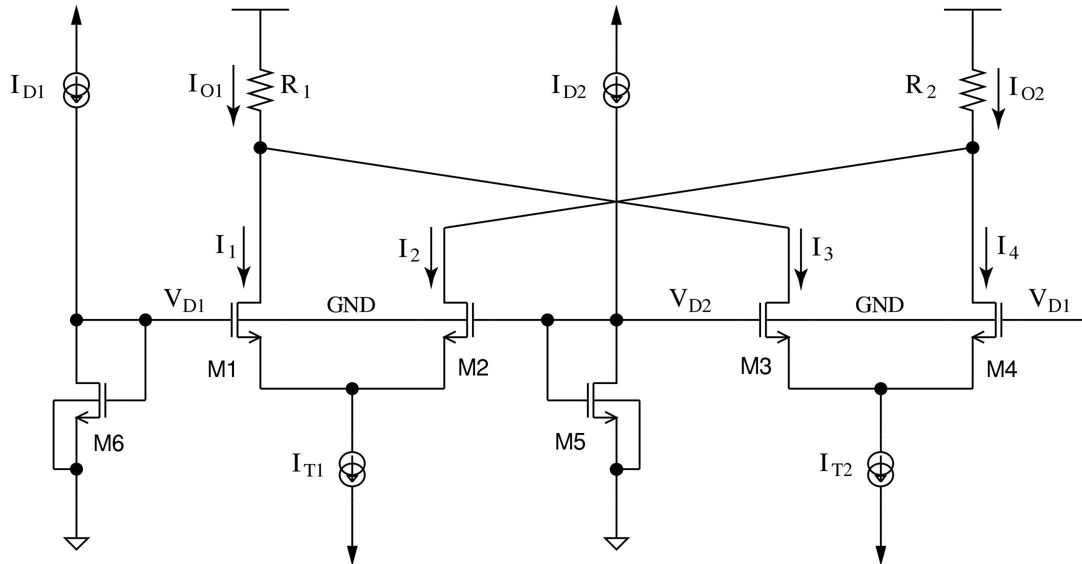


Figure 5.7: NMOS Gilbert cell multiplier circuit.

Evaluating the NMOS circuit of Figure 5.7, the multiplier without a DC offset has a significant bias mismatch in V_{gs} values between devices. Looking at Figure

5.8, this mismatch can be seen. Figure 5.8(a) shows V_{gs} across the full scale I_T range(0→20 μA). Here, since I_{T1} is so small, its effects on total distortion are not significant, and the output current can be made quite linear. The multiplier behaves like a single differential pair with diode-connected inputs. Notice that $V_{gsdiff2}$ and $V_{gsdiode}$ match somewhat. However, in Figure 5.8(b), the tail current input is at a minimal dynamic range ($I_{T1} = 9\,\mu$A and $I_{T2} = 11\,\mu$A). Here I_T becomes significant when converted to $V_{gsdiff1}$. The V_{gs} curves are quite different between the differential and diode connected devices. This results in significant distortion as differential input ranges decrease.

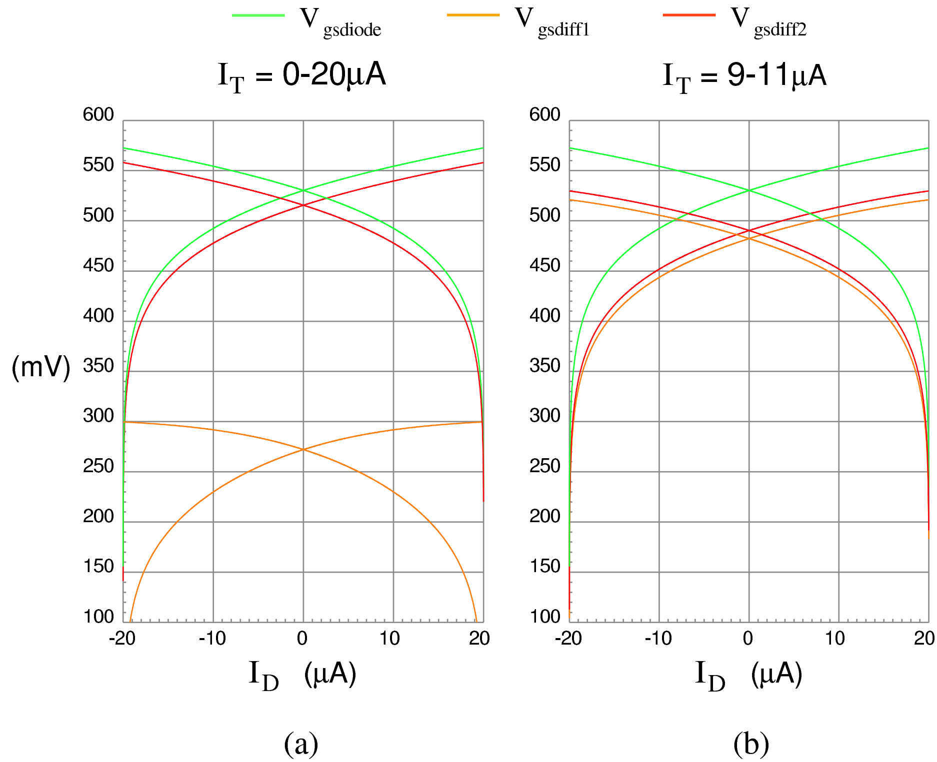


Figure 5.8: V_{GS} Bias mismatch with no offset.

Figure 5.9 shows the V_{gs} plots when DC offset is added to the tail current inputs. Here it can be seen that the V_{gs} values of all devices match more closely. As I_{T1} and I_{T2} converge in a differential sweep, they converge on 20 μA, rather than 10

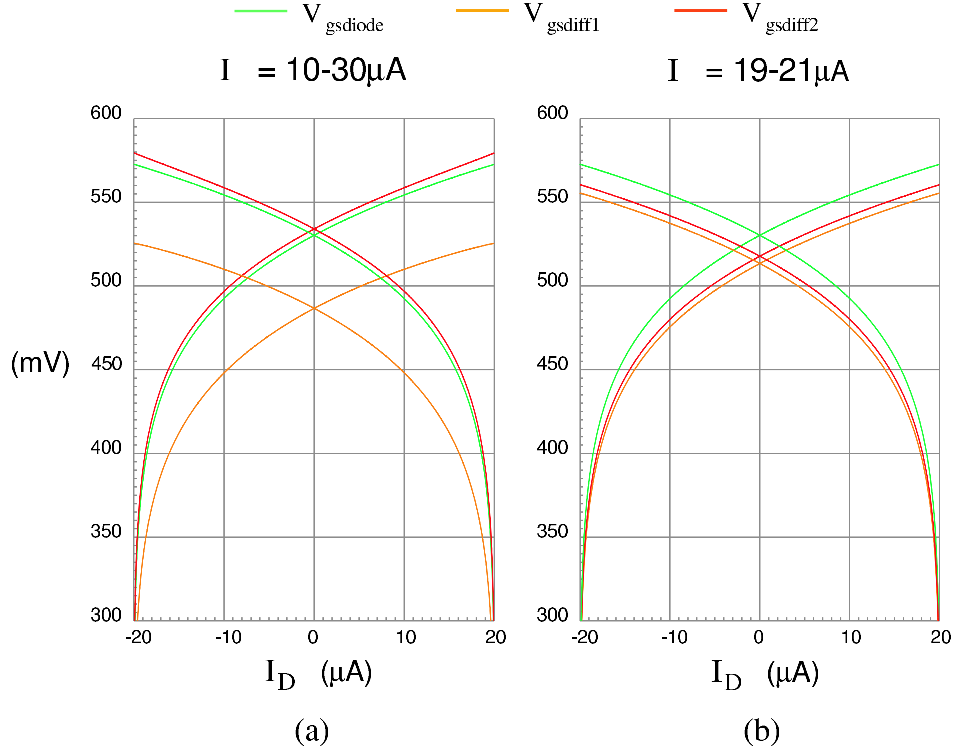


Figure 5.9: V_{GS} Bias mismatch with offset.

μA. Even though there is still significant distortion on the output, it is reduced enough that the subthreshold linearizing techniques can now be used to reduce distortion across the whole dynamic input range. Sweeping I_T gives similar behavior.

Using the input-offset multiplier, convex slope distortion cancellation can be used to cancel the concave slope distortion caused by the drift currents. As described in Section 4.5.2, if $L_{effdiff} < L_{effdiode}$, convex distortion will result on the diffusion current components. Gate length can be chosen to make the drift and diffusion current distortion cancel.

Chapter 3 mentions the effects of channel length modulation. This effect is included in the concave slope distortion caused by the drift currents and can be reduced by the device mismatching that creates convex slope, as mentioned above.

The NMOS Gilbert cell architecture of Figure 5.7 is used to create the "superthreshold" multiplier circuit. Choosing $L_{diff} = 0.49\ \mu$m and $L_{diode} = 1\ \mu$m will create the convex slope distortion needed. The device width is 30 μm for both W_{diff} and

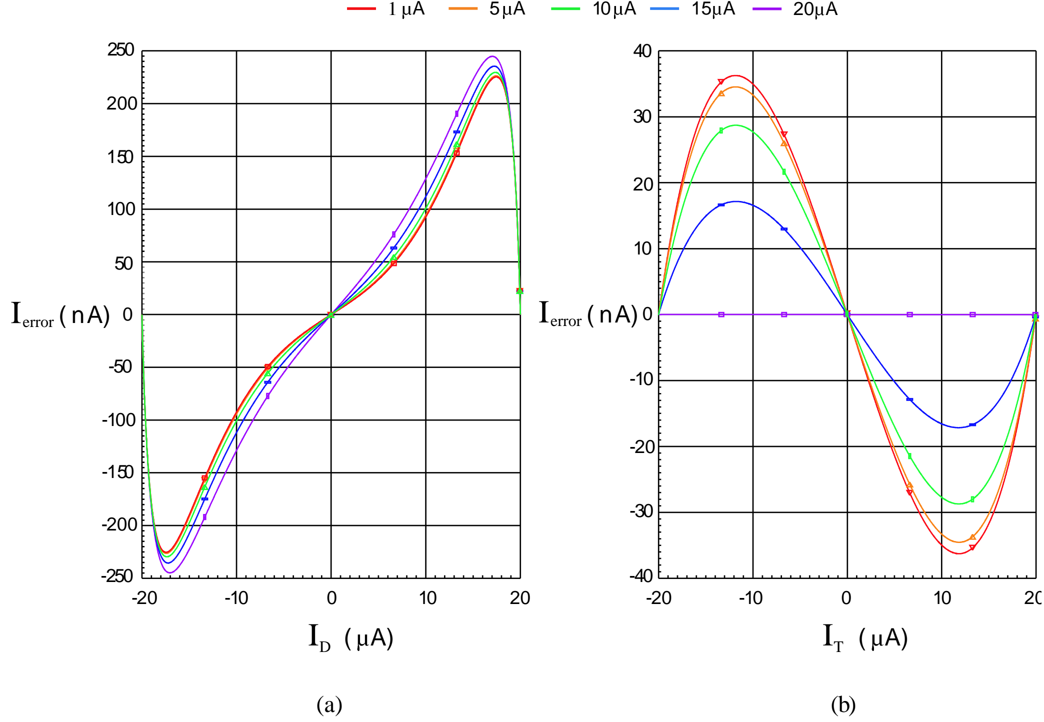


Figure 5.10: Superthreshold DC linearity: NL_{error} across input ranges.

W_{diode}. Input current values specified above (0→20μA) and (10→30μA) are used here. NMOS devices are chosen to maximize speed (due to higher mobility). The body effect caused by all devices sharing the same substrate (causing V_{bs}) actually helps counter the concave distortion caused by the drift currents.

With much larger device currents than the subthreshold circuits, the inversion coefficient increases significantly, putting the devices in moderate inversion for most of the input range. For the superthreshold circuit, IC = 2.167 at 20 μA device currents, based on $I_0 = 0.30758\,\mu$A for an NMOS device.

Figure 5.10 shows the DC linearity. Less than 0.611 % nonlinearity can be achieved across 100 % of the dynamic input range. The DC results are tabulated in Table 5.3.

With larger input currents, the AC performance improves by an order of magnitude over the shallow subthreshold circuit. The 3dB bandwidths are 114 MHz and 330 MHz for I_D and I_T inputs, respectively. The current gain is unity.

Table 5.3: Superthreshold circuit, DC output nonlinearity.

Opposite $I_{D/T}$ range	% NL Error, I_D Sweep	% NL Error, I_T Sweep
20uA	0.611	5e-7
15uA	0.589	0.043
10uA	0.574	0.072
5uA	0.565	0.086
1uA	0.563	0.091

The transient performance is also much improved over the subthreshold circuits. The large currents charge parasitic capacitances much quicker. Figure 5.11 shows the THD for the superthreshold circuit. The I_D input is at least an order of magnitude faster than the shallow subthreshold circuit at the same levels of full scale distortion. The I_T input is more than two orders of magnitude faster than the subthreshold circuits, operating in excess of 100 MHz with less than 1 % THD at the full input range. This is due to the increased input currents and the high linearity at full scale I_D (as documented in Section 3.4). At I_{Dmin} distortion increases.

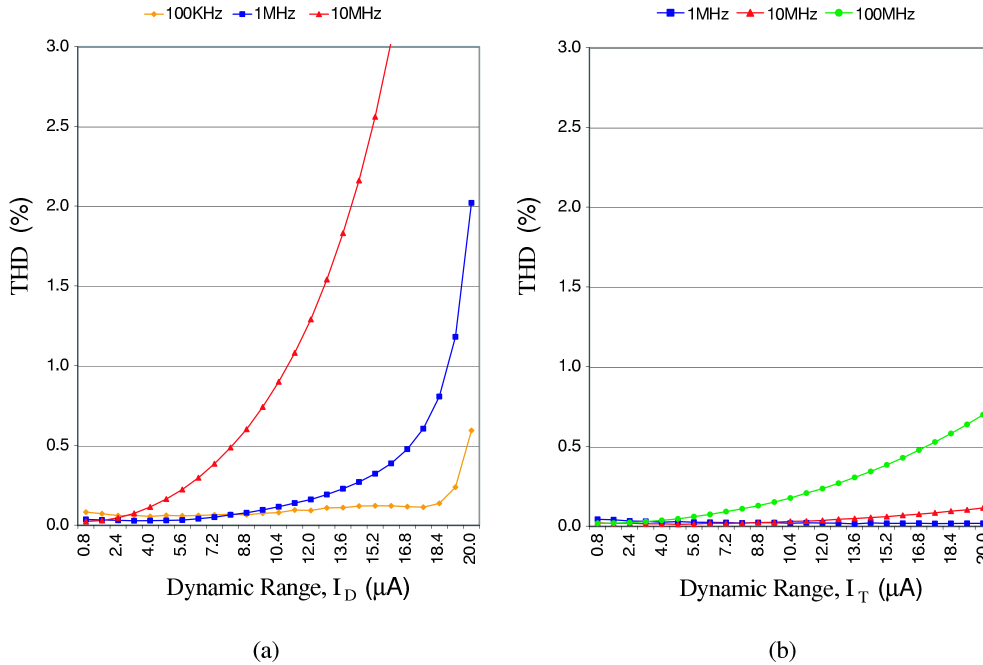


Figure 5.11: THD for “Superthreshold” WI circuit.

With the larger device currents and sizes, process sensitivities are minimized. The most significant sensitivity is device matching. Good layout can minimize this.

A drawback of the input-offset technique is that, as the description states, a DC offset is required on the input, and correspondingly, exists on each single-ended output. This can cause need for further circuitry at the inputs and outputs of the multiplier to level-shift the signals.

Chapter 6

Test Results

Three weak inversion circuits were fabricated in an AMIS 0.35-μm CMOS process: the deep subthreshold circuit, the shallow subthreshold circuit, and a variation of the superthreshold circuit. These circuits were chosen primarily based on testability. The superthreshold circuit tested is a previous version of the circuit shown in Figure 5.7, which was fabricated previous to the subthreshold circuits in a different wafer lot.

For the subthreshold circuits, the circuit representation shown in Figure 5.1 was fabricated with the device and resistor values documented in Chapter 5, with the following exceptions. Some small protection resistors were added to circuit ports connect to gates and drains to add ESD protection. These added resistors had very minimal effect on circuit performance. No further ESD protection circuitry was added to the subthreshold circuits. This kept on-silicon, non-multiplier distortion sources to a minimum. Due to the small signal currents, large resistors were used to convert output currents to voltages for measurements on the subthreshold circuits. That is why large resistors were added to the deep subthreshold circuit. Also, the shallow subthreshold circuit used 100 kΩ loads connected to 0.3 V, rather than 1 kΩ loads connected to 1.75 V. Simulations show a small reduction in DC linearity with this setup. Input currents were created by current sources which consisted of a 10 MΩ in series with a voltage source. Only DC linearity was measured on these circuits.

Figure 6.1 shows the nonlinear error of the deep subthreshold circuit, for a linear ramp on both inputs. The nonsweeping input was held at the maximum input range for both plots, allowing for maximum gain at the output. As can be seen,

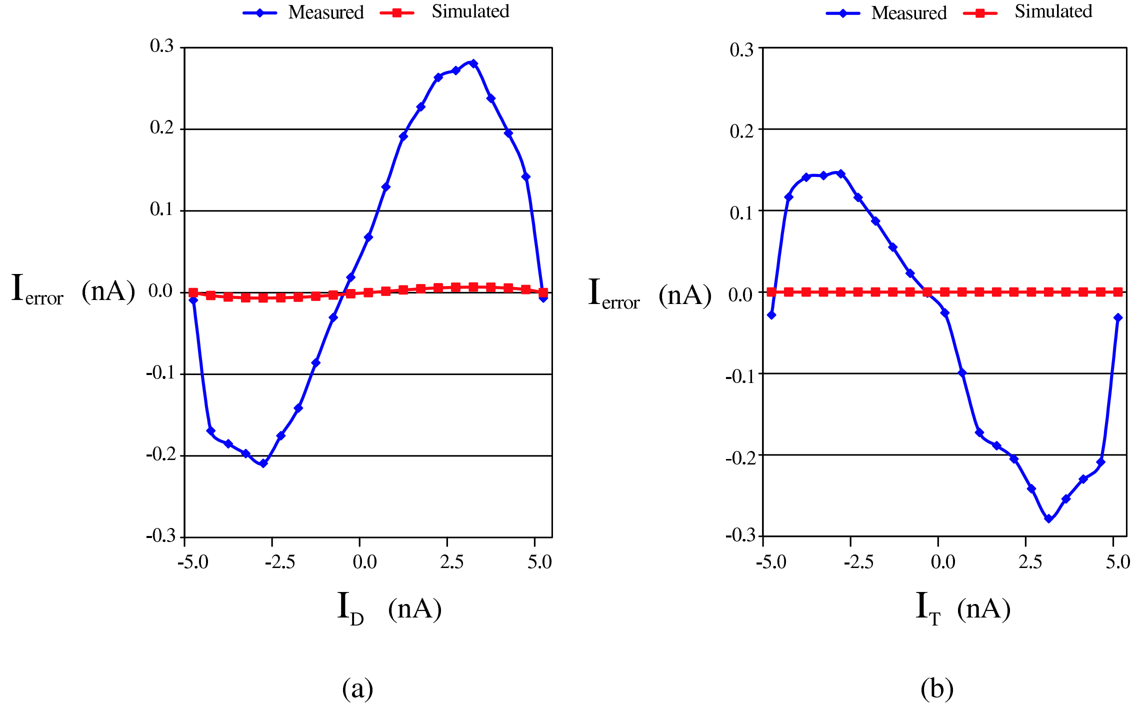


Figure 6.1: Test results: Deep subthreshold DC linearity.

there is a large difference in I_{error} between simulation and silicon. This is caused by off-chip loading of the test equipment. The maximum specified input impedance on the voltage meters used to measure the converted output voltages is 10 GΩ to ground. Both multiplier inputs are biased at around 3 V across the full input ranges. So each meter probe connected at the inputs is drawing at least 0.3 nA from a maximum of 5 nA on the inputs. This leakage current into the probes is greater than 6 % of the maximum input currents. Monitoring the VDD source on the diode connected devices, more than 0.3 nA was drawn by the meter probes. This leakage current translates into offset in the input currents that cause the bulk of the nonlinearity shown in Figure 6.1. These results emphasize the point that devices biased in deep subthreshold suffer from the effects of even small leakage currents. However, on-chip leakage currents will be significantly less that 0.3 nA (more in the pA range), so nonlinearity should be significantly reduced on-chip. Even though the wave form shapes correlate between simulation and silicon (see Figure 6.1(a)), the I_{error} amplitude is inaccurate due to the test probe leakage currents, so it is not included in the final results.

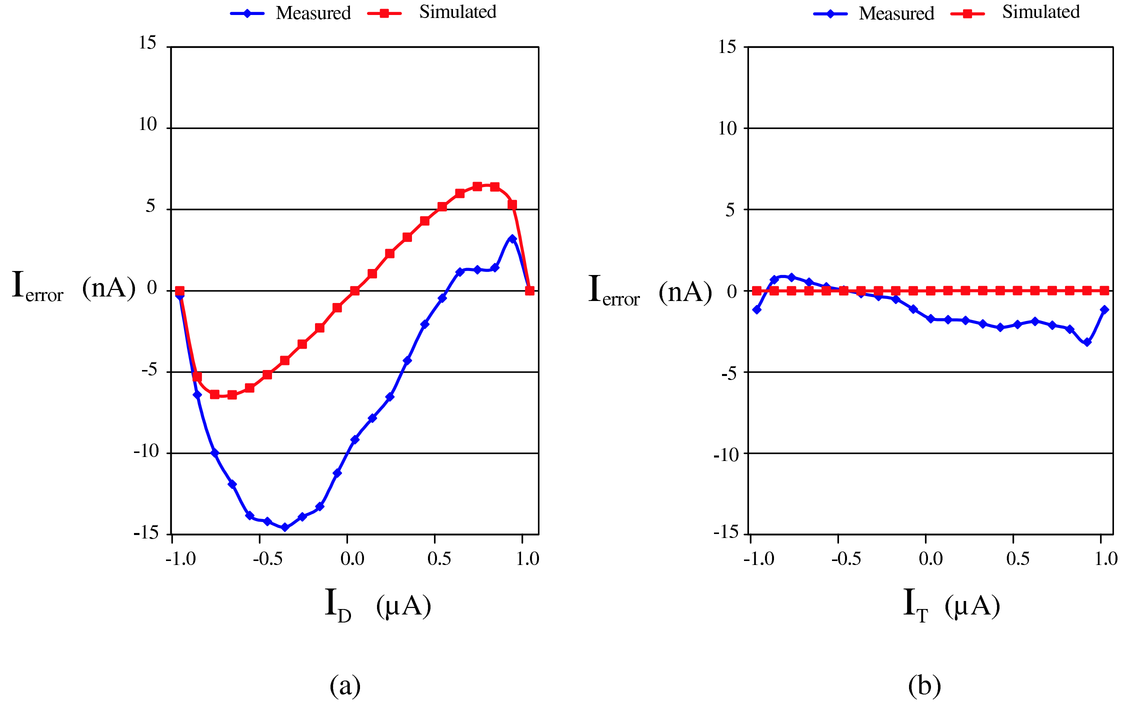


Figure 6.2: Test results: Shallow subthreshold DC linearity.

The shallow subthreshold circuit was not as sensitive to off-chip leakage currents because input currents are larger (1 μA, rather than only 5 nA in deep subthreshold). Therefore, nonlinearities introduced by leakage currents are much smaller. Figure 6.2 shows the nonlinear error of the output currents. The maximum ranges on opposite inputs were tested. Final nonlinearity is 0.73 % for the I_D input sweep, and 0.16 % for the I_T input sweep. Nonlinearity values are across 100 % of the dynamic input range.

Comparison of the simulated and measure curves shows a level of correlation in shape and amplitude. This is mostly apparent in Figure 6.2(a). In Figure 6.2(b) the simulated nonlinear error is so small that the correlation in curve shape cannot be seen on this plot. But if the shape of the measured value is compared to the shape in Figure 5.2, a correlation can be seen, both I_T plots showing concave slope distortion.

As mentioned previously, an early version of the superthreshold circuit was tested. This circuit is shown in Figure 6.3. Here a “wave-shaping” stage (inside the dashed box) has been added to the Gilbert cell configuration to extend the linear

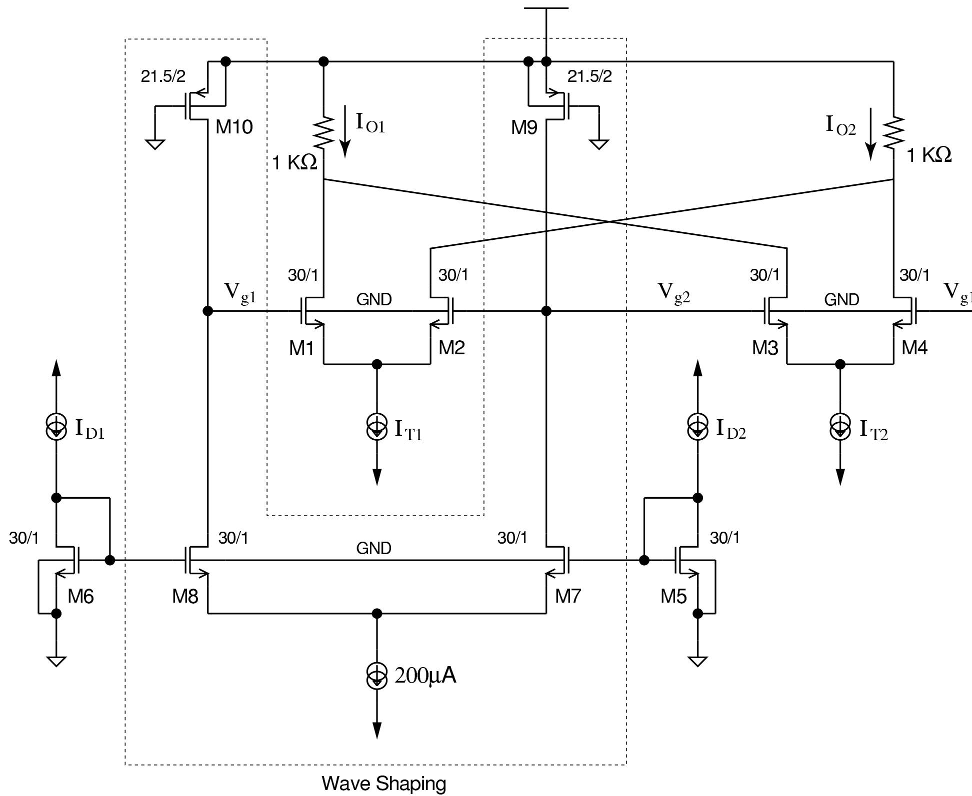


Figure 6.3: "Wave-shaping" superthreshold circuit.

range. This stage helps improve linearity close to the input rails, allowing a larger input range before the slope falls off, while having minimal effect on circuit performance at mid input ranges. Further understanding of distortion cancellation with concave and convex distortion in subthreshold has made it possible to remove this stage on the latest superthreshold circuit. Frequency performance in the final multiplier circuit is 22 % better than the original "wave-shaping" multiplier, and has better linearity. However, no silicon existed for this latest circuit when testing was done on the circuits.

The nonlinear error of the differential output of the wave-shaping superthreshold circuit is plotted in Figure 6.4. The measured nonlinearity is 2.53 % for the I_D input, and 0.05 % for the I_T input. This data is for the maximum range on the opposite inputs, at 100 % of the dynamic input range. Correlation in the output characteristic shape can be seen, but the amplitude correlation is not as strong.

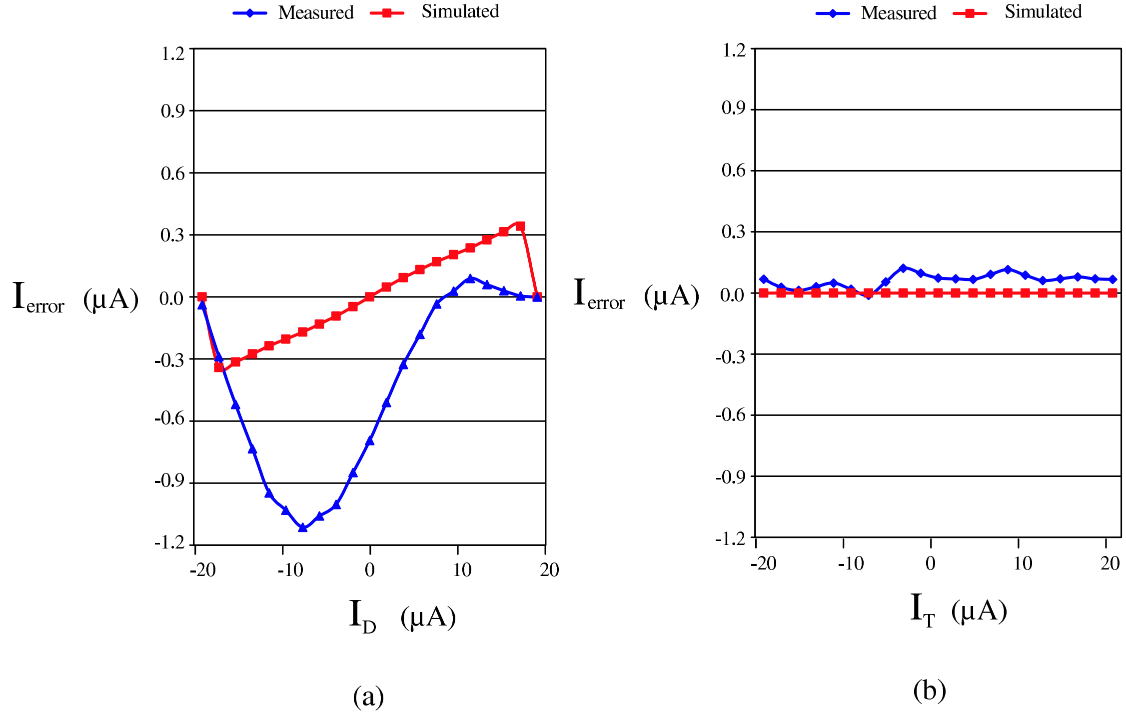


Figure 6.4: Test results: Superthreshold DC linearity.

Evaluating simulations on this version of the superthreshold circuit shows a sensitivity to process variation and device mismatch. At the WC1 corner (slow PMOS, fast NMOS), up to 4 % distortion can be expected from this circuit. Device mismatch simulation (like Monte Carlo) gives up to 5.7 % distortion. Reviewing the processing data, the wafer lot for this circuit ran towards the WC1 process corner. Combination of process variation with device mismatch could cause the level of nonlinearity shown in Figure 6.4.

A point to consider regarding simulating the superthreshold circuit is the capability of the models. The superthreshold circuit operates in the weak and moderate inversion regions, above and below the threshold voltage. Modeling the transition region between superthreshold and subthreshold is difficult. BSIM3 models handle this transition region using "smoothing functions" to smooth the transition from square-law drift current equations, to exponential diffusion current equations [6]. Inaccuracies in these models at this transition could cause weaker correlation between

simulation and silicon. Therefore, some of the multiplier behavior in this region may not be precisely simulated by the models.

The superthreshold circuit documented in Chapter 5 is much less sensitive to process variation, comparing it to the wave-shaping circuit. However, device mismatch sensitivities are similar to the wave-shaping circuit. In fact, with smaller channel lengths on the differential devices, device mismatch can cause up to 7.5 % distortion. The increase in device mismatch sensitivity is due to the smaller gate lengths of the differential pair devices (0.49 μm versus 1 μm). Device mismatch is one of the limitations of the Gilbert cell multiplier configuration. Good layout techniques can help minimize this effect.

Figure 6.5 is a plot of the physical layout of the shallow subthreshold circuit. Test results for the shallow subthreshold circuit showed minimal device mismatch distortion. To achieve this, common centroid layout was used for the differential pair devices. All devices are positioned with gates in the same direction to minimize implant variations. Also, symmetry is also used with close proximity of matching devices. All of these techniques help minimize device mismatch.

Table 6.1: Final Results: % NL error at full scale opposite input.

Circuit	I_D Test	I_D Simulation	I_T Test	I_T Simulation
Deep Sub		0.068		0.001
Shallow Sub	0.73	0.324	0.16	9e-5
Superthresh		0.611		5e-7
Wave shaping superthresh	2.53	0.854	0.05	0.00032

The final test results are tabulated in Table 6.1. Simulation results are at the typical process corner, with no device mismatch or test environment conditions. After removing test limitations, corner and device mismatch simulations can be run on each circuit that match the levels measured at test.

Figure 6.5: Shallow subthreshold circuit physical layout.

Chapter 7

Conclusions

Data presented in this thesis shows that it is possible to build CMOS current-mode multiplier circuits based on the bipolar Gilbert cell architecture. Biasing in the subthreshold region provides an opportunity to utilize exponential currents similar to bipolar technology. However, the complexities introduced by the different conduction mechanism between a MOSFET in subthreshold and a BJT, due to the different carrier injection mechanism, introduce many challenges and limitations when trying to linearize the CMOS multiplier. It is important to understand the behavior of the ideality factor, particularly with relation to the threshold voltage, V_t. Performance limitations also must be considered when operating in subthreshold, where multiplier operating frequency is limited by the slow charging of parasitic capacitances.

A key discovery in this thesis is the ability to cancel inherent distortion, by deliberately introducing distortion. This is seen in the shallow subthreshold and superthreshold circuits, where ideality factor mismatch (caused by device mismatch) is used to counter short channel effects and drift current distortion. This allows for multiplier operation at higher currents and smaller gate lengths, which improves AC performance (allowing bandwidths up to 330 Mhz). The main drawback of the high performance superthreshold circuit was the required introduction of input offset to help minimize the drift current distortion, which introduced DC output offset.

The low currents used in the deep subthreshold multiplier (5 nA) provides a multiplier solution for low power applications. These circuits offer high linearity at minimal power consumption.

Table 7.1 compares simulation and test results from the multiplier circuits presented in this thesis to other multiplier architectures found in literature. As mentioned in Chapter 6, poor correlation in NLerror between simulation and silicon exists for the deep sub threshold circuit due to difficulties measuring very small currents. Therefore, test data is not included for the deep sub threshold circuit. Bandwidth and power consumption is also not reported for any of the presented circuits due to test limitations. From the data presented in Table 7.1, it can be seen that performance with relation to linearity, % output range, operating frequency and power consumption is competitive with most other CMOS multiplier circuits. Although the Gilbert cell architecture is sensitive to device mismatch at processing, viable CMOS multiplier circuits can be built based on the techniques presented in this thesis.

Table 7.1: CMOS multiplier performance.

Author(S)/Multiplier	Year	% NL_{error}	% Output Range	BW (MH_Z)	Power (µW)
Deep Sub I_D (Sim)	2012	0.068	100	0.05	0.033
Deep Sub I_T (Sim)	2012	0.002	100	0.13	0.033
Shallow Sub I_D (Sim)	2012	0.324	100	8.3	6.6
Shallow Sub I_T (Sim)	2012	9e-5	100	11.4	6.6
Shallow Sub I_D (Silicon)	2012	0.73	100		
Shallow Sub I_T (Silicon)	2012	0.16	100		
Superthresh I_D (Sim)	2012	0.611	100	114	132
Superthresh I_T(Sim)	2012	5e-7	100	330	132
Superthresh I_D (Silicon)	2012	2.5	100		
Superthresh I_T (Silicon)	2012	0.05	100		
Liu and Chang	2004	1.0	5	0.33	3.14
Sakurai and Ismail	2004	1.0	75	30	>1000
Song and Kim	1995	0.45	40	30	>1000
Qin and Geiger	1987	0.5	75	0.5	>1000
Bult and Wallinga	1986	0.4	40	4	>1000
Wong, Salama and Kalyan	1986	3	100	1.6	>1000
Babanezhad and Ternes	1985	1.3	100	0.08	>1000
Soo and Meyer	1982	0.3	74	1	>1000

7.1 Suggestions for Further Research

- Develop mathematical models for the Gilbert cell in weak inversion, modeling contributions of drift and diffusion currents.

- Build strong inversion, active region multipliers with high bandwidth, by CMOS standards.

- More research into the relationship between the threshold voltage and the ideality factor in subthreshold.

- Use EKV models to simulate all circuits in an effort to get better correlation between simulation and final silicon.

- Apply the CMOS Gilbert cell multiplier presented in this thesis to communications and signal processing applications.

- Research ways of reducing device mismatch sensitivities in the Gilbert cell architecture.

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