A
Dissertation
On

Low Power Low Voltage Amplifier for removal of offset and Noise

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CERTIFICATE

This is certified that the dissertation entitled "**Low Power Low Voltage Amplifier for Removal of Offset and Noise**" is a bonafide work of **Priyank Agarwal (**University Roll No. 10/VLSI/2k10), a student at Delhi Technological University. This work was completed under my direct supervision and guidance and forms a part of the Master of Technology (VLSI Design and Embedded Systems) course and curriculum. He has completed his work with utmost sincerity and diligence.

The work embodied in this major project has not been submitted for the award of any other degree.

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ABSTRACT

The biggest challenge for analog designers in CMOS technology is to remove the offset and flicker noise. Ideally an amplifier should produce zero as output, when its differential input signal is zero. In practical at the output, some offset voltage or current has been present. Noise also has become a giant problem in CMOS technology when it is compared to its previous technologies like bipolar technology. Today noise is the most important issue for CMOS platform. Any undesirable signal which interferes with desired signal is called noise. Mostly it deteriorates the signal's inherent characteristics. It decides the minimum input signal value which can be accurately measured. There are a number of sources from where noise can originate.

When the signal magnitude is large compared to the system noise, then noise does not play any momentous role, but when signal of interest is comparable to the system noise, then it becomes really tedious to distinguish between noise due to devices and the signal of interest. Thus, offset and noise are major design constraint. Our aim in this thesis is to design a low power low voltage amplifier system with emphasis on offset and flicker noise removal circuitry, which operates using signals of low frequency and amplitude and provides a necessary gain without introducing significant noise from the devices, especially noises that are dominant in low frequency region.

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CHAPTER 1

INTRODUCTION

1.1 MOTIVATION:

In the last few decades, semiconductor materials and devices have grown rapidly with vast applications in the field of consumer electronics. They have completely changed the whole arena of the information communion. Ground breaking developments in the CMOS platform, has catalyzed this evolution.

Complementary Metal-Oxide Semiconductor (CMOS) technology provides enormous power savings and very high integration density for both digital and analog circuit designs. Initially, the analog performance of other cost-consuming technology platform like GaAs or bipolar process technology was estimated to be better than CMOS technology platform. But due to increased process robustness and constant downscaling, the performance of CMOS technology in analog design, has been outstandingly enhanced.

CMOS platform has well established advantages and its analog performance is similar to other processes. But it has some major drawbacks for analog/RF applications [1].

The first drawback and the major issue for concern is noise, as unfortunately CMOS is extremely noisy.

The second important issue is the dc offset which intrudes into the circuit due to component mismatch present due to lithographic error and other fabrication process imperfections.

Today, noise is the most important issue for CMOS platform. Any undesirable signal which interferes with desired signal is called noise. Mostly it deteriorates the signal's inherent characteristics. This is more when 1/f noise of CMOS technology is compare to bipolar technology. It decides the minimum input signal value which can be accurately measured. There are varieties of places from where noise can originate.

Root Mean Square (RMS) value of the noise increases with the square root of the bandwidth as shown in the expression 1-1. Hence higher bandwidth also makes noise removal a herculean task.

RMS Value of thermal noise voltage is given by:

$$E[V_{TN}] = \sqrt{4kTR\Delta f} \qquad \text{.....1.1}$$

Where $k =$ Boltzmann's constant

$T =$ Absolute temperature in Kelvin

$R =$ Resistance in ohms

$\Delta f =$ Bandwidth

When the signal magnitude is large compared to the system noise then noise does not plays any momentous role but when signal of interest is comparable to the system noise then it becomes really tedious to distinguish between noise due to devices and the signal of interest. Then the noise becomes major design constraint [2].

Signal to Noise Ratio (SNR) is very significant parameter for the circuit's small signal performance.

SNR is given as:

$$SNR = 20\log_{10}\frac{V_S^{RMS}}{V_N^{RMS}} \qquad \text{……..1.2}$$

Where V_S^{RMS} =RMS input signal voltage

V_N^{RMS} =RMS noise voltage

SNR calculates the margin (in dB) between the system noise and the input signal. Larger the value of SNR, lesser is the signal prone to be distorted by the noise.

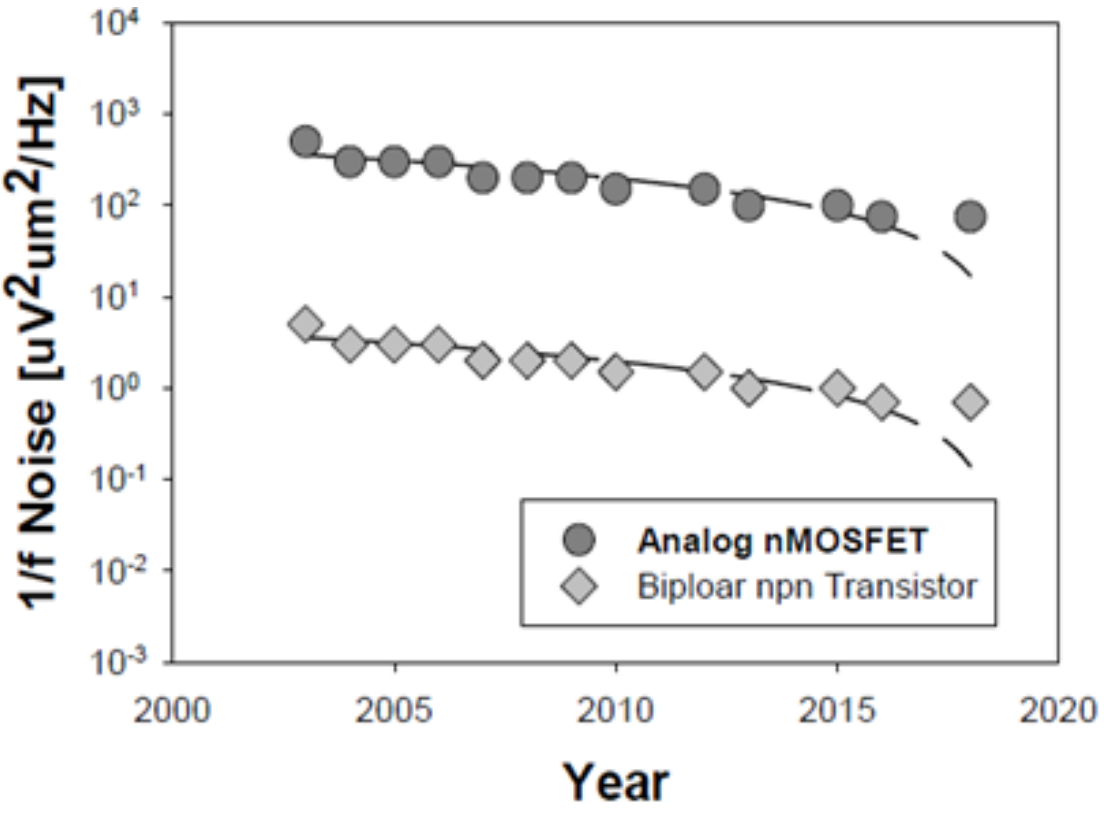

Fig1.1 International Technology Roadmap for Semiconductor for 1/f Noise [7]

The biggest challenge for analog designers in CMOS technology is flicker noise. This noise becomes a giant problem in CMOS technology when it is compared to its previous technologies like bipolar technology.

From the fig 1.1 where graph has been plotted between the variation in the flicker noise present in MOS and Bipolar technologies (plotted on the Y-axis) over the years (plotted on X-axis), it is clear that the MOS technology is more prone to flicker noise. The poor flicker noise parameter of CMOS technology makes this platform reluctant for analog designers. When the analog designer decides to design an analog circuit by using “noisy” CMOS technology, then many challenges are there in designing an analog circuit. So an optimum circuit has to be designed by using appropriate available design parameters in order to remove 1/f noise.

There exist several offset and 1/f noise reduction techniques in CMOS circuits including a convention method, enlarging of an active area of a MOSFET based on the 1/f noise property: inversely proportional to the active area [1].This method is quite simple to implement but loose a unique advantage of the technology downscaling, a performance enhancement (e.g., cut-off frequency enhancement) in a short-gate-length device.

Hence there are many other offset and flicker noise removal techniques which are very efficient in removal of low frequency noise and offset. But all have some loopholes and have some trade-offs.

Our aim in this thesis is to design a complete low power low voltage amplifier system with emphasis on offset and flicker noise removal circuitry, which operates at the signals of low frequency and amplitude and provides a necessary gain.

1.2 OBJECTIVE

1. To study origin of offset and noise in devices.
2. To study types of offset and noise.
3. To study existing technique for the removal of offset and flicker noise.
4. To observe the drawbacks of existing technique.
5. To design a proposed low power low voltage amplifier for removal of offset and noise.

1.3 METHODOLOGY AND TOOLS USED

CADENCE VIRTUOSO

a. Virtuoso Schematic Editor.
b. Spectre Simulator.
c. Virtuoso Layout Editor .
d. Assura.

METHODOLOGY AND TOOLS USED

Cadence Design tools is an EDA software that is used extensively in designing and manufacturing semiconductor devices and circuits for various fields. They are used in different design and verification process like Custom IC design, logic design, design and verification of system, verification at functional level, digital implementation, design of RF circuits and PCB, IC packaging and Sip Design. For a designer the Custom IC Design Tools is an essential tool of the Cadence design Systems as it includes the whole process flow starting from schematic entry up to post layout simulation. The Table 1 below mentions the tool used for the given ASIC process:

PROCESS	TOOL
Schematic Entry	Cadence Virtuoso Schematic Editor
Circuit simulation	Cadence Virtuoso Analog Design Environment
Full custom layout	Cadence Virtuoso Layout Suite
Physical verification	Cadence Assura Physical Verification
Extraction	Cadence Assura RCX
Post layout simulation	Cadence Virtuoso Analog Design Environment

Table 1: ASIC Design Flow and the Cadence Tools used for them.

The designing can be done for analog, digital, mixed-signal, or RF design and results are analyzed. The sections to follow will have explanation of tools.

1.3.1 CADENCE VIRTUOSO SCHEMATIC EDITOR

Cadence Virtuoso Schematic Editor provide users the advantage of easy and fast design entry .The well-defined component libraries and wire routing are further useful in RTL designing and gate level designing.

The tool can work for hierarchical designs and ensure the connectivity in the design.

1.3.2 CADENCE VIRTUOSO ANALOG DESIGN ENVIRONMENT

For Virtuoso platform the ADE allows for advanced design and simulation environment. It also gives designer the liberty to do parasitic extraction along with

comparison flow [29].The verification done by Virtuoso ADE is highly accurate and set standards [29].

1.3.3 CADENCE VIRTUOSO LAYOUT SUITE

This is a physical layout tool that supports custom, analog, digital as well as mixed signal design at the device, cell, and block levels.

1.3.4 CADENCE ASSURA PHYSICAL VERIFICATION

After the physical layout has been done, Cadence Assura Physical Verification Tool verifiers the layout against DRC, LVS , RC Extraction and etc. It allows schematic-to-layout cross-checking with scope correct, extract, and compare errors [29].

1.3.5 CADENCE VIRTUOSO

Following are the feature of simulator tool used for research work

- Full custom IC design tool working in ICFB environment
- Supports 0.18µ CMOS technology

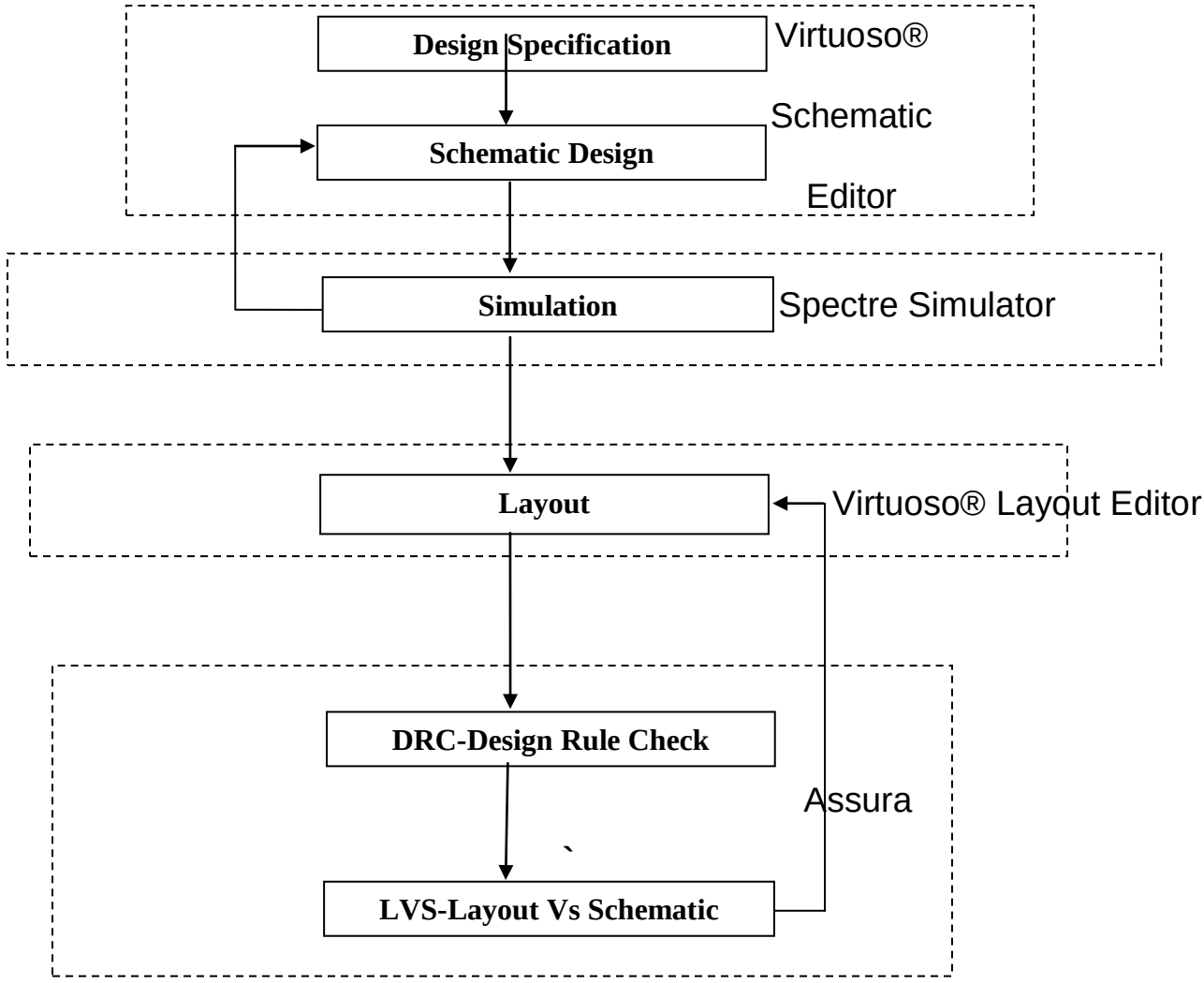

Fig1.2 Custom IC Design Flow [32]

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The thesis has been divided into six chapters:

CHAPTER 1 gives the brief introduction of the Offset and Noise and brief overview of the CADENCE Virtuoso tool.

CHAPTER 2 presents various offset and noise issues present in the MOS devices and also modeling of the noise present in MOS has been done. Also various methods of removal of the offset and noises have also been given.

CHAPTER 3 gives the review of work and also specifies the need for development of the new proposed low power low voltage amplifier system.

CHAPTER 4 proposes theoretical analysis of each and every module of the proposed system and also deals with the mathematical design analysis of each and every module of the new low power low voltage amplifier system.

CHAPTER 5 gives various responses of each module and also responses of overall design have been given.

CHAPTER 6 provides the conclusion for the entire work.

CHAPTER 2

OFFSET AND NOISE

2.1 OFFSET

Ideally an amplifier should produce zero as output, when its differential input signal is zero. In practical at the output, some offset voltage or current has been present. DC offset can be defined as the subtraction of the dc voltages across the two output terminal keeping the two input terminals grounded [30]. The DC offset produced by the amplifier can lead to

1. Loss of information when the input is comparable to the generated offset.

2. Can lead to saturation of transistors .

The major cause of DC offset is the mismatching of devices.

2.1.1 WHAT IS DEVICE MISMATCH

Manufacturing variations results in process and device parameter variations from, wafer to wafer, and device to device and can be categorized as systematic or random[9]. A systematic shift is injected in the device characteristics and circuit performance due to such variations [14].

Mismatching take the form of offsets voltages in amplifiers; and limit the signal resolution in circuits such as comparators and analog-to-digital converters [16]. Degradation of the temperature behavior and low precision of voltage and current reference often occur as result of variations in device parameter values [16]. Also, matching between transistors directly impacts the achievable accuracy in digital-to-analog converters [10].

The offset that we have described here is Static offset voltage.

Static offset voltage:

In case of differential amplifier the effect of mismatch is most dominantly reflected by the generation of offset voltage and offset current. As defined earlier that offset voltage is a result of current that flows into the differential input pair even when no input is applied.

The dc behavior of an amplifier with mismatch is identical to an ideal amplifier without mismatches with an offset voltage source in series and a current source in parallel [28].

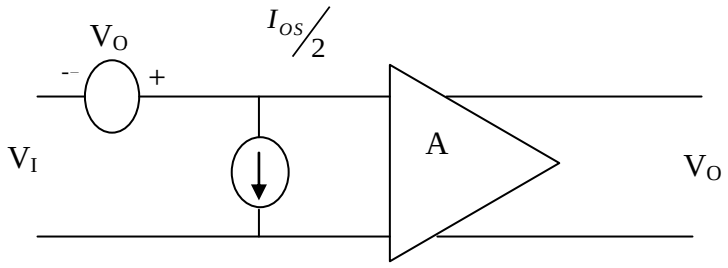

FIG2.1: Modeling of offset voltage in an ideal amplifier [28]

The offset voltage V_{OS} can be evaluated to approximation from equation (2.1) given below:

$$V_{OS} = \Delta V_T + \frac{(V_{GS} - V_T)}{2}\left(-\frac{\Delta R_L}{R_L} - \frac{\Delta(W/L)}{(W/L)}\right) \qquad (2.1)$$

Where V_{OS} is the offset voltage inherent in the amplifier,

ΔV_T indicates the variations in threshold voltage,

(V_{GS}-V_T) is the over drive voltage and

$\left(\frac{\Delta R_L}{R_L}\right)$ and $\left(\frac{\Delta(W/L)}{(W/L)}\right)$ are the changes in the load resistance and the aspect ratio respectively.

So it can be derived that the changes in the threshold voltage directly results in offset generation while changes in overdrive voltage and aspect ratio also lead to offset generation.

The threshold voltage differences ΔV_T and the current factor differences $\Delta\beta$ where $\beta \equiv \mu C_{ox}\left(W \diagup L\right)$ are the main causes of the V_{DS} and V_{GS} mismatch for matched pair MOS transistors [14]. These random differences have a normal distribution with zero mean and a variance dependent on device area W, L [14].

$$\sigma^2(\Delta V_T) = \frac{A_{VT}^2}{W.L} \tag{2.2}$$

$$\left(\frac{\sigma^2(\Delta\beta)}{\beta}\right)^2 = \frac{A_\beta^2}{W.L} \tag{2.3}$$

Where W is the poly silicon width and L is the gate length, and the proportionality constants A_{VT} and A_β are technology dependent [14].

2.2 NOISE:

Any undesired signal which interferes with the desired signal is called Noise. It is a phenomenon caused by the small fluctuations of analog signal within the component themselves. Noise results from the fact that electric charge is not continuous but the result of quantized behavior. Noise is generated through processes such as random motion ,trapping and random arrival of charge carriers. The thing which makes noise

most important is that it sets the lower limit on the capability of any particular device or circuit to reliably detect small signals. Noise signals are generally random with random phase and no known polarity. Because of this it is conveniently expressed in rms value. Noise is classified mainly in to two main categories:

1. Artificial Noise: It is caused due to various noise sources present in the environment we can also called it as a external noise. Examples of Artificial noise noise are crosstalk between adjacent circuits, hum from Dc power supplies, electrostatic and magnetic coupling between circuit and ac power line and so on.It is removed by adequate shielding, filtering or by changing the layout of circuit component.

2. Intrinsic Noise: It is generated in the device or circuit itself by the device physical related noise phenomenon. Here we will consider it for the MOSFET.

The various types of Intrinsic Noise are:

1. Thermal Noise: Thermal noise is due to the random thermal motion of electron and is independent of the dc current flowing in the component. It is usually measured as a random voltage across a resistor. It is due to the random collision of carriers with the atom in the material[2].In a resistor of value R it can be expressed as:

RMS Value of thermal noise voltage is given by:

$$E[V_{TN}] = \sqrt{4kTR\Delta f} \qquad \text{……2.4}$$

Where k =Boltzmann's constant

T = Absolute temperature in Kelvin

R = Resistance in ohm

Δf = Band width.

2. Flicker Noise: It is generally referred as 1/f Noise. As signifying by his name, noise is dominated by the frequencies which exist in the low frequency region. It is mostly due to generation and recombination of carriers. It is associated with the carrier traps which are created by the imperfection and crystal defects in interfaces and junction between the materials. They capture and release energy in random fashion and with random time constant which give rise to noise signals with energy concentrated at low frequency. The general consensus is that the 1/f noise is due to conductivity fluctuation,1/f noise in semiconductor is taken as an instantaneous change in the conductivity of material either through number or through mobility fluctuation.[3]

2.2.1 MODELING OF NOISE COMPONENTS IN CMOS

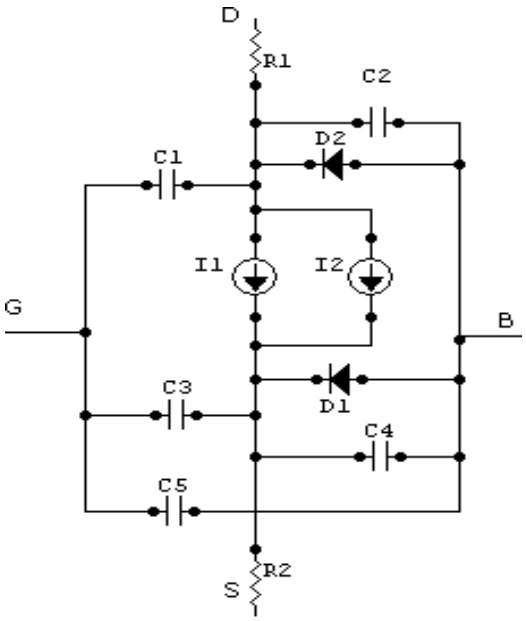

Fig 2.2 Complete Large-Signal Model for the MOS Transistor Including Noise[4]

Where

D=Drain, G=Gate, B=Body, S=Substrate

D1, D2 = pn junction formed at the source -substrate and drain-substrate junctions respectively.

R1, R2 = ohmic resistance of drain and source respectively.

C2, C4 = capacitance b/w drain-substrate and source-substrate respectively.

C1, C3, C5 = capacitance b/w drain-gate, source-gate and gate-body respectively.

I1= Drain current through the MOS.

I2= Current source modeling the noise present in the MOS.

In the large signal model current source I2 in parallel with the I1.I2 represents noise present in the MOS device.

In [22,28] it has been shown that this I2 comprises of:

1. Thermal Noise.
2. Flicker Noise.

Thermal noise is function of random thermal motion of the charge carriers (mostly electrons) [4].

$$i_n^2 = \left[\frac{8kTg_m(1+\eta)}{3}\right]\Delta f \qquad \text{.....2.5}$$

Flicker Noise has a typical form which can be given by [4].

$$i_n^2 = \left[\frac{(kF)I_D}{fC_{OX}L^2}\right]\Delta f \qquad \text{.....2.6}$$

Hence the overall mean-square current noise is given as [4].

$$i_n^2 = \left[\frac{8kTg_m(1+\eta)}{3} + \frac{(kF)I_D}{fC_{OX}L^2}\right]\Delta f \qquad \text{.....2.7}$$

Where

Δf = a small bandwidth (typically $1\ Hz$) at a frequency f .

$\eta = g_{mbs} / g_m$

K = Boltzmann's constant

T = temperature (Kelvin)

g_m = small-signal transconductance from gate to channel

KF = flicker noise coefficient (F-A)

f = frequency (Hz)

The equivalent input mean-square voltage noise reflects mean–square current noise to the gate of the MOS components [4]:

$$e_n^2 = \frac{i_n^2}{g_m^2} = \left[\frac{8kT\ (1+\eta)}{3g_m} + \frac{kF}{2fC_{OX}WL\ K'} \right] \Delta f\ (V^2) \qquad \text{.....2.8}$$

Our aim is to remove flicker noise and as flicker noise is dominant source below 100 KHz [4] so equivalent input mean square voltage noise spectral density is given by:

$$e_{eq}^2 = \left[\frac{kF}{2fC_{OX}WL\ K'} \right] \Delta f \qquad \text{.....2.9}$$

Input voltage noise spectral density is [4]:

$$e_n^2 = \frac{e_{eq}^2}{\Delta f} = \frac{kF}{2fC_{ox}WLK'} = \frac{B}{fWL} \left(V^2 / Hz \right) \qquad \text{.....2.10}$$

B= constant for n-channel and p–channel device for given process.

2.3 METHODS TO REDUCE NOISE COMPONENTS IN CMOS

As can be seen from the equation 2.8 that the noise of the MOSFET mainly consist of 2 parts.

These are

1. Thermal Noise
2. Flicker Noise

Removal of thermal noise can be achieved by increasing the transconductance g_m. It is clear from the equation 2.2.4 that thermal noise is inversely proportional to small signal transconductance, which can be achieved by large dc current or large W/L ratios.

$$g_m = \sqrt{2K'(W/L)|I_D|}\,. \qquad \text{.....2.11}$$

There are three approaches of minimizing flicker noise of the CMOS device.

1. First is proper selection of circuit topology and transistors i.e. NMOS v/s PMOS, Proper control on dc currents and aspect ratios of the transistors also minimize flicker noise. Topology of the circuit defines the manner in which various components of the circuits are connected. Components can be connected either in series topology, parallel topology or any other topology. The one principle that is key in minimizing noise is to make the first stage gain as high as possible [4]. Compared to all these methods, selection of transistors is much easy. Empirically PMOS transistors have two to five times less 1/f noise [4]. Hence input stage of the differential amplifier should have PMOS as the source coupled transistors.

2. Second method for the minimization of flicker noise is replacing the MOSFETs by BJTs. Because the 1/f noise of BJTs is lower than the 1/f noise of MOSFETs, the corner frequency (the intersection of the 1/f and the thermal noise) is lower for BJTs [4]. Therefore in the circuit applications where low frequency noise (frequency<1 KHz) is important, BJTs should be preferred than MOSFETs. But the disadvantage of the BJTs are they are very much power hungry and occupy large area.

3. Most popular method for noise removal is to use external means. Further details of external means will be discussed in next chapter.

CHAPTER 3

LITERATURE SURVEY

In reality besides the scaled down digital processes we always need analog processes to perform a variety of critical tasks such as to connect the digital with external world. one such function is high precision amplification with low power consumption. As we know that high precision CMOS amplifiers are always limited by offset and 1/f noise. Basically there are two techniques Auto zero Technique and chopper stabilization technique(CHS) which are used in low frequency offset and noise removal in CMOS technology.

3.1 AUTO ZERO TECHNIQUE

The basic principal behind the auto zero technique is to sample the unwanted quantity (noise and offset) and then subtract it from the instantaneous value of the signal either at the input or output. If the offset noise is only present then it will get cancelled with time.

The auto zero process consist of two phases:

1. Sampling phase (ϕ1)
2. Signal processing phase (ϕ2)

In the sampling phase(ϕ1) the output and input of the amplifier are shorted together so that the offset voltage and the input noise is sampled and stored in capacitor in capacitor c. During the sampling phase the amplifier is disconnected from the signal path and its input are short circuited as shown in fig3.1.Thus the input is fixed to a common mode voltage and the offset is nulled by using a feed back.

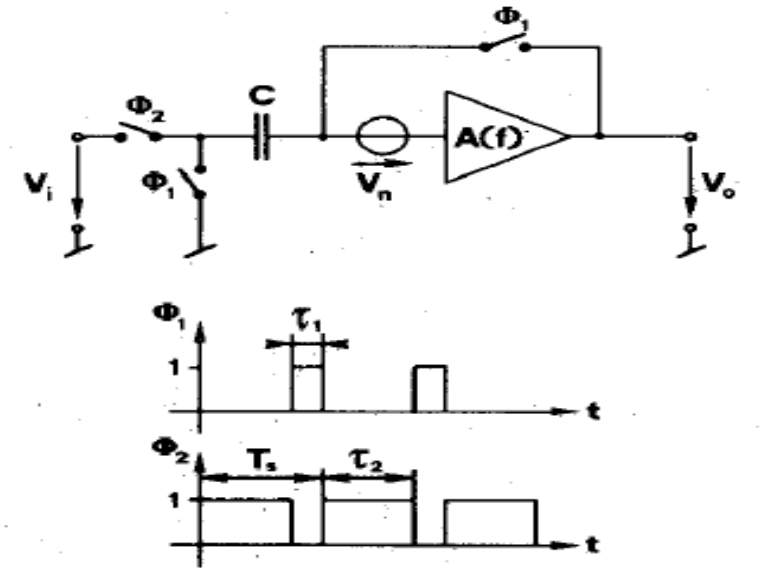

Fig3.1 Auto zero amplification principle [6].

In the second phase (ϕ2) which is signal processing phase the amplifier is connected to signal path and the input terminal is connected to amplifier. Thus the Noise sampled is subtracted from the instantaneous noise of the amplifier.

The offset cancellation is limit by the charge injection due to auto zero switch. In addition to basic high pass filtering action , the wide band noise is sampled down to base band increasing the resultant in band power spectral density.

The efficiency of Auto zero technique for low frequency noise reduction will strongly depend on the correlation between the noise sample and the instantaneous value of noise from which this sample is subtracted.[6]

Here if the noise is low frequency random noise it will get reduced at low frequency but at the cost of an increase in noise floor due to aliasing of wide band noise inherent to sampling process. The alternative to auto zero technique is chopper stabilization technique which is discussed below.

3.2 CHOPPER STABLIZATION TECHNIQUE:

The chopper stabilization technique is widely used for reducing the dc offset voltage and low frequency noise that usually degrades the performance.

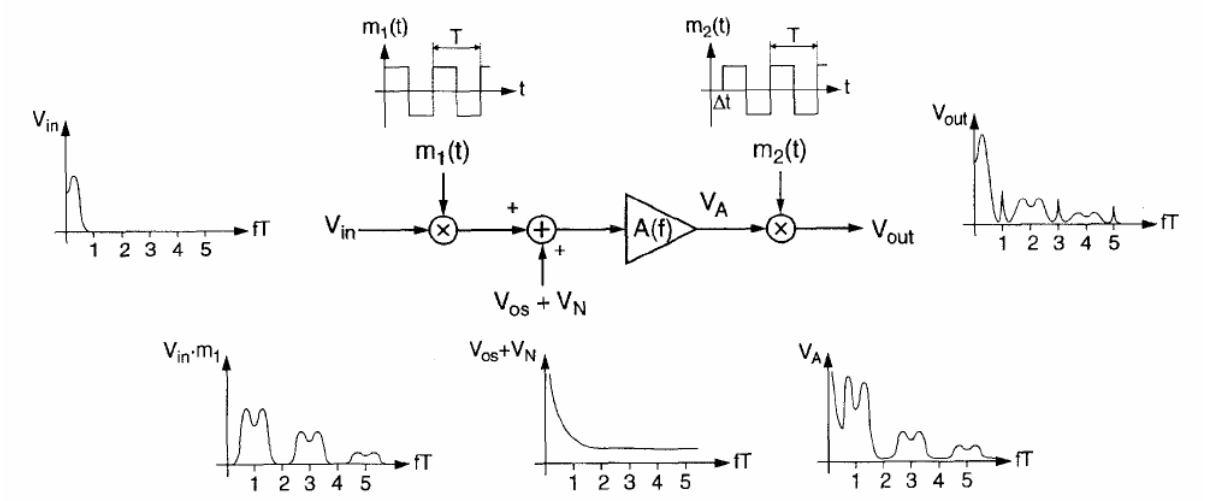

Fig3.2 chopper stabilization principle [9].

The principle of chopper stabilization technique applies modulation to convert the signal in to high frequency signal where there is no 1/f noise and then demodulate it back to base band after amplification. The principle is illustrated in the figure 3.2.

Suppose the signal is band limited to half of the chopper frequency so that no aliasing occurs and the amplifier is ideal with no noise and offset.Here the input will get multiplied by the carrier signal which would be a square wave of time period $T=1/F_{chop}$ after this the signal is transposed to odd frequency harmonic of the fundamental signal [9].

The signal is then passed through a amplifier the output of which is passed through a demodulator where it gets demodulated to its original base band signal.

Consider the input of chopper amplifier is a dc signal Vin after passing it through a modulator the signal at the output has is a square wave of time period T and amplitude Vin.It is then passed through a amplifier of gain Ao*Vin. Thus the output of amplifier has amplitude Ao*Vin which is then demodulated to remove the offset and noise and the signal after demodulation is a DC signal of value Ao*Vin.

Since we can see that here noise and offset are modulated only once they are transferred to odd harmonics of output chopping square wave ,leaving the amplifier ideally without any offset and noise [9].

The problem of chopper stabilization technique is the generation of parasitic offset due to first modulation. Increased complexity is also a significant demerit. For the cases where bandwidth is greater compared to chopping frequency dynamics in the frequency domain get more complex.

Hence in order to remove the drawbacks of existing techniques, a novel method of designing of low power low voltage amplifier is discussed in the next chapter.

CHAPTER – 4

DESIGN OF INDIVIDUAL BLOCKS

The low power low voltage amplifier system aims in removing flicker noise and offset from the complete low power amplifier system is shown below

Fig. 4.1 Block Diagram of Proposed low Power low voltage Amplifier System

The five basic blocks which are used in the design of proposed low power low voltage amplifier system are:

1) Preamplifier
2) Modulator
3) Gain Stage
4) Demodulator
5) Low pass Filter

The first block of the low power amplifier system is preamplifier. The main objective of a preamplifier system is to provide low input noise response along with the gain. The preamplifier strengthens the input signal without introducing extra noise in the signal, making it compatible for modulation operation.

Output of the preamplifier is applied to the modulator stage. It modulates low frequency signal by the high frequency carrier signal (10 KHz). Thus the modulator stage shifts low frequency signal in to high frequency signal and removes the possibility of flicker noise which is present mostly at low frequency.

The major gain stage that we have applied is composite cascode opamp it should have high gain. It should also be immune to external disturbances i.e. it should have good Power Supply Rejection Ratio (PSRR).

The output of gain stage (composite cascode) which is the amplified signal at high frequency is passed through the demodulator stage which demodulates the signal with same carrier frequency by which it is amplified by the modulator. Now the demodulated signal is the low frequency signal. The output of the demodulator stage is passed through the low pass filter which removes the noise and offset which are still at high frequency. Low pass filtering action removes the unwanted signal. Individual blocks of the proposed design are discussed from below:

4.1 PREAMPLIFIER

Preamplifier is the first stage of the proposed design. The main objective of a preamplifier system is to provide low input noise response along with the gain . The two stage op-amps are best suited for preamplifier design. They have low noise response and they also have high gain. The only drawback with two stage amplifiers is that its speed is least. But this drawback is compensated, as the applied input signal is itself of very low frequency. Hence high speed is not required for the preamplifier application.

At the input of preamplifier a low frequency signal is applied.The design of preamplifier is designed to have low input noise response. As we know that holes have lesser mobility as compare to electron and the majority charge carrier in pmos are holes that's why pMOS has intrinsically lesser flicker noise as compared to nMOS.Because of low mobility, there is less captures and release in pMOS devices as compared to nMOS. So the circuit designed using pMOS as input have less input noise response. Empirically, pMOS transistors have about two to five times less 1/f noise than nMOS transistors [4].

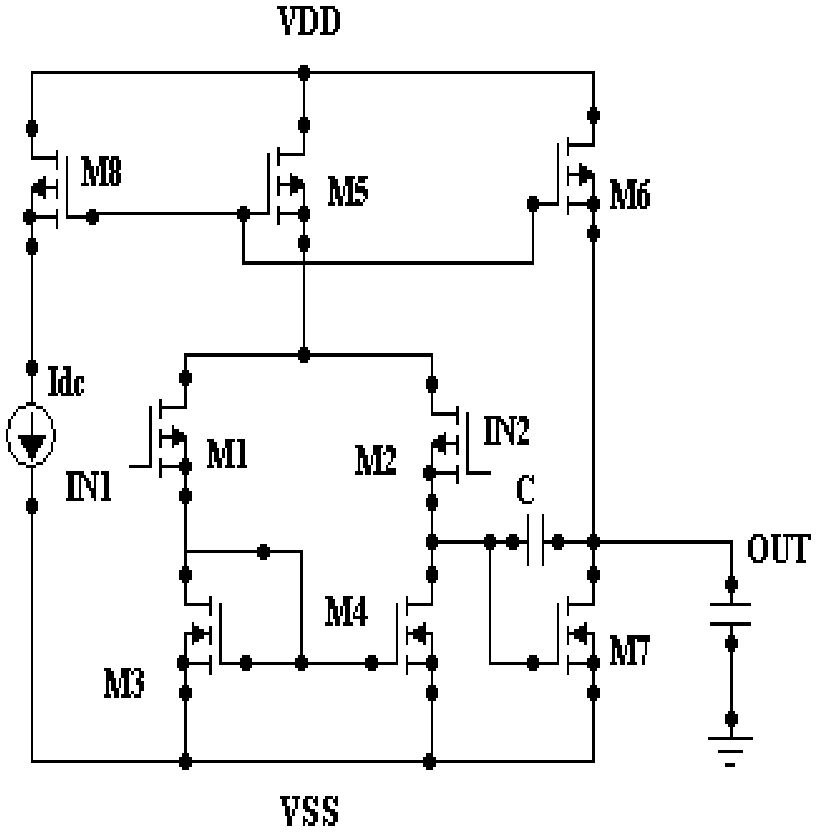

Fig. 4.1.1 Circuit Diagram of Two Stage Preamplifier

Therefore we have designed the preamplifier using pMOS transistors. Inputs IN1 and IN2 are applied at the PMOS transistors M1 and M2. M1 and M2 form differential

pair. NMOS transistors M3 and M4 form current mirror sink. M5, M6 and M8 are the PMOS transistors. M5 and M8 are used for biasing pupose. M6 and M7 form output stage of the amplifier. Capacitor C is compensation capacitor used for stablity purpose.

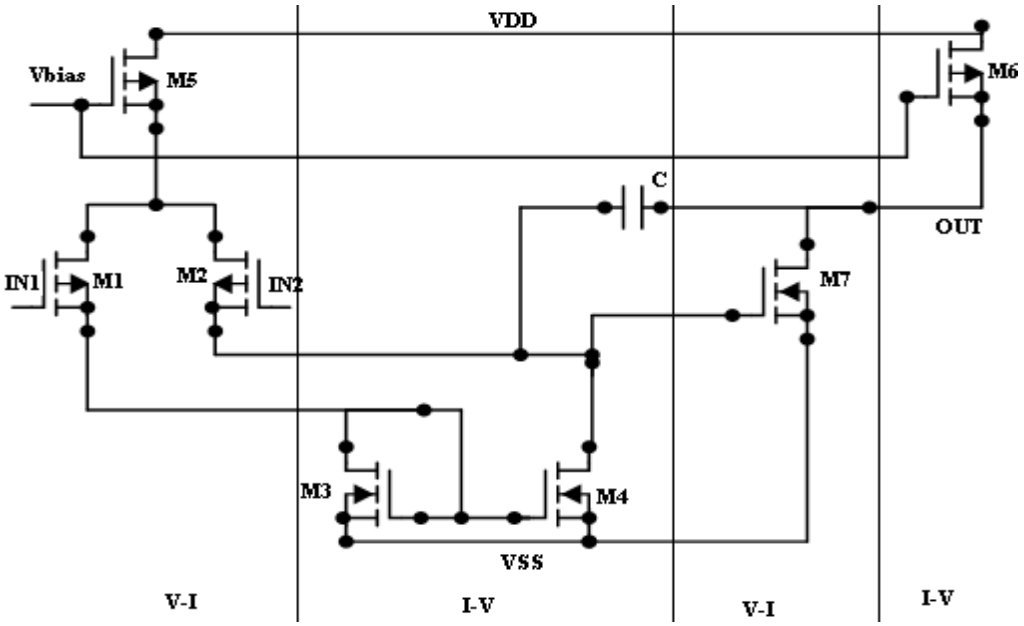

Fig. 4.1.2 Two-Stage PMOS Op-Amp Broken into V-I and I-V Stages [4].

The amplifier generally consist of cascade of voltage to current or current to voltage converting stages.A voltage to current stage is called transconduactance stage and a current to voltage stage is called load stage.The preamplifier that we have used is called two stage op-amp because it consists of series connection of voltage to current and current to voltage stages as shown in fig. 4.2.

The first stage consists of PMOS differential amplifier formed by M1 and M2, converting differential input voltage into differential current. NMOS current mirror sink M3 and M4 further convert these differential currents into differential voltages.

M7 is the common source NMOS ,forms the second stage, which converts the second stage input voltage into current.A current-source load PMOS M6 acts as a load for nMOS M7, hence converting current to output voltage.

Because of the CMOS amplifiers the intrinsic noise penetrates in to the signal.These CMOS amplifiers provide desirable gain but at the cost of distortion in the signal. These CMOS amplifiers are designed through transistors, which are original source of all type of intrinsic noises.

When the preamplifier works on a signal of low frequency the ficker noise distorts the signal.Thus in order to remove flicker noise from signal it should be modulated. At high frequency flicker noise is absent and only thermal noise is present, which can be easily removed by the methods discussed in section 2.3.

DESIGN OF PREAMPLIFIER

4.1.1STEPS OF DESIGNING TWO STAGE OPERATIONAL AMPLIFIERS[4].

Step 1:

The first step towards designing the opamp is to select an optimal value of compensation capacitor C_C depending on the capacitance of load C_L.

For getting the value of phase margin approximately around 60^0 the pole should be placed 2.2 times higher than the GB [4].

$$C_C > (2.2/10)C_L \qquad \text{.....(4.1.1)}$$

Step 2:

Based on slew rate requirement the biasing current I_{Bais} is calculated .The value of I_{Bais} is changed in case the design does not meet the required specification.

$$I_5 = SR \times (C_C) \qquad \text{……..(4.1.2)}$$

Step 3:

The positive input–common mode range determines the value of aspect ratio of transistor Q_3 .The value is calculated for the transistor to be in saturation.

$$S_3 = \frac{I_5}{(K_3^{'})[V_{DD} - V_{in}(\max) - |V_{T03}|(\max) + V_{T1}(\min)]^2} \qquad \text{……...(4.1.3)}$$

.

As Q_3 and Q_4 together form a current mirror load thus

$(W/L)_3=(W/L)_4$

Step 4:

The transconductance of the differential input transistors can be estimated from the values of compensation capacitor and gain bandwidth product.

$$g_{m1} \approx GB(C_C) \qquad (4.1.4)$$

The aspect ratio of Q_1 can then be calculated from using the following relation:

$$S_1 = \frac{g_{m1}^2}{K_1^{'}(I_5)} \qquad (4.1.5)$$

For balanced input the differential configuration should have $(W/L)_1=(W/L)_2$.

Step 5:

The aspect ratio of the transistor Q_5 can be estimated using the specification given for the negative input common mode range which is given as:

$$V_{DS5} = V_{in}(\min) - V_{SS} - \left(\frac{I_5}{\beta_1}\right)^{\frac{1}{2}} - V_{T1}(\max) \quad (4.1.6)$$

From this relation, V_{DSS}(sat) can be evaluated. Using this value of V_{DSS} and $I_{5,}$ $(W/L)_5$ is calculated as :

$$S_5 = S_8 = \frac{2(I_5)}{K_5^{'}(V_{DS5})^2} \quad (4.1.7)$$

Hence the design of the first stage that is excluding the output stage is complete

Step 6:

Based on the relationship given by equation (4.1.8), the transconductance of Q_6, g_{m6} is obtained from the following relationship:

$$p_2 = \frac{-gm_6}{C_L} \quad (4.1.8)$$

$$g_{m6} = 2.2g_{m2}(C_L/C_C) \quad (4.1.9)$$

To achieve the proper mirroring of the first stage current mirror load , V_{SG4} should be equal to V_{SG6} thus,

$$S_6 = S_4 \frac{g_{m6}}{g_{m4}} \quad (4.1.10)$$

Since the values of S_6 and g_{m6} are known therefore the value of I_6 can be easily calculated

$$I_6 = \frac{g_{m6}^2}{2K_6^{'}S_6} \quad (4.1.11)$$

The balance equation is used to calculate the device size of Q_7.

$$S_7 = S_5\left(\frac{I_6}{I_5}\right) \qquad (4.1.12)$$

By using the above steps we have got the following aspect ratios.

Transistor	Aspect Ratio
M1	$600\mu/1\mu$
$M2$	$600\mu/1\mu$
$M3$	$2\mu/1\mu$
$M4$	$2\mu/1\mu$
$M5$	$30\mu/1\mu$
$M6$	$44\mu/1\mu$
$M7$	$10\mu/1\mu$
$M8$	$30\mu/1\mu$

Table 4.1 Aspect ratio of NMOS and PMOS used.

Hence in order to convert the signal of low frequency into the signal of high frequency, modulators are needed. Hence the next stage of low power low voltage amplifier syatem is amplitude modulator which converts low frequency signal in to high frequency signal.

4.2 MODULATOR /DEMODULATOR

Amplitude modulator is simply a multiplier. It multiplies the input signal with high frequency carrier signal to get modulated signal which has very high frequency.

Suppose m(t) is the applied input signal and c(t) is a high frequency carrier signal. Modulator simply multiplies both these signal to give a modulated signal with a very high frequency which is comparable to that of carrier frequency.

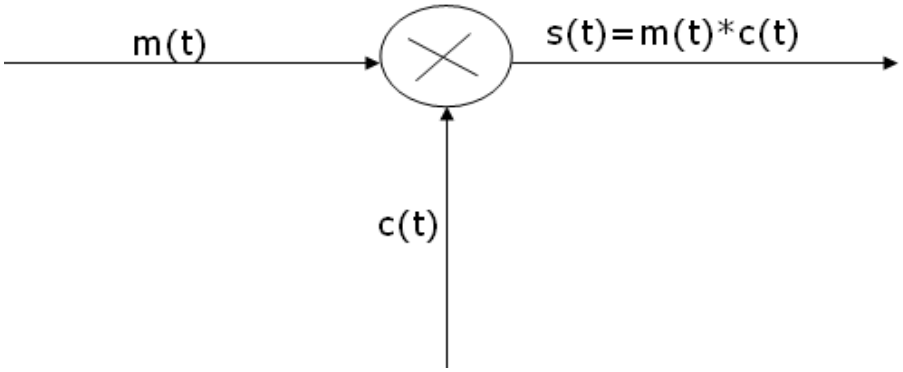

Fig.4.2.1 Logical Block of Modulator/Demodulator

The various waveforms in the multiplier are shown below:

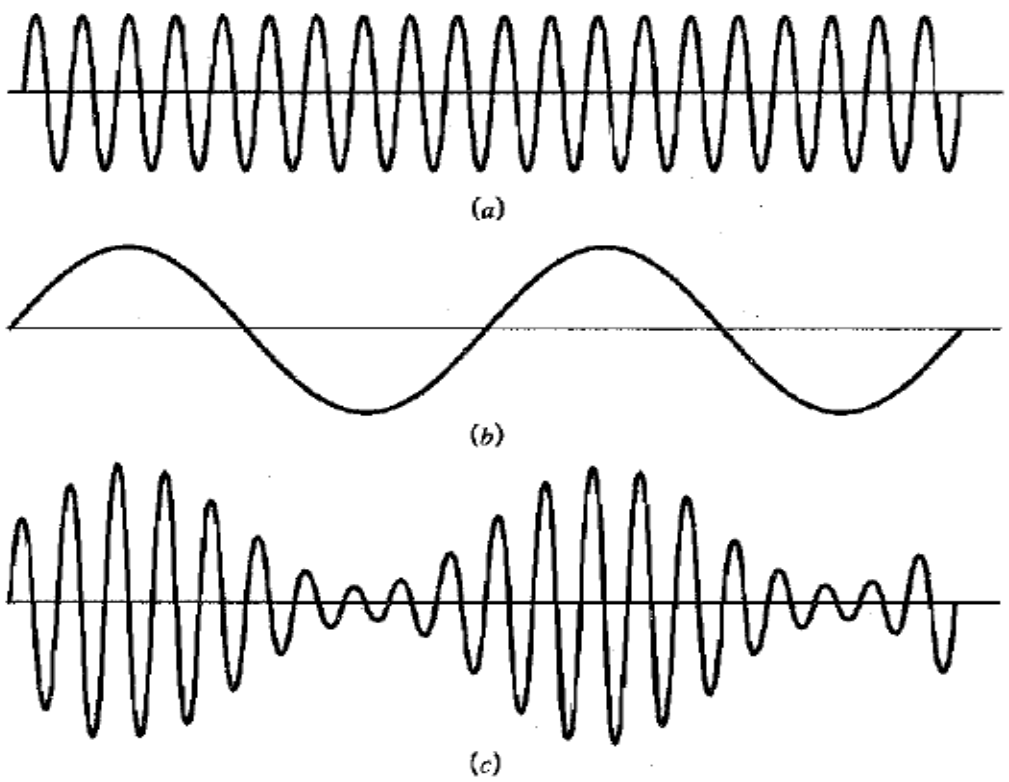

Fig. 4.2.2 Various Waveforms. (a) Carrier Wave c(t). (b) Input Signal m(t). (c) Modulated Signal s(t) [21].

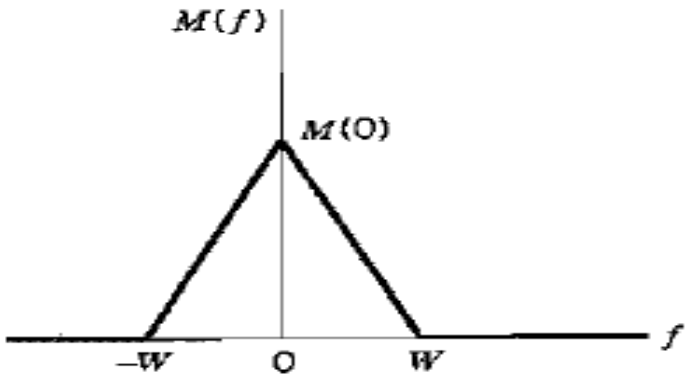

Fig. 4.2.3 Spectrum of Baseband Signal M(f) [21].

In order to show the frequency shifting propery of the modulator consider a low frequency signal m(t). It is being modulated by the high frequency signal

$$c(t) = A_c \cos(2\pi f_c t) \qquad \text{.....4.2.1}$$

Where A_c = amplitude of the carrier signal.

f_c = carrier frequency

The modulated signal is described by:

$$s(t)=A_C[1+k_a m(t)]\cos(2\pi f_C t) \qquad \text{.....4.2.2}$$

where k_a = amplitude sensitivity of the modulator. It is responsible for the generation of s(t).

Two conditions are necessary for modulation:

a. $|k_a m(t)| < 1$ for all t.

b. $f_c >> W$ where W is bandwidth of the signal m(t).

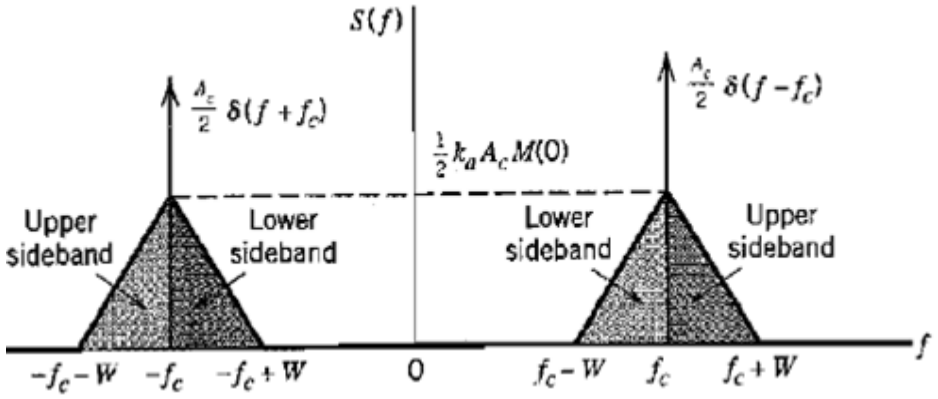

Fig. 4.2.4 Spectrum of AM Wave S(f) [21].

Taking fourier transform of the modulated signal s(t) gives:

$$S(f)=(A_C/2)[\delta(f-f_C)+\delta(f+f_C)]+(k_a A_c/2)[M(f-f_C)+M(f+f_C)] \qquad \text{…4.2.3}$$

Hence from figure 4.2.3 and 4.2.4 it is clear that by modulation input signal of low frequency is translated to high frequency. Frequency spectrum of M(f) is translated to the frequency f_c (as shown in equation 4.2.3) which is much larger than W (bandwidth of the signal).

Simliarly demodulator is also a multiplier which multiplies the modualted signal s(t) with same carrier signal c(t) . The resultant is an orignal baseband signal as was explained in [21].

Hence modulator/demodulator used in this proposed design is an analog CMOS multiplier. They perform linear multiplication of the two applied signals a and b to yield

$$y=k*a*b \qquad \text{.....4.2.4}$$

Where k=Multiplication constant with suitable dimension [13].

DESIGN OF MODULATOR/DEMODULATOR

The multiplier which we have used is basically a four quadrant multiplier. Programmable transconductance components are used here to realize the multiplier.

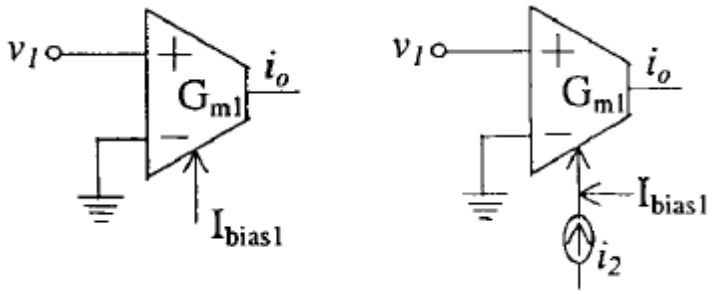

Fig. 4.2.5 Multiplication Operation Using Programmable Transconductor (a) Without i2, (b) Using i2 [13]

Fig 4.2.5(a) shows conceptual transconductance amplifier. Output current i_0 of the transconductance amplifier is given by

$$i_0 = G_{m1} v_1 \qquad \text{……..4.2.5}$$

For bipolar transconductance, G_{m1} becomes :

$$G_{m1} = \frac{I_{bias1}}{2V_t} \quad \text{(as per [13])} \qquad \text{……..4.2.6}$$

where thermal voltage is given by:

$$V_t = \frac{kT}{q} \qquad \text{……..4.2.7}$$

Where:

T = Absolute Temperature in kelvin.

K = Boltzmann's' constant.

q = Charge of an electron.

From equation 4.2.6 and 4.2.7 it is clear that output current i_0 is controlled by the I_{bias1} and input voltage v_1.This forms the basis of programmable transconductance amplifier.[13]

In Fig. 4.2.5(b) bias current is replaced by a small signal i_2, which can be used to introduce second input signal v_2.

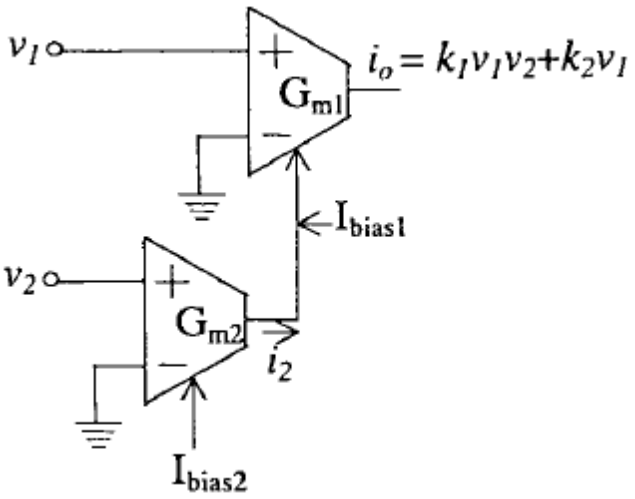

Fig. 4.2.6 Multiplication Operation Using Programmable Transconductor Using Second Input V_2 [13].

As shown in Fig.4.2.7 second input signal $v_2(t)$ is transformed into a current,

$$i_2(t) = G_{m2} v_2(t) \qquad \text{……..4.2.8}$$

and

$$I_{bias1} = i_2 \qquad \text{……..4.2.9}$$

Hence it is clear that second input voltage $v_2(t)$ acts as a control voltage for transconductance amplifier G_{m1}.

Hence, output current of fully programmable transconductance amplifier, shown in Fig.4.2.7, is given by:

$$i_0(t) = G_{m1}v_1 = \frac{I_{bias1} + G_{m2}v_2(t)}{2V_t}v_1(t) \qquad \text{……..4.2.10.}$$

Using equation 4.2.6 in 4.2.10 we obtain

$$i_0(t) = \frac{I_{bias2}v_1(t)v_2(t)}{4V_t^2} + \frac{I_{bias1}v_1(t)}{2V_t} \qquad \text{……..4.2.11}$$

$$i_0(t) = k_1v_1(t)v_2(t) + k_2v_1(t) \qquad \text{……..4.2.12}$$

Thus, $i_0(t)$ represents the multiplication of two signals $v_1(t)$ and $v_2(t)$ and an unwanted component $k_2v_1(t)$ [20].Hence in order to remove these unwanted components, we used single-quadrant multiplier cancellation method.

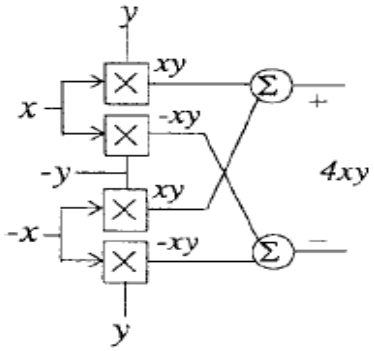

Fig. 4.2.7 Four-Quadrant Multiplier Basic Structure Using Single Quadrant Multiplier [13].

Simultaneous cancellation of all the common mode components (X and Y) and higher order component is obtained through the multiplier topology shown in Fig.4.2.7.

This topology operates on the following equality:

$$[(X+x)(Y+y)+(X-x)(Y-y)]-[(X-x)(Y+y)+(X+x)(Y-y)]=4xy \quad \text{.....4.2.13}$$

Where

(X, Y) represent common mode components and (x, y) represent small input signals respectively.

MOSFETs are the transconductance device; hence they are best suited for the implementation of the cancellation schemes.

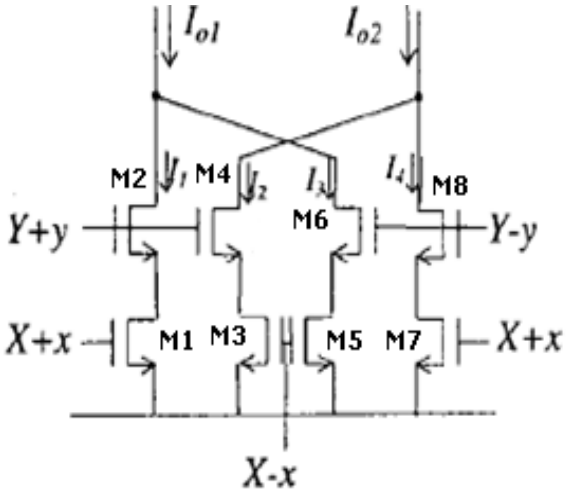

Fig. 4.2.8 Fully Differential Four-Quadrant Multiplier [13].

This configuration is based on the topology as shown in Fig 4.2.7 and corresponds to Equation 4.2.13 yielding:

Io=Io1-Io2= (I1+I3)-(I2+I4) = 4Kxy …..4.2.16

Where

$$I_1 = K[X + x - V_T - \frac{Y + y - V_T}{2}]$$

$$I_2 = K[X - x - V_T - \frac{Y + y - V_T}{2}]$$

$$I_3 = K[X - x - V_T - \frac{Y - y - V_T}{2}]$$

$$I_4 = K[X + x - V_T - \frac{Y - y - V_T}{2}]$$

In order to represent this product in voltage form we pass this difference of current through the impedance Zf.

$$V_o = Z_f I_o = 4KZ_f xy$$ ….4.2.17

From equation 4.2.17 it is clear that configuration shown in fig. 4.2.9 multiplies the two applied input signals and also removes nonlinear terms.

Considering the fact that PMOS transistors need less drain current with larger overdrive voltage (VGS-VTH) compared with nMOS transistors, pMOS transistors are preferably chosen in the input terminals for operations in either saturation region [12].

Hence NMOS transistors of fig. 4.2.9, which are operating in saturation region (M5-M8) should be replaced by pMOS transistor for sound multiplier operation.

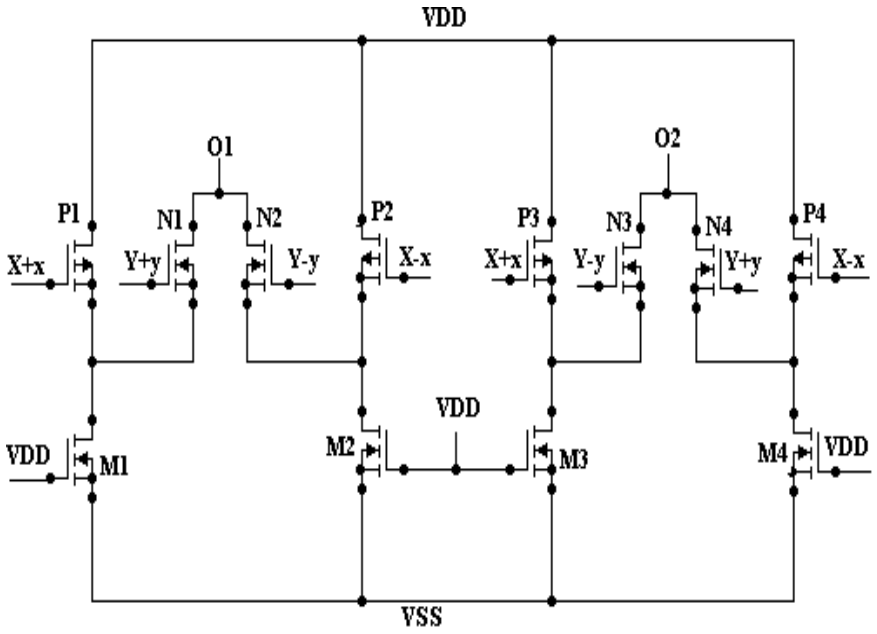

Fig. 4.2.9 Multiplier Topology [12]

A potential advantage of the structure shown in fig. 4.2.9 is that a larger input range can be obtained with only pMOS transistors in their saturation region [12].

NMOS transistors N1,N2,N3 and N4 are operating in linear region and PMOS transistors P1,P2,P3 and P4 operate in saturation region. The programmable transconductance pairs are (N1,P1) , (N2,P2), (N3,P3) and (N4,P4).

Transistors M1-M4 are also NMOS transistors and act as a current sink. X, Y at the input terminals of P1-P4and N1-N4 represents the dc bias components whereas x, y represent small input signals.As whole topology of our multiplier is same except the choice of transistors, this topology achieves multiplication by the equation 4.2.17.Hence we can represent it also as

$$V_{01} - V_{02} \propto xy \qquad \text{.....4.2.18}$$

ASPECT RATIO OF TRANSISTOR

TRANSISTOR	ASPECT RATIO
M1	$0.8\mu/0.35\mu$
M2	$0.8\mu/0.35\mu$
M3	$0.8\mu/0.35\mu$
M4	$0.8\mu/0.35\mu$
N1	$0.8\mu/0.35\mu$
N2	$0.8\mu/0.35\mu$
N3	$0.8\mu/0.35\mu$
N4	$0.8\mu/0.35\mu$
P1	$0.8\mu/0.35\mu$
P2	$0.8\mu/0.35\mu$
P3	$0.8\mu/0.35\mu$
P4	$0.8\mu/0.35\mu$

Table 4.2 Aspect ratio of NMOS and PMOS used [12].

4.3 GAIN STAGE

The input to the gain stage is a modulated signal of very high frequency. Hence first of all amplifier should be able to operate on very high frequency signals. Moreover as it is the major gain stage, its gain should also be high. Operation of this gain stage should be unaffected by the external disturbances like variation in power supply voltage. Otherwise artificial noise will penetrate into the signal through this stage.

Here we will use the high gain, low power general purpose opamp which has a structural simplicity of classical widlar structure.we use composite cascode connections in both the stages to achieve high gain with low power consumption.It employs two gain stages followed by a unity gain buffer stage.With only two gain stages miller compensation capacitor can be used.

This work increases the gain of Mosfet just like BJT by using the composite cascode stages in subthreshold region.The structure of composite cascode connection is shown in figure below:

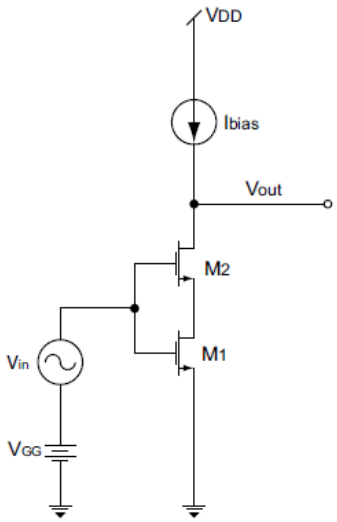

Fig. 4.3.1 composite cascode amplifier [25]

The input of M1 and M2 share a common input signal Vin which is dirven by a single source V_{gg} .If M1 and M2 have same aspect ratio then M1 will operate in triode region whereas M2 will be in active region.Now composite cascode will work like a common source stage with high voltage gain.If aspect ratio of M2 is much higher then M1 then M1 is placed in strong inversion region whereas M2 will be in weak inversion region.[25]

Assuming the current has higher output impedence,the output impedence is

$$\mathrm{rout} = \mathrm{rds1} + \mathrm{rds2} + (\mathrm{gm2} + \mathrm{gmb2})\mathrm{rds1rds2}. \qquad \text{.....4.3.1}$$

Now the voltage gain is

$$\mathrm{A0} = -[\mathrm{gm1rds1} + \mathrm{gm2rds2} + \mathrm{gm1rds1}(\mathrm{gm2} + \mathrm{gmb2})\mathrm{rds2}] \qquad \text{.....4.3.2}$$

If the current source load has finite resistance R instead of assumed infinite output impedence

The voltage gain becomes

$$A0 = \frac{-[gm1rds1+gm2rds2+gm1rds1(gm2+gmb2)rds2)]}{1+1/R[rds1+rds2+(gm2+gmb2)rds1rds2]} \qquad \text{.....4.3.3}$$

The practical composite cascode structure:

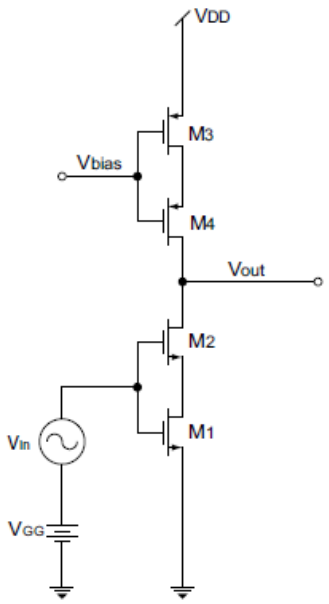

Fig. 4.3.2 Practical composite Cascode Amplifier [25].

Here the aspect ratio of M4 is much greater than that of M3 and the aspect ratio of M1 is greater than M2.M4 is in subthreshold region whereas M3 is in active region.The output impedence looking in to the drain of M4 is given by eq 4.3.1.If the impedence looking in to the drain of M4 is equal to the impedence looking in to the drain of M3 then the voltage gain will be:

$$A0 = -[gm1rds1 + gm2rds2 + gm1rds1(gm2 + gmb2)rds2]/2 \quad \ldots\ldots\ldots\ldots\ldots\ldots 4.3.4$$

Composite cascode opamp

Figure 4.3.3 shows the composite cascode opamp.In composite cascode opamp high gain can be obtained by operating in weak inversion region.

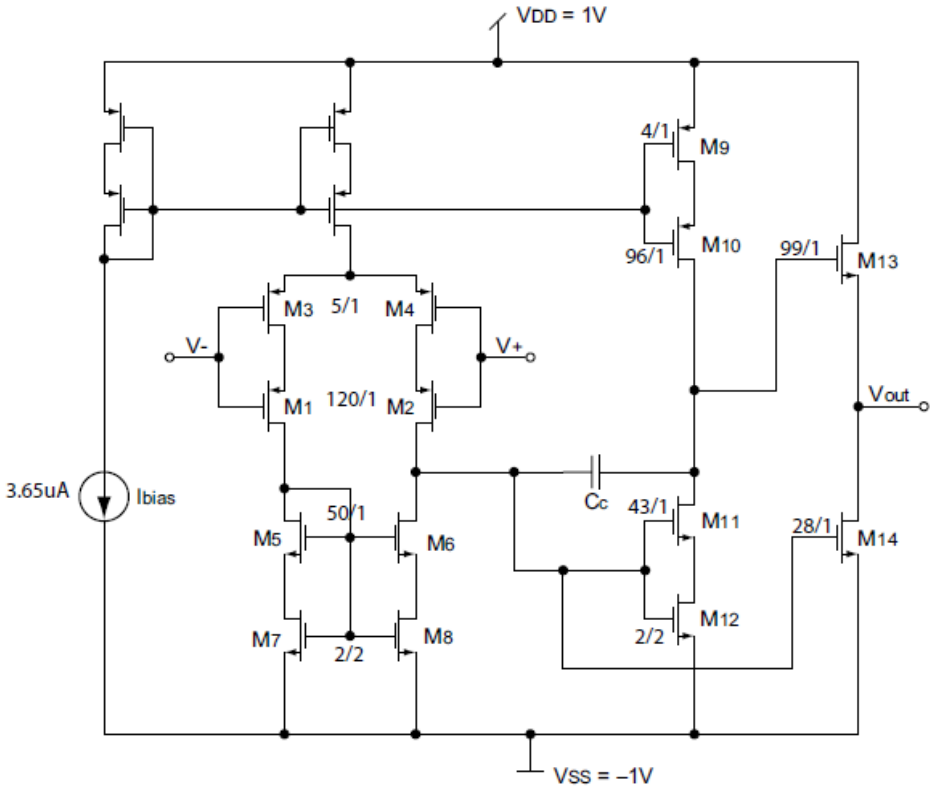

Fig. 4.3.3 Composite Cascode Amplifier[20]

It uses the classical widlar architecture which consists of two gain stages followed by a buffered output stage.The various stages are explained below.

Design of composite cascode opamp using 3 stages:

1st stage-Input Differential Composite cascode stage

The first stage is the differential to single ended composite cascode stage.

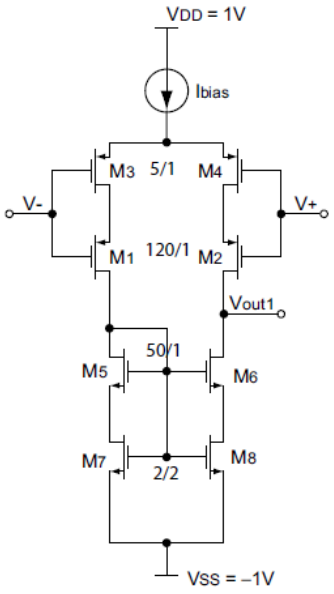

Fig. 4.3.4 opamp input differential composite cascode stage[25]

Composite cascode connection in the NMOS and PMOS allows the input to swing from positive power supply to negative power supply. Here the aspect ratio of output transistor is kept much higher then the aspect ratio of lower transistor. More over the gain here is also independent of drain current. Here the drain connected device M2 operates in weak inversion region while the source connected device M1 operates in strong inversion region. Here the current mirror is used to provide bias current to input stage and the bias voltage to output stage[25].

The bias current for the input differential stage is only 3.65ua.It is used to provide the robust bias current.

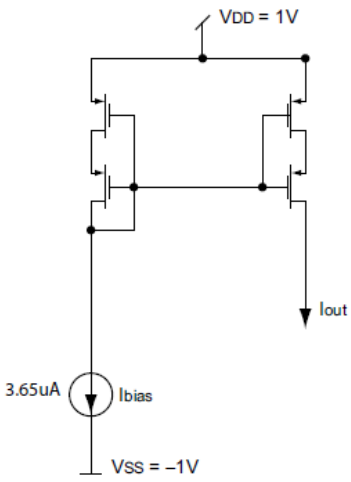

Fig. 4.3.5 opamp composite cascode current mirror[25]

2nd stage-Common source stage

The second stage is common source stage implemented as composite cascode stage.The compensating capacitor is inserted between the input and output of common source stage to apply the miller feedback effect.

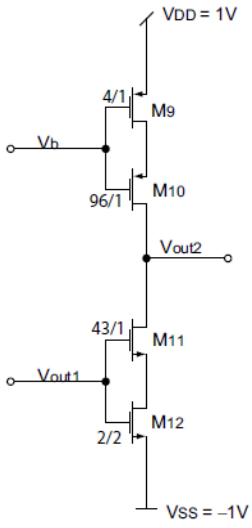

Fig. 4.3.6 opamp second composite cascode stage[25]

3rd stage-Output source follower with a current sink load

This is the output stage of composite cascode amplifier.It is use as a buffer to drive an external load. Here source follower with current sink load load is used as shown below.The output buffer stage has low output impedence which allows loading by large capacitive load or small resistive load.The figure is as shown below.

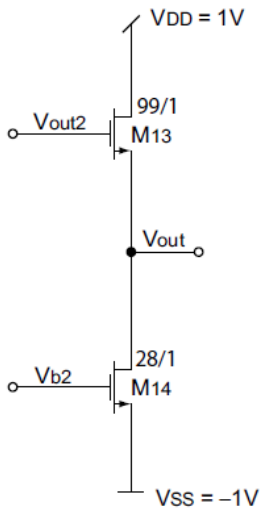

Fig. 4.3.7 opamp output source follower stage[25].

After amplification through the gain stage, signal is demodulated by the demodulator in order to get back original baseband signal, as was discussed in [25].

4.4 LOW PASS FILTER

The final stage of our proposed design is low pass filter. An electrical filter is basically a frequency selective circuit that passes a specified band of frequencies and blocks or attenuates signals of frequencies outside this band..Basically filter is an electrical circuit which isolates signal of desired frequency from the unwanted signal's frequency. In general the filter is an electrical circuit that changes or alters the

signal's amplitude or phase with respect to the frequency[10]. Its operation principle is that it attenuates amplitude of the unwanted frequency signal and passes the signal of desired frequency band to pass with unity or some gain. In other words gain of the filter is directly dependent on the signal frequency.Filters may be classified as a number of ways:

1.Analog or Digital

2.Passive or Active

3.Audio frequency or Radio Frequency

Analog filters are designed to operate analog signal whereas digital filters are used to process analog signal using digital technique.[10]

Depending upon the type of elements used filter can be classified as active or passive. Elements used in passive filter are resistors, capacitors and inductors. Elements used in active filter are Transistor and opamp in addition to resistor and capacitor[10].

The type of element used decide the operating frequency range of filter.RC filters are used for audio or low frequency opamp whereas LC filter or crystal filter are used for high frequency or radio frequency operaton.

The band pass filter has two 3dB frequencies i.e. f_L and f_H, where f_L is lower cutoff frequency and f_H higher cut-off frequency. It passes only those signal whose frequency lies in between f_L and f_H ($f_L < f_{signal} < f_H$).

Butterworth low pass filter is the most common active filter. It is simplest in construction and ideally it does not haves any ripple in its pass band region.

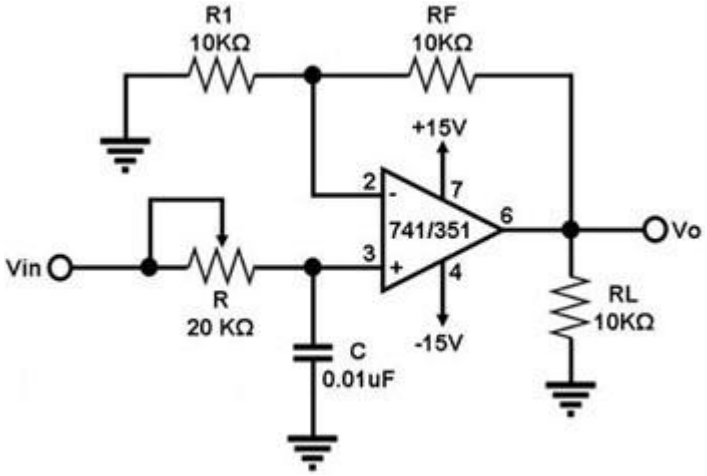

Fig. 4.4.1 Circuit diagram of first Order Butterworth lowpass filter[10]

Butterworth lowpass filter is designed through the first order active low pass filter. The composite cascode opamp has been used in the design of this active filter. Reason for choosing composite cascode op amp is its high gain. Noise response of this op amp is better than its counterparts.

Here the cut off frequency is given by

$F_H = \frac{1}{2\pi RC}$ =High cut off frequency of the filter.

CHAPTER 5

RESULTS

In this chapter, we have shown the analysis of various modules that have we used in the design of the low power low voltage amplifier system . Initially we have shown responses of individual blocks followed by the response of overall system.

Basically we have shown two responses of all the individual blocks and of overall system. Transient response and AC response of each individual block has been shown. Input inferred noise response has been shown for both the gain stages used in the system i.e. preamplifier and the composite cascode amplifier.

1. Transient response: Transient response of a system is a graph plotted between the system variables or parameters versus time. It shows variations of these system parameters with time. This response helps us to verify that the individual module is functioning properly or not. Through this response, frequency and nature of the signal can also be identified.

2. AC Response: It is plot of output response of the system versus frequency. It provides the information about the gain provided by the system. Here we have also plotted ac gain and phase plot which gives the value of ω_{pc} and ω_{gc} which determines the stability of the system.

3. Input-Referred Noise Response: It is the graph plotted between the input-referred noise versus frequency. It indicates the extent up to which input signal is being corrupted by the design's noise. Basic idea of the input-referred noise is to model the

consequences of all the sources of the noise present in the design, by noise sources at the input. These noise sources are modeled in such a way that the noise present at the output stage noise is simply obtained by multiplying gain of the amplifier with the input-referred noise.

5.1 PREAMPLIFIER

5.1.1. PREAMPLIFIER SCHEMATIC

The preamplifier schematic is shown below.

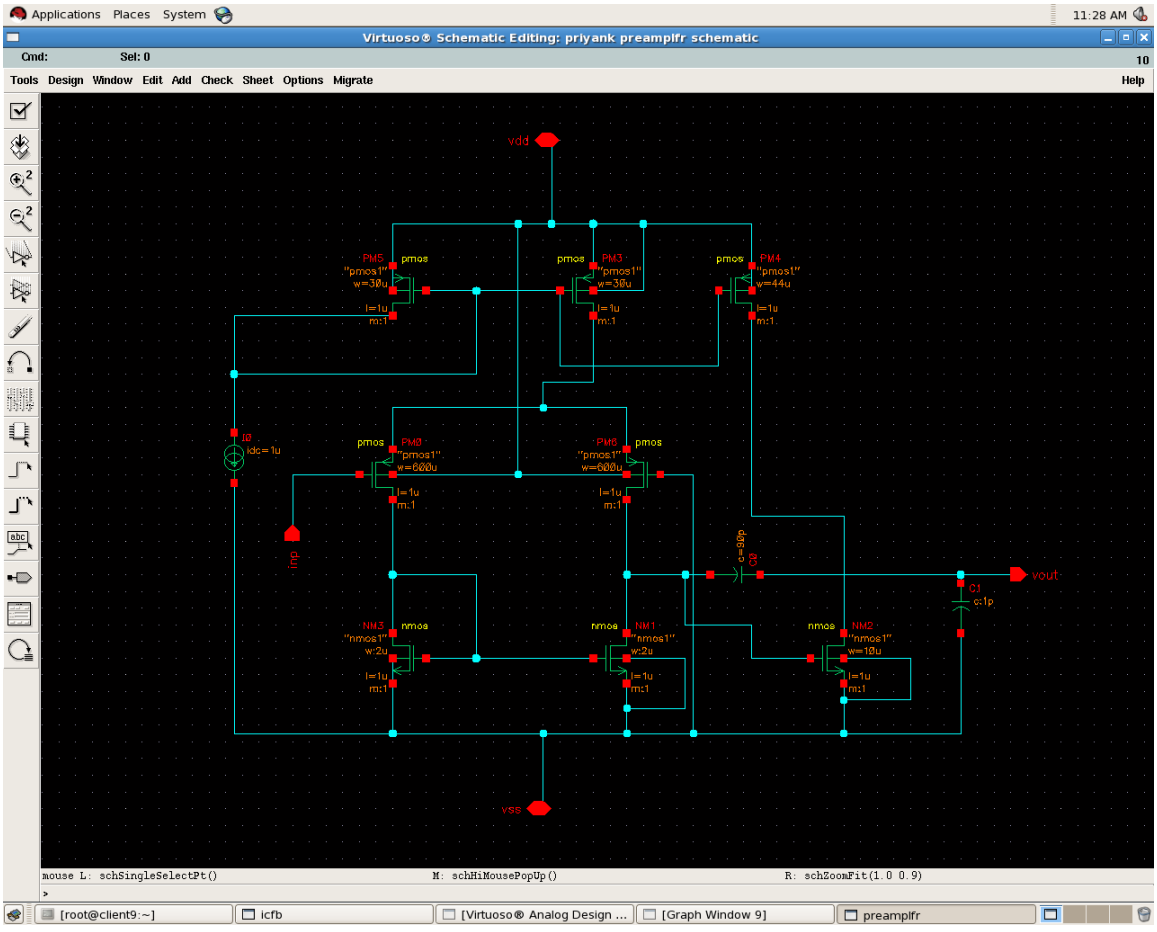

Fig. 5.1.1 Preamplifier schematic

5.1.2) NOISE RESPONSE

Here we have shown noise response of PMOS two-stage amplifier. The curve in red shows variation of the input-referred noise with frequency in frequency domain.

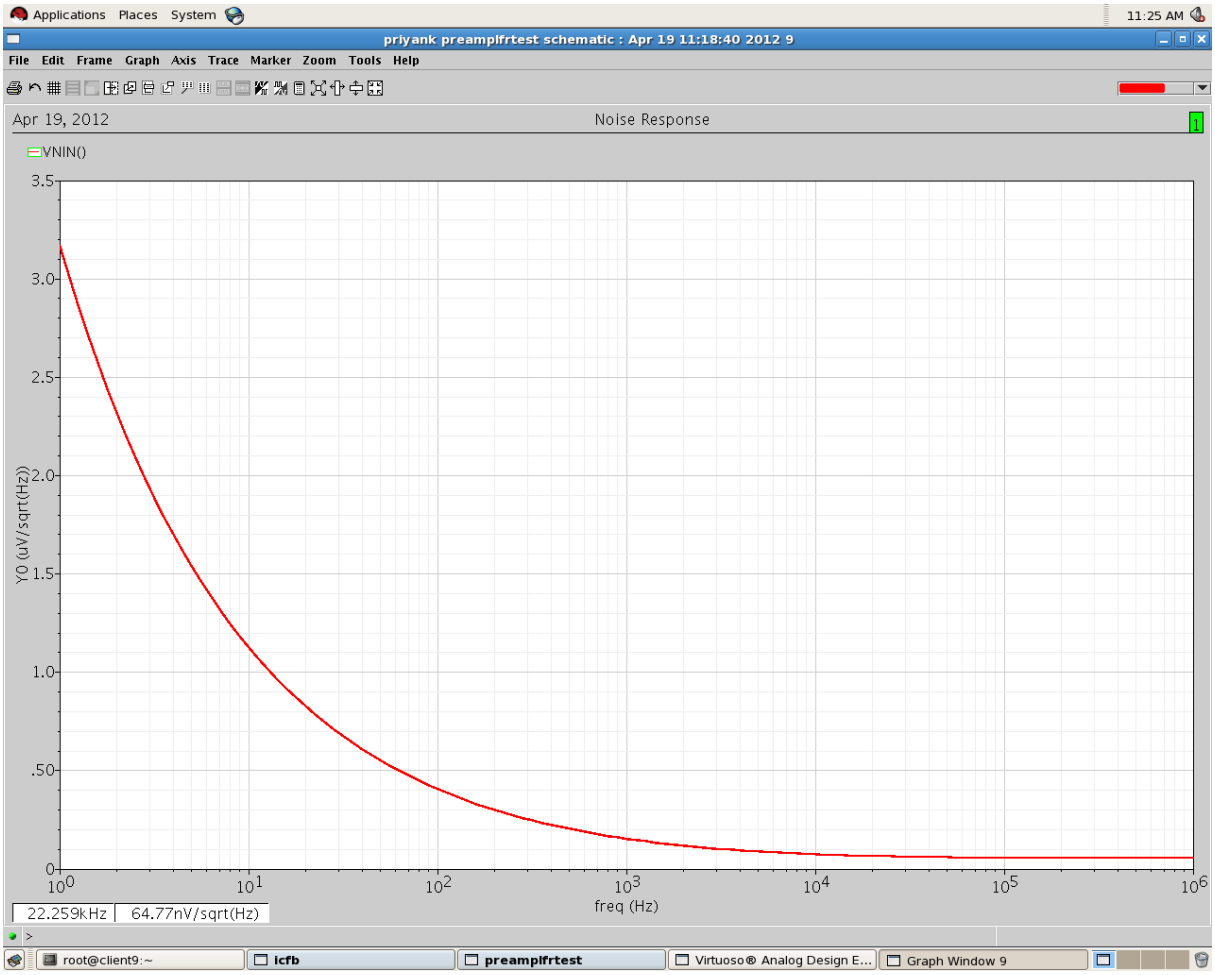

Fig. 5.1.2 Noise Response of PMOS Two-Stage Op-Amp

The input referred noise response of PMOS two stage opamp is 64 nanovolt/sqrt(Hz).

5.1.3) TRANSIENT RESPONSE

Input to the preamplifier is sinusoidal signal. If the preamplifier is working properly then it should give sinusoidal output without any clipping. Gain is not important constraint for this amplifier because it is used as a preamplifier which should have low input referred noise response.

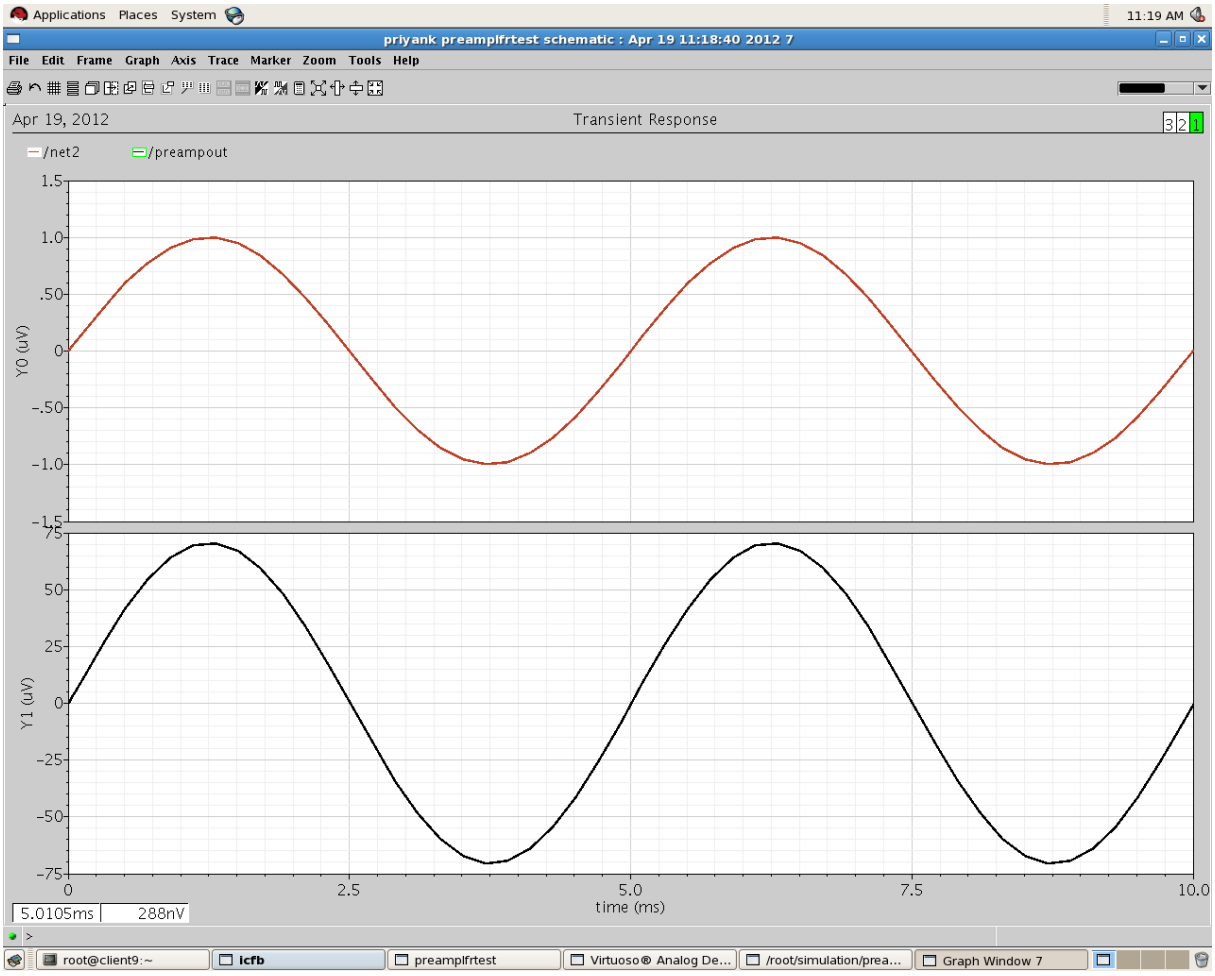

Fig. 5.1.3 Transient Response of pMOS Two-Stage Op-Amp

Here net2 – input (red)

preampout – output (black)

5.1.4 a) AC Response:

Here a: input (red)

out: output (green)

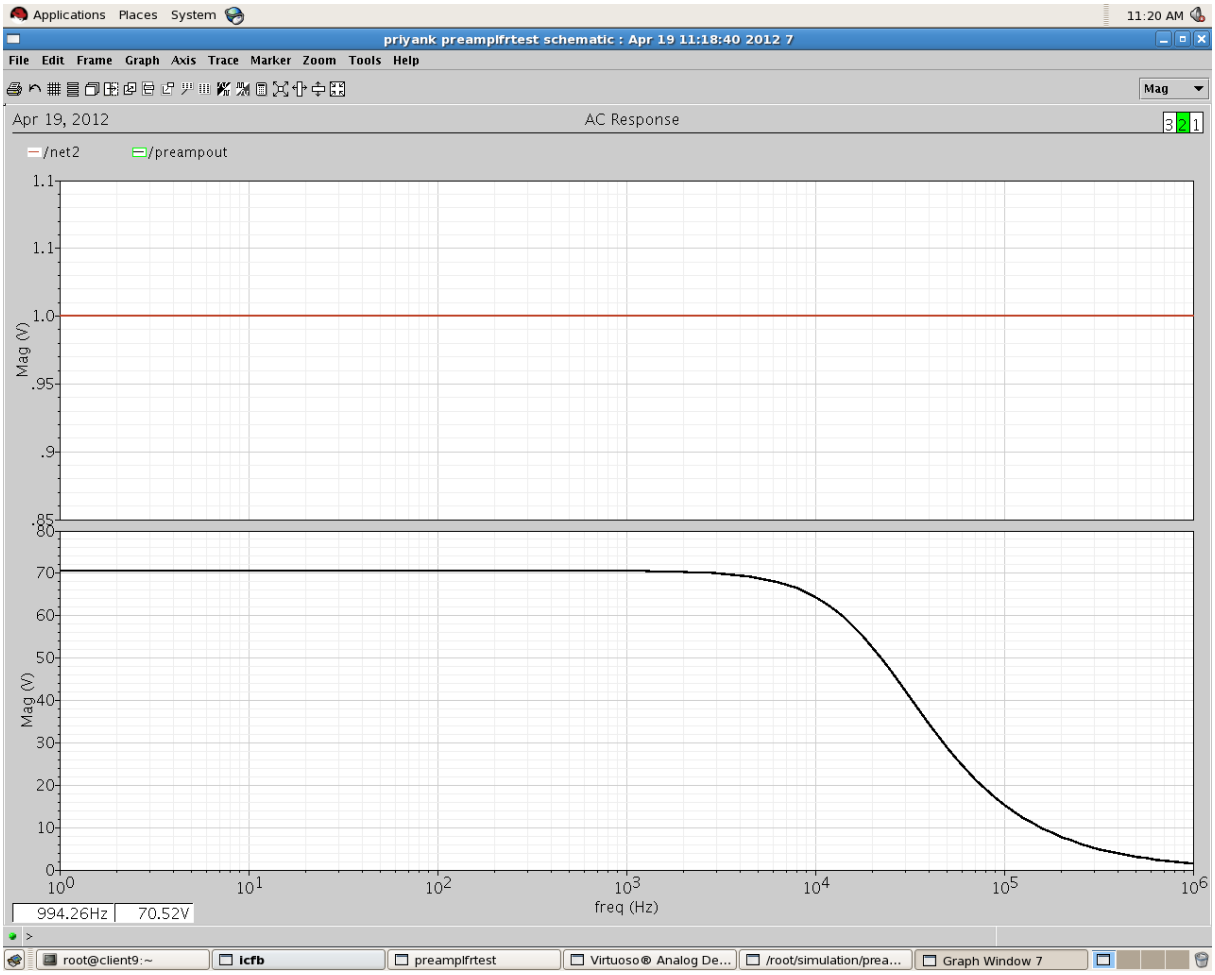

Fig. 5.1.4 AC Analysis of pMOS Two-Stage Op-Amp

From the AC response it is clear that preamplifier is providing constant gain at the operating frequency. It is first gain stage of our low power low voltage amplifier system which provides gain of 70 V/V.

5.1.4 b) AC Gain and phase plot:

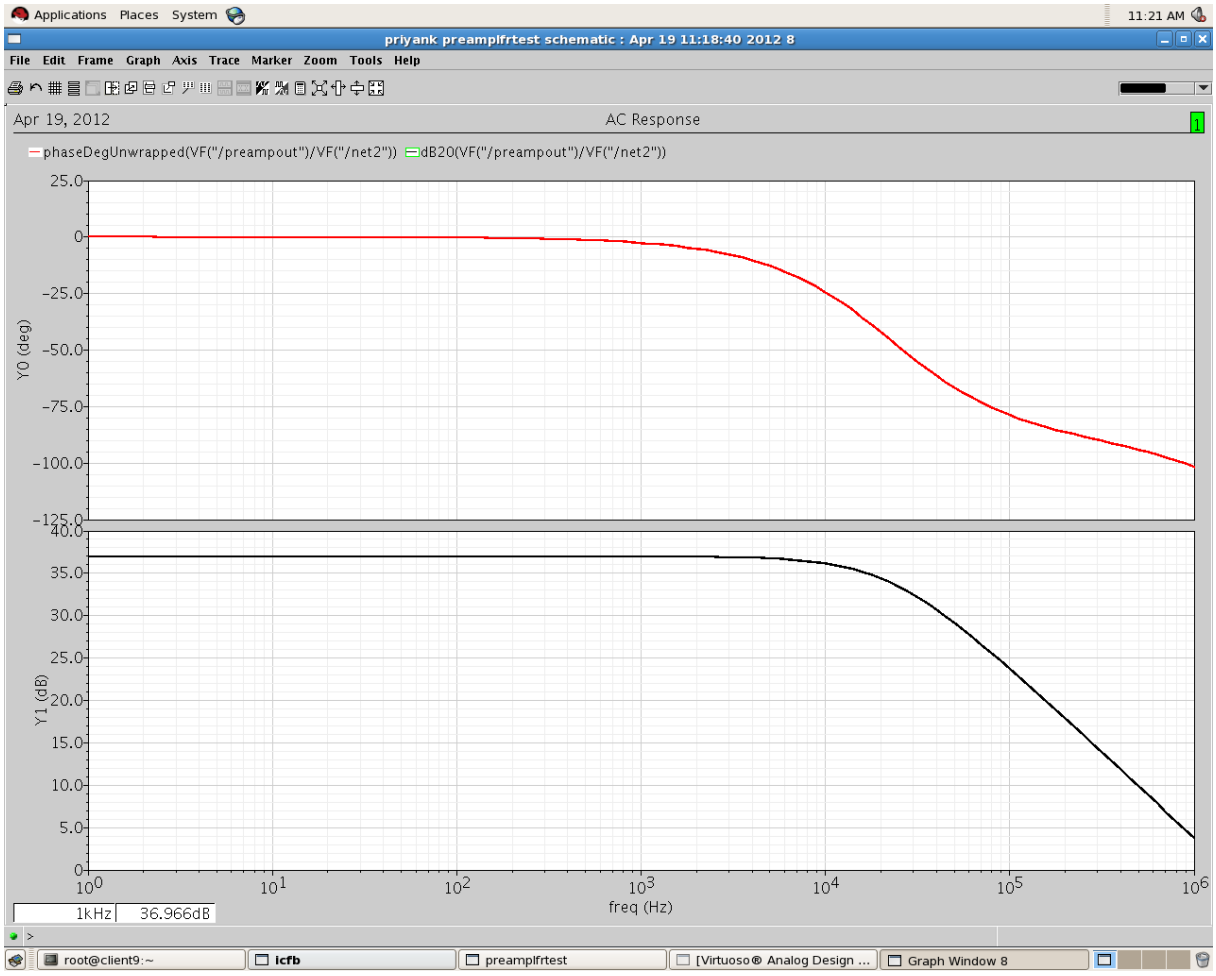

Fig. 5.1.5 AC gain and phase plot of PMOS Two-Stage Op-Amp

As we can see from the graph that ωpc > ωgc. ωpc is phase cross over frequency and ωgc is gain cross over frequency.Thus the system is stable. It means that the gain margin and phase margin both are positive.

5.1.5) calculation of Bandwidth of preamplifier system

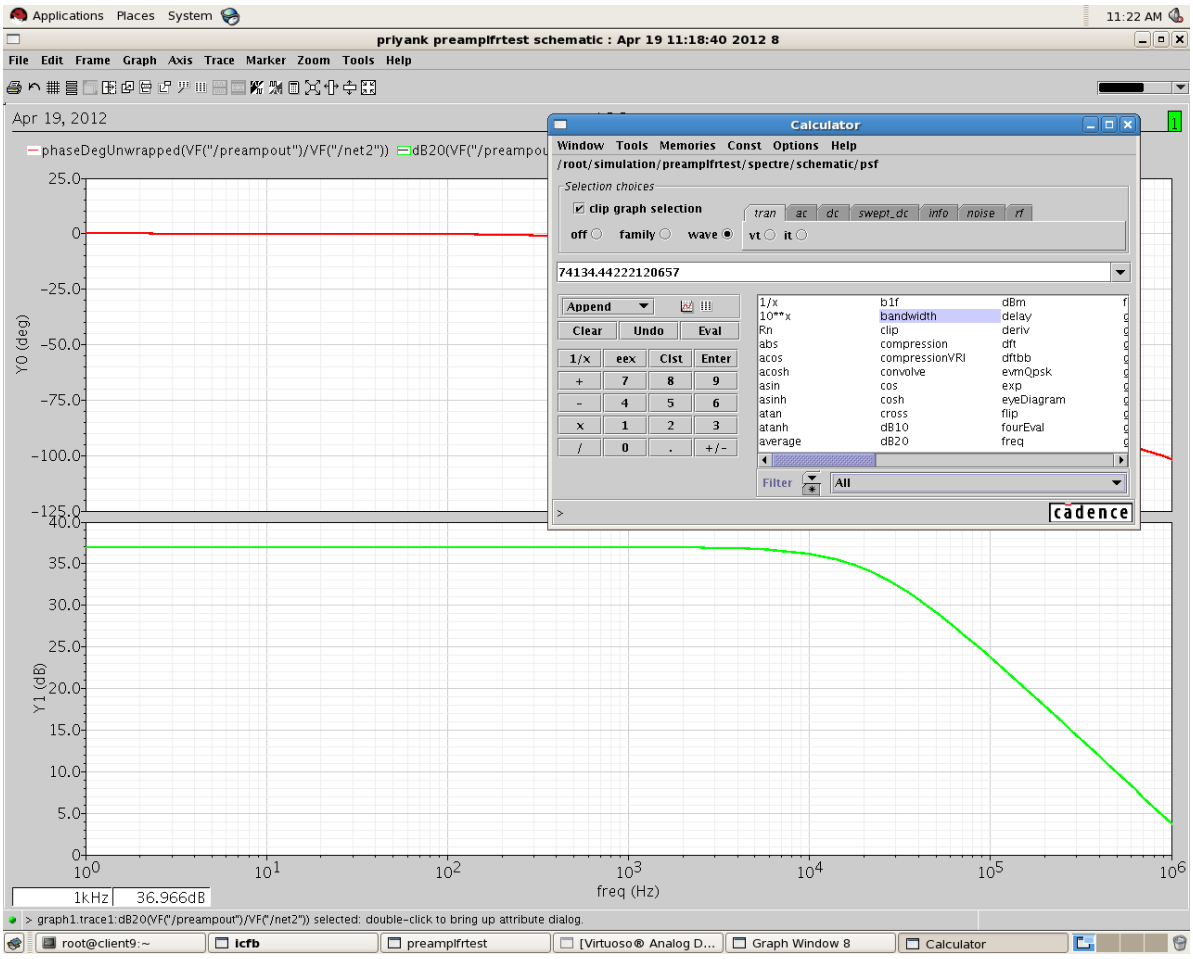

Fig. 5.1.6 Bandwidth of PMOS Two-Stage Op-Amp

As we can see from the graph that the band width of the 2 stage pmos is 74 KHZ.

5.2 MODULATOR/DEMODULATOR

5.2.1 MODULATOR SCHEMATIC

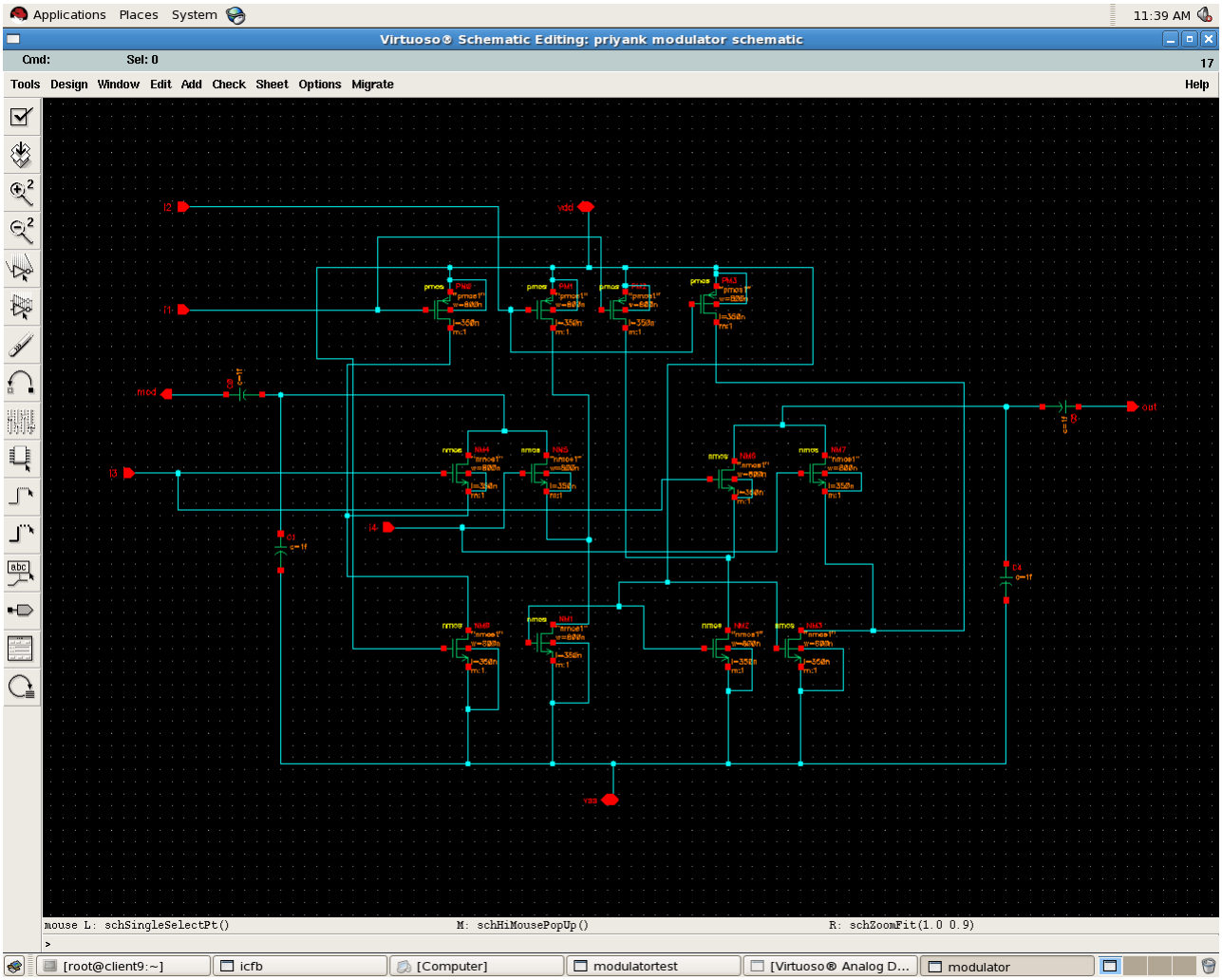

Fig. 5.2.1 Modulator Schematic

5.2.2 TRANSIENT RESPONSE

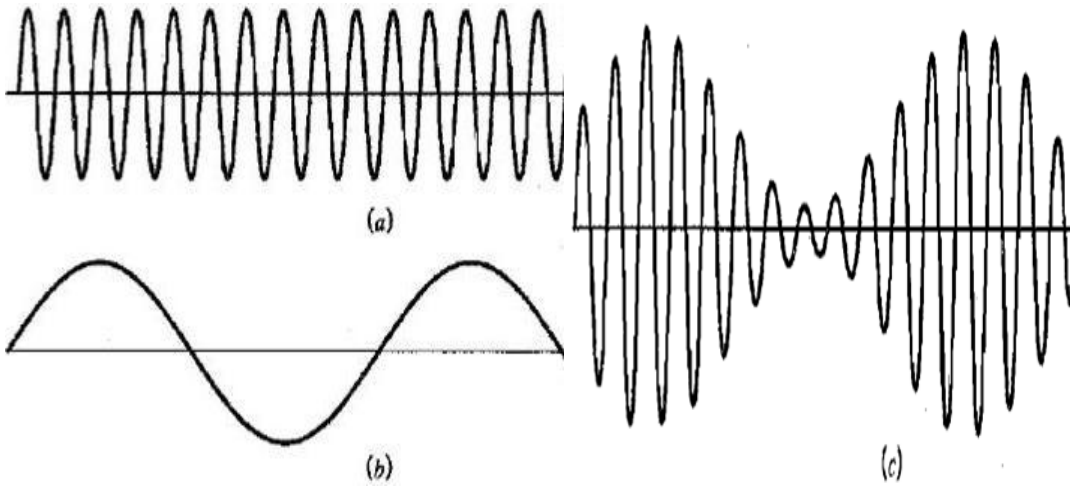

Fig. 5.2.2 Various Waveforms of Multiplier. (a) Carrier wave (b) Input signal (c) Modulated signal [19].

Most important constraint for the multiplier is that it should multiply two input signals.

The resultant output waveform can be only seen through its transient response.

5.2.2 TRANSIENT ANALYSIS

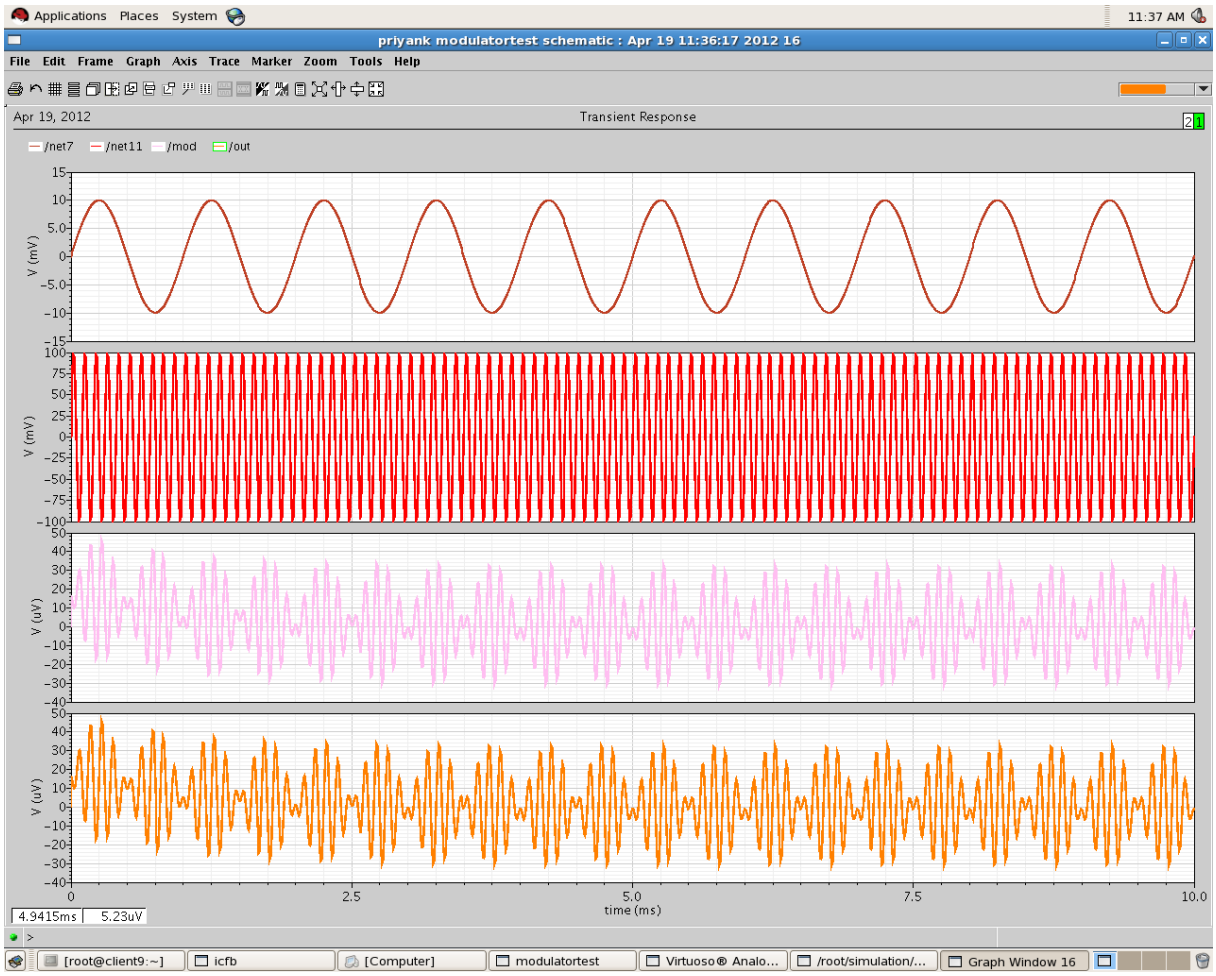

Fig. 5.2.3 Various Transient Waveforms of Multiplier. (A) Input Signal(net 7) (B) Carrier Wave (net11) (C) Modulated Signal (mod and out)

As we can see from the wave form that modulation has been done properly.

5.2.3 TRANSIENT ANALYSIS WITH CARRIER SIGNAL AT HIGH FREQUENCY

Fig. 5.2.4 Various Transient Waveforms of Multiplier. (A) Input Signal(NET 7 AND NET13)
(B) Carrier Wave (NET11 and NET 9) (C) Modulated Signal (MOD and OUT)

5.2.4 MODULATOR AC ANALYSIS

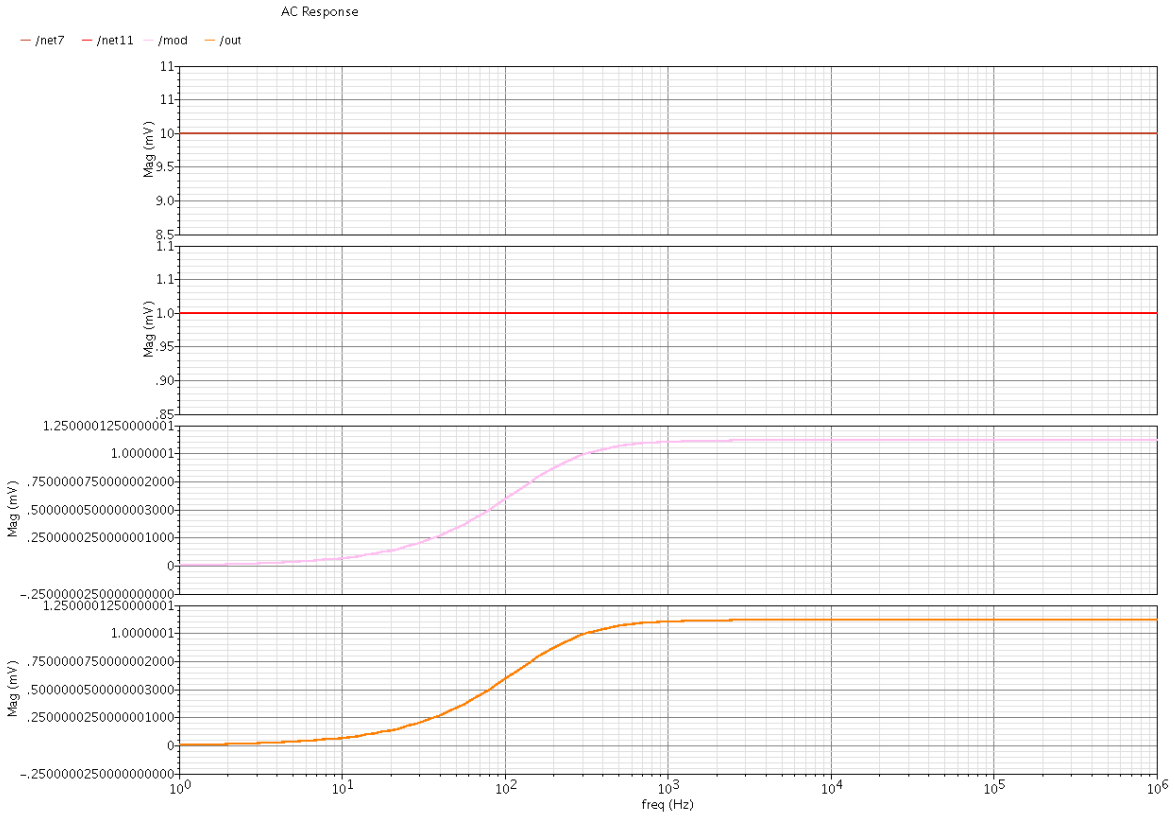

Fig. 5.2.5 Various AC Waveforms of Multiplier. (A) Input Signal(net 7) (B) Carrier Wave (net11) (C) Modulated Signal (mod and out)

As we can see from the waveform that modulator has been working properly in the frequency range in which we want to use it.

5.3 COMPOSITE CASCODE AMPLIFER

5.3.1 SCHEMATIC OF COMPOSITE CASCODE AMPLIFIER

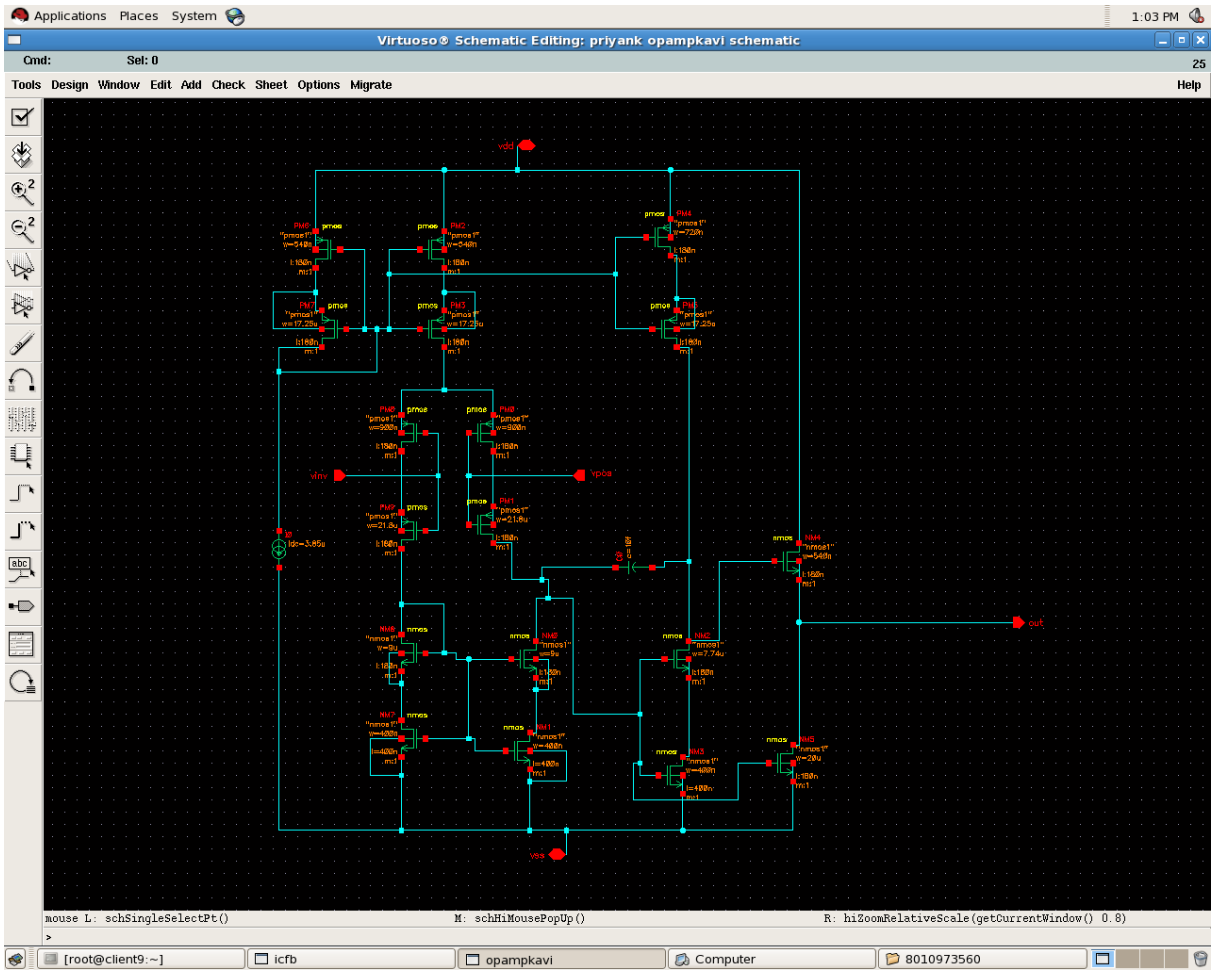

Fig. 5.3.1 Composite cascode amplifier Schematic

5.3.2 TRANSIENT ANALYSIS

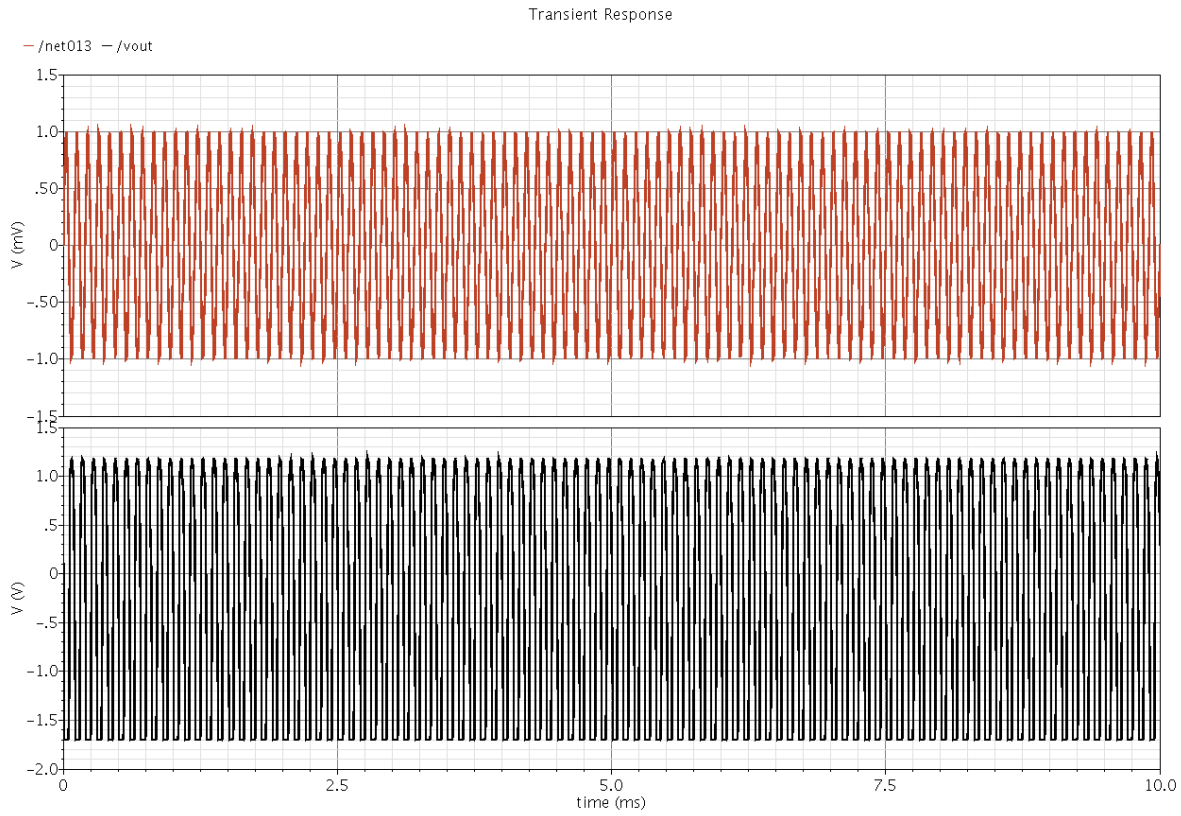

Fig. 5.3.2 Transient Response of Composite Cascode Amplifier

Here gain : output (black)

input : input (red)

5.3.3 AC ANALYSIS

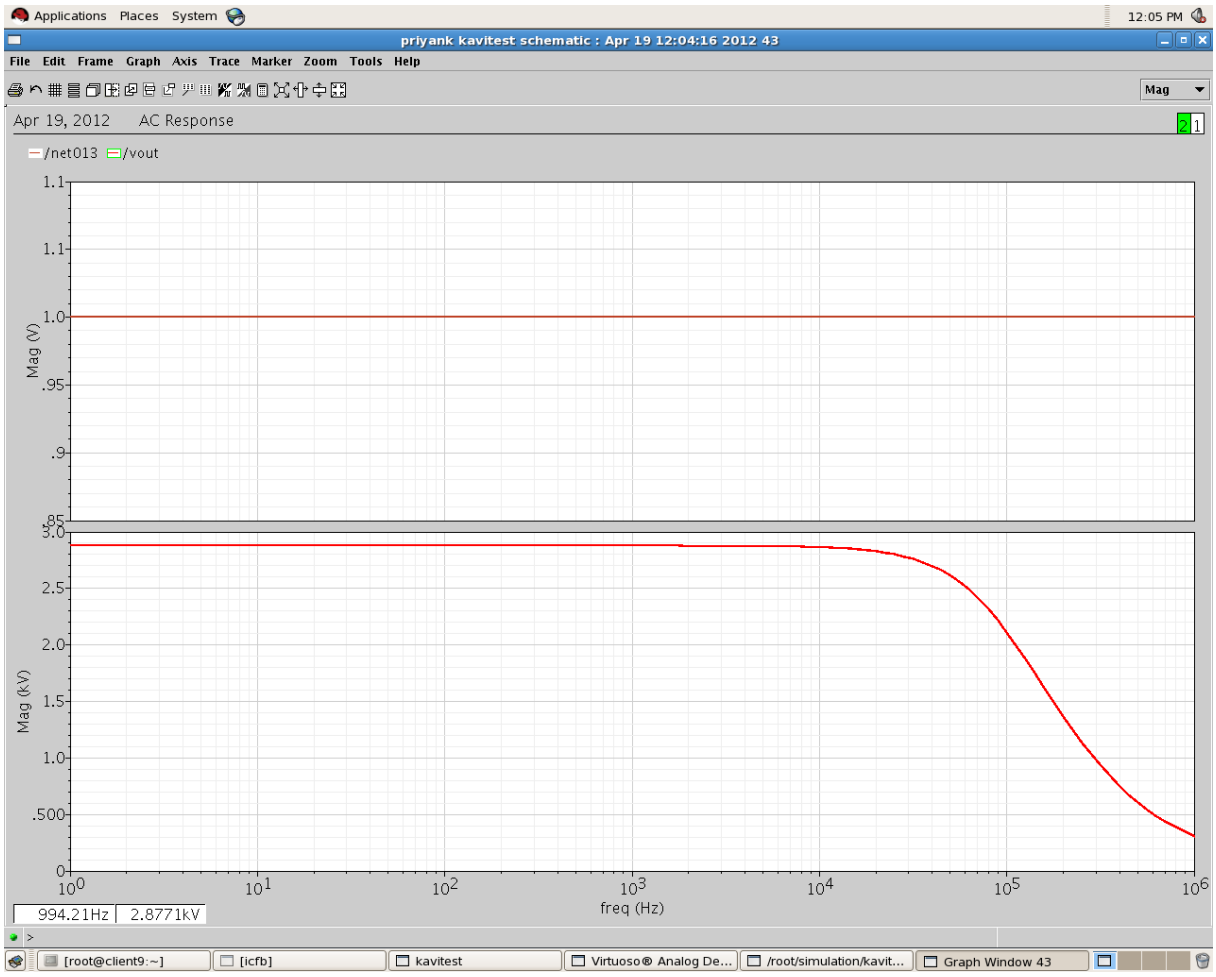

Fig. 5.3.3 AC Response of composite Cascode Amplifier

Here gain – output (red)

input – input (green)

Gain of the composite cascode amplifier is 2.8 KV/V.

5.3.4 GAIN AND PHASE PLOT OF COMPOSITE CASCODE AMPLIFIER

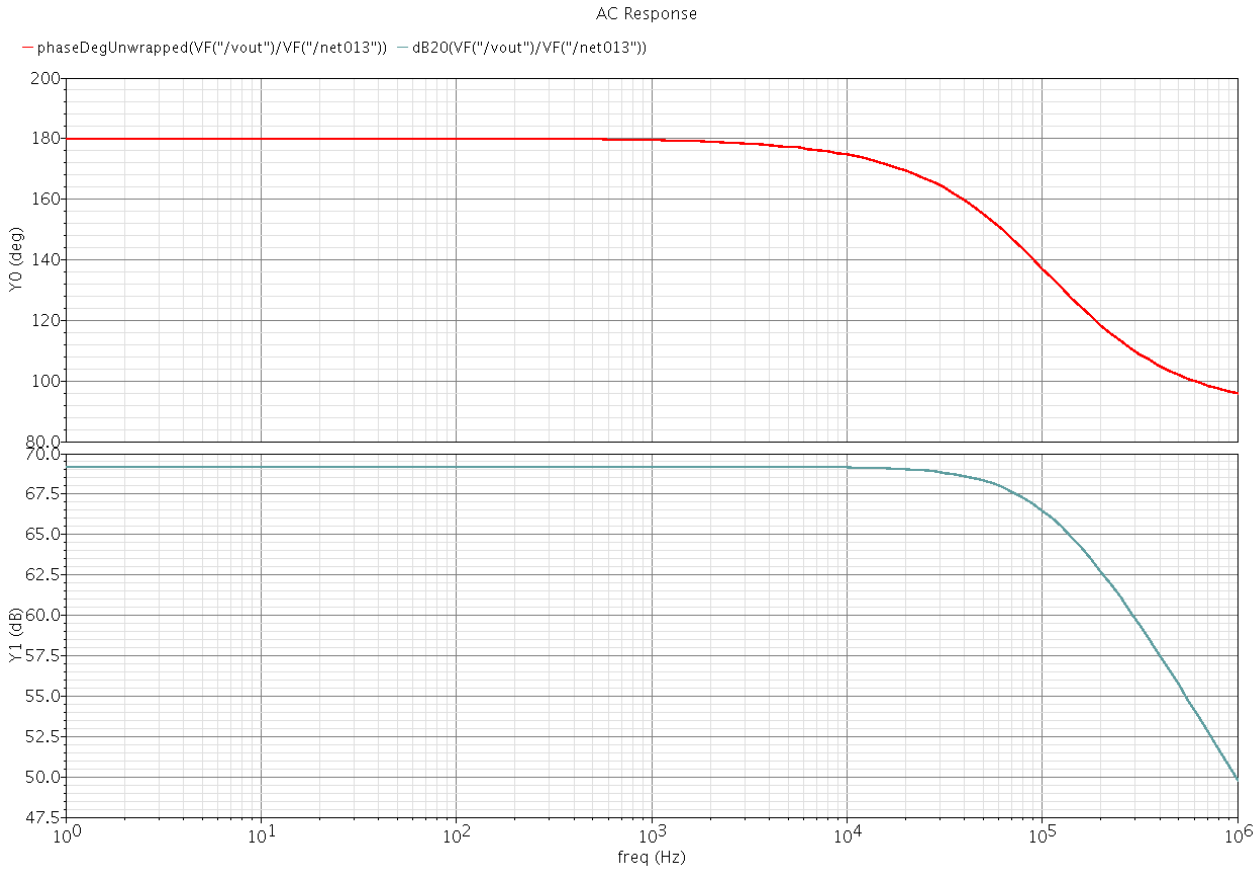

Fig. 5.3.4 Gain and phase plot of composite Cascode Amplifier

Bandwidth of Composite cascode amplifier =80.39 KHz.

5.3.5 Noise Analysis of composite cascode amplifier.

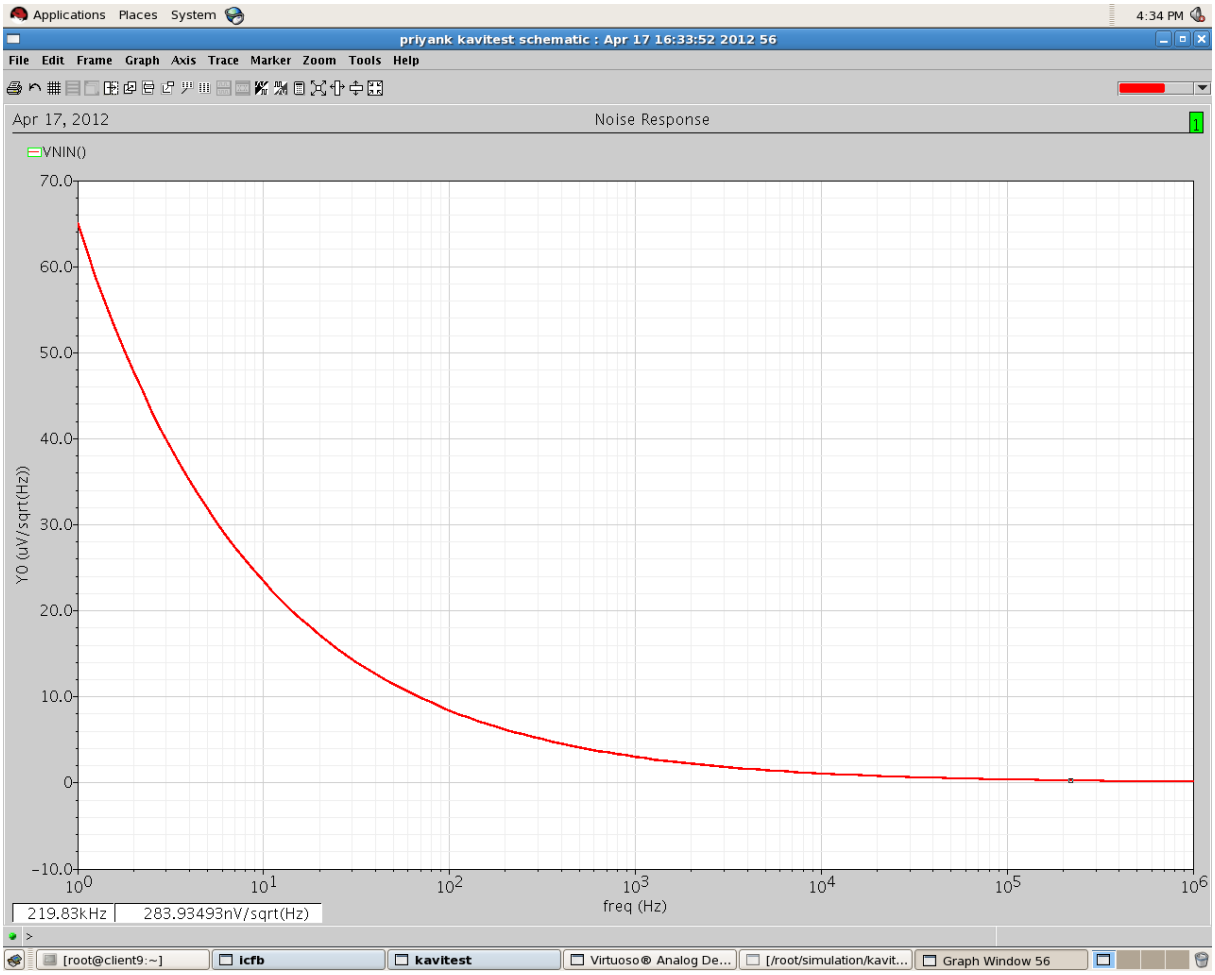

Fig. 5.3.5 Noise Response of composite Cascode Amplifier

The noise response of composite cascode amplifier is 283 nv/sqrt(Hz).

5.4 filters

5.4.1) Low pass Filter schematic

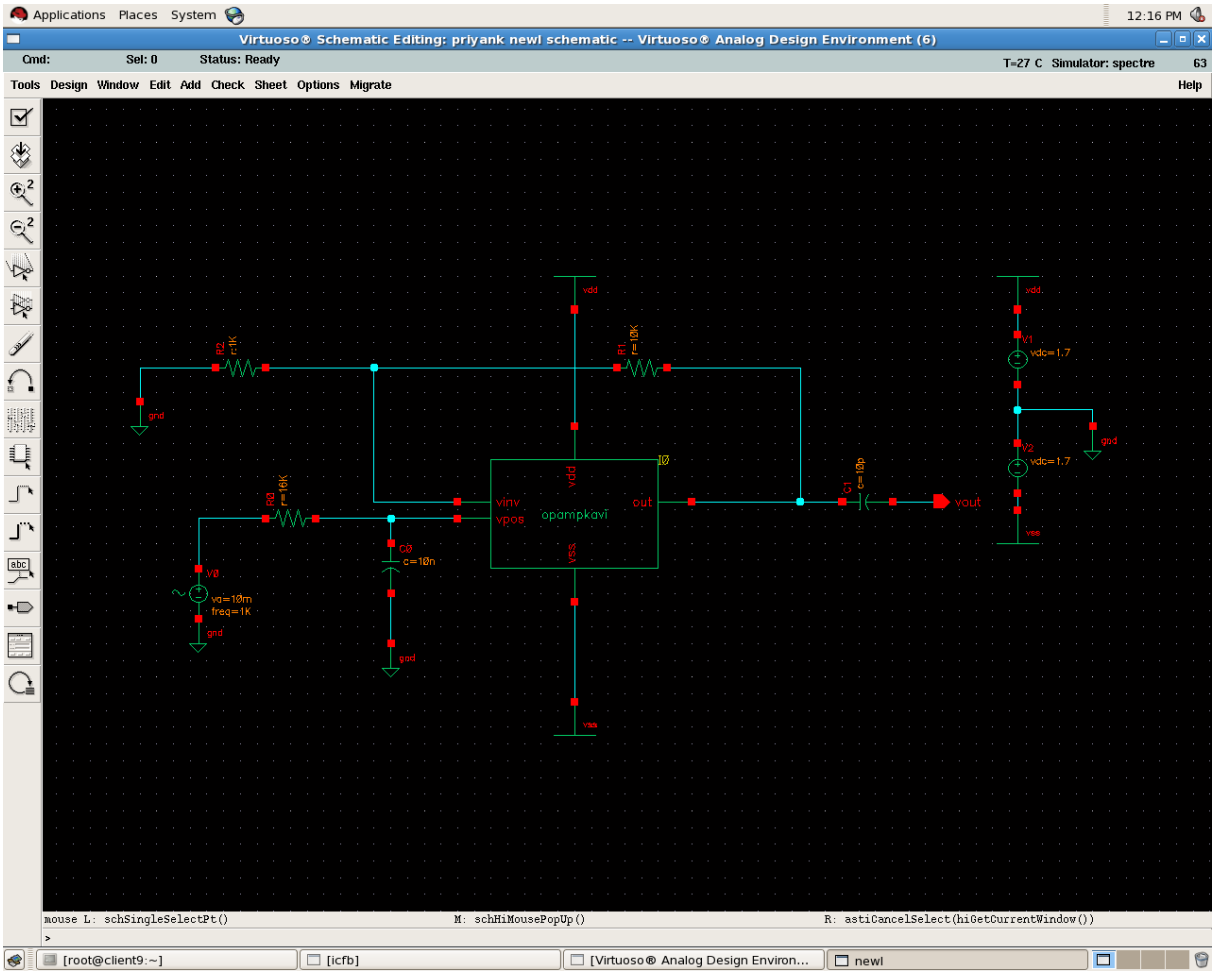

Fig. 5.4.1 Low pass filter schematic

5.4.2)Transient response of Low Pass Filter

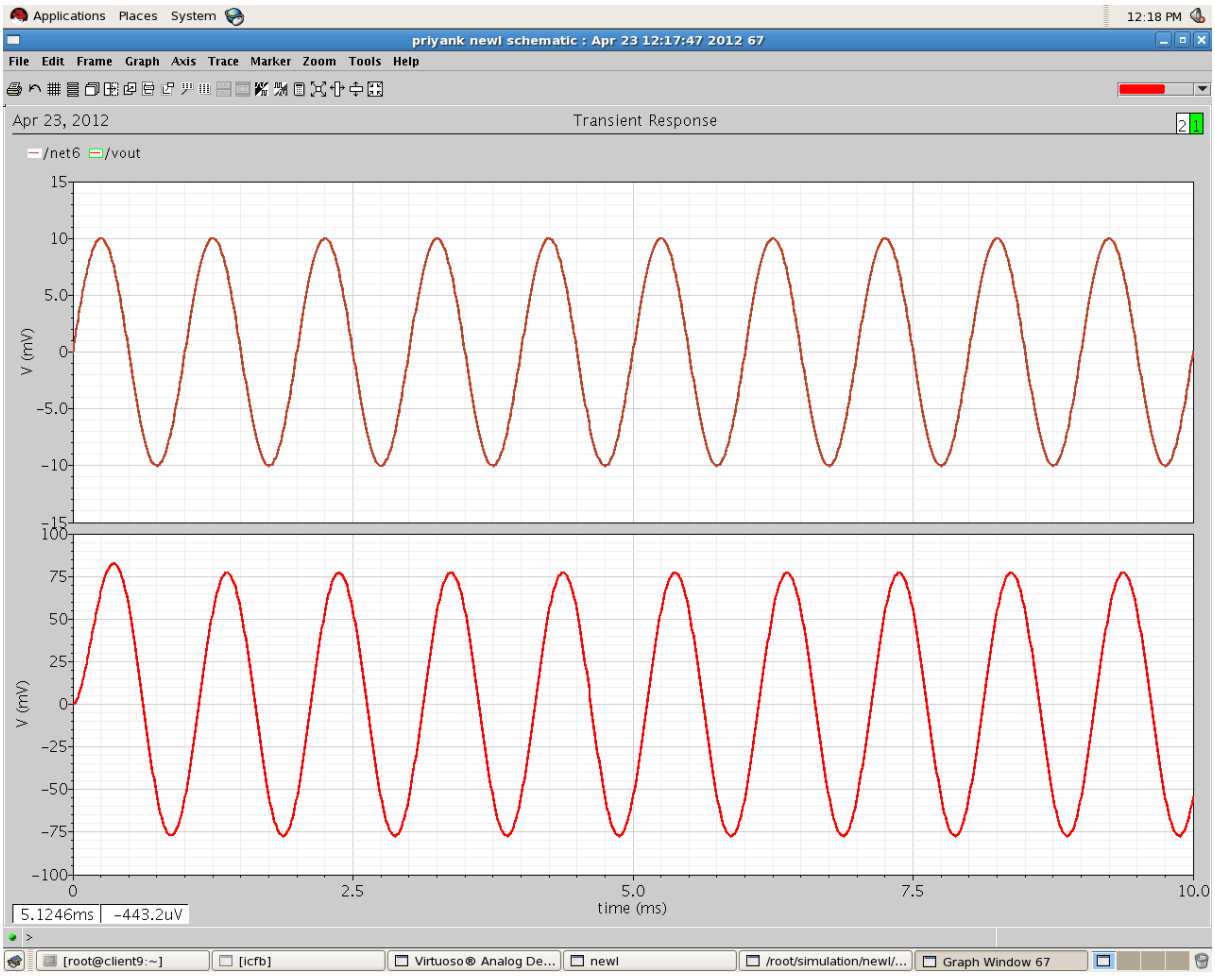

Fig. 5.4.2 Transient Analysis of low pass filter

5.4.3) AC Analysis of Low Pass Filter

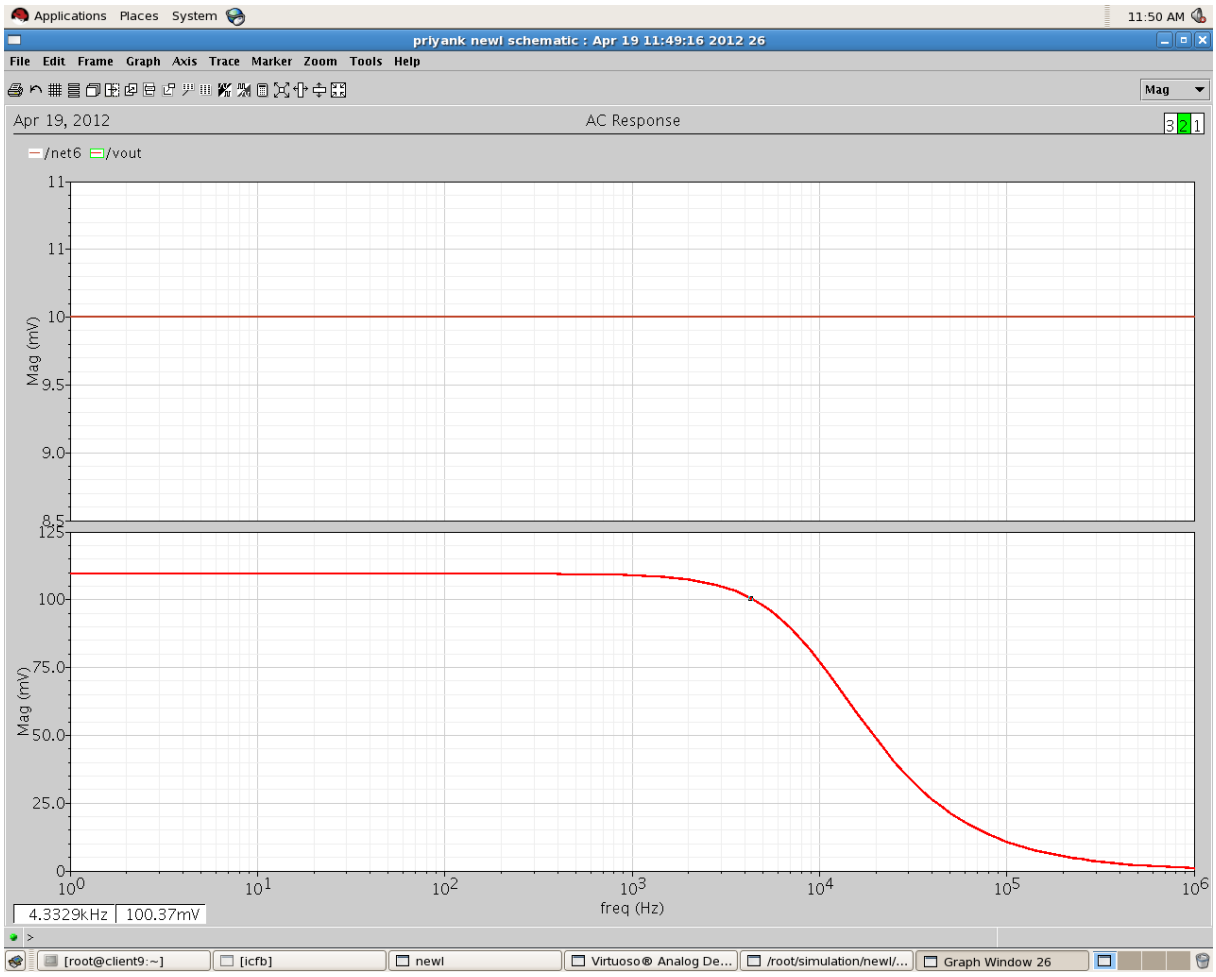

Fig. 5.4.3 AC Analysis of Low pass Filter

5.4.4)Transient Analysis of High Pass Filter

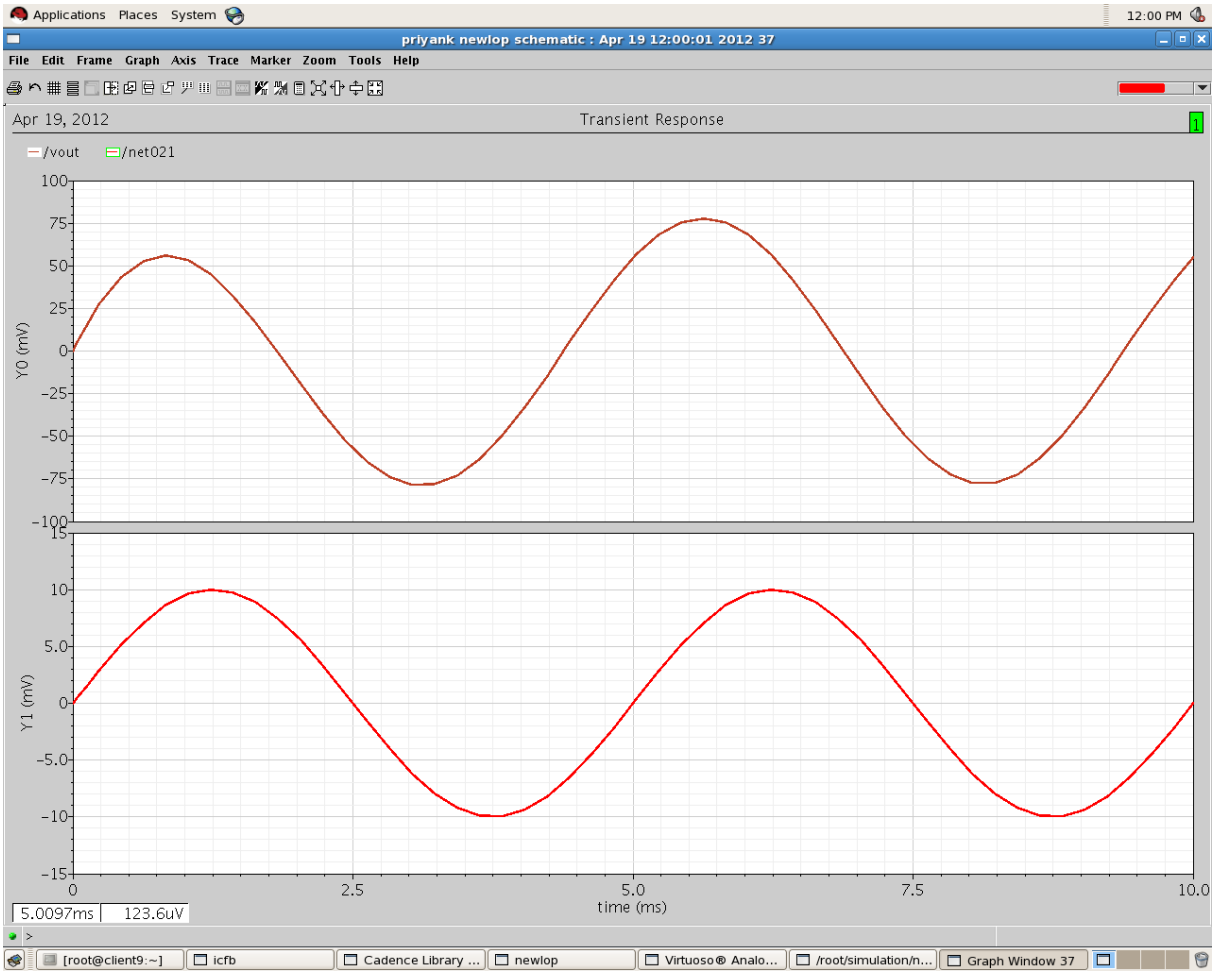

Fig. 5.4.4 Transient Analysis of High pass filter

5.4.5) AC Analysis of high Pass Filter

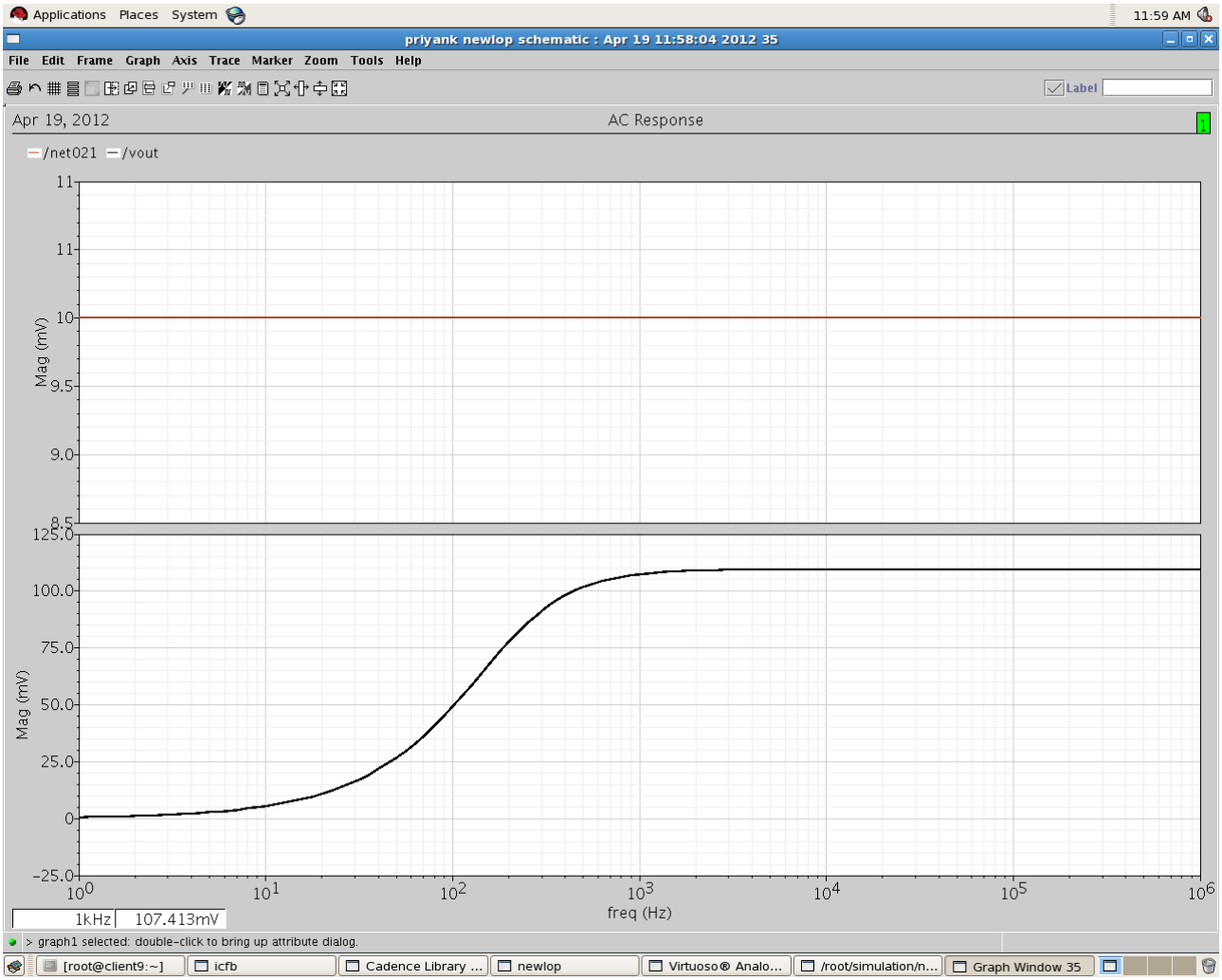

Fig. 5.4.5 AC Analysis of High pass Filter

5.4.6)Transient Analysis of Band Pass filter

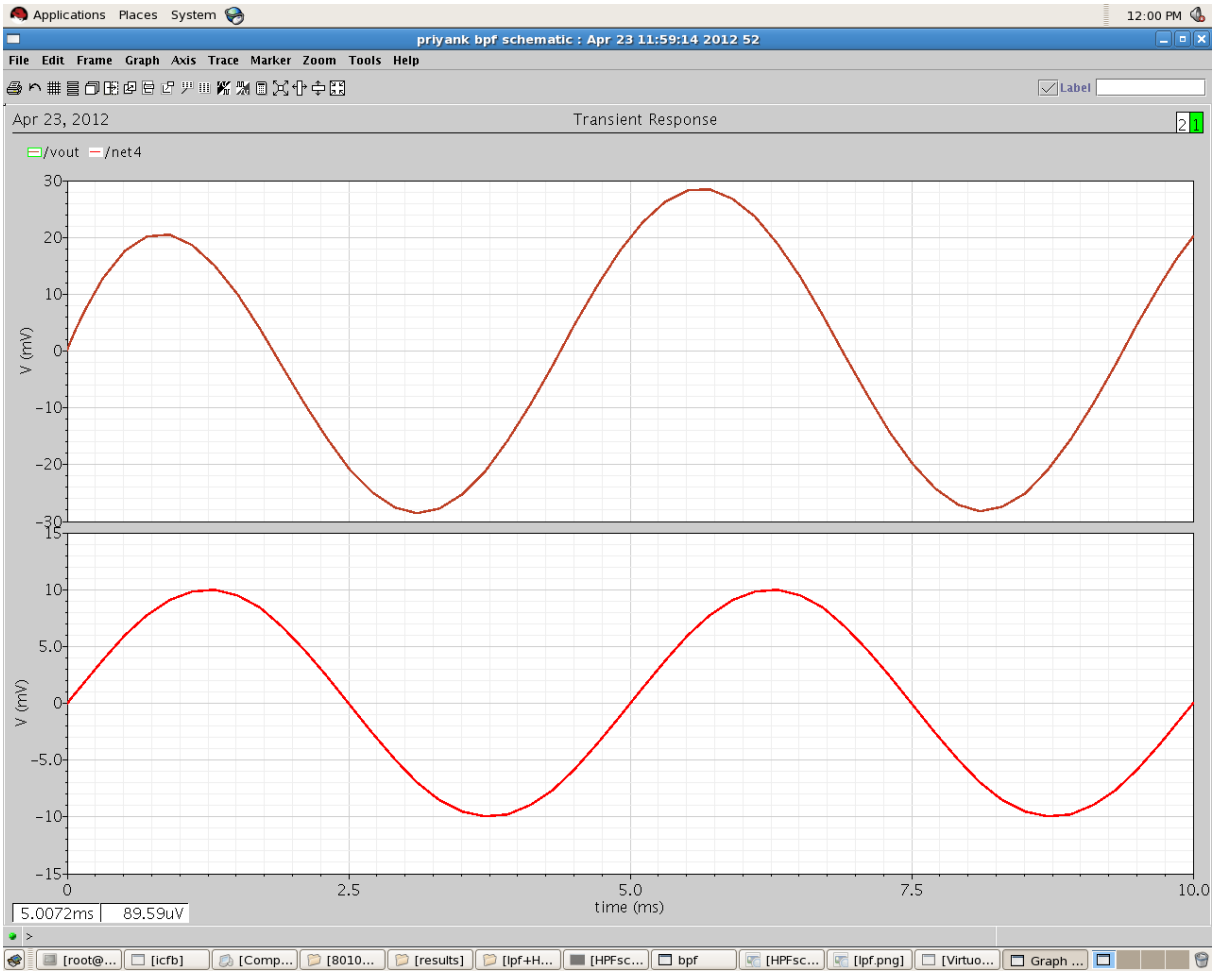

Fig. 5.4.6 Transient Analysis of Band pass filter

5.4.7)AC Analysis of Band Pass filter

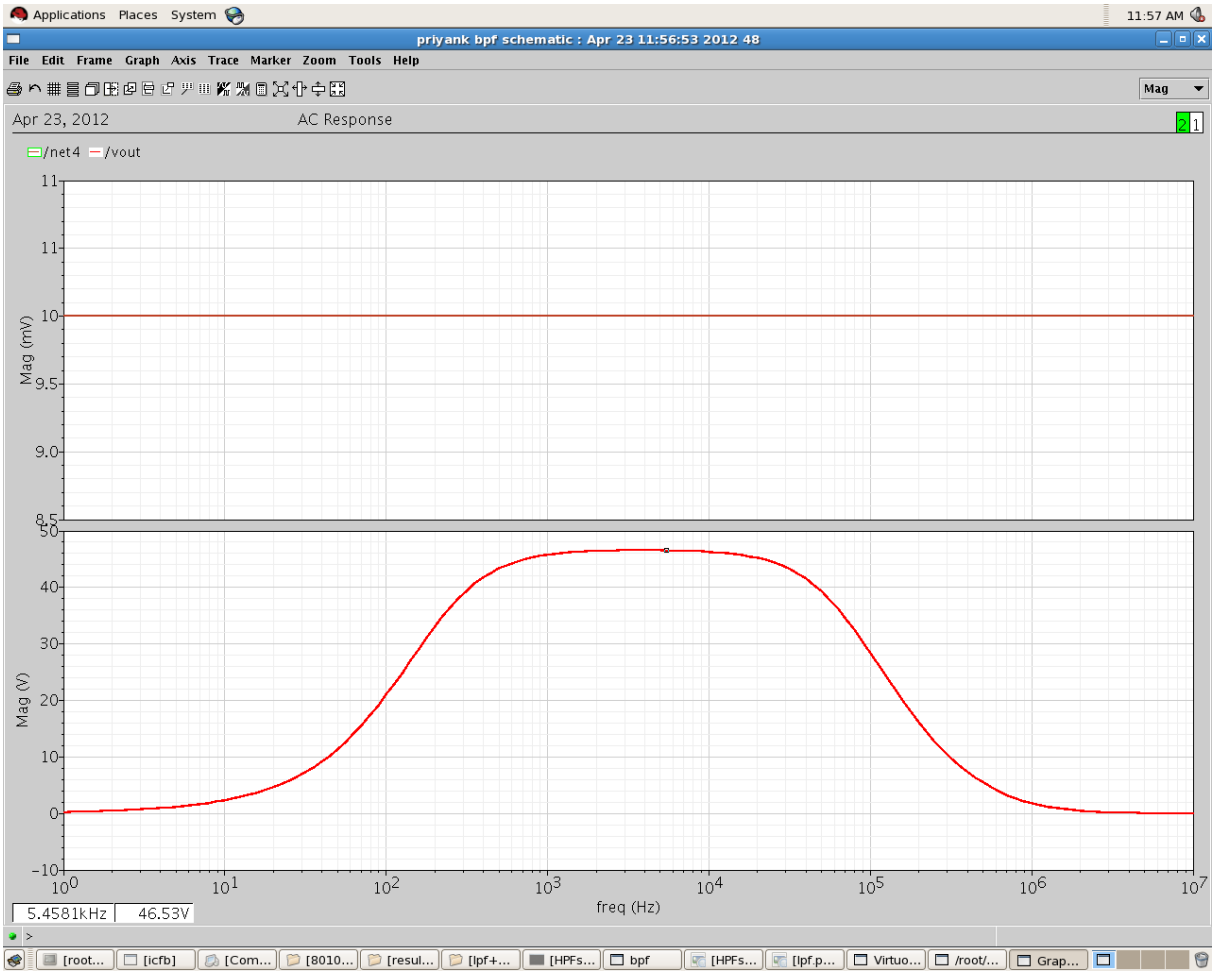

Fig. 5.4.7 AC Analysis of Band pass Filter

The analysis of all the 3 filters ie,low pass,band pass and high pass filter has been done.

5.5 COMPLETE SYSTEM RESPONSE

As low pass filter is the final stage of the low power low voltage amplifier system so we have combined analysis of low pass filter with the analysis of whole system.

5.5.1 COMPLETE SYSTEM SCHEMATIC

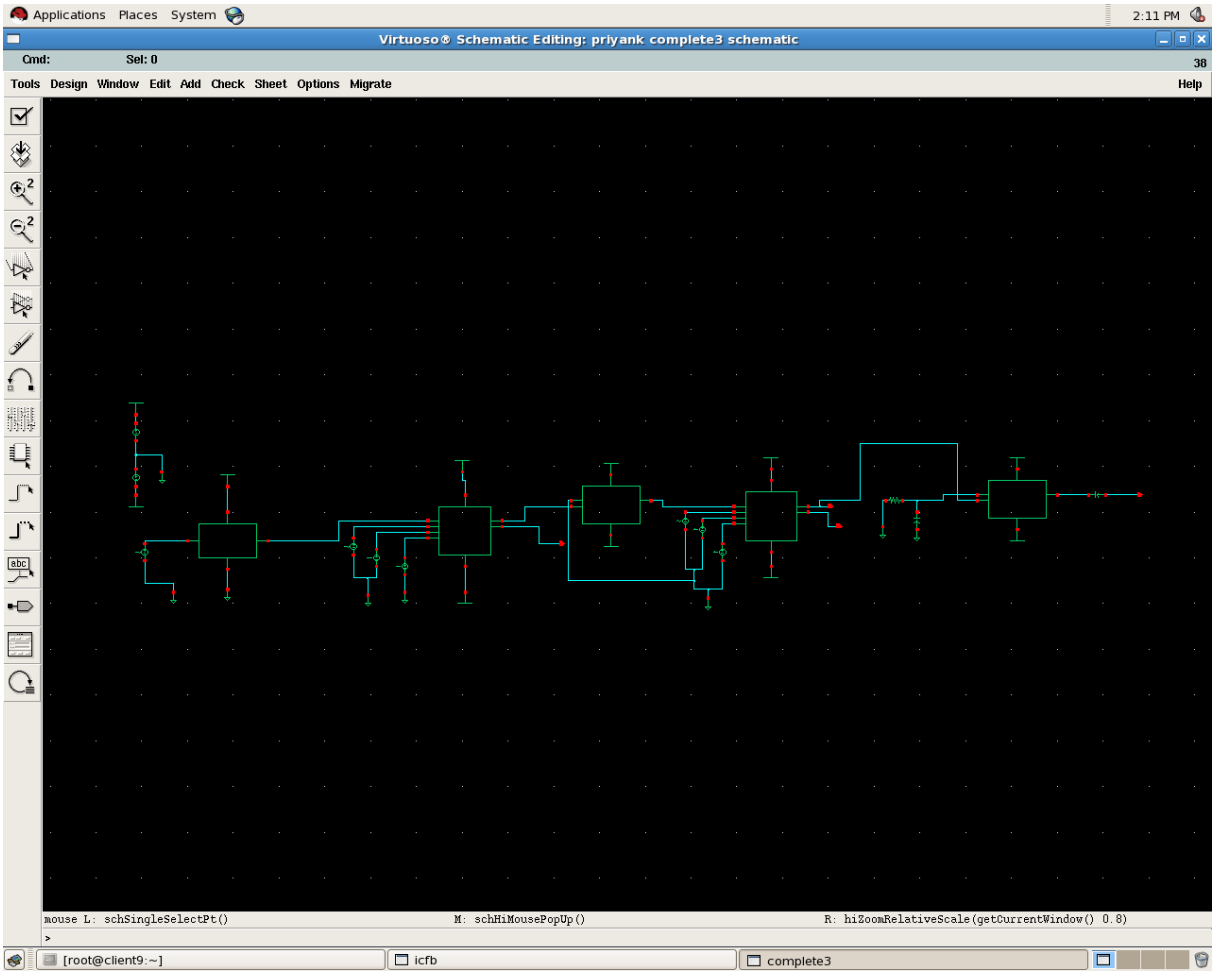

Fig. 5.5.1 Schematic of complete system

5.5.2 Total power consumed.

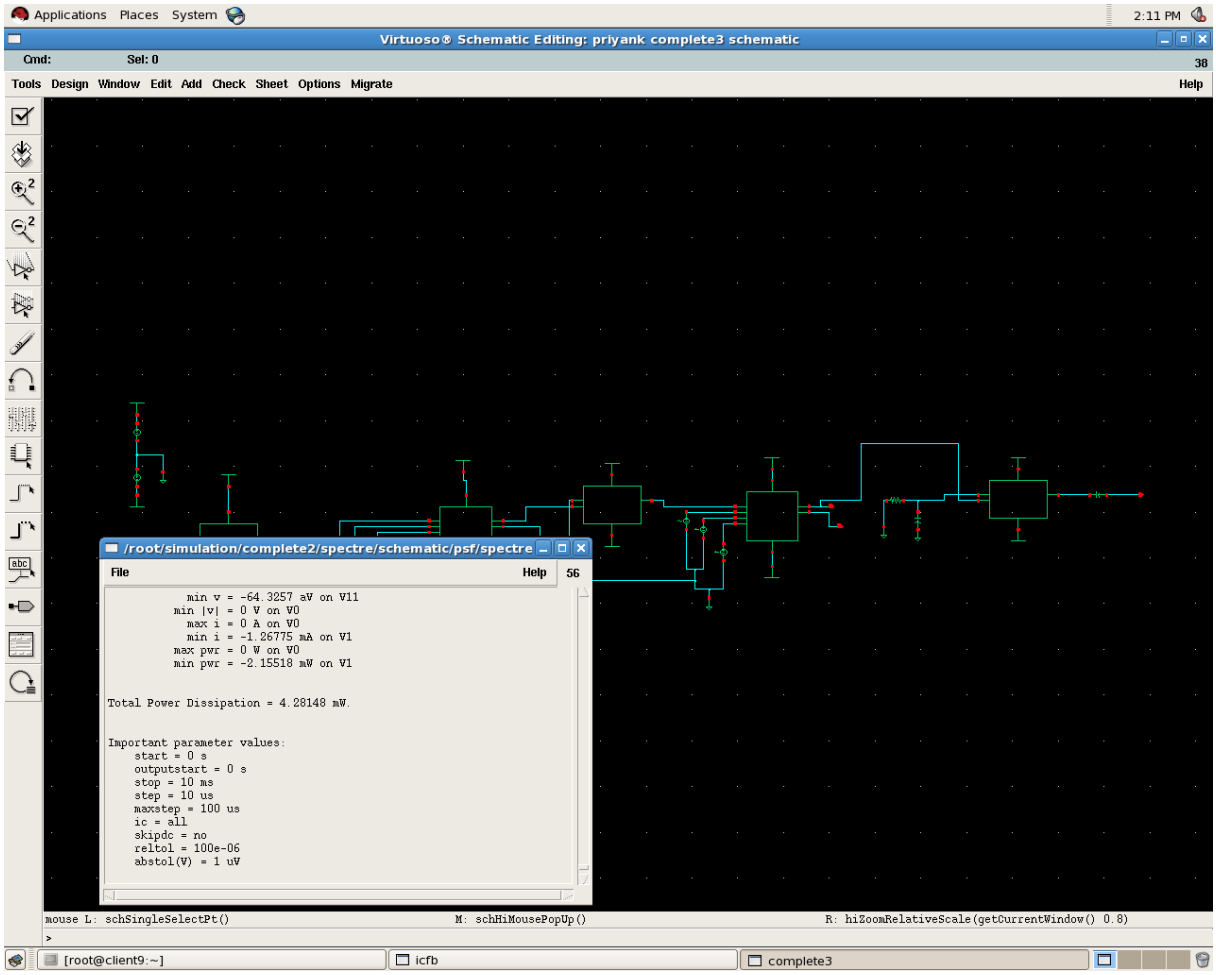

Fig. 5.5.2 Power consumed by complete system

Thus the total power consumed is 4.2 mw. And the power supply that we have used is 1.8V.Thats why it is called low power low voltage amplifer**.**

5.5.3 Noise Analysis of complete system

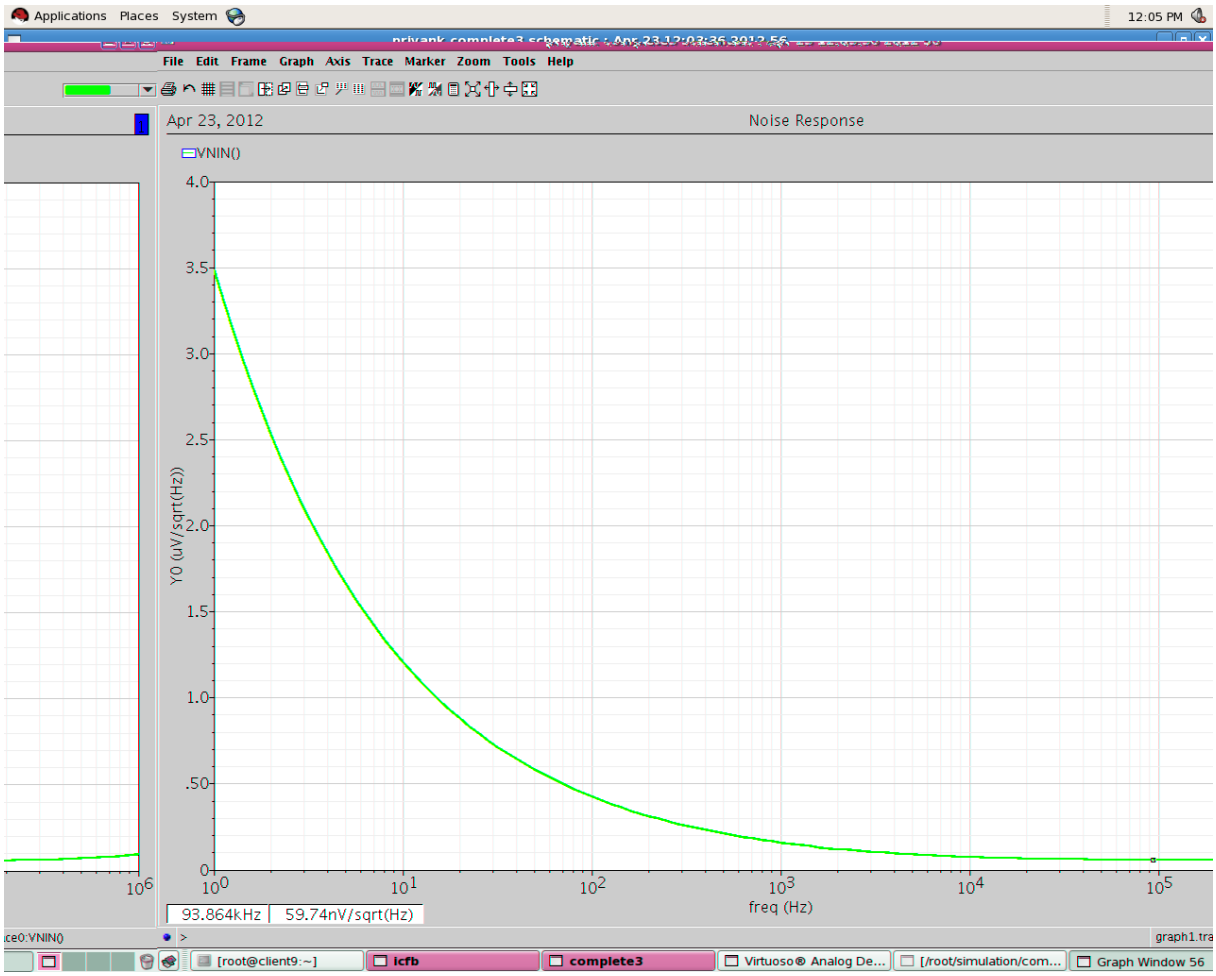

Fig. 5.5 Input referred noise response of Whole Low Power Low Voltage Amplifier system

As we can see from the graph that at 94 KHZ it shows the input referred noise response of 59.4 nano volt/sqrt(HZ).

5.5.4Transient Analysis of complete system.

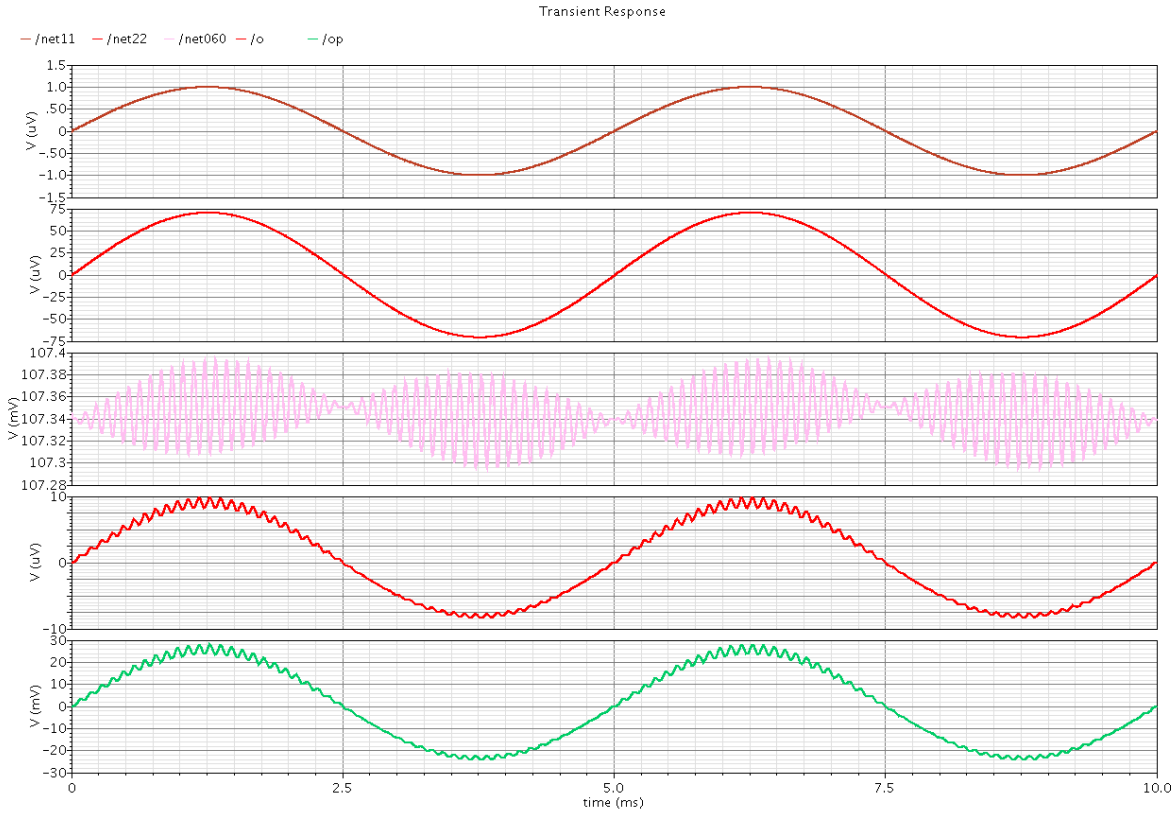

Fig. 5.5 Transient Response of Whole Low Power Low Voltage Amplifier system

Here net11:input

Net22:output after preamplifier

Net 060:output after modulator and gain stage

Net /o:output after demodulator

Net/op: Final output

Transient response shows that whole system is working properly as input sinusoidal is being obtained at the output without any distortion or clipping. As the output wave form is symmetrical about zero.Thus,the offset has been removed. From fig. 5.5 we find the gain of whole low power amplifier system is =25 KV/V.As our system is operating on 1.8v and it is consuming only 4.2 mw that's why it is called low power low voltage amplifier system.

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

A novel design of low power low voltage amplifier system for the removal of offset and noise has been presented in this thesis. It employs preamplifier, modulator, composite cascode amplifier, demodulator and low pass filter. The analysis of individual blocks as well as the analysis of complete system when connected in cascade is shown. The low pass filtering action removes the unwanted spectral generation around the even harmonics. The proposed low power low voltage amplifier system overcomes the drawbacks of existing offset and noise removal techniques of auto zero and chopper stabilization. Auto zero suffers from the main disadvantage of unreliability while in case of chopper stabilization the offset only get shifted to higher frequency instead of totally removed. It also provides much better gain to the applied signal without distorting the signal characteristics. To support above facts simulation waveforms have been included.

This system can be used in variety of applications where system operates on low frequency and amplitude signal. In fact this system is much cheaper and is also much more compact then the existing techniques.

As a further step, the layout of the system can be prepared and eventually the system can be fabricated and utilized in real life applications.

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