M. TECH. PROJECT REPORT

ON

Implementation of Simulated Inductor with recently introduced active building blocks

Submitted by

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CERTIFICATE

This is to certify that the thesis entitled **"IMPLEMENTATION OF SIMULATED INDUCTOR WITH RECENTLY INTRODUCED ACTIVE BUILDING BLOCKS"** being submitted by V V Udaya Bhanu in the partial fulfillment for the award of degree of Master of Technology in Control and Instrumentation of Electrical Engineering Department of Delhi Technological University is a record of bonafide work done by him under my supervision and guidance. It is also certified that dissertation has not been submitted elsewhere for any other degree.

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ABSTRACT

In this work few simulations of inductors is performed with recently developed active devices. Firstly, a Bipolar transistors based Operational Transconductance Amplifier (OTA) was used for realizing floating positive and Negative Inductance. The simulated inductance values can be controlled electronically by adjusting the bias currents of the OTA. Each inductance simulators comprises of only two OTAs and one grounded capacitor, without any external resistors and components matching requirements. The performance of the floating Positive inductance is verified by an series RLC resonant circuit while the performance of the Negative floating inductance is verified by an inductance cancellation circuit [1]. Secondly, a current mode CMOS based Modified Dual Output Differential Difference Current Conveyor (MDO-DDCC) is used for realizing a grounded inductor. The grounded inductance simulator comprises of only one current conveyor, two resistors and one grounded capacitor. The performance of this inductance is verified by an parallel RLC resonant circuit [2]. Lastly, a Bipolar transistor based Four Terminal Floating Nullor (FTFN) with electronically tunable current gain was proposed. It mainly employs a transconductance amplifier, an improved translinear cell, two complementary current mirrors with variable current gain and five improved Wilson current mirrors which provide high bandwidth and suitability to implementation in monolithic bipolar technology. The performance of this FTFN is verified by a Voltage to Current converter and an All pass filter [3]. Then, this FTFN is employed for realizing a floating inductance comprising of four resistors and one capacitor. The performance of this floating inductance is verified by an Low Pass and High Pass filter [4]. All the above computer simulations were performed on Pspice simulator. The Bipolar Transistors were employed using AT&T ALA 400 transistors parameters while, the CMOS were employed using 0.35um TSMC CMOS technology parameters.

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