CHAPTER-1

INTRODUCTION

The demand for electronic circuits with extremely low supply voltages and power consumption is important in development of microelectronic technologies. In many applications, additional requirements appear, particularly the extreme speed, on accuracy, compactness, cost etc. Simultaneous fulfillment of the above demands is problematic. Thus, in order to fulfill all the demands depending upon the requirements, electronic circuits have grown and provide ease to the circuit manufacturer in the past few decades.

Inductor, one of the most widely used passive devices is one of them, which keeps on modifying depending upon the requirements of the circuit manufacturer. The inductor is widely used in analog signal processing. The applications can be found in communications, electronics and measurements such as active high-Q filters, quadrature oscillators, resonance circuits or analog phase shifters. For integrated circuits, a spiral inductor can be realized. However, inductors of practical values on silicon wafer suffer from the use of large areas of chip, their inductance values are not variable. Moreover, the spiral inductor can be realized in an integrated circuit, it still has some drawbacks in the usage of space, weight, cost and tenability. Therefore, they are generally replaced by active inductance simulators. Chapter 2 basically deals with the literature review providing attention on the number of active inductance simulators based on different design techniques have been developed in the literature [5-75].

One of the major problem with inductor to be realized in an integrated circuit is its size and tenability .In order to realize the Inductor in an integrated circuit a the attention is focused on high performance Operational Transconductance Amplifier based inductance circuits, which is been taken in Chapter 3. The main advantage of OTAs is that they are suitable for working with current mode signal processing devices. Moreover, the proposed inductance simulation performed enjoys several features for instance, both positive and negative floating inductance can be simulated with little modification in the circuit, electronic tenability, circuit simplicity, use of grounded capacitor which can be easily fabricated for VLSI, free from component matching.

The performance of the proposed Positive and Negative Inductance is verified with Series RLC resonant circuit and Inductance cancellation circuit. In the last two decades, the evolution of modern applications of analog signal processing has followed the trends of so-called current mode, where signals, representing the information, are in the form of electric currents. In contrast to the conventional voltage mode, which utilizes electric voltages, the current mode circuits can exhibit under certain conditions among other things higher bandwidth and better signal linearity. Since they are designed for lower voltage swings, smaller supply voltages can be used. The main advantage of using current mode technique is because the non-linear characteristics exhibited by most field effect transistors. A small change in the input or controlling voltage results in a much larger change in the output current. Thus for a fixed supply voltage, the dynamic range of a current mode circuit is much larger than that of a voltage mode circuit. If a supply voltage is lowered, one can still get the required signals represented by the current. Secondly, the current mode circuits are much faster as compared to voltage mode circuits. The parasitic capacitances present in the analog circuits must be charged and discharged with the changing voltage levels. In a current mode circuit, a change in current level is not necessarily accompanied by a change in the voltage level. Hence, the parasitic capacitances will not affect the operating speed of the circuit by a significant amount. Other advantages of using current mode circuits are that they do not require specially processed capacitors or resistors; they are more compatible with digital CMOS technology making integration of mixed signal circuits more feasible. Simultaneously with the development of current-mode applications, the mixed- mode circuits are also analyzed because of the necessity of optimizing the interface between the sub-blocks, which are working in different modes. The mixed-mode operation and even the comeback to the conventional voltage mode also have another justification: it appears that some generally accepted statements about the advantages of the current mode probably have no real basis.

Thus, the Chapter 4 deals with one of the universal current mode building block i.e. current conveyor which is used to implement the inductor. In this chapter a modified Dual Output Differential Difference Current Conveyor (MDO-DDCC) is been used to realize the grounded inductance simulator. The main advantage with this

topology for realizing grounded inductance is that it uses only single current conveyor, tow resistors and a grounded capacitor.

The differential difference current conveyor is proven to be useful in many voltage and current mode analog signaling application thus allowing analog designers for implementation of integrated circuits with less active elements. Moreover, MDO-DDCC also provide the flexibility of dual output which provide freedom of taking either positive or negative output directly to the analog designers.

In Chapter 5 one of the recent developing current mode device i.e Four Terminal Floating Nullor (FTFN) based Inductance simulator was proposed. FTFN has the advantages of current mode device like higher bandwidth, wider dynamic range, simpler circuitry, low power consumption and flexibility in designing. A bipolar transistor based tunable FTFN has been proposed in which current gain can be tuned by adjusting the bias currents. The performance of the proposed tunable FTFN was verified by an Voltage to Current Converter and an All Pass Filter. The proposed tunable FTFN is used further to realize a floating inductance. The main advantages of the proposed inductance are that it only employs four resistors and 1 capacitor. The performance of the proposed inductor simulator was verified by a Low pass and High pass filter.

Chapter 6 deals with the conclusion and the future directions for the improvement of this project.

CHAPTER 2

LITERATURE REVIEW

With the advent of technology day by day during mid-1940 every next year there was some new electronic device in the market which tries to dominate the market share of the earlier products. At that time the devices are been made with the knowledge of market value of that product which is been happening till now but now the manufacturer also take care of other important factors like the ease of usage, environmental factors and other key factors.

One of the most important inventions which bring the boost in the field of electronics was the invention OPAMP in 1941 which was vacuum tube based. During early 40's to early 60's many new modifications came on the vacuum tube opamp either it's on the type of the manufacturing technique or some better properties of the earlier one. But the remarkable invention which just catches the sight of every electronic circuit's designer was the monolithic opamp which was small and easy to use with the eye-catching property of decreased price. After that both the opamp and electronic circuits mark their presence in the market. In the early 60's inductor size and cost was one the important problem with every electronic circuit designer thus in order to overcome these problems many research papers were presented.

In the mid 60's an attempt was made to manufacture a inductor with single differential input opamp (DVopamp) along with few passive components (R, C) [5]. Usually the two functions of positive-immittance inversion, for transforming a capacitance into an equivalent coil, and negative-immittance conversion, for cancelling the loss of the equivalent coil, are carried out separately, using one or more distinct amplifiers for each process. In this paper a single differential input opamp is been used to make an inductor. In the same year another paper was presented which also used the (DVopamp) but its performance was better that the earlier one in terms of Q factor which appears to be limited primarily by the losses in the capacitors used [6]. Then in early 70's an attempt was made to manufacture a grounded inductor using unity gain opamp along with few passive components [7]. In the year 1970 first attempt was made to make an inductor using Gyrator which has resulted some new circuits for inductor fabrication [8]. In the next year opamp based negative impedance converter was used

to fabricate the inductor [9]. In the mid 70's a lossy inductance was fabricated which require only two amplifiers to produce a floating inductance with series or parallel resistance[10], the circuits described in this paper were much more sensitive than the circuits which were presented earlier. In the same year active RC realization of a lossy floating inductor is presented. The circuit uses two operational amplifiers each in the unity gain connection along with three resistors, and two capacitors, and has low L and Q sensitivities to passive as well as active components [11], the main advantages of this inductor circuit was low component count, unity spread in resistors and capacitors, easy adjustment, low sensitivities, absolutely stable configuration, unity gain. During the same time another paper was presented which give further proof of the usefulness of the complementary property, by applying it to generalize existing two operational amplifier four-terminal gyrator circuits for lossless grounded inductance realization, such that they can simulate also the lossless floating inductance[12]. In the early 80's resistance controlled inductor circuit were fabricated. This RC circuit is proposed for the realization of lossless floating inductance employing three operational amplifiers as unity-gain summers, three external resistors and a single grounded capacitor this new circuit realizes an inductance that is controllable through a single resistor [13]. The inductor circuits obtained using RC circuits have remarkable sensitivity properties this lead to a new realization of general second-order driving-point impedances with only one opamp and with a minimum number of capacitors and resistors. The method is based upon an interesting property of active RC driving point impedances which is derived in the paper [14]. During early 90's opamp based grounded inductor was made which is very easy to understand and is based on general techniques [15]. During mid-95 a four operational mirrored amplifier (OMA) based floating impedance configurations are presented which require only three OMAs while preserving all other advantageous features of the earlier structures [16]. In the year 2005 current conveyor based inductor circuits were also started its journey to further modify the inductor circuit while maintain all previously discussed advantageous features [17]In the year 2008, using a minimum number of passive components, i.e., new grounded and floating inductance with two modified current-feedback operational amplifiers (MCFOAs), are proposed. The type of the simulators depends on the passive element selection used in the structure of the circuit without requiring critical active and passive component-matching conditions and/or cancellation constraints [18].

During early 60's when the first monolithic design of opamp was presented at the same time operational transconductance amplifiers (OTA) were also fabricated. It is essentially a controllable resistance amplifier. The control input is a current. Like an operational amplifier, there are differential inputs. These inputs are used to modulate the control current. Thus Unlike an opamp, the output of the OTA is a current. Unlike an op amp, there is not a single resistor in the OTA circuit. The working of OTA is primarily based on the working of current mirrors. Since the OTA are originated from OPAMP hence the OTA based inductor model were not that mush old.

In the mid 2005 a paper was presented which employs OTRA based grounded parallel immitance (combination of inductance and admittance) simulator topology. The proposed circuits use two OTRAs and require fewer passive components than most of the counterparts in the literature. The other key reason to use OTRA was the grounding of input terminals because of which most of the effects of parasitic capacitances and resistances disappear [19]. During the same time another paper was presented in which the finite bandwidth effect which was neglected in the previous work is now been included. Furthermore, the accuracy of this passive equivalent circuit is compared with the active OTA-based floating inductor [20]. In the same year 2 circuits which are floating positive and negative inductance simulators using Operational Transconductance Amplifiers (OTAs). The main advantage was the simulated inductance values can be controlled electronically by adjusting the bias current of the OTA. Moreover, inductance simulator comprises only 2 OTAs and 1 grounded capacitor without any external resistor and component matching requirements [21].Then during mid-2007 a research paper was presented which primarily focuses on the alternatively structured higher performance practical OTA-based floating inductor which requires four OTAs which was found to be practically far superior to its Three-OTA counterpart [22].After this a paper proposes a novel systematic method of generating active inductor circuits. It is a graph-based approach that consists of building a flow-graph of a structure without inductors, whose transfer function is equivalent to the impedance or the admittance of an inductor, and then generating the equivalent circuit with only RC elements along with OTA controlled sources and, in some cases switches. The switches are controlled by the type of the graph (a voltage graph or a current graph) [23]. In the paper [21] four OTA based floating inductor was

made which is been reduced to one inductor based floating inductor having all the desirable properties of the earlier OTA based inductor [24].

Though, the use of OPAMP and OTA based inductor circuit has decreased the size and reliability of inductor circuits extensively, but in few cases it is been required to use the inductor in the integrated circuits where the OPAMP and OTA based inductor circuit started showing constraints on minimizing the size of integrated circuit in which it is to be used. Thus in order to overcome this issue complementary-symmetry metal oxide semiconductor (CMOS) based inductor circuit got the popularity. The words "complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions.

In the mid 90's a RF CMOS active inductor is described. The circuit is based on a CMOS GIC. The advantage of this CMOS based inductor to its counterparts was the inductor loss which was reduced by applying gain enhancement techniques based on cascoding. Moreover, the proposed new inductors exhibit lower loss, high self-resonance frequency and wider inductive region [25]. After few years an CMOS based fully differential floating active inductor is realized by exploiting the intrinsic capacitance of the transistor. This technique allows the simulated inductor to operate closer to the f_t of the technology. The advantages of using active inductors are evidently the reduction of chip area and processing cost which would have occurred in the fabrication of a high-performance integrated passive inductor, and also the increased tunability. However the main disadvantage is that noise in an active inductor is proportional total inductance quality factor, leading to a trade-off between power and dynamic range [26]. In the year 2000 another paper was presented which tries to overcome some of the problems faced by earlier CMOS based designs. This new circuit configuration of VHF CMOS transistor-only active inductor which allows very high frequency operation under low power supply voltages (< 2 V) is proposed. Gain enhancement techniques are applied to reduce the inductor losses achieving high Q and wide operating bandwidth [27]. After few year Fully CMOS compatible, highly suspended spiral inductors have been designed and fabricated on standard silicon substrate (1-30Ω-cm in resistivity) by surface micromachining technology (no substrate

tech involved). this is the CMOS compatible spiral inductor is capable of achieving Q factor of 70 at 6GHz frequency which is the highest Q factor ever reported on standard silicon substrate at this frequency [28].The main problem with these Fully CMOS based spiral inductor was to measure its inductance accurately. This problem was solved in a paper presented after 2 years in which different methods were presented for the calculation of inductance. The experimental circuit for inductance measurement, designed in this paper is produced in CMOS 0.35μm technology which includes several inductors of different shapes made of metal3 and metal4 [29]. In the same year floating and grounded inductance was simulated using only one Current Controlled Current Differencing Transconductance Amplifier (CCCDTA) was presented. The main advantage of this simulated inductance was the electronic control of inductance by adjusting just the bias current of the CCCDTA. The floating inductance simulator comprises 1 CCCDTA, 2 voltage buffers and 1 grounded capacitor, while the grounded inductance simulator comprises only 1 CCCDTA, 1 voltage buffer and 1 grounded capacitor without any external resistors and component matching requirements [30]. During the same period of time another paper came in which 4-OTA and 3-OTA based floating inductor circuit was fabricated structure which perform identically in the ideal phenomena where all OTA's are nonidealties i.e. parasitic elements, perform a similar comparative study of the 3-OTA and 4-OTA effect of finite open-loop bandwidth and noise have been neglected. But it is been proposed in this paper that the 4-OTA based floating inductor is better than the 3-OTA based inductor this conclusion has been made based upon the assumption that all OTAs are of the bipolar type[31]. In 2010 CMOS technology is used to fabricate an digitally controlled lossless floating inductor. The proposed inductor is based on current conveyors and resistor array to provide digital tuning of the inductance value. The programmable floating inductor can be tuned from 0.42763 mH to5.67 mH [32]. After few months Q-enhanced inductor using the tapped-inductor feedback technique was presented. Compared with conventional transformer feedback architectures, this proposed technique not only compensates for resistive losses with low power consumption but also provides a high-inductance inductor. The proposed method improves the Q-factor as well as the power consumption of conventional transformer feedback architectures [33]. In the mid 2011 another paper was presented in which frequency dependent floating inductor (FI) simulator circuit employing two CBTAs and three passive components was proposed.

The presented circuit can realize floating FDNR, inductor, capacitor or resistor depending on the passive component selection. Since the passive elements are all grounded, this circuit is suitable for fully integrated circuit design. The circuit does not require any component matching conditions, and it has a good sensitivity performance with respect to tracking errors [34]. Some observations are made on the progress in its realization and application over the past four decades. Recently, in the early 2012 a low voltage design of an active circuit for realizing a floating inductance depending on the selection of passive circuit elements was described. The circuit employs only two differential voltage second-generation current conveyors (DVCCIIs) at low voltage levels (±0.75 V) and does not require passive element matching. The circuit has a grounded capacitor for simulating the floating inductance [35].

With the growing interest in current mode analogue circuits, an historical account of the invention of the current conveyor is given. Some observations are made on the progress in its realization and application over the past four decades. New results on the monolithic implementation of the current conveyor are presented in the end of the literature review of current conveyor based inductor.

While making a voltage controlled waveform generator in the mid 60's Mr. Sedra has fortunately made a current controlled waveform generator under the supervision of Mr. Smith. But without being discouraged from his failure he tried to improve the earlier version of the circuit which resulted in the FIRST GENERATION CURRENT CONVEYOR-I(CC-I) whose characteristics is given below:

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (2.1)$$

To increase the versatility of the current conveyor, a second version in which no current flows in terminal Y, was introduced in 1968 called to be as SECOND GENERATION CURRENT CONVEYOR (CC-II)

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (2.2)$$

Now days even more modified current conveyor started coming with little changes resulting in improved characteristics behavior of its earlier counter parts. Although

more than twenty years old, the current conveyor appears to be an ‘idea whose time has come'. This optimistic view is based on the growing interest in analogue current mode signal processing, the improved fully integrated conveyor realizations and the vast literature on the application of current conveyors.

In the early 70’s improvised version of second current conveyor was presented which is used to form a function generator, gyrator, NIC, DVCCS/DVCVS etc. [36]. Then during early 80’s an active RC realization of a grounded inductance using the DVCCS/DVCVS as the active element is given. The circuit uses a single grounded capacitor which controls the magnitude of the inductor. Sensitivities to all passive and active circuit components are very low [37]. Then during the same time another paper was presented in which a single second generation CC-II as the active element and three passive components is proposed. The inductance is seen to be suitable for moderate applications [38] while in the other it was shown that inductors can be simulated with current conveyors using a very small number of passive components, namely only one capacitor and two/three resistors [39]. During the same time a new circuit which uses a single second generation CC-II, a single capacitor, and only two resistors a lossy frequency-independent floating inductance without requiring any equality constraint is presented [40].During the same year there were some errors were shown on the work done by Mr. Senani which was presented in [41] which were been reasoned appropriately [42]. In the same year two new schemes for grounded inductor simulation with single grounded capacitors using the CC- II were reported. The main advantage of this paper was that the Q factor can be independently adjusted and hence are suitable for high quality application.

Moreover the inductance and its Q factor are and it L and *Q* are insensitive to the changes in the active CC- II parameters changes [38]. After few years two new active *RC* networks employing CC-II as active elements, are proposed for the realization of series/parallel floating RL impedances. The attractive features of the circuits are that they do not require any component matching, facilitate independent control of inductance value through a single resistor, and employ a single capacitor along with a low resistor-count [43].During the same year a new lossless synthetic floating inductance circuit, employing a grounded capacitor and CC-IIs as active elements is presented which in contrast to recently reported circuits during that year does not require any component matching condition for the desired realization. The

other novel features of the circuit are the use of a minimum possible number of passive components and inductance control through a single grounded resistor [44]. Next year three new active *RC* synthetic floating inductance circuits were proposed which realize lossless floating inductance and series and parallel *RL* impedance, respectively employing three and two CC-II as active elements. The novel features of the new circuits are that in contrast to available OPAMP circuits for floating inductance simulator, the circuits presented here do not require component matching for the desired realization, the new circuits employ a minimum possible number of passive elements (only two resistors and a capacitor), in all the new circuits, the inductance value is independently controllable through a single resistance [45]. Then during early 80's a grounded inductor using single CC-II was proposed. The realization method is quite versatile and can produce a grounded impedance that may be bilinear RL , ideally inductive or inductive with a positive or negative resistive part either in series or in parallel [46]. Then there were some modification in the work done in [35] i.e. the floating inductance circuit may be shown to be a DVCCS analogue of a previously published floating inductance circuit using operational amplifiers. A more thorough treatment of the comparison of three recently reported inductance simulation circuits is presented in reply to the comments made [47]. During the end of the same year a paper was presented in which an simulating ideal floating inductance was presented. The main advantage of this paper is that the floating inductance was tunable through a single resistor and it has been shown that it is possible to simulate these realizations with unmatched passive components [48]. Then during early 80's a CCII-based circuit using a single grounded capacitor for single resistance controlled lossless floating inductance simulation was presented [49]. Then during early 90's a lossless floating immittance using CCIIs was proposed. The main advantage in that paper was that the simulated circuit was capable of introducing Nullator Norator technique by which many simulation circuits can be derived systematically [50]. During the mid-90's a number of new second order current mode circuits were presented. For the derivation of these circuits a new current mode building block, the general current conveyor, is used. Then using these new circuits' inductors outputs were compared which are more reliable and close to the ideal characteristics of grounded inductor [51]. Thus an era had begun where changes in the CC-II were started observing which resulted in the development of third generation of current conveyor (CC-III). During 2000 an actively

simulated grounded lossy inductors using CC-III was proposed. The main advantage of using CC-III was that they do not require passive component matching to obtain the desired type of inductance [52]. During the end of 2003 a novel floating inductance simulator, based on CC-II was presented. The circuit shows the capability of regulation and, in theory, cancellation of the undesired inductance series resistance, with consequent increase in the low frequency operating range [53]. Then during the mid-2005 a lossless floating inductor using CCCIIs and single capacitor is presented. The proposed inductance simulator can be tuned electronically by changing the biasing currents of the CCCIIs [54]. During 2006 two novel circuits for realizing floating inductance depending on the passive component selection are proposed. Both of the proposed simulators employ CCCIIs and only grounded passive elements [55]. The main advantage of this paper was that it does not require critical component matching constraints thus it is easy to fabricate the presented circuits in fully IC technology. During the mid of 2007 a novel hybrid inductor is proposed. The circuit is a hybrid of an operational amplifier and a current conveyor with three passive elements, and offers advantages over conventional current conveyor implementations in its ability to produce high quality factor inductors [56]. The other advantage of the proposed hybrid circuit of the new introduced inductor was that it can be used as a monodirectional floating inductor, a grounded inductor or a true bidirectional inductor. In the true bidirectional mode only the number of active components is increased over the monodirectional mode without increasing the number of passive components required. Then in the year 2008 a paper was presented in which the inductor in been made using CC-II with improved performance even at low frequency [57]. During February a differential voltage current conveyor transconductance amplifier (DVCCTA) device with a single RC section is used to make a synthetic grounded lossless inductor circuits. The advantage of this inductance over its counterparts was that it is practically active insensitive to the device port mismatch errors and there is no component matching constraint [58]. During the mid of the same year an paper was presented which suggested the realizations of emulators transforming memristive devices into effective floating memcapacitive and meminductive systems. The emulator’s circuits are based on second generation current conveyors and involve either four single-output or two dual output current conveyors [59].

The concept of Nullator, Norator and Nullor was originated during 1961-1964, Y. Carlin and Youla [60]. Till about 1984 they were widely used for generating equivalent networks of BJT and op-amps based circuits such as gyrators and impedance converters/inverters. However, nullator, norator and nullor got real stimulus when fully floating versions of opamps and nullors were shown to be more versatile and flexible in several applications by a number of researches during 1984-1990 such as Nordholt [61], Senani [62] where the term four terminal floating nullor was coined. Thus FTFN got going and soon attracted the attention of the circuit. In the year 1987 Senani suggested a CCII based FTFN which become the preferred choice of the designers later it got modified depending upon the requirements of the analog designers [63]. Later AD844 was used to build the FTFN. During the early 2000 many researches were going on the use of FTFN like single resistance controlled sinusoidal oscillator based on FTFN suggested by Liu [64], realizing of R-L and C-D immittances using single FTFN by Lee [65], build a current mode inverse filter [66] etc. During 2000 Kuntman and Cam suggested a CMOS based FTFN model [67] which is composed of two translinear cell and one cascade current mirrors. The main advantage of the proposed circuit is quite suitable for wideband, accurate and wide dynamic range current-mode signal processing. Then, FTFN with tunable current gain models also came in the same year [68, 69]. In the year 2001 multiple output FTFN start coming in the market [70]. In the year 2002 fully balanced model of FTFN was proposed. The main advantage of the proposed circuit was low power and CMOS implementation [71]. Then, these BJT and CMOS based FTFN were started using in applications like filter design, tunable multiple output FTFN based filter [72]. In the year 2007 a multiple output OTA based FTFN was suggested. The main advantage with this method was the tunability, constant bandwidth, and minimum number of passive components utilization [73]. Presently FTFN are utilized for realizing various filters, oscillator's design [74]. In the year 2010 PFTFN based lossless inductance circuit was also suggested by P. Kumar [75] with minimum passive components which was further used to implement filters circuits.

CHAPTER 3

OPERATIONAL TRANSCONDUCTANCE AMPLIFIER BASED INDUCTOR

3.1 Introduction

Presently, there is the interesting desirability of building active filters and other signal processing circuits without the use of physical coils. Although, a spiral inductor can be realized in an integrated circuit, it still has some drawbacks in the usage of space, weight, cost and tunability

In this chapter attention is subsequently focused on the inductance simulation using high-performance active building blocks i.e. Operational Transconductance Amplifier (OTA) based Positive floating Inductor which is used extensively as a building blocks for instrumentation application which include voltage controlled oscillators, active filter design, oscillator design, analog phase shifters and cancellation of parasitic element etc. The building blocks considered here is Bipolar Transconductance Amplifier, which is used for the successful implementation of Operational Transconductance Amplifier.

Not only the positive inductance simulator, but also the negative inductance simulator is also important circuit. It is found in many applications such as active filter design, oscillator design, analog phase shifters, impedance matching in microwave circuits, to minimize reflection at the input of antenna, to compensate bond wire inductance and cancellation of undesirable inductance.

To summarize, the main thrust of the work presented here has been on the review of the prominent work in the area of active building block based Floating Positive and Negative Inductance based devices. The recently developed Active devices based Operational transconductance Amplifier with their so many advantages has been used to develop many processing elements used in electronics and instrumentation control.

3.2 Operational Transconductance Amplifier (OTA)

The operational transconductance amplifier (OTA) is an amplifier whose differential input voltage produces an output current proportional to the transconductance of the amplifier. Thus, it is a voltage controlled current source (VCCS) device. There is usually an additional input for a current to control the amplifier's transconductance. The OTA is similar to a standard operational amplifier in that it has a high impedance differential input stage and that it may be used with negative feedback. The OTA is popular for implementing voltage controlled oscillators (VCO) and filters (VCF) for analog music synthesizers, because it can act as a two-quadrant multiplier, for this application the control input has to have a wide dynamic range of at least 60 dB, while the OTA should behave sensibly when overdriven from the signal input (in particular, it should not lock up or phase reverse). Viewed from a slightly different angle an OTA can be used to implement an electrically tunable resistor that is referenced to ground, with extra circuitry floating resistors are possible options as well.

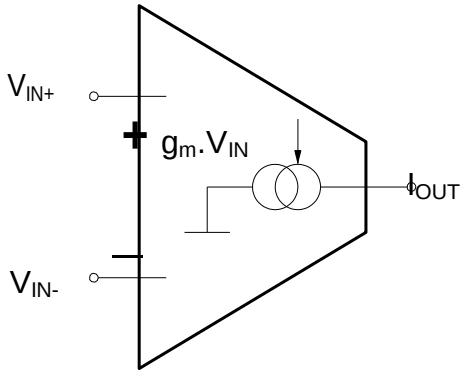

Fig3.1: Ideal OTA

The OTA is not as useful by itself in the vast majority of standard op-amp functions as the ordinary op-amp because its output is a current. One of its principal uses is in implementing electronically controlled applications such as variable frequency oscillators and filters and variable gain amplifier stages which are more difficult to implement with standard op-amps.

The primary application for an OTA is however to drive low-impedance sinks such as coaxial cable with low distortion at high bandwidth. Hence, improved OTA such as the MAX436 or OPA660 have optimized these characteristics, but made it either impossible (MAX436) or considerably harder (OPA660) to use them as two-quadrant multipliers. Four quadrant multipliers on the other hand are hideously expensive, so that obsolete OTA like the CA3080 are still in widespread use across the world.

3.3 Principle of Operation

An OTA is a voltage controlled current source, more specifically the term "operational" comes from the fact that it takes the difference of two voltages as the input for the current conversion an ideal OTA has infinite input and output impedances. Output current of OTA is given by:

$$I_0 = g_m(V_2 - V_1) \tag{3.1}$$

Where, g_m is the transconductance parameter of OTA.

For a bipolar OTA, the transconductance can be expressed by:

$$g_m = \frac{I_b}{2V_T} \tag{3.2}$$

Where, I_b and V_T are bias current and Thermal voltage, respectively.

The symbol and the equivalent circuit of the OTA are illustrated in Fig3.2(a) and 3.2(b), respectively. V_1 and V_2 being the input voltage ,I_0 is the output current which is proportional to the difference of the input applied voltage and I_B being the bias current which controls the transconductance of the amplifier.

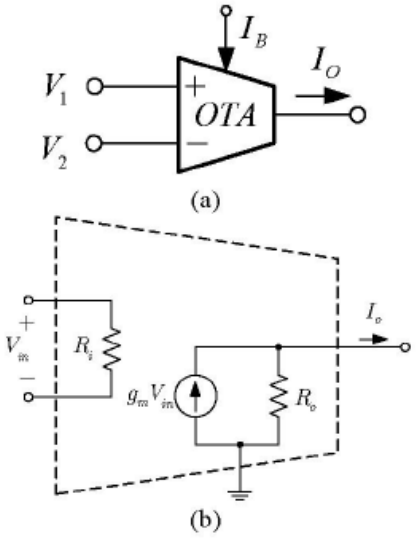

Fig3.2: OTA (a) Symbol (b) Equivalent circuit

To summarize the operation of an ideal OTA has two voltage inputs with infinite impedance (i.e. there is no input current). The common mode input range is also infinite, while the differential signal between these two inputs is used to control an ideal current source (i.e. the output current does not depend on the output voltage) that functions as an output. The proportionality factor between output current and input differential voltage is called Transconductance. Any real OTA will thus have circuitry to process the input voltages with low input current over a wide common mode input range, to produce an internal representation of the input differential voltage and to provide a current to the output that is relatively independent of the output voltage. Since an OTA can be used without feedback, the maximum output current and with it the transconductance can often be adjusted.

In the present thesis report, the Dual output OTA is simulated with bipolar junction transistor based circuit as shown below along with the impedance characteristic shown in Fig3.4. The main features of the proposed circuits are that: they employ only single grounded capacitor which makes it easier to realize in VLSI circuits, they don't not need any matching conditions of the element. In addition to that, the inductance can be controlled via input bias currents.

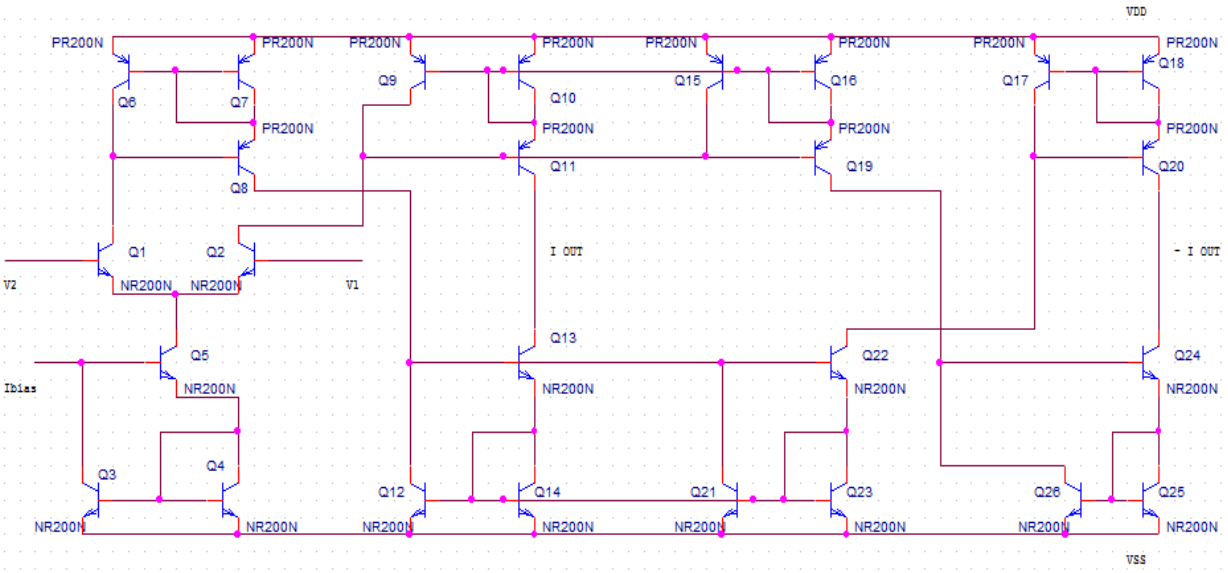

Fig3.3: Internal construction of Dual Output OTA

The impedance characteristic of the OTA used for construction of Inductor is shown in fig3.4, where it is been shown with the respect to the frequency. To prove the performance of the proposed circuit, computer simulation program was used for examination on Pspice software. The PNP and NPN transistors used employed in the proposed circuit were simulated by using the parameters of ALA400 transistors array from AT&T. The following values were used for the simulation: supply voltages ±1.5 V, bias currents 250uA.

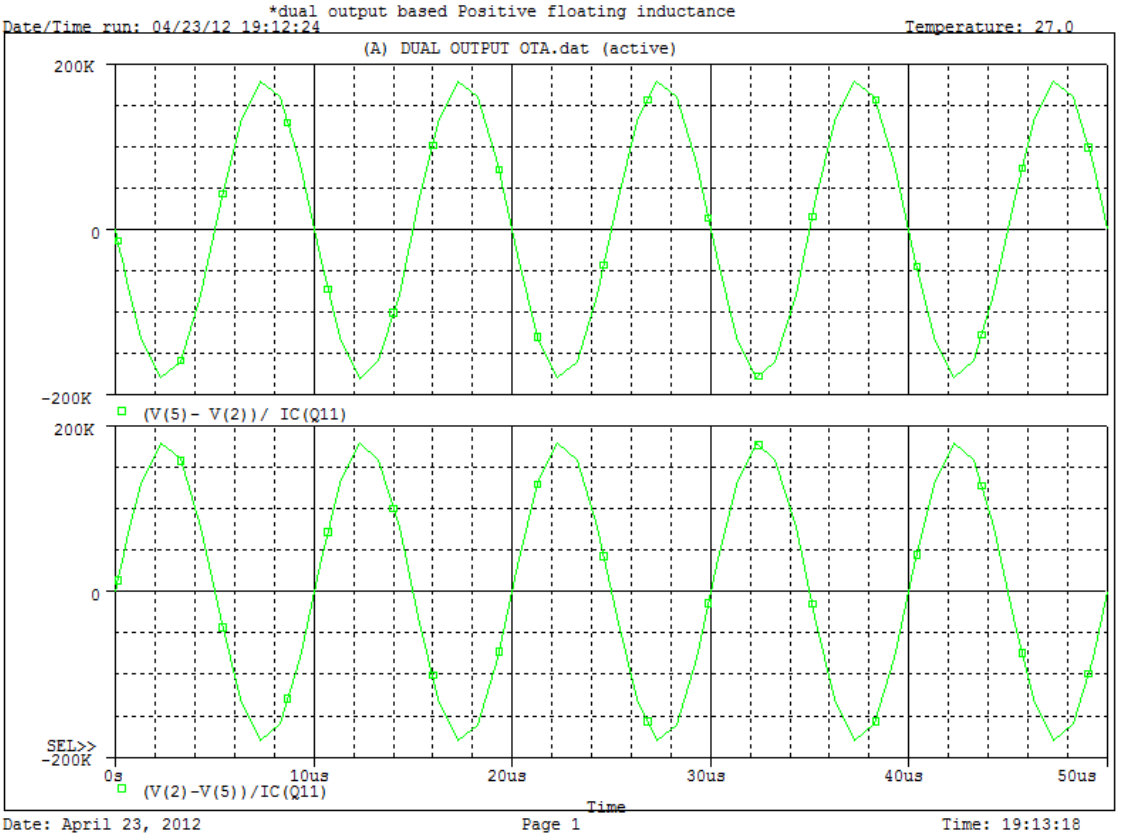

Fig3.4: Impedance characteristic of Dual Output OTA

Result

The frequency response of the dual output OTA shown above clearly reveals that there is 180^0 Phase difference as we change the variable difference in input voltage consideration. Moreover, the Impedance of the OTA is of the range of 0.2MΩ which can be taken as infinite input impedance as required.

3.4 Proposed Floating Positive Inductance Simulator

Fig3.5 depicts the proposed floating positive inductance simulator, where I_{b1} and I_{b2} are input bias currents of the OTA1 an OTA2, respectively. OTA1 is single output whereas OTA2 is dual output OTA.

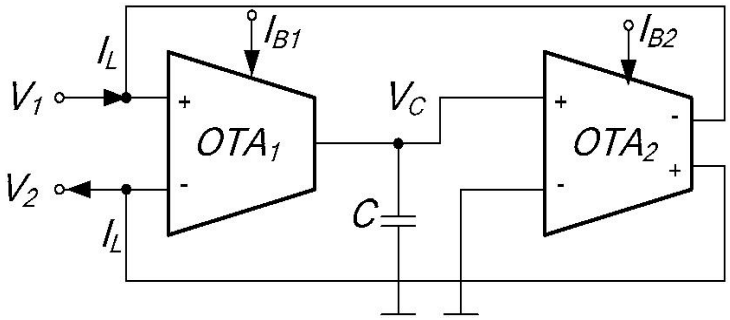

Fig3.5: Proposed Floating Positive Inductance simulator

The features of proposed circuits are that the proposed circuits consume less number of OTA, they employ only single grounded capacitor, which is convenient to realize in integrated circuits, they do not need any matching condition of the element. In addition, the inductances can be controlled via input bias current.

Considering the circuit in Fig3.5 and using the OTA properties as discussed earlier, we will get:

$$V_C = g_{m1}\frac{V_1 - V_2}{sC} \tag{3.3}$$

The output current I_L can be found as:

$$I_L = g_{m2}\,g_{m1}\frac{V_1 - V_2}{sC} \tag{3.4}$$

From the above equation, the input impedance of the circuit can be written as:

$$Z_L = \frac{V_1 - V_2}{I_L} = \frac{sC}{g_{m1}g_{m2}} \tag{3.5}$$

From equation 3.5, it is obvious that the circuit shown in figure 3.2 simulates a floating inductance with a value:

$$L_{eq} = \frac{C}{g_{m1} g_{m2}} \tag{3.6}$$

3.5 Simulation results

To prove the performances of the proposed circuit, the PSPICE simulation program was used for the examinations. The PNP and NPN transistors employed in the proposed circuit were simulated by using the parameters of the PR200N and NR200N bipolar transistors of ALA400 transistor array from AT&T. The performance of the Positive inductance simulator was proved by deriving current and voltage characteristic of the proposed positive Inductor, Impedance characteristic and then using the same in series RLC circuit.

Following values were used for the simulation: supply voltages *±1.5V* DC*,* bias currents $I_{b1} = I_{b2}$ = 100uA to 500uA and capacitor value *C=0.7nF* i.e. connected between the output of the first OTA1 and the other end is grounded*.* The value of R and C in the series RLC circuit was taken to be as R=15K and C=1nF.

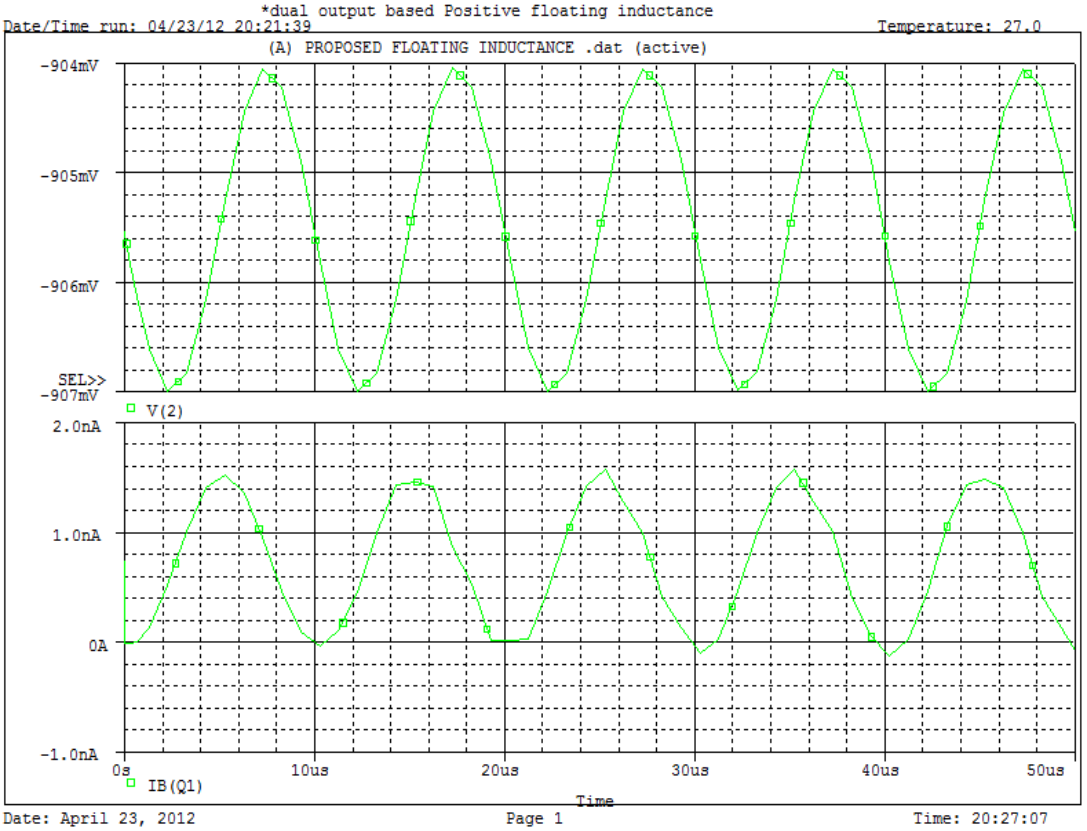

Fig3.6: Output Current and Voltage characteristics of the proposed Positive Floating Inductor

Result

The above graph shows the output voltage and current characteristic of the proposed inductor. The graph clearly revels that the voltage leads the Current which is the main characteristic of the Inductor.

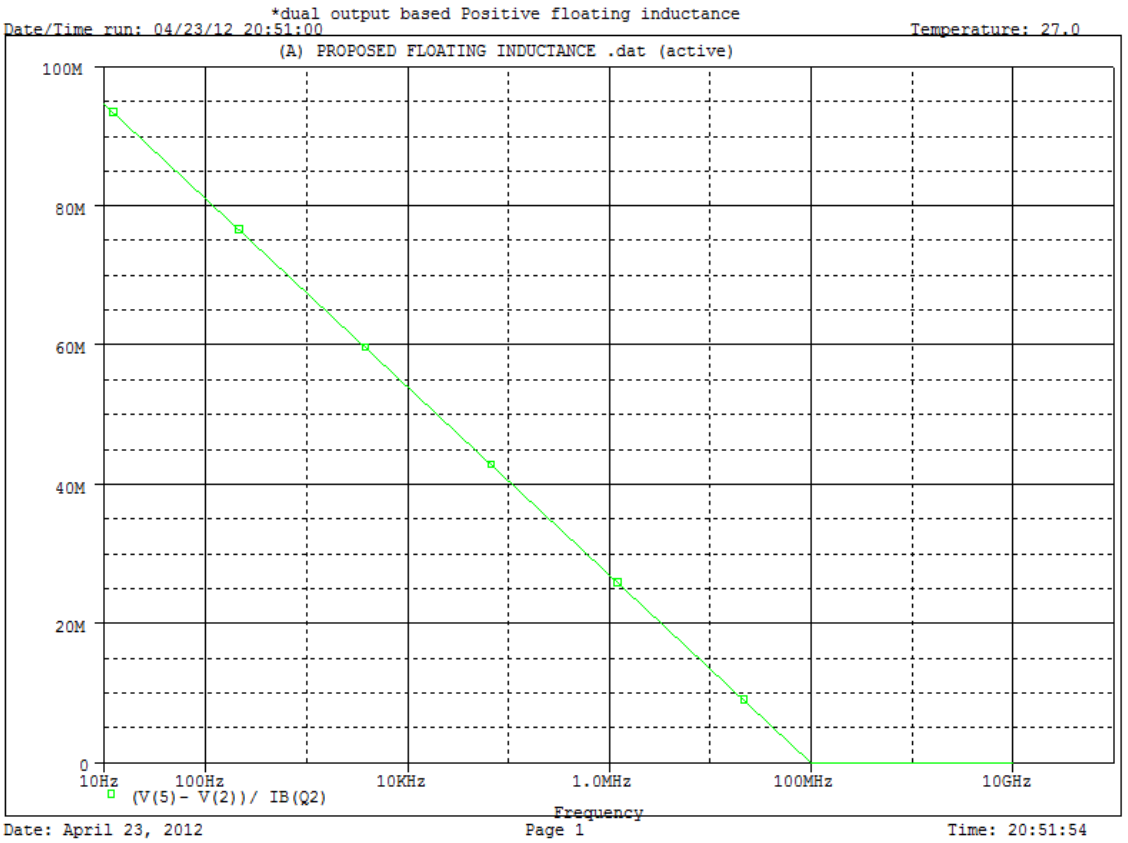

Fig3.7: Impedance characteristics of the proposed Positive Floating Inductor

Result

The impedance characteristic of the proposed positive inductor is shown with the help AC analysis, which clearly revel the frequency response of the inductance of the proposed positive floating inductance.

3.6 Application of the simulated positive Inductor when used in series RLC circuit

The performance of the Positive inductance simulator was proved by using the same as inductor in the series RLC circuit and determining its parameters as shown below.

Following values were used for the simulation: supply voltages *±1.5V* DC, bias currents I_{b1} =250uA I_{b2} = 250uA and capacitance of *C=0.7nF* i.e. connected between the output of the first OTA1 and the other end is grounded. The value of R and C in the series RLC circuit was taken to be as R=220Ω and C=10nF. Typical waveforms of the current through the proposed Series RLC resonant circuit as shown in Fig3.8 are shown in fig3.9:

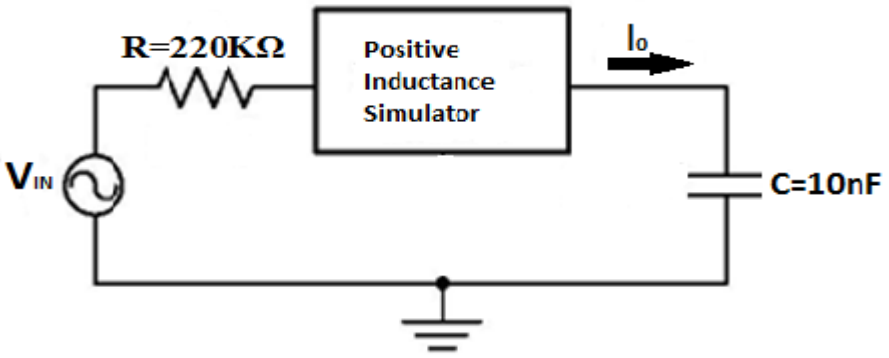

Fig3.8: series RLC resonant Circuit

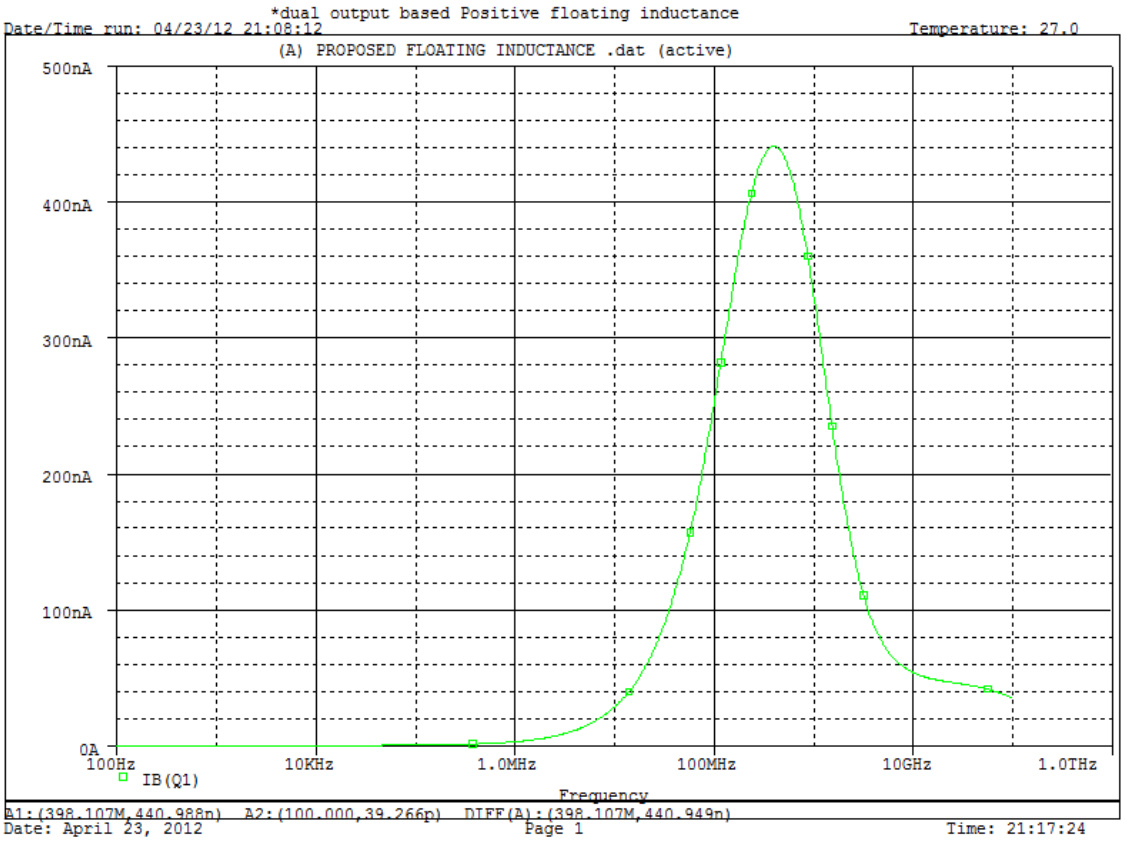

Fig3.9: Current characteristics of the Series RLC resonant circuit

Result:

Bandwidth of the Series resonant circuit = 959.22244MHz

Resonant Frequency = 398.107MHz

Quality factor = Resonant Frequency/ Bandwidth = 0.41

Moreover at Resonance, $f_r = \frac{1}{2\pi\sqrt{LC}}$

Which gives Inductance = 1.59uH (Approx).

3.7 Proposed Floating Negative Inductance Simulator

The proposed floating negative inductance simulator, using OTA properties as described earlier can be used to construct a Negative Inductance Simulator as shown in Fig3.10

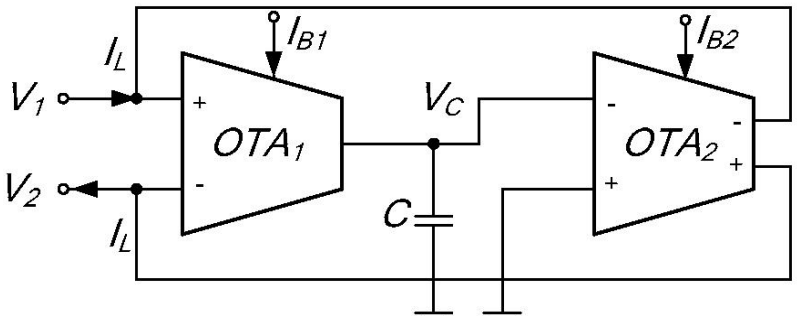

Fig3.10: Proposed floating Negative Inductance simulator

For the case of Negative Inductance Simulator:

$$Z_L = \frac{V_1 - V_2}{I_L} = \frac{sC}{g_{m1}g_{m2}} \tag{3.7}$$

It can be seen from equation 3.7 that the circuit shown in figure 3.8 act as an Negative Inductance simulate with a value

$$L_{eq} = \frac{C}{g_{m1}g_{m2}} \tag{3.8}$$

Negative Inductance value can be easily adjusted by electronically controlling I_{b1} and I_{b2}, i.e. by controlling the bias currents we control the transconductance of the OTAs by which we indirectly control the output current which is the function of the difference of the input voltages.

3.8 Simulation Results

To prove the performances of the proposed circuit, the PSPICE simulation program was used for the examinations. The PNP and NPN transistors employed in the proposed circuit were simulated by using the parameters of the PR200N and NR200N bipolar transistors of ALA400 transistor array from AT&T. The performance of the Negative inductance simulator was proved by deriving current and voltage characteristic of the proposed Negative Inductor, Impedance characteristic and then using the same in Impedance cancellation circuit.

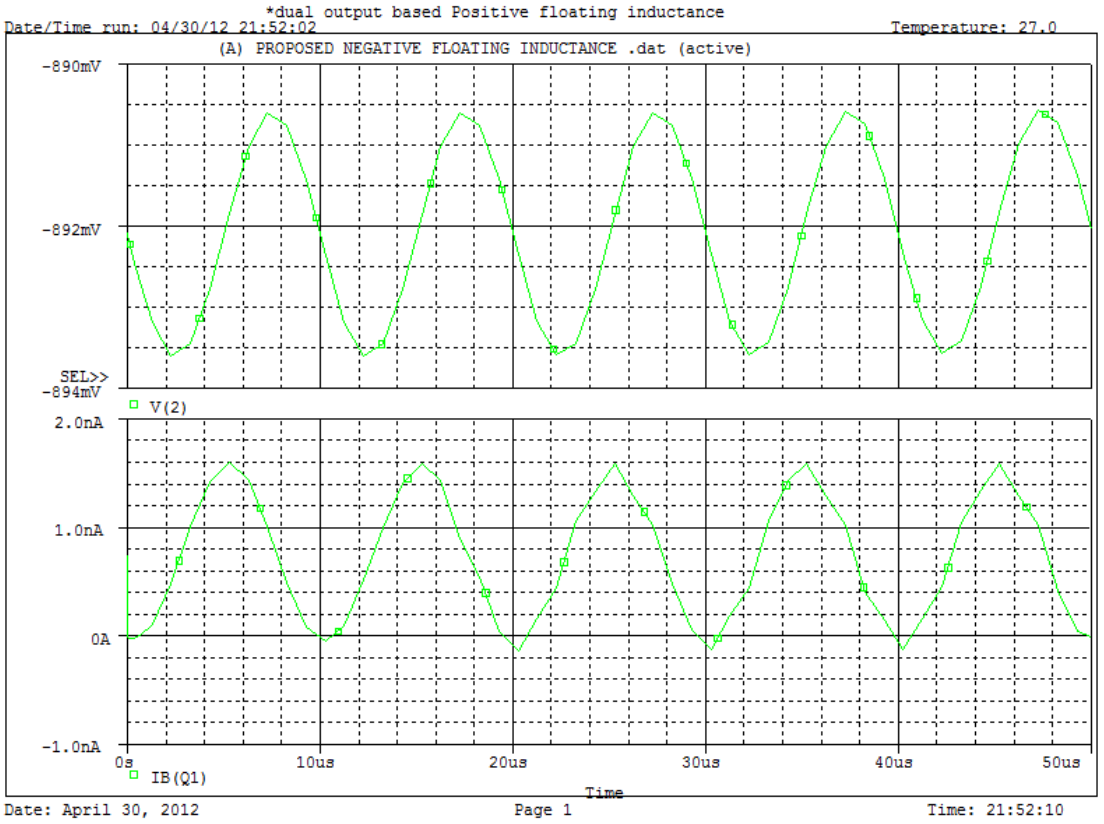

Fig3.11: Current and Voltage characteristics of the proposed Negative Floating Inductor

Result

The above graph shows the output voltage and current characteristic of the proposed inductor. The graph clearly revels that the current leads the voltage which is the main characteristic of the Negative Inductor.

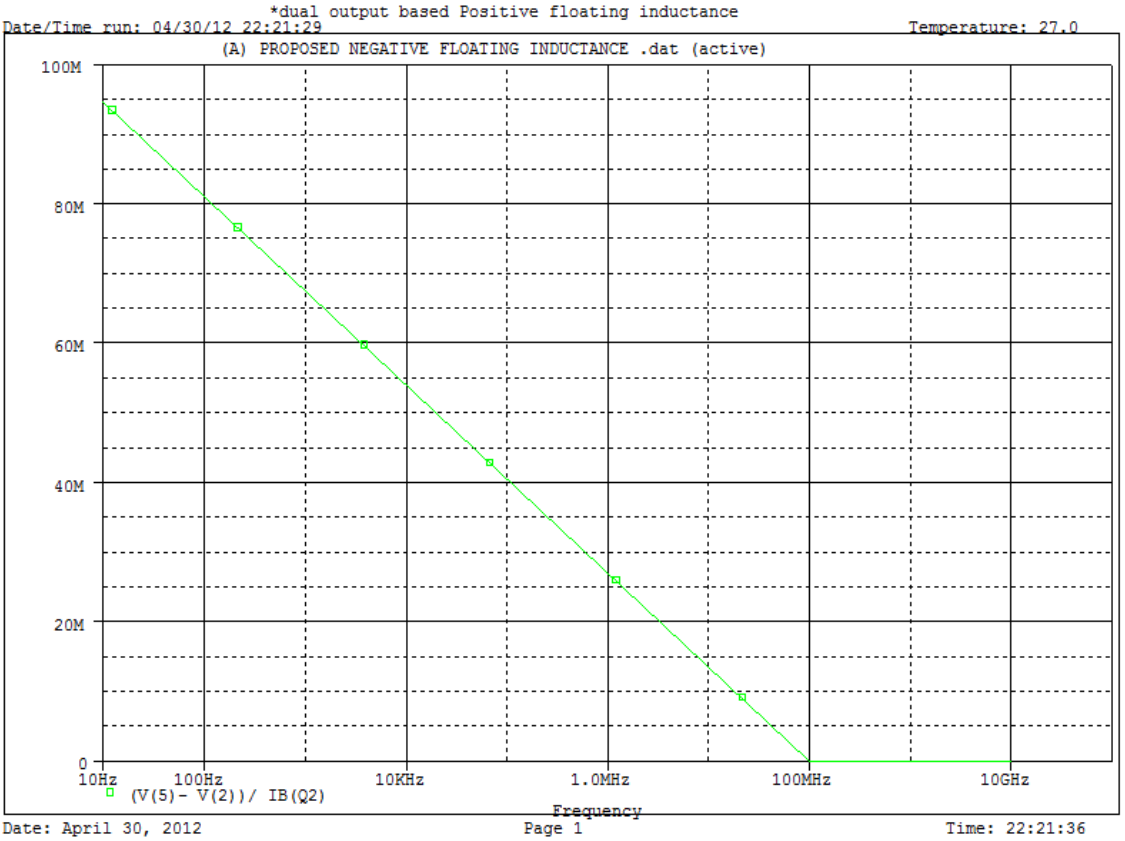

Fig3.12: Impedance characteristics of the proposed Negative Floating Inductor

Result

The impedance characteristic of the proposed positive inductor is shown with the help AC analysis, which clearly revel the frequency response of the inductance of the proposed positive floating inductance.

3.9 Application of Negative Inductance simulator in Inductance Cancellation circuit

The performance of the Negative inductance simulator was proved by using the same as inductor in the series RLL Inductance cancellation circuit and determining its parameters as shown below:

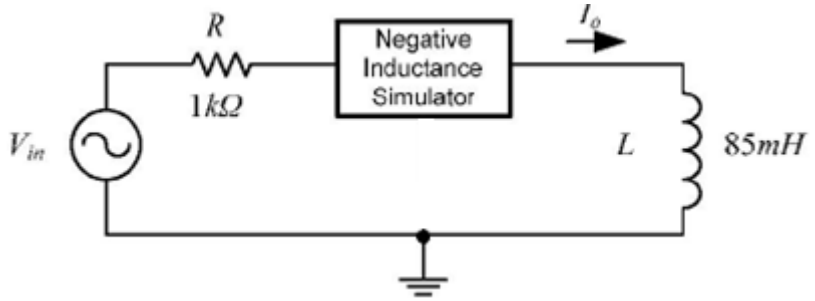

Fig3.13: Inductance cancellation circuit

Following values were used for the simulation: supply voltages *±1.5V*, bias currents $I_{b1} = I_{b2} =$ 250uA, capacitor value C=*0.7nF* which is connected between the output of the OTA1 and the other end is grounded, $V_{IN=}1.5V$. the value of the R and L in the series RLL circuit is taken as R= 1KΩ and L= 85mH.. Typical waveforms of the circuits simulated were shown below.

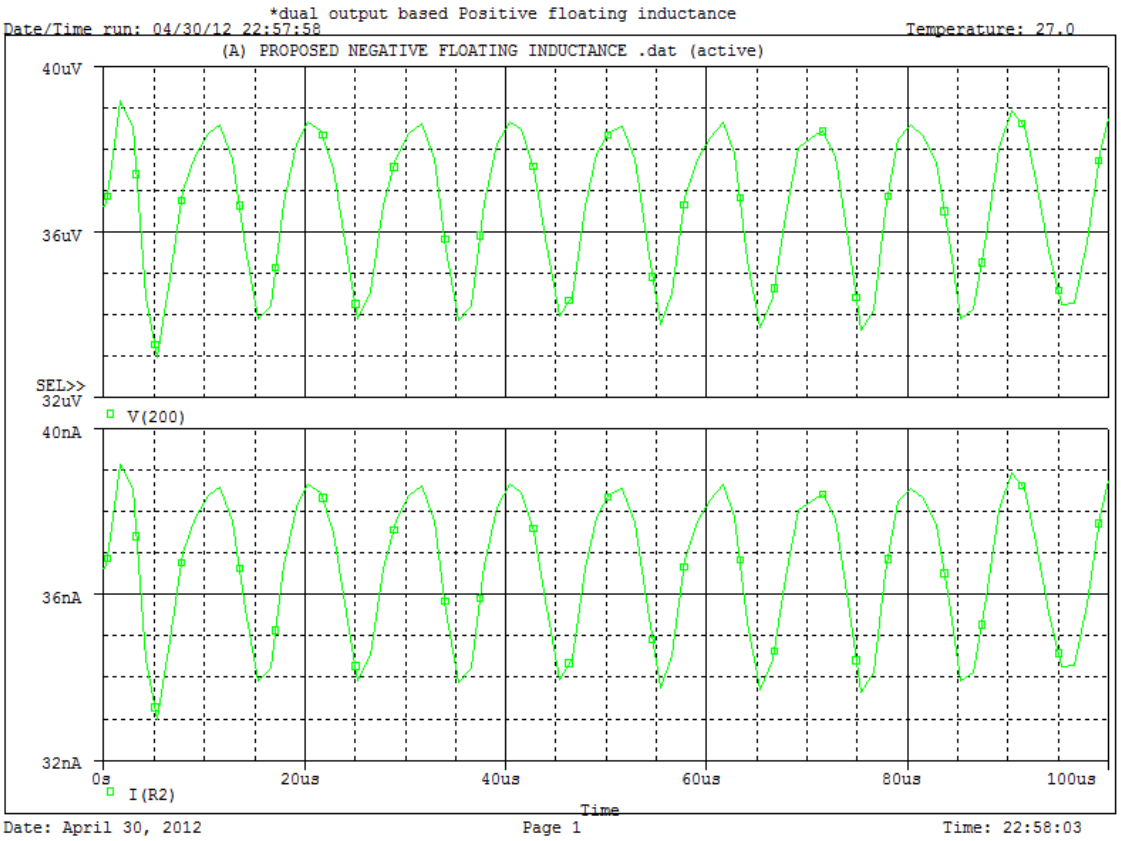

Fig3.14: Inductance cancellation circuit simulated with Proposed Negative floating Inductance

Result

The graph clearly revels that the Voltage and Current across the resistor are in same phase as required since in Negative Floating Inductance current lead the voltage by 90^0 where as in inductor Voltage lead the Current by 90^0 resulting in cancellation of both.

3.10 Conclusion

A generalized Positive and negative Floating Inductance simulator were proposed, which are suitable for realizing in bipolar monolithic integrated circuit form. Simulation results obtained from PSPICE program verify the high qualification performances of the proposed circuit. Some application examples have been demonstrated, that the use of the proposed scheme is attractive.

CHAPTER 4

CURRENT CONVEYOR BASED INDUCTOR

4.1 Introduction

This chapter presents the survey of current mode building blocks available in various forms. Thereafter, CMOS implementations and simulation for verifying the port relationships of Modified Dual Output based Lossless grounded Inductance simulation is discussed. These building blocks are used later in the chapter for constructing RLC parallel resonant circuit.

The growth of analog Integrated circuit design has been impeded by the process technologies that are mostly optimized for digital applications only. With the evolution of submicron technologies such as 0.35 micron, 0.18 micron and 0.13 micron, the supply voltages have been reduced to 3.3 Volts and lower. This makes it difficult to design a voltage mode CMOS circuits with high linearity and wide dynamic range. Recently, current mode circuits have become a viable alternative for future applications because of their inherent advantages over voltage mode circuits.

The main advantage of using current mode technique is because the non-linear characteristics exhibited by most field effect transistors. A small change in the input or controlling voltage results in a much larger change in the output current. Thus for a fixed supply voltage, the dynamic range of a current mode circuit is much larger than that of a voltage mode circuit. If a supply voltage is lowered, one can still get the required signals represented by the current.

A second advantage of current mode circuits is that they are much faster as compared to voltage mode circuits. The parasitic capacitances present in the analog circuits must be charged and discharged with the changing voltage levels. In a current mode circuit, a change in current level is not necessarily accompanied by a change in the voltage level. Hence, the parasitic capacitances will not affect the operating speed of the circuit by a significant amount.

Other advantages of using current mode circuits are that they do not require specially processed capacitors or resistors; they are more compatible with digital CMOS technology making integration of mixed signal circuits more feasible.

4.2 Current Conveyor

The current conveyor (CC) is the basic building block of a number of applications both in the current and voltage and the mixed modes. The principle of the current conveyor of the first generation was published in 1968 by K. C. Smith and A. S. Sedra. Two years later, today's widely used second-generation CCII was described, and in 1995 the third-generation CCIII. However, initially, during that time, the current conveyor did not find many applications because its advantages compared to the classical operational amplifier (opamp) and were not widely appreciated. Moreover, during that era most of the analog designers prefers opams as their first choice for designing. An integrated circuit Current Conveyor, namely PA630, was introduced by Wadsworth in 1989 (mass produced by Phototronics Ltd. of Canada) and about the same time, the now well-known AD844 (operational trans-impedance amplifier or more popularly known as a current feedback op-amp) was recognized to be internally a CCII+ followed by a voltage follower. An excellent review of the state-of-the-art of current-mode circuits prior to 1990 was provided by Wilson.

Today, the current conveyor is considered a universal analog building block with wide spread applications in the current mode, voltage mode, and mixed mode signal processing. Its features find most applications in the current mode, when its so-called voltage input *y* is grounded and the current, flowing into the low-impedance input *x*, is copied by a simple current mirror into the *z* output.

Since 1995 in particular, we have witnessed many successive modifications and generalizations of the basic principle of CCII in order to use this circuit element more efficiently in various applications. A summary of the behavioral models of selected conveyors is presented here:

4.2.1First generation Current Conveyor: CCI

The current conveyor as initially introduced, is a 3-port device whose black-box representation is as shown in fig4.1.

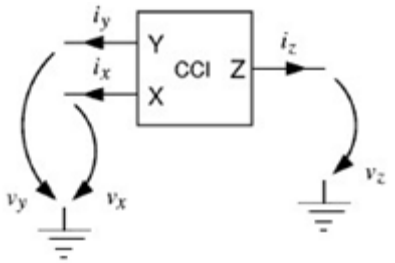

Fig4.1: Black Box representation of Current Conveyor

The operation of this device is such that if a voltage is applied to input terminal Y, an equal potential will appear on the input terminal X. In a similar fashion, an input current I being forced into terminal X will result into an equal amount of current flowing into terminal Y. As well as the current I will be conveyed to the output terminal Z such that terminal Z has the characteristics of a current source of value I with high output impedance.

As can be seen, the potential of X being set by that of Y, is independent of the current being forced into port X. Similarly, the current through input y, being fixed by that of X, is independent of the voltage applied at Y. Thus, the device exhibits a virtual short circuit input characteristics at port X and a dual virtual open-circuit input characteristics at port Y.

Mathematically, the input-output characteristics of CCI can be described by the following equation:-

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 1 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_X \\ I_Y \\ V_Z \end{bmatrix} \quad (4.1)$$

Where, the variables represent total instantaneous quantities. The (+) sign applies for the CCI in which both I_z and I_x flow into the conveyor and it is denoted by CCI+. The (–) sign applies for the opposite polarity case denoted by CCI-. To visualize the interaction of the port voltages and currents described by the above matrix equations the nullator-norator representation as shown in Fig4.2 may be used:-

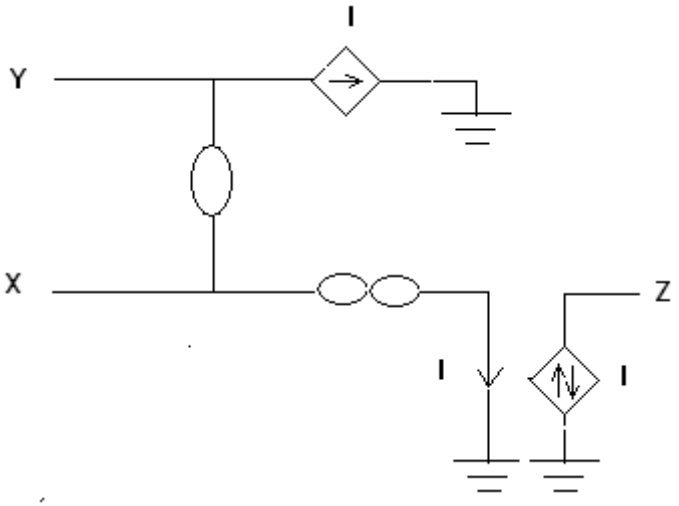

Fig4.2: Nullator-Norator representation of CCI

In fig4.2, single ellipse is used to represent the nullator element and two intersecting ellipses to represent the norator element. The nullator element has constitutive equation V=0 and I=0 whereas, the norator has an arbitrary current-voltage relationship. Clearly, the nullator element is used to represent the virtual short circuit apparent between the X and Y terminals. Also included in the circuit are two dependent current sources. These are used to convey the current at port X to ports Y and Z.

Negative Impedance Converter:

An early application of CCI was its use as a negative impedance converter (NIC). For this application terminal Z is grounded and the resistor to be converted is connected either between X and ground or between Y and ground. If resistor R is connected between X and ground, then looking into Y one sees a resistance (–) R that is short circuit stable. Alternatively if R is connected between Y and the ground then the input resistance at X is (–) R and is open circuit stable. The fig4.3 depicts the following observation diagrammatically.

. A major problem that hindered the fabrication of the CCI in IC form in the 1960s is its use of high quality PnP devices. Since complimentary devices are available in CMOS technology, it is easy to fabricate a CMOS current conveyor.

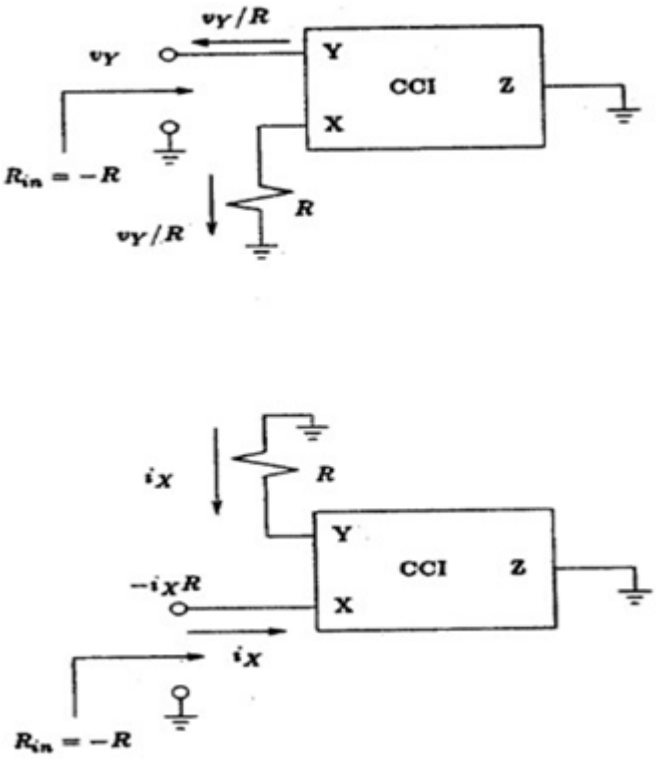

Fig4.3: CCI implementation of Negative Impedance Converter (NIC)

4.2.2 The Second generation Current conveyor: CCII

To increase the versatility of current conveyor, a second version in which no current flows in terminal Y was introduced. This building block has since proven to be more useful than CCI. Utilizing the same block diagram representation of Fig4.1, CCII is described by:-

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 1 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_X \\ I_Y \\ V_Z \end{bmatrix} \quad (4.2)$$

Thus, terminal Y exhibits infinite input impedance. The voltage at X follows that applied to Y, thus X exhibits zero input impedance. The current supplied to X is conveyed to the high impedance output terminal Z where it is supplied with either positive polarity (in CCII+) or negative polarity (in CCII-).In terms of nullor the port behavior of the second generation current conveyor (positive or negative) can be depicted as shown in Fig4.4

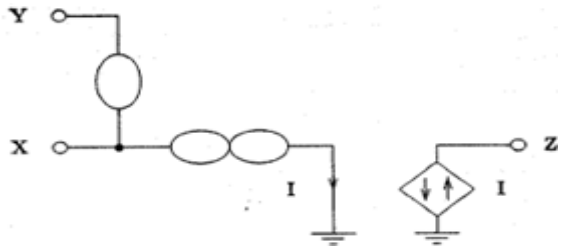

Fig4.4: Nullator-Norator representation of a CCII

The similarity and difference between CCI and CCII are clearly evident from their equivalent circuits. In the case of a CCII-, the dependent current source is redundant, current flowing into terminal X must flow out of terminal Z. Hence the equivalent circuit of CCII- can be represented with a single nullor element as shown in Fig4.5.

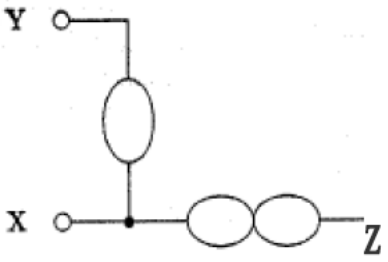

Fig4.5: A simplified representation of CCII-

The first widely recognized application of CCII was in realization of controlled sources, impedance converters, impedance inverters, gyrators and various analog computation devices.

4.2.3 The Third Generation Current conveyor: CCIII

This structure was published by Fabre in 1995. Structurally it is quiet similar to CCI with the exception that the current in port X and Y flow in opposite directions. It is represented by push-pull topology built from four simple CCIs. Its main application is in Current measurement. Utilizing the same block diagram representation of Fig 4.1of the CCI, CCIII is described by the following equation:-

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & -1 & 1 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_X \\ I_Y \\ V_Z \end{bmatrix} \quad (4.3)$$

The CCIII was explained diagrammatically in fig4.6

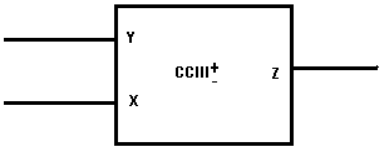

Fig4.6: Block diagram representation

4.3 Modified Dual Output Differential Difference Current Conveyor (MDO-DDCC):

Several generations of current conveyors have been defined over the years**.** Undoubtedly, the second generation conveyor (CCII) is the more well known of the device. But, we have selected Modified Dual Output Differential Difference Current Conveyor for realizing inductance since it can provide multiple output currents I_z of both directions, thus combining both the positive and the negative CCII in a single device. Secondly, the differential difference Current conveyor offers more freedom during the design of voltage and mixed-mode applications. Thus, the DDCC provides universality of Dual output, Differential Difference and Current conveyor characteristic into a single package allowing the ease to the manufacturer using the device.

The proposed grounded inductor topologies can be classified based on the number of active and passive elements employed and whether they realize a lossy or lossless kind of inductors. Most of these circuits employ two or more current conveyors to realize grounded inductance. The proposed topologies employ a single current conveyor but they do not realize pure inductance. Although there are circuits reported in papers which realize pure inductance with only one modified inverting type second-generation current conveyor (MICCII) and a single minus-type modified inverting first-generation current conveyor (MICCI-), respectively, in addition to a grounded resistor both of the circuits employ a floating resistor and a floating capacitor.

The five new lossless grounded inductance simulators recently presented in [76] employ only a single Fully Differential Second-Generation Current Conveyor (FDCCII), two grounded resistors and a grounded capacitor. Although these circuits seem to be the most attractive inductance simulators, the complicated CMOS structure of the FDCCII brings a drawback to them.

Differential difference current conveyor (DDCC) [77] and Differential voltage current conveyor (DVCC) [78] are proven to be useful in many voltage-mode (VM) and current- mode(CM) analog signal processing applications, such as VM filters, CM filters, mixed-mode filters, sinusoidal oscillators and immitance function simulators. The DDCC and DVCC allow CC applications to be

extended to the domain of voltage differentiating functions. Therefore, such kinds of CCs give a higher degree of freedom to analog designers allowing the implementation of more functions using less active elements. A circuit with a minimum number of components is expected to simplify the design. The Modified Dual Output Differential Difference Current Conveyor (MDO-DDCC) is shown below with its terminal characteristic:

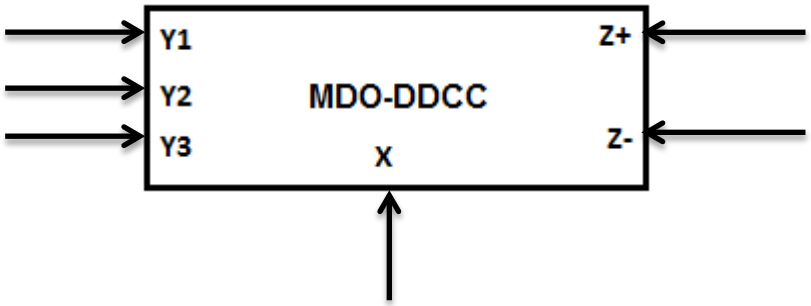

Fig4.7: Block diagram representation of Modified dual output-Differential Difference Current conveyor

The terminal relations o f a M D 0 CCII can be characterized by:

$$\mathrm{I}_{y1} = I_{Y2} = I_{y3} = 0 \tag{4.4.}$$

$$V_X = \beta_1 V_{Y1} - \beta_2 V_{Y2} - \beta_3 V_{Y3} \tag{4.5.}$$

$$I_{z+} = 0.5\alpha_1 I_X \tag{4.6.}$$

$$I_{z-} = -\alpha_2 I_X \tag{4.7.}$$

Where, β and α are the voltage and current gain which are ideally Unity

The Y terminals are high-impedance voltage inputs, Z terminals are the high-impedance current outputs and X terminal exhibits a low-impedance. The β_i (i = 1, 2, 3) and α_j (j = 1, 2) represent the voltage and current gains of the MDO-DDCC, respectively, which are ideally equal to unity.

4.4 Realization of Modified Dual Output Differential Difference Current Conveyor (MDO-DDCC) based Inductance:

The proposed grounded inductance simulator is shown in Fig4.8. It uses one MDO-DDCC and three passive elements. To find the input impedance of the circuit, a voltage source V_{IN} is connected to the Y_2 terminal of the MDO-DDCC of the proposed circuit.

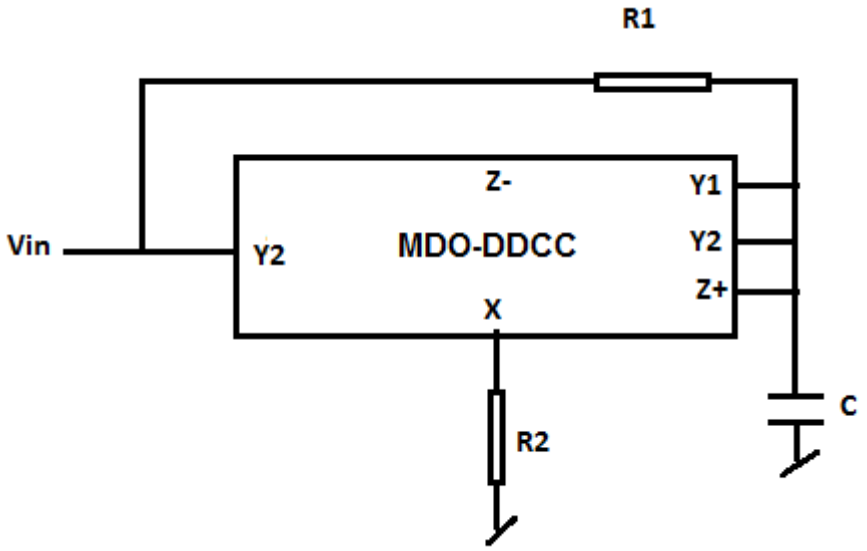

Fig4.8: Proposed grounded lossless inductance simulator

.

Applying KCL at V_{in} terminal of the circuit in Fig. 4.8, we obtain:

$$I_{IN} = \frac{-V_{IN}+2V_{Z+}}{R_2} + \frac{V_{IN}-V_{Z+}}{R_1} \quad (4.8)$$

Setting, $R_1 = R_2 = R$ (4.9)

,

$$I_{IN} = \frac{V_{Z+}}{R} \quad (4.10)$$

Similarly, writing KCL at terminal V_{Z+} of the proposed circuit gives,

$$\frac{V_{IN}-V_{Z+}}{R} = 0.5\ \frac{(V_{IN}-V_{Z+})}{R} + SCV_{Z+} \quad (4.11)$$

Which is simplified to :

$$V_{Z+} = \frac{V_{IN}}{2SCR} \quad (4.12)$$

Now by using above equations we get :

$$z_{IN} = \frac{V_{IN}}{I_{IN}} \quad (4.13)$$

or,

$$Z_{IN} = 2sCR^2 = sL_{eq} \quad (4.14)$$

Therefore,

$$L_{eq} = 2CR^2. \quad (4.15)$$

4.5 CMOS realization of Modified Dual Output Differential Difference Current Conveyor (MDO-DDCC) based Inductance

The MDO-DDCC has been simulated using the CMOS structure of fig4.9 with DC supply voltage equal to ±1.5V and bias voltage equal to I_{BB}= -0.9V. All MOS transistors are operated in saturation region. The simulations are based on .35µm TSMC CMOS technology.

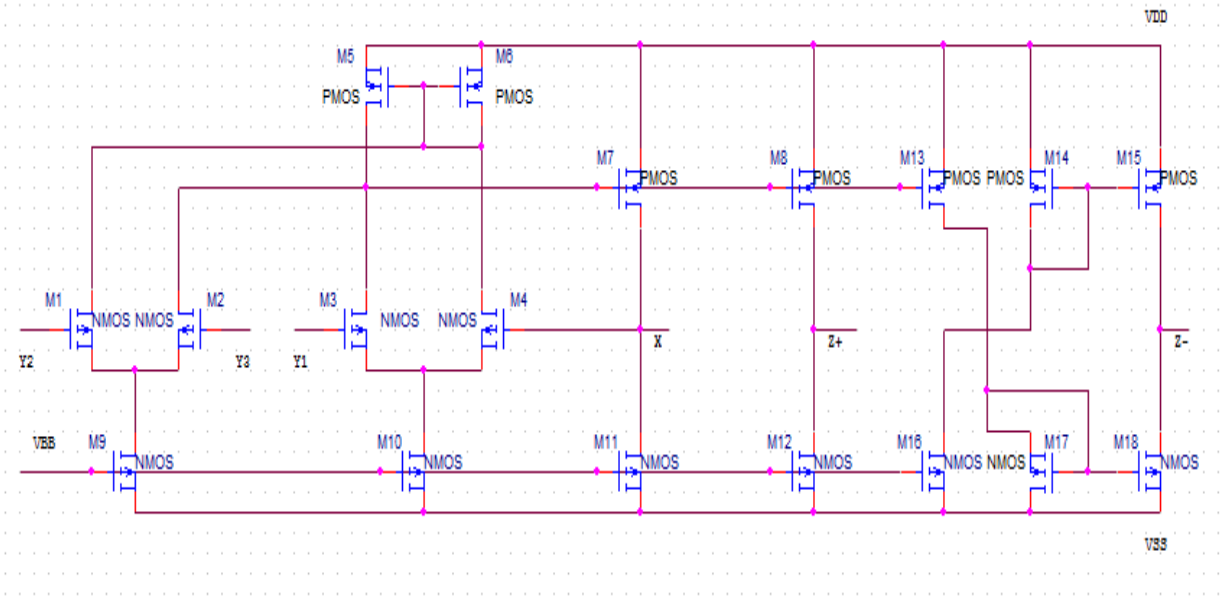

Fig4.9: CMOS structure of MDO-DDCC

In order to demonstrate the port relations of the MDO-DDCC based inductance realization computer simulations are performed using CMOS based MDO-DDCC schematic as given in fig4.8 and fig4.9, with a AC input of 5mv, $R_1$and R_2 each having a value of 1KΩ and the value of capacitance is varied to 2.5nF, 4.5nF and 6.5nF so as to obtain different values of Inductance. The simulation results for I_{z+} and I_{z-} are shown in Fig4.10. Fig4.11, Fig4.12 and Fig4.13 shows the magnitude and phase response of the resonant RLC circuit with proposed MDO-DDCC based inductance.

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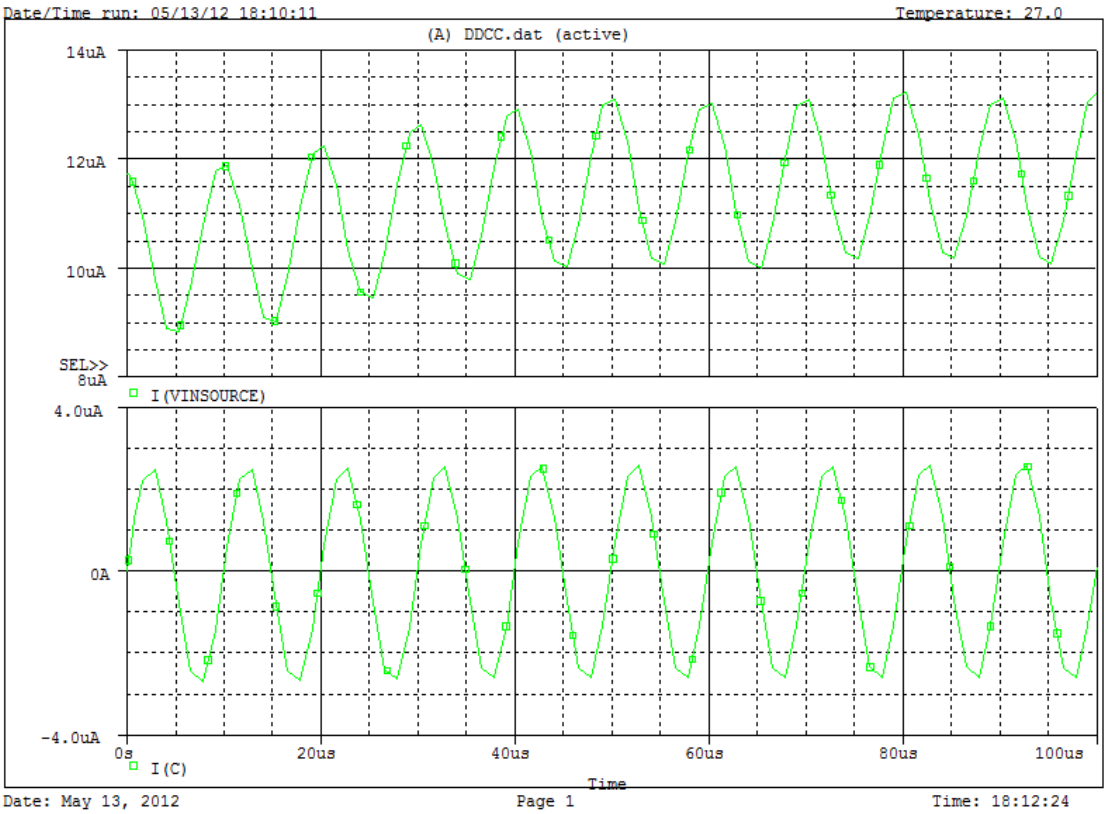


Fig4.10: Output port characteristic of Iz+ and Iz-

Result:

The above computer simulation clearly fulfills the theoretical results.

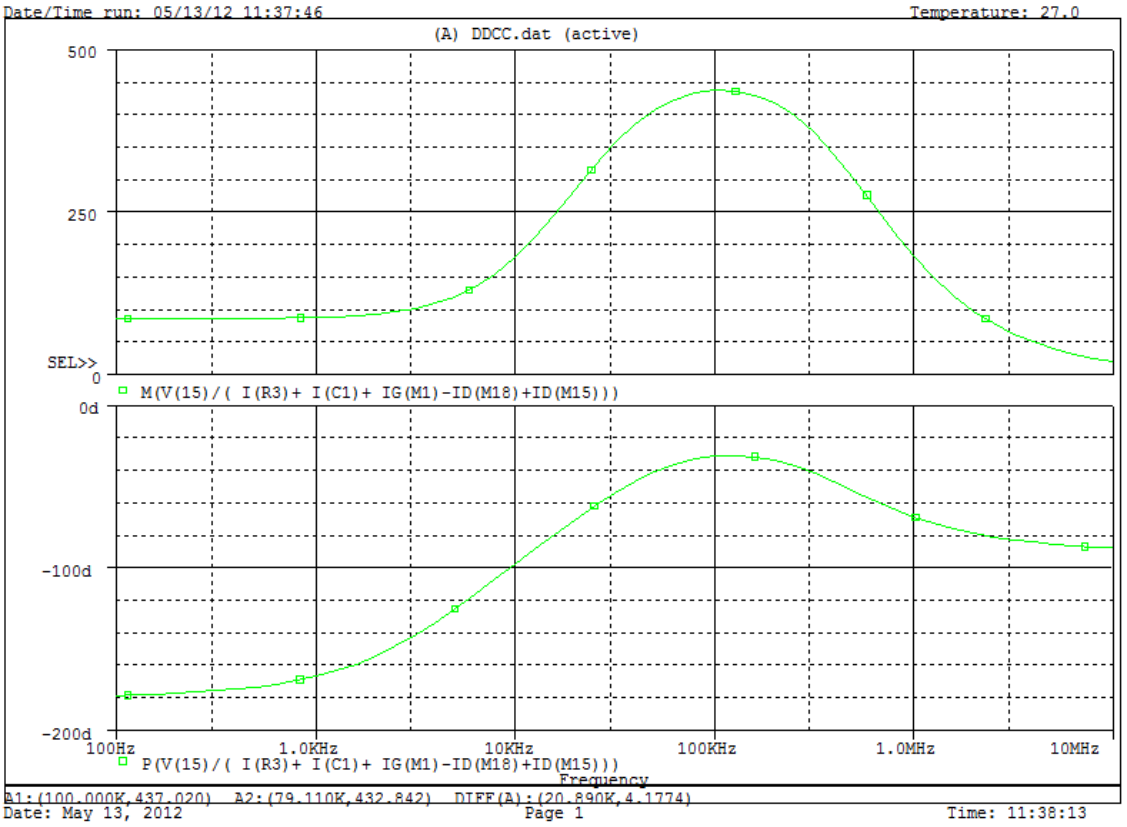


Fig4.11: Impedance response of Parallel Resonant RLC circuit for L=5mH, C= 2.5nF, R=1KΩ

Result:

At resonance,

Bandwidth of the Series resonant circuit = 456.526KHz

Resonant Frequency = 100KHz

Moreover, $f_r = \frac{1}{2\pi\sqrt{LC}}$

Which gives Inductance = 3.17mH (Approx).

The mismatch in the result is due to non-ideality variables i.e β and α.

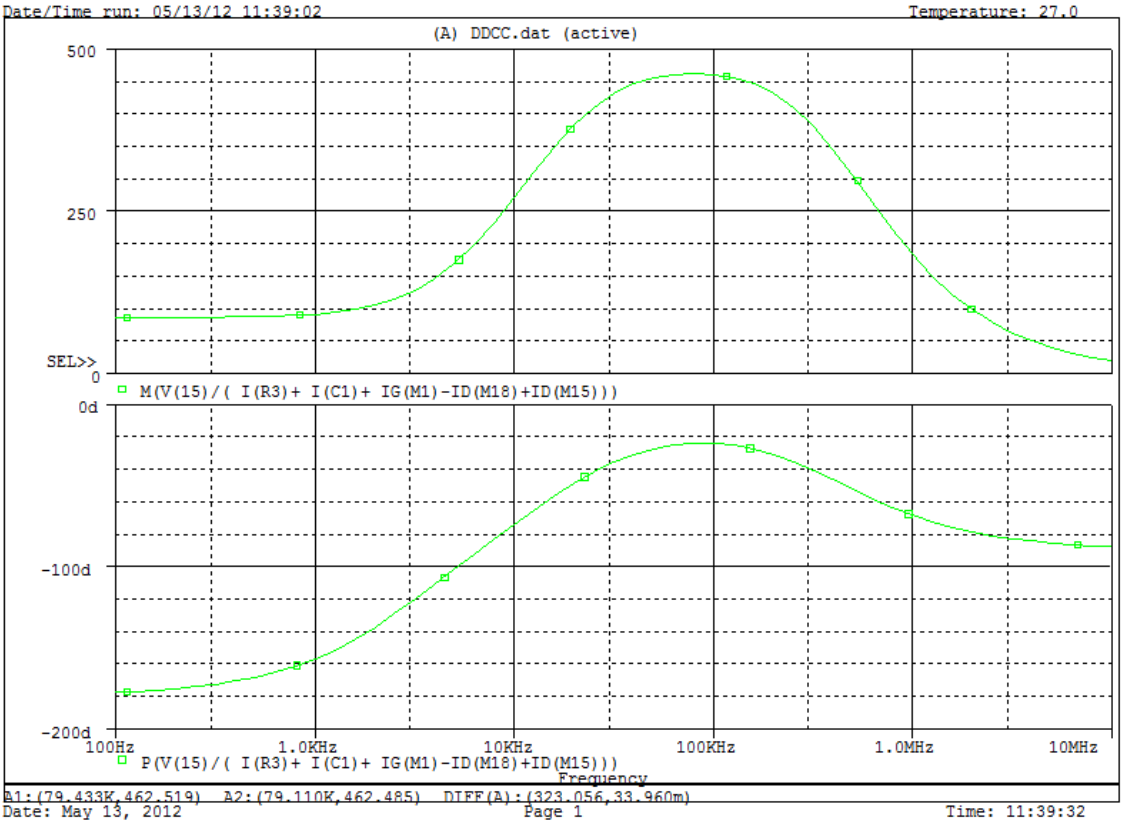


Fig 4.12: Impedance response of Parallel Resonant RLC circuit for L=9mH, C= 4.5nF, R=1KΩ

Result:

At resonance,

Bandwidth of the Series resonant circuit = 431.050KHz

Resonant Frequency = 79.433KHz

Moreover, $f_r = \frac{1}{2\pi\sqrt{LC}}$

Which gives Inductance = 5.02mH (Approx).

The mismatch in the result is due to non-ideality variables i.e β and α.

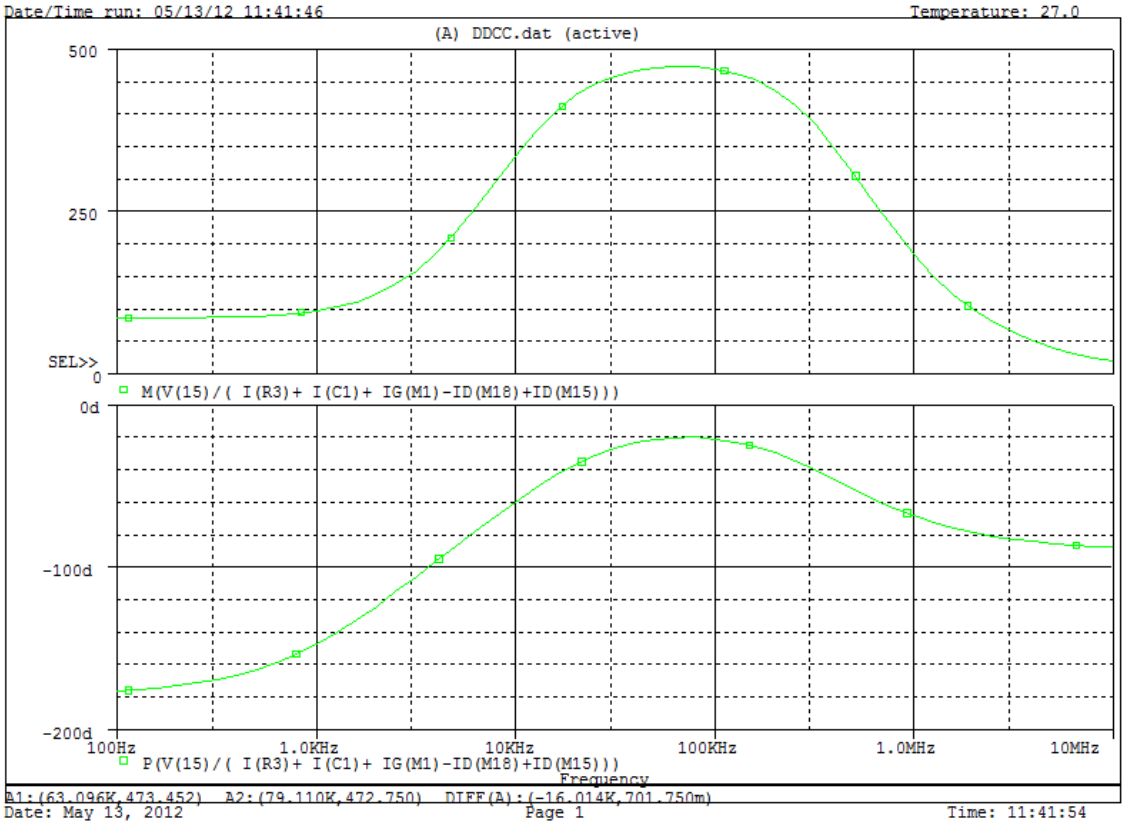


Fig 4.13: Impedance response of Parallel Resonant RLC circuit for L=13mH, C= 6.5nF, R=1KΩ

Result:

At resonance,

Bandwidth of the Series resonant circuit = 421.282KHz

Resonant Frequency = 63.096KHz

Moreover, $f_r = \frac{1}{2\pi\sqrt{LC}}$

Which gives Inductance = 7.96mH (Approx).

The mismatch in the result is due to non-ideality variables i.e β and α.

4.6 Conclusion:

A grounded inductor simulator topology has been presented. The proposed topology allows a design with a minimum number of active and passive components, such as one MDO-DDCC, two resistors and one grounded capacitor. The non-ideality effects of the MDO-DDCC on the proposed inductor have been investigated. To demonstrate the validity of the proposed grounded inductor and its behavior is tested in a parallel resonant circuit. The computer simulation on Pspice is used to realize the theoretical analysis.

CHAPTER 5

FOUR TERMINAL FLOATING NULLOR BASED INDUCTOR

5.1 The Nullator, Norator and Nullor:

The Nullator and Norator are theoretical active devices that have been used in the analysis, design and synthesis of linear circuits. Known since the 1950's, these are concepts that, in spite of their enormous potential for the design of electronic circuits, have not been considered widely. One of the possible reasons is that, unlike others like the resistance and capacitance, these elements do not respond to the idealization process of any physical device.

Few attempts were made to use both Nullator and Norator as single terminal active devices, but proved instead that they are not physically realizable. Later, Tellegen also showed these devices were mathematical concepts without a physical content. Few years later it was proposed that the combination of Nullator and Norator could be accepted as a physical device, called Nullor. This is so because the Nullor has two ports and is characterized by two equations.

Nullator

Fig5.1 shows a two terminal Nullator which does not allow current flow through it, and the voltage across its terminals is zero under all conditions.

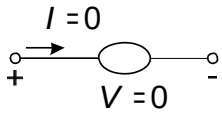


Fig5.1: Nullator symbol representations

Norator

A Norator, as shown in Fig5.2 has an arbitrary voltage and current across its terminals. This element has no constitutive equation.

Fig5.2: Norator symbol representations

Nullor

Together, both Nullator and Norator form the Nullor, as shown in Fig5.3.

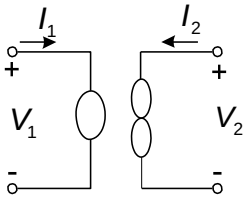


Fig5.3: Two-port Nullor symbol

It is defined as a two-port network element, whose transmission matrix is the null matrix, that is:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \quad (5.1)$$

A characteristic that makes the Nullor attractive is that it is a universal active element. This concept means that together with capacitors and resistors we can implement a maximum number of functions (ideally all) with the minimum number of such devices. That is, if a suitable set of linear and nonlinear passive elements is available, then no active elements other than Nullors are needed to implement any linear or nonlinear circuit function. In particular the Nullor, resistance and capacitance form a complete set for linear circuits.

5.2 Equivalence and properties of Nullators and Norators:

Fig5.4 shows equivalencies of combinations of Nullators and Norators. By connecting these two elements with others, and making use of these properties, it is shown the potentiality and usefulness of the Nullor for analysis, realization and design of electric circuits. Various circuit elements such as the ideal transistor and operational amplifier can be modeled with such equivalences.

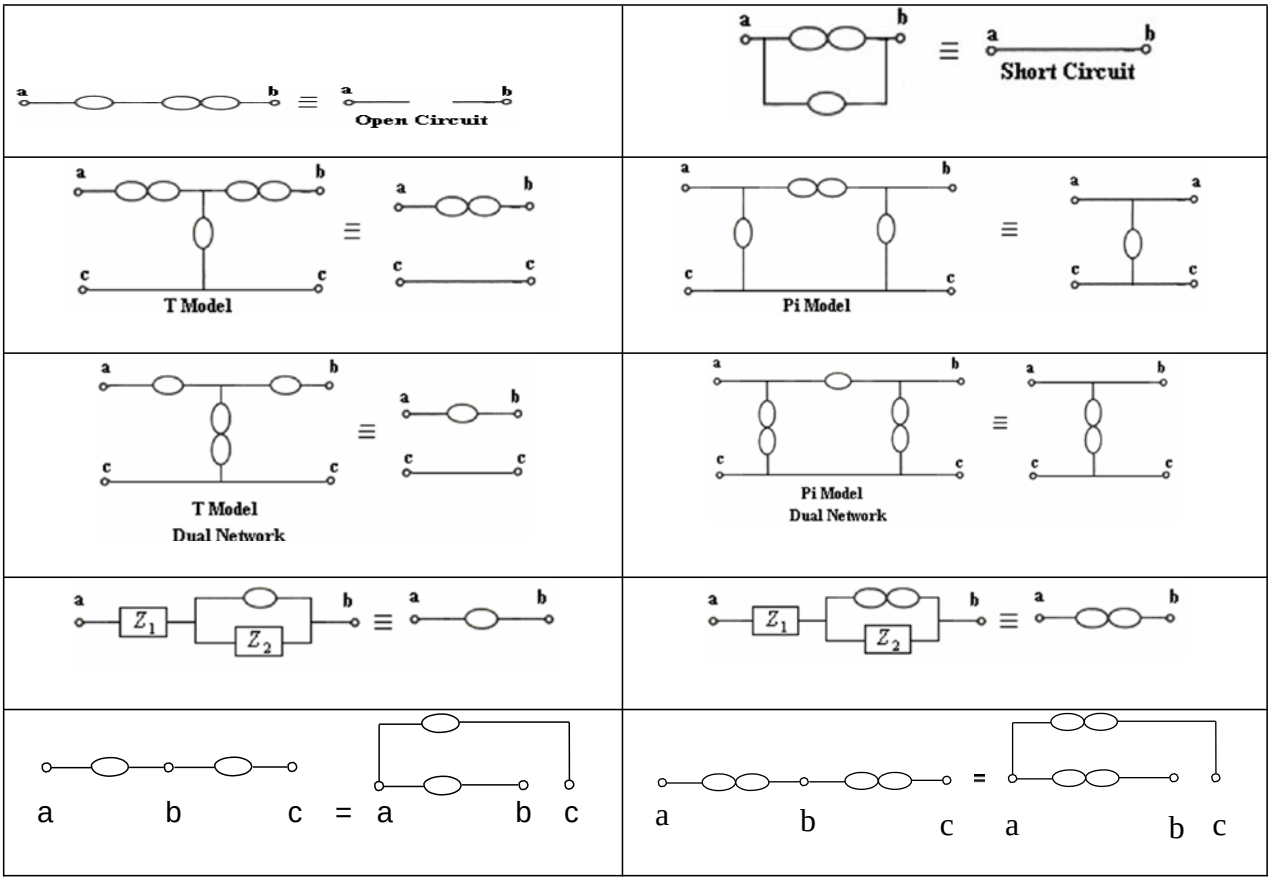


Fig5.4: Nullator and Norator equivalences

5.3 Nullor as a modeling device:

The Nullor has been used extensively as a modeling device in linear circuits. An example of this arouse from circuits realized with triodes with difficulties on device modeling. To overcome this modeling difficulty, the Unitor was proposed. The Unitor, in Fig5.5 is defined as a floating three terminal element which acts as a unilateral unity-gain voltage transfer element from 1 to 2, with 3 as a common node, and as a unilateral unity-gain current transfer element from 2 to 3 with 1 as a common node.

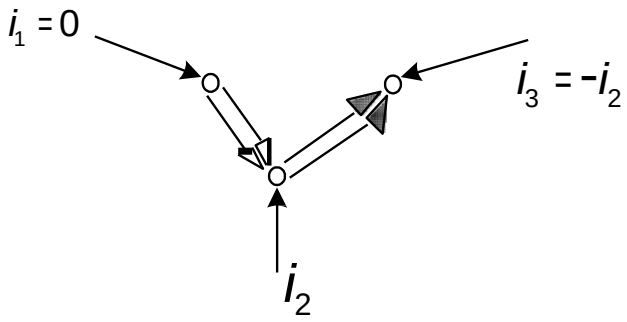


Fig5.5: Unitor and its port description

The corresponding equations are:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \quad \begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \tag{5.2}$$

Unity Gain Voltage Transfer Unity Gain Current Transfer

This representation gave recognition to the ac modeling of ideal transistors by means of Nullor devices as shown in Fig5.6. Thus, a Unitor is equivalent to a three terminal Nullor. Due to the already mentioned fact, that a complete set is composed by an interconnection of resistances, capacitances and Nullors.

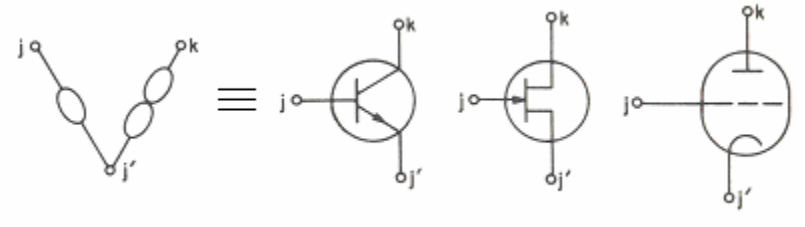


Fig5.6: AC modeling of transistors and triodes by a Unitor, or three terminal Nullor

5.4 Nullors and transistors:

Ideal AC transistors can be modeled by a Nullor in which the Nullator and Norator share a common terminal as shown in Fig5.6. The equivalent model for single transistors shown in Fig5.6 can be used to form four terminal elements with transistors, using equivalencies applicable to the two terminal elements of Nullators and Norators. Such equivalencies were shown in Fig5.4 while Fig5.7 shows the realized Nullor. Hence, it can be said that the simplest AC Nullor consists of two transistors.

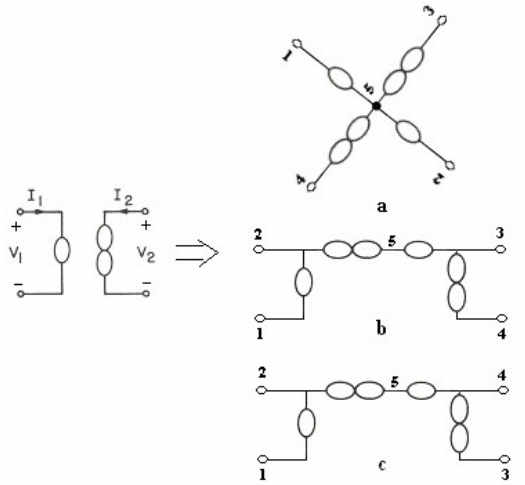


Fig5.7: Composite transistor representations for a four terminal Nullor.

5.5 Operational Amplifier, Current Conveyor and Nullor:

The current conveyor and the operational amplifier have been two dominant active devices in the analog market. An operational amplifier is considered a voltage- mode device whereas the current conveyor a current-mode active device. Both devices can be represented by means of Nullor equivalent circuits.

An Operational Amplifier is a voltage amplifier with high gain. The symbol for the ideal and non-ideal operational amplifier is shown in Fig5.8.

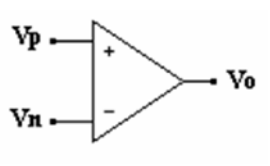
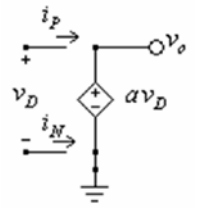
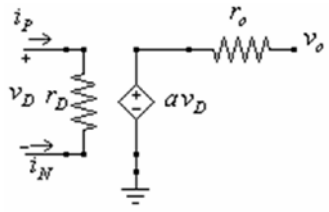
Symbol	Ideal Finite Gain Model	Basic Model
		

Fig5.8: Operational Amplifier symbol, ideal and non-ideal model

The ideal terminal conditions of the operational amplifier are:

Voltage Gain (A) = ∞

Differential Resistance r_d = ∞ (5.3)

Output resistance r_o = 0

Differential Voltage V_d → 0 and V_n = V_p

It is observed from these terminal conditions and the ideal model that an operational amplifier is realized by a voltage-controlled voltage source. That is, an infinite gain operational amplifier is a special case realization of a Nullor.

In the same way as the operational amplifier, the Current-Conveyor (CCII) introduced by Sedra and Smith in 1970 can be used to implement many analog signal processing functions. Fig5.9 shows the current-conveyor symbol. The Definition of the CCII is shown in matrix form equation (5.4)

Fig5.9: Current-conveyor circuit symbol

$$\begin{bmatrix} I_X \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_Y \\ V_Z \end{bmatrix} \tag{5.4}$$

In other words, the terminal Y exhibits infinite input impedance. The voltage at X follows that applied to Y, thus X exhibits zero input impedance. The current supplied to X is conveyed to the high-impedance output terminal Z where it is supplied with either positive polarity (CCII+) or negative polarity (CCII-). Thus, a simplified version of equation (5.4) results in:

$$I_X = 0$$

$$V_X = V_Y \tag{5.5}$$

$$I_Z = \pm I_Y$$

These conditions cast light on the relation on CCII, Unitor and Nullors. Equation (5.2) describes the behavior of a Unitor i.e. unity-gain voltage transfer ($V_x = V_y$) and unity-gain current transfer ($I_z = \pm I_x$). As a result of this, a CCII is equivalent to a Unitor, and to the already mention three terminal Nullor.

5.6 Operational Amplifier realizations based on nullors:

Fig5.10 shows a nullor based general immittance converter (GIC). It can transform to an impedance or admittance with a terminated load.

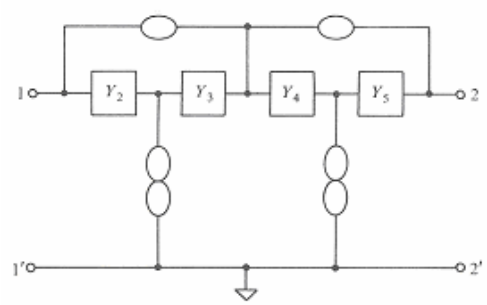


Fig5.10: Nullor based general immittance converter

If, for example terminals 2-2' are terminated with conductance $G_{6,}$ the driving-point admittance Y_{1d} for $Y_2 = G_2, Y_3 = sC_3, Y_4 = G_4$ *and* $Y_5 = G_5$ is calculated as:

$$Y_{1d} = \frac{G_2 G_4 G_6}{S\, G_3 G_5} \tag{5.6}$$

One of the main applications of GIC's is the inductance simulation. The general idea of inductance simulation is simply to replace the inductance elements of a passive LC filter by GIC-simulated inductances. As one would expect, the non-ideal performance of the simulated inductance becomes of critical importance on most active filters that are designed this way.

Fig5.11 shows the equivalent operational amplifier network of Fig5.10. Each admittance has been replaced by either a conductance (G_2, G_4, G_5, G_6) and by a capacitance C_3. The equivalent inductance value is:

$$\mathrm{Z_{1d}} = \frac{1}{\mathrm{Y_{1d}}} = s\frac{\mathrm{G_3 G_5}}{\mathrm{G_2 G_4 G_6}} \tag{5.7}$$

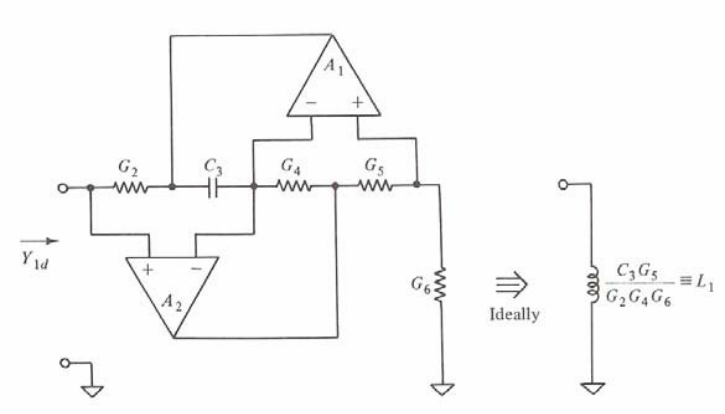
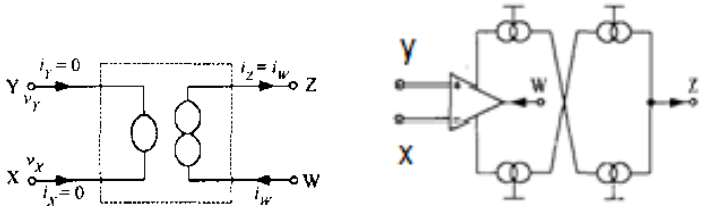


Fig5.11: Equivalent GIC using operational amplifiers

5.7 Nullor Model of the FTFN:



(a) (b)

Fig5.12: Model of the FTFN (a) an ideal nullor model
(b) possible implementation model

An FTFN is a high gain transconductance amplifier with floating input and output terminals or can be called as an operational floating amplifiers (OFAs). The nullor model of an ideal FTFN is shown in Fig5.12 (a), where the port characteristics can be described as :

$$I_Y = I_X = 0 \, , V_X = V_Y \; and \; I_Z = I_W \qquad (5.8)$$

It should be noted that the output impedance of the W and Z ports are generally arbitrary. However, most of the FTFNs are traditionally realized from the basic type shown in Fig5.12 (b), where the output impedance of the W-port is very low and that of the Z-port is very high. This type of FTFN is also called as operational mirrored amplifiers (OMAs). In addition, the usefulness of the FTFN can be extended if eqn. (5.8) is implemented in such a way that the current transfer ratio between I_W and I_Z can be varied by electronic means, in which case a more generalized tunable FTFN can be investigated.

5.8 Four Terminal Floating Nullor (FTFN) :

A nullor approximation with both input and output ports floating is called a Four Terminal Floating Nullor (FTFN). An approximation of the FTFN as in is shown in Fig5.13

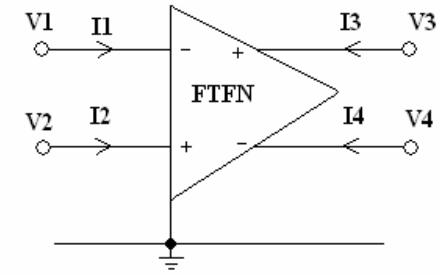


Fig5.13: Four Terminal Floating Nullor block representation

At the input the nullator is defined by:

$$I_1 = -I_2$$
$$I_1 = 0 \qquad (5.9)$$
$$V_1 - V_2 = 0$$

And the norator by:

$$I_3 = -I_4 \qquad (5.10)$$

The equation $I_3 = -I_4$ makes the FTFN fulfill Kirchhoff current law, $I_1 = -I_2$ is the equation added to the all-zero chain matrix (2.1).From these equations it is seen that the FTFN accurately equates two voltages connected to the terminals of the input port, like a standard operational amplifier, but in addition, it accurately equates two currents connected to the terminals of the output port. That is why some researchers claim that an FTFN combining both voltage and current mode capabilities is a more versatile analog building block than the operational amplifier or second-generation current conveyor. For such purpose, different physical realizations of a nullor have been proposed and some of these are presented next.

5.9 Proposed Tunable Four Terminal Floating Nullor :

The circuit implementation and representation of the proposed tunable FTFN, namely TFTFN, with variable current gain is shown in Fig5.14 and Fig5.15, which is suitable for the implementation in bipolar integrated circuit form.

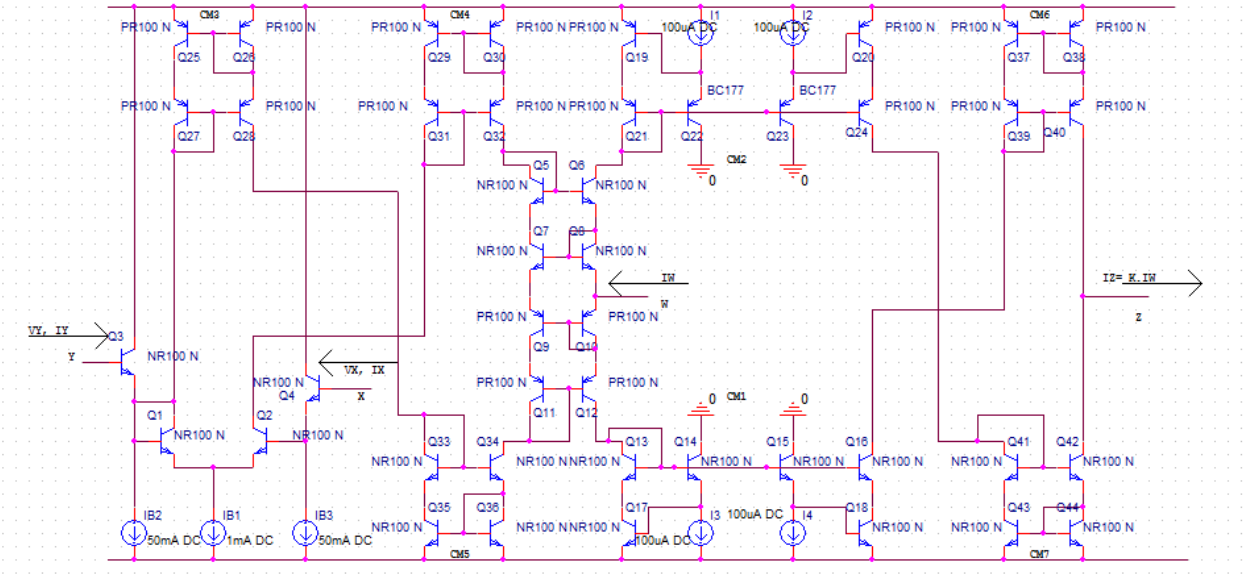


Fig5.14: The proposed tunable FTFN Circuit Diagram

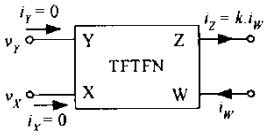


Fig5.15: The proposed tunable FTFN: Block Representation

5.10 Circuit Description:

The proposed circuit consists of a transconductance amplifier Q_1-Q_4, an improved translinear cell Q_5-Q_{12}, complementary current mirrors with controlled current gain CM1-CM2 and five standard improved Wilson current mirrors CM3-CM7.

Transistors Q_1–Q_4 and the bias currents I_{B1}-I_{B3} function as a transconductance amplifier with very high input impedance so that $i_y = i_x = 0$. If Q_1-Q_4

are perfectly matched, then the voltage at node X will follow the voltage at the port Y, or $V_X = V_Y$. Group of transistors Q_5-Q_{12} forms an improved translinear cell, which Q_7-Q_{10} functions as a dual translinear loop. It should be noted that the so called "piled- stage structure" consisting of eight transistors which can improve performance and accuracy of the basic loop is employed, where the standard translinear condition $V_{CB} = 0$ are forced by the additive cascode transistors Q_5, Q_6, Q_{11} and Q_{12}. Ideally, it is required that the pair of transistors Q_7-Q_8 and Q_9-Q_{10} are closely matched and the cascode current mirrors CM3, CM4 and CM5 have the exactly unity gain.

Consequently, for $V_X = V_y = O$, the quiescent currents through Q_6, Q_8 and Q_{10}, are respectively equal to the quiescent current of the diode-connected transistors Q_5 and Q_{11}, and are equal to $I_b/2$. This translinear cell performs as a current follower, where it allow an input current I_W to source and sink at terminal W. By two complementary variable-gain current mirrors CM1- CM2 and assuming that the current gain of the current mirrors CM6-CM7 are equal to unity, the current I_W flowing through the port W will be reflected and inverted to the port Z, which has the current transfer ratio as $k = Iz/Iw$. The output impedance at the port W is low since it is looking into the emitters of translinear cell's transistors while the output impedance of the port Z is very high due to the effective parallel combination of output impedances of the cascode current mirrors CM6 and CM7.

Therefore, this TFTFN will provide a unity voltage transfer between ports Y and X, and a current transfer between ports W and Z that the gain value is equal to *k.* The voltage and current characteristics of this device can be characterized as follows:

$$I_Y = I_X = 0, V_X = V_Y \text{ and } I_Z = KI_W \tag{5.11}$$

We can see that the proposed FTFN in Fig5.13 can be tuned electronically by adjusting the ratio of the external bias currents I_1 / I_2.

5.11 Simulation results:

The proposed Tunable Four terminal Floating Nullor was simulated using AT&T ALA400-CBIC-R process parameter of NR100N and PR100N for npn and pnp transistors, respectively. The bias currents were set to I_{B1} = 1 mA, I_{B2} = I_{B3} =50 uA and the supply voltages were set to +V = -V = 5V. In order to demonstrate the successful working of FTFN the output current characteristic and transconductance were tested on Pspice simulation which are shown below:

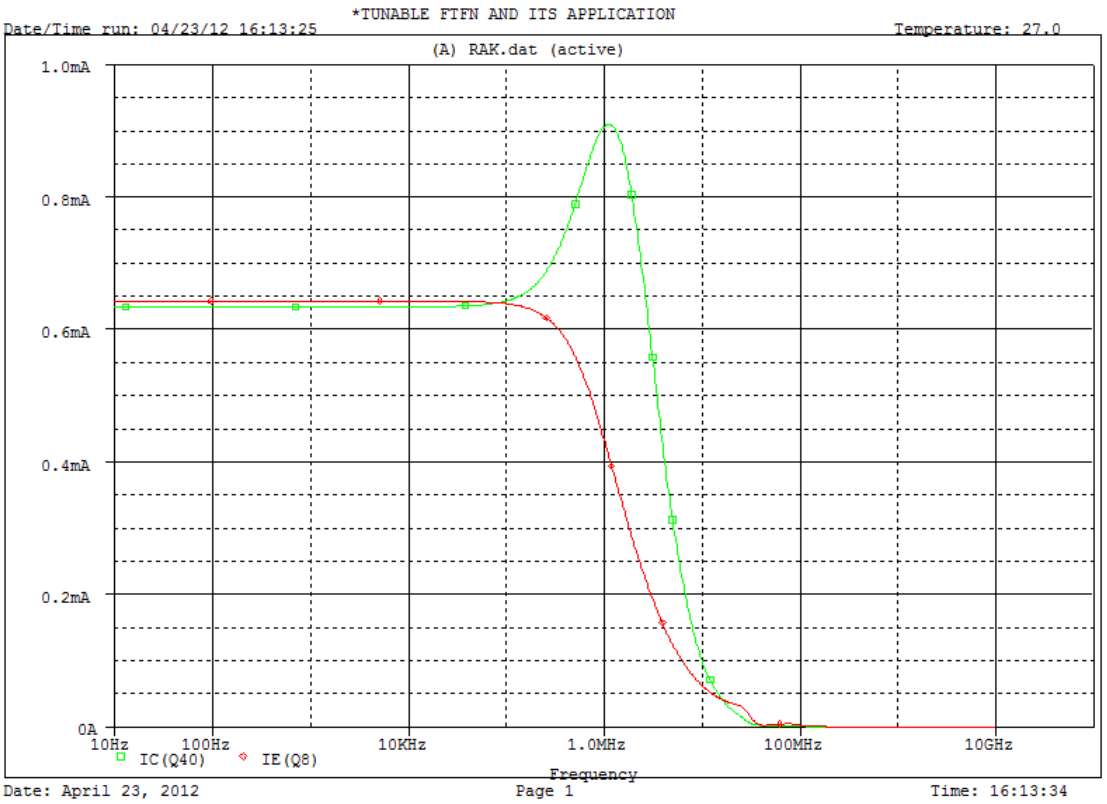


Fig5.16: Output Current characteristic of the simulated FTFN (Iz and Iw)

RESULT:

The graph shown above clearly describes that that I_z and I_w were nearly equal upto 500 KHz. Thus we can say that the operating range of this FTFN is maximum upto 500 KHz.

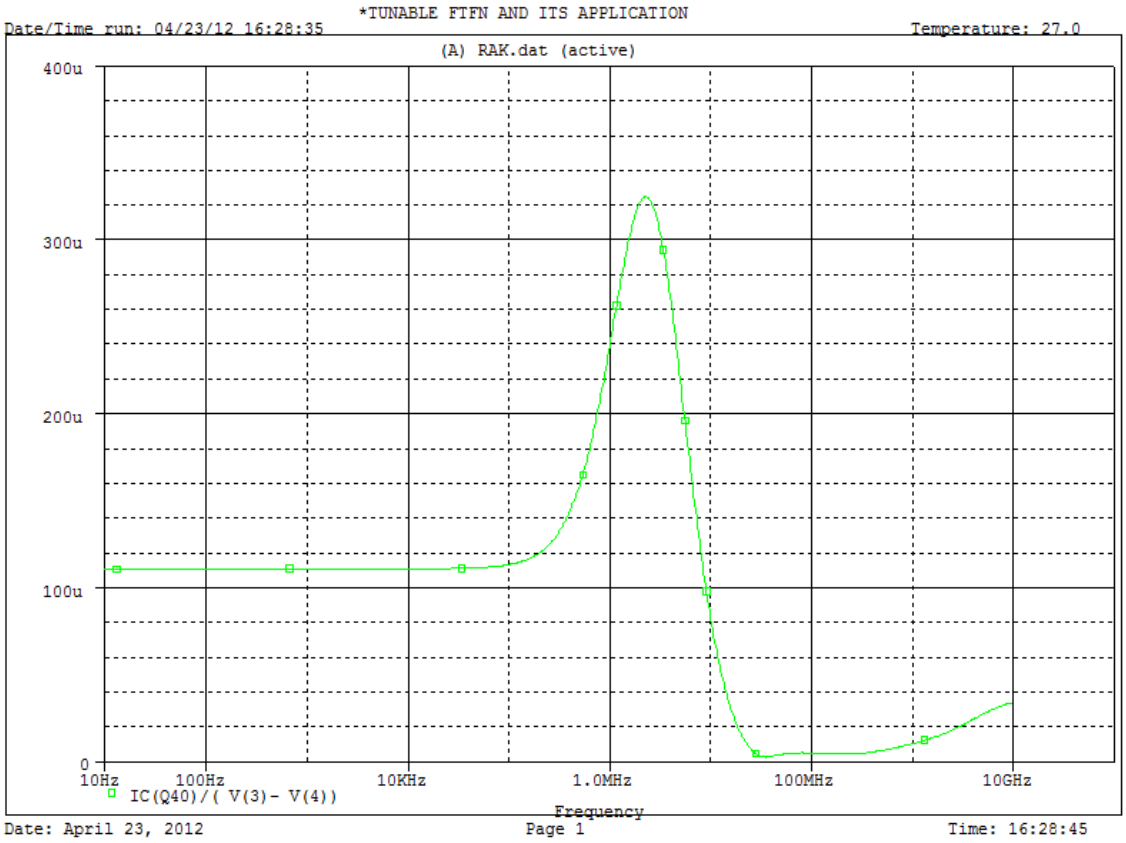


Fig5.17: Transconductance Gain of Simulated FTFN

RESULT:

The above graph clearly revels that the transconductance of the simulated FTFN is 115 mho upto 500KHz which is the maximum operating frequency range of the simulated FTFN.

5.12 Application of Simulated FTFN:

In order to test the proper functioning of the simulated FTFN it been used to simulate some well-known circuits which are taken below:

5.12.1 Voltage to Current Converter

In order to demonstrate the tunable performances of the proposed circuit, the TFTFN was used to construct the voltage-to-current converter shown in Fig5.18 with R_W = 1 kΩ and output Z short-circuited.

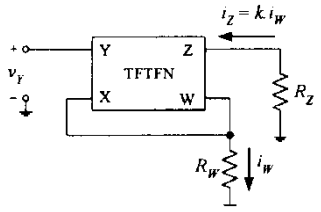


Fig5.18: TFTFN-based voltage-to-current converter

The voltage transfer characteristic from port Y to port X is shown in Fig5.19 below:

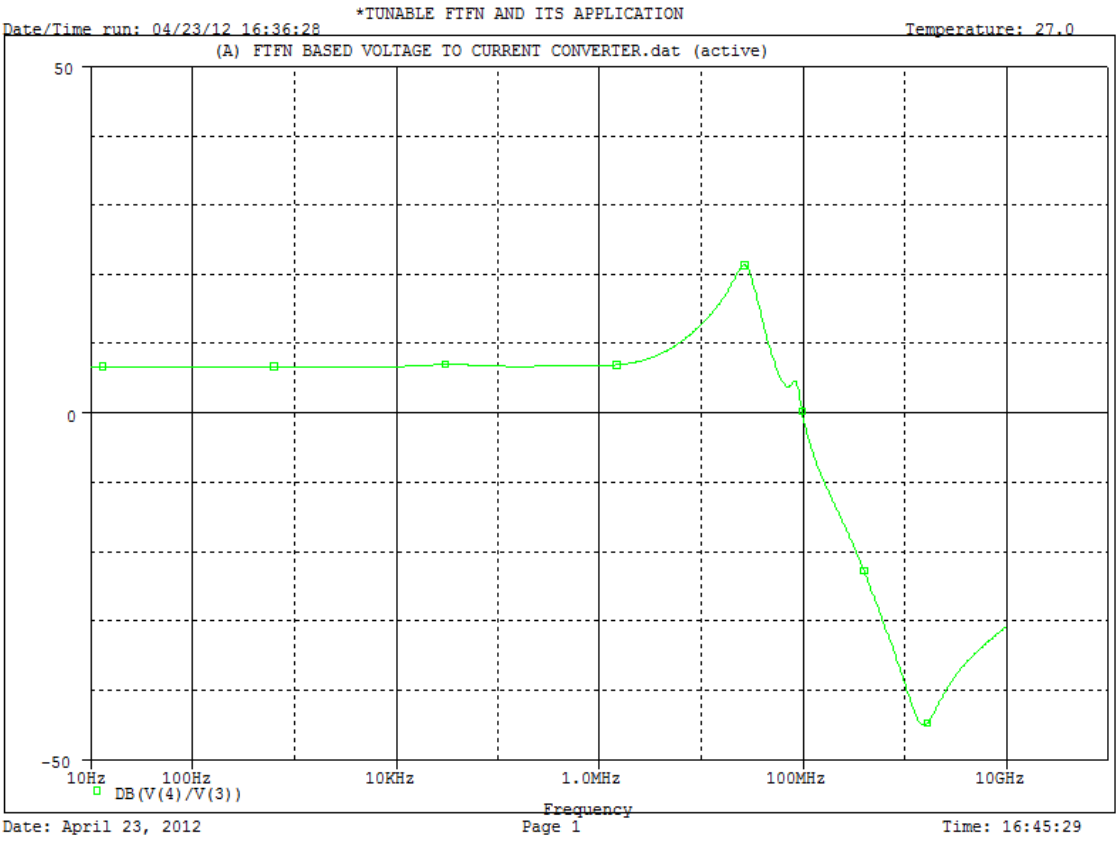


Fig5.19: voltage transfer characteristic from port Y to port X of the simulated FTFN

RESULT:

The output of the computer simulation clearly matches with the graph given in the paper.

The frequency response for the TFTFN based Voltage-to-current converter as shown in Fig5.18 of the current gain *k*, for three different values of the DC bias current I_1 whereas I_2 is set to 100 uA. The simulated current transfer characteristic proves that the circuit can exhibit an electronically tunable current gain over a very wide current range.

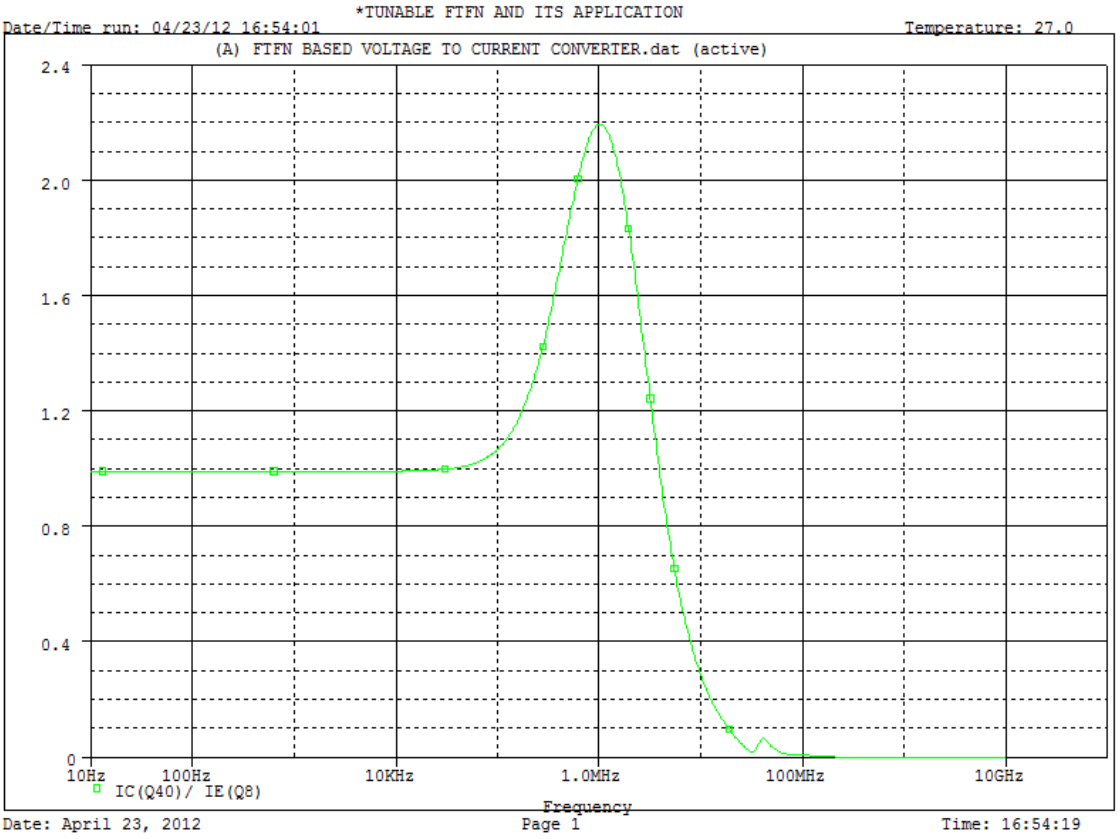


Fig5.20: Current transfer characteristic Iz /Iw when the external bias current I_1 was set to 80uA

RESULT:

The output of the computer simulation clearly matches with the graph given in the paper.

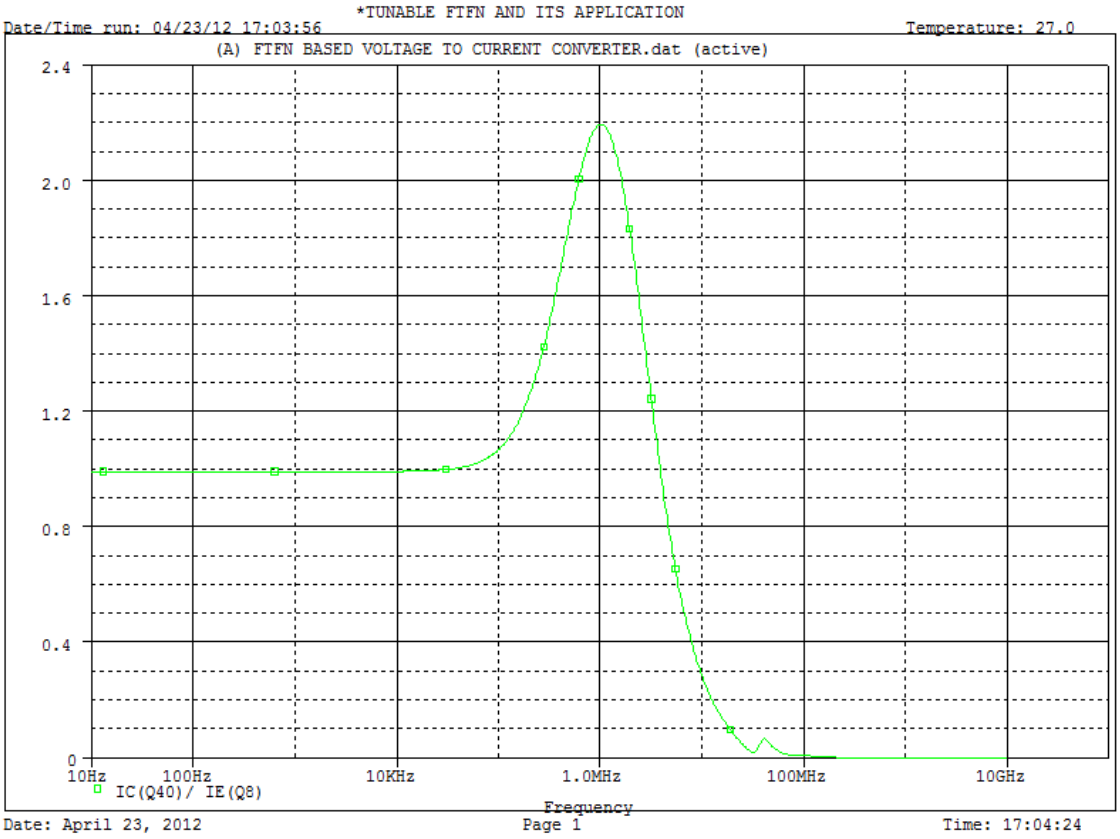


Fig5.21: Current transfer characteristic Iz /Iw when the external bias current I_1 was set to 100uA

RESULT:

The output of the computer simulation clearly matches with the graph given in the paper

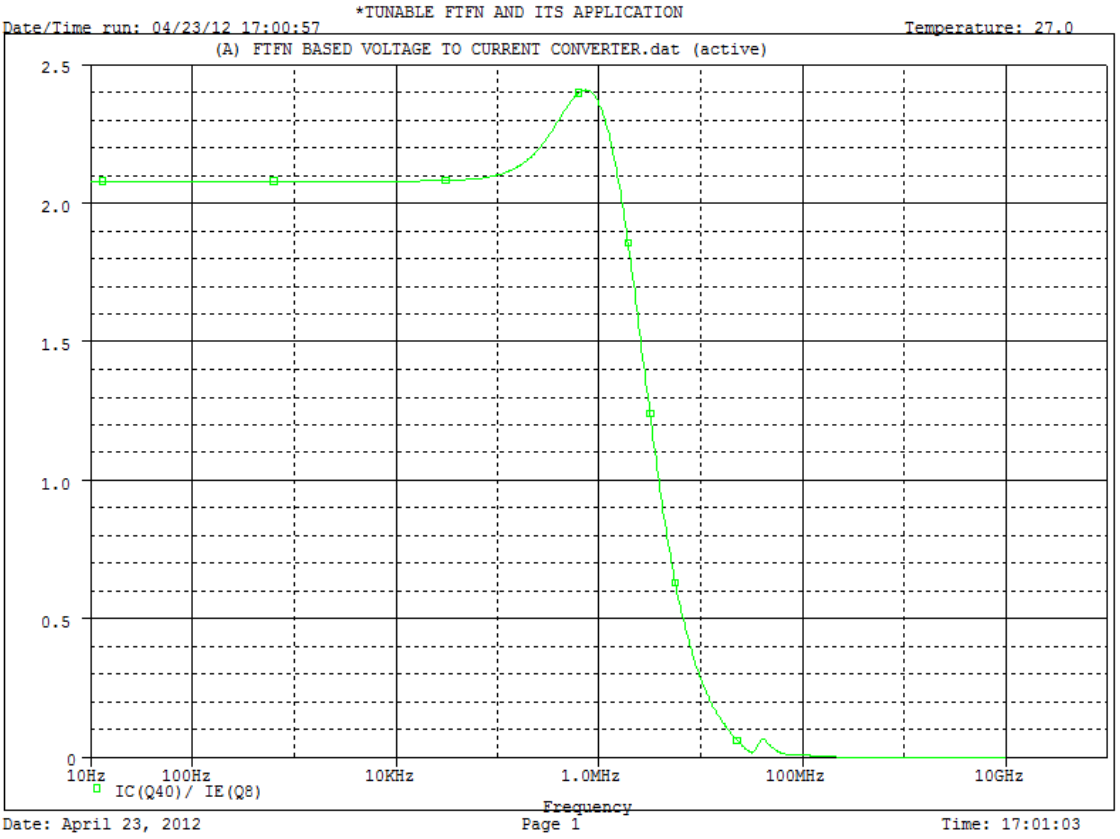


Fig5.22: Current transfer characteristic Iz /Iw when the external bias current I_1 was set to 130uA

RESULT:

The output of the computer simulation clearly matches with the graph given in the paper.

5.12.2 TFTFN based All Pass Filter:

In this section, the proposed TFTFN as a tunable active element will be described for constructing an electronically tunable current mode all pass filter shown in Fig5.23

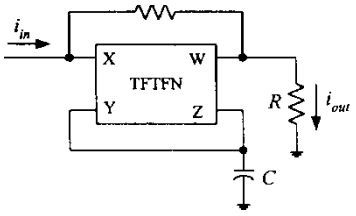


Fig5.23: Current-mode allpass filter using TFTFN

As the second example of the proposed TFTFN, it was constructed an electronically tunable current mode allpass filter shown in Fig5.23. The circuit is based on a current-mode allpass filter by using FTFN with grounded capacitor, routine analysis yields the current transfer function expressed by:

$$\frac{I_{OUT}}{I_{IN}} = \frac{1-(\frac{sRC}{K})}{1+(\frac{sRC}{K})} \tag{5.12}$$

and ,

$$\phi_d = -2\tan^{-1}(wRC/K) \tag{5.13}$$

Where, ϕ_d is the phase angle of the filter. As an example, the simulation results of a current-mode allpass filter in Fig5.23 were presented with R_1=1kΩ, C =1nF, this phase shifter was designed for a 90° phase shift when, k = 1 i.e. I_1= I_2 = 100 pA. Fig5.24 shows the phase characteristic of the simulated FTFN on the frequency responses of the filter shown in Fig5.23. This confirms the validity of the results of the theoretical analysis.

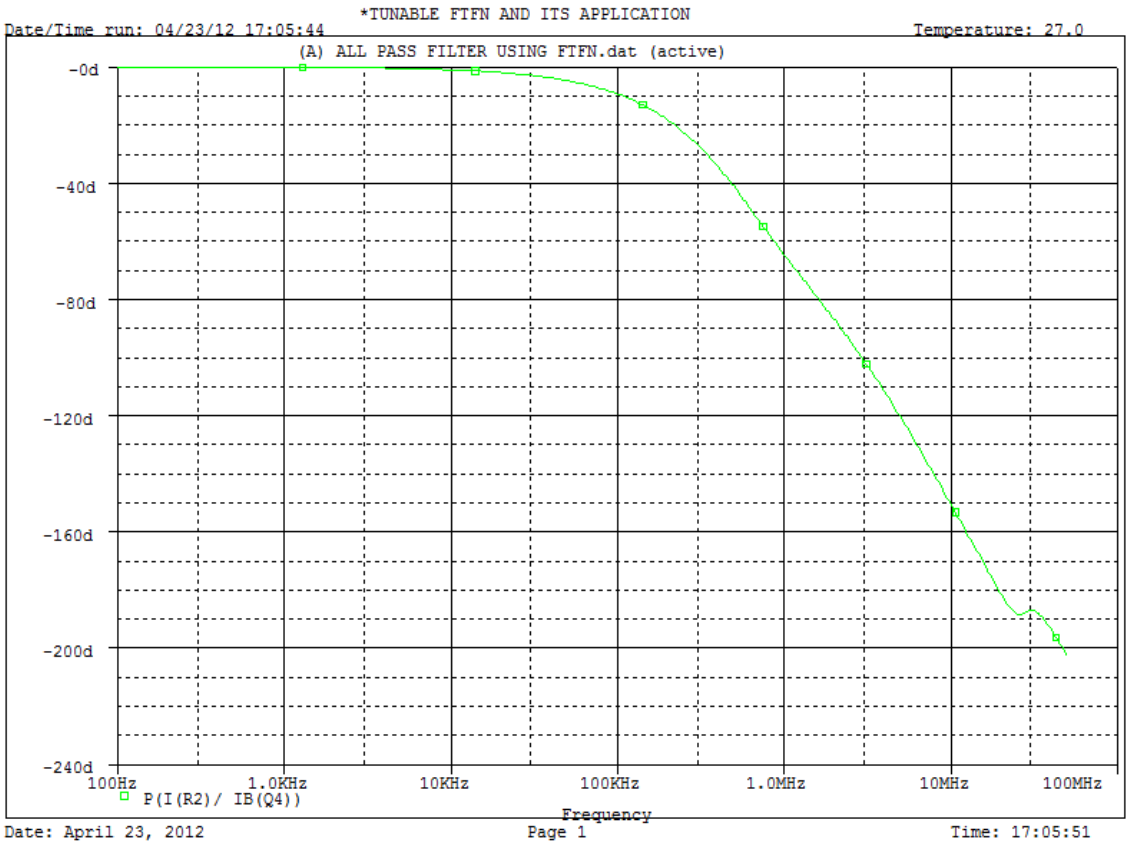


Fig5.24: Phase characteristic of the TFTFN-based Current mode All Pass Filter

RESULT:

The output of the computer simulation clearly matches with the graph given in the paper

5.13 FTFN Based Inductor:

An inductance simulator topology based on an FTFN has been introduced for inductor less realization of circuits that contains both grounded and floating inductor elements. The FTFN-based inductance simulator, shown in Fig5.25, allows one to simulate not only a grounded inductor but also a floating inductor. Although the FTFN-based inductance simulator structure is shown in floating inductor form in Fig5.25, this simulator may also be used as a grounded inductor by connecting one port of the floating inductance to ground.

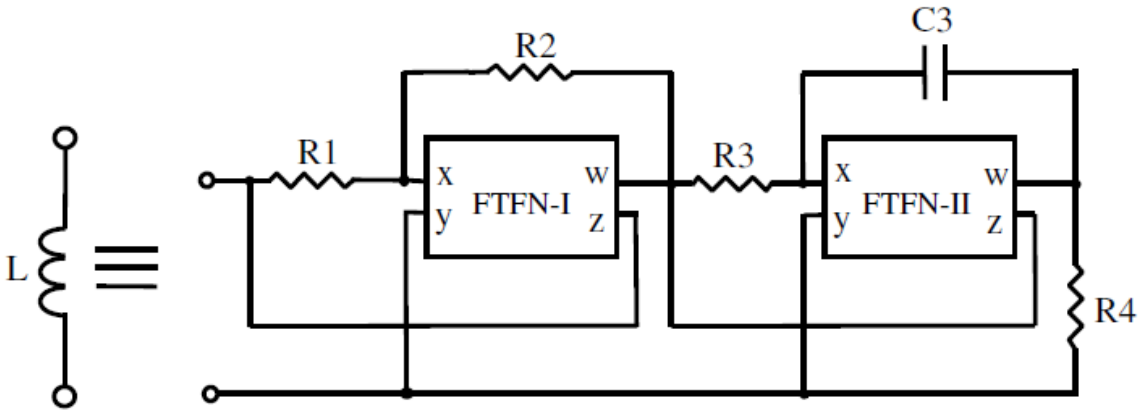


Fig5.25: FTFN-based Inductor Circuit

Routine analysis yields the equivalent inductance between the two terminals as:

$$L_{EQ} = \frac{C_3 R_1 R_2 R_3}{R_4} \qquad (5.14)$$

In order to test the proper functioning of the simulated FTFN it been used to simulate some well-known circuits which are taken below:

5.13.1 Low pass LR filter using FTFN based Inductor:

On selecting,

$$R_1 = R_2 = R3 = R_4 = 1K\Omega \text{ and } C_3 = 18nF ,$$

we would obtain $L_{eq} = 18mH$.

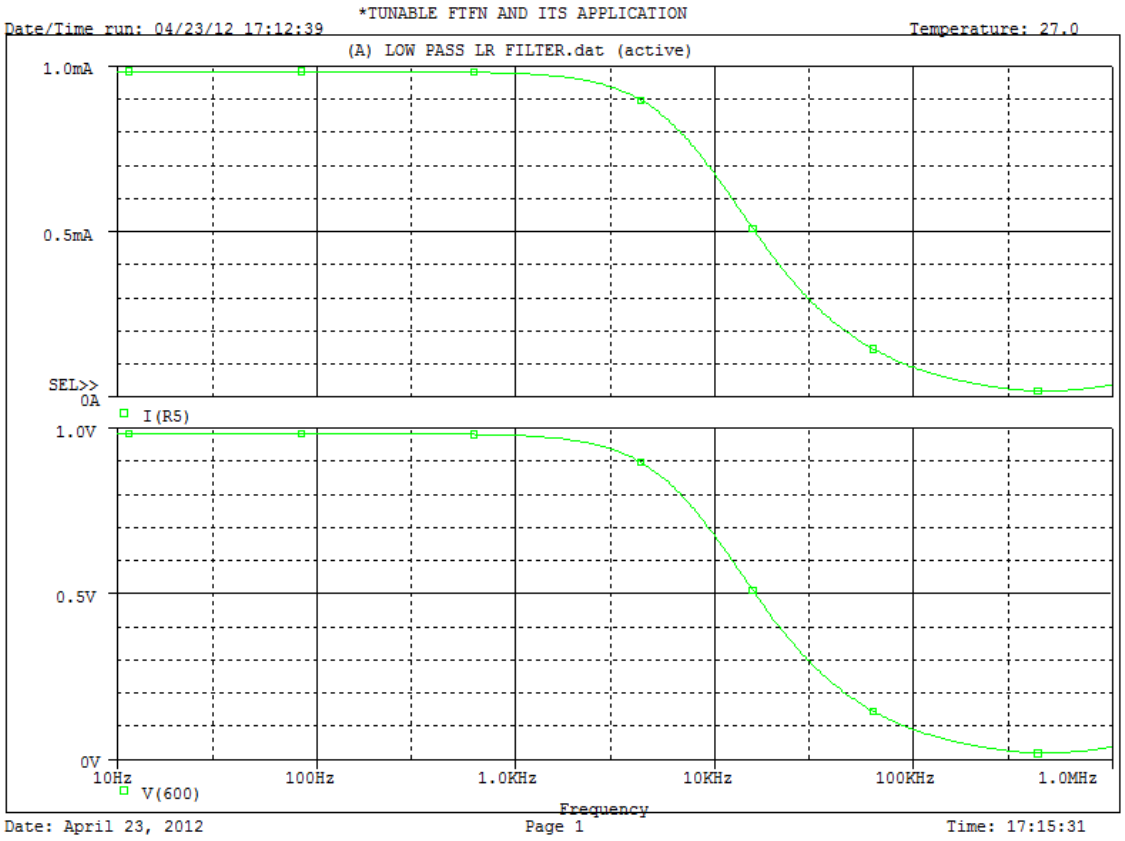


Fig5.26: FTFN-based LR low pass filter output

Result:

3db Cut off Frequency (*fo)* of Low Pass RL filter = 9.43387KHz

Moreover at Cut off frequency, $f_o = \frac{R}{2\pi L}$

Which gives Inductance = 16.8791 mH (Approx).

5.13.2 High pass RL filter using FTFN based Inductor:

On selecting,

$R_1 = R_2 = R3 = R_4 = 1K\Omega$ and $C_3 = 18nF$,

we would obtain $L_{eq} = 18mH$.

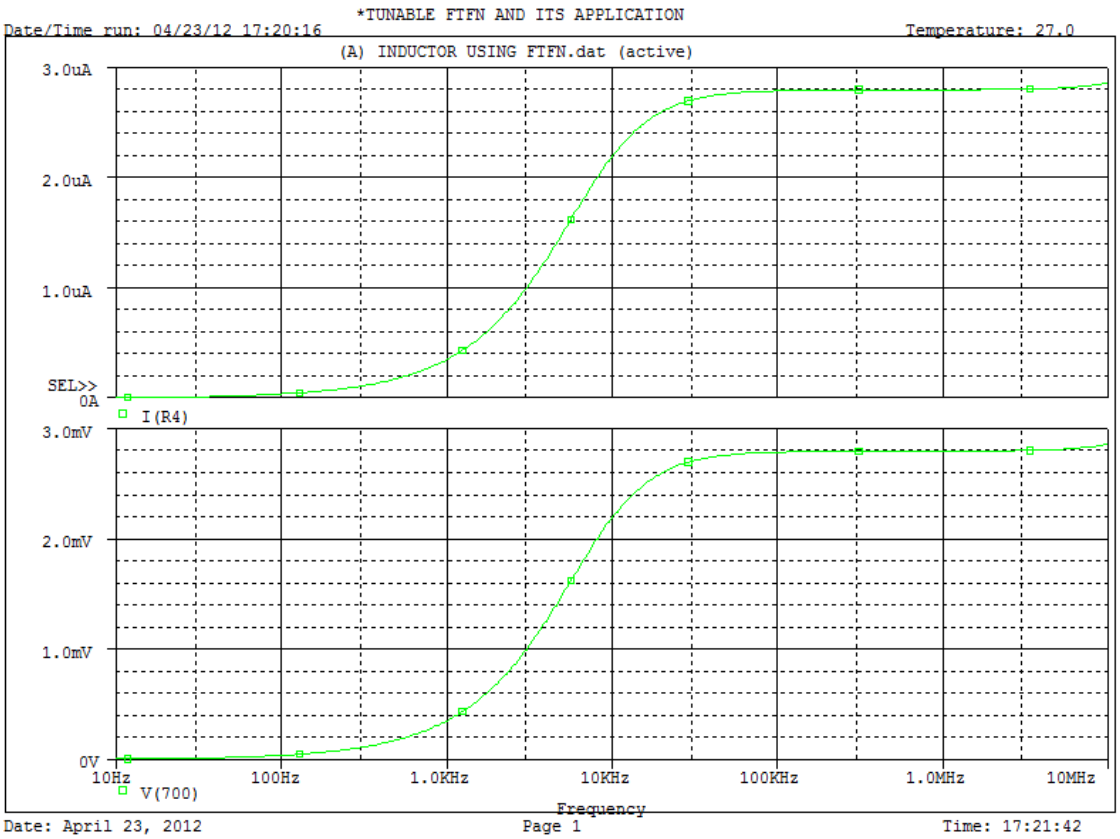


Fig5.27: FTFN-based RL High pass filter output

Result:

3db Cut off Frequency (*fo)* of Low Pass RL filter = 8.33604KHz

Moreover at Cut off frequency, $f_o = \frac{R}{2\pi L}$

Which gives Inductance = 19.1020mH (Approx).

5.14 Conclusion:

A generalized electronically tunable FTFN, which is suitable for realizing in bipolar monolithic integrated circuit form, has been presented. Simulation results obtained from PSPICE program verify the high qualification performances of the proposed circuit. Some application examples have been demonstrated, that the use of the proposed scheme is attractive.

CHAPTER 6:

CONCLUSION AND FUTURE SCOPE

In this report Inductance simulation was carried out using active devices.

In the first chapter an introduction was presented which briefly describes the importance of Inductor in Integrated circuits and an overview of the work presented in this report.

In the second chapter Literature Review was presented which briefly describes the modification of inductor depending upon its requirements in different technologies.

In the third chapter BJT based Operational Transconductance Amplifier was presented which was further used to realize floating positive and negative inductance. The inductance realization was further checked on series RLC circuit and Inductance cancellation circuit.

In the fourth chapter CMOS based Modified Dual output Differential Difference Current Conveyor was presented which was further used realizing lossless grounded inductance. The inductance realization was further checked on Parallel RLC circuit.

In the fifth chapter BJT based Four Terminal Floating Nullor was presented which was further used for realizing floating and grounded inductance. The FTFN circuit was further checked on Voltage to Current converter and an all pass filter while the FTFN based inductor was checked on High pass and Low Pass RL circuits.

These signal processing circuits have been simulated on PSpice. Results closely match with theoretical values.

SCOPE FOR FURTHER WORK:

In the present work the emphasis was on Inductance realization using active devices. Lots of research activity is currently under way in the direction of active devices based inductance simulation. Several directions in which the present work can be extended have been given below:

- Minimization of active devices required for realizing active devices.
- Minimization of active blocks required for realization of inductance.
- Realization of electronically tunable inductance.
- Minimization of passive components required for inductance simulation.
- Realization of inductance using low voltage power supply.

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APPENDIX

AT&T ALA 400-CBICR transistor parameters:

NPN Transistors:

*NR100N - IX PNP TRANSISTOR

.MODEL NXI NPN(RB=524.6 IRB=0 RBM=25 RC=50 RE=1

+IS=121E-18 EG=1.206 XTI=2 XTB=1.538 BF=137.5

+IKF=6.974E-3 NF=1 VAF=159.4 ISE=36E-16 NE=1.713

+BR=0.7258 IKR=2.198E-3 NR=1 VAR=10.73 ISC=0 NC=2

+TF=0.425E-9 TR=0.425E-8 CJE=0.214E-12 VJE=0.5

+MJE=0.28 CJC=0.983E-13 VJC=0.5 MJC=0.3 XCJC=0.034

+CJS=0.913E-12 VJS=0.64 MJS=0.4 FC=0.5)

*NR200N - 2X NPN TRANSISTOR

.MODEL NX2 NPN(RB=262.5 IRB=0 RBM=12.5 RC=25 RE=0.5

+IS=242E-18 EG=1.206 XTI=2 XTB=1.538 BF=137.5

+IKF=13.94E-3 NF=1.0 VAF=159.4 ISE=72E-16 NE=1.713

+BR=0.7258 IKR=4.396E-3 NR=1.0 VAR=10.73 ISC=0 NC=2

+TF=0.425E-9 TR=0.425E-8 CJE=0.428E-12 VJE=0.5

+MJE=0.28 CJC=1.97E-13 VJC=0.5 MJC=0.3 XCJC=0.065

+CJS=1.17E-12 VJS=0.64 MJS=0.4 FC=0.5)

PNP Transistors:

*PR100N - IX PNP TRANSISTOR

.MODEL PXI PNP (RB=327 IRB=0 RBM=24.55 RC=50 RE=3

+IS=73.5E-18 EG=1.206 XTI=1.7 XTB=1.866 BF=110.0

+IKF=2.359E-3 NF=1 VAF=51.8 ISE=25.1E-16 NE=1.650

+BR=0.4745 IKR=6.478E-3 NR=1 VAR=9.96 ISC=0 NC=2

+TF=0.610E-9 TR=0.610E-8 CJE=0.180E-12 VJE=0.5

+MJE=0.28 CJC=0.164E-12 VJC=0.8 MJC=0.4 XCJC=0.037

+CJS=1.03E-12 VJS=0.55 MJS=0.35 FC=0.5)

*PR200N - 2X PNP TRANSISTOR

.MODEL PX2 PNP(RB=163.5 IRB=0 RBM=12.27 RC=25 RE=1.5

+IS=147E-18 EG=1.206 XTI=1.7 XTB=1.866 BF=110.0

+IKF=4.718E-3 NF=1 VAF=51.8 ISE=50.2E-16 NE=1.65

+BR=0.4745 IKR=12.96E-3 NR=1 VAR=9.96 ISC=0 NC=2

+TF=0.610E-9 TR=0.610E-8 CJE=0.36E-12 VJE=0.5

+MJE=0.28 CJC=0.328E-12 VJC=0.8 MJC=0.4 XCJC=0.074

+CJS=1.39E-12 VJS=0.55 MJS=0.35 FC=0.5)

0.35 µm TSMC CMOS transistor parameters:

NMOS Model:

.MODEL NMOS NMOS (LEVEL = 3

+ TOX = 7.9E-9 NSUB = 1E17 GAMMA = 0.5827871

+ PHI = 0.7 VTO = 0.5445549 DELTA = 0

+ UO = 436.256147 ETA = 0 THETA = 0.1749684

+ KP = 2.055786E-4 VMAX = 8.309444E4

+KAPPA = 0.2574081 RSH = 0.0559398 NFS = 1E12 TPG = 1

+ XJ = 3E-7 LD = 3.162278E-11 WD = 7.046724E-8

+ CGDO = 2.82E-10 CGSO = 2.82E-10 CGBO = 1E-10

+ CJ = 1E-3 PB = 0.9758533 MJ = 0.3448504

+ CJSW = 3.777852E-10 MJSW = 0.3508721)

PMOS Model:

.MODEL PMOS PMOS (LEVEL = 3

+ TOX = 7.9E-9 NSUB = 1E17 GAMMA = 0.4083894

+ PHI = 0.7 VTO = -0.7140674 DELTA = 0

+ UO = 212.2319801 ETA = 9.999762E-4

+THETA = 0.2020774 KP = 6.733755E-5

+VMAX = 1.181551E5 KAPPA = 1.5 RSH = 30.0712458

+NFS = 1E12 TPG = -1 XJ = 2E-7 LD = 5.000001E-13

+WD = 1.249872E-7 CGDO = 3.09E-10 CGSO = 3.09E-10

+CGBO = 1E-10 CJ=1.419508E-3 PB=0.8152753 MJ=0.5

+ CJSW = 4.813504E-10 MJSW = 0.5)

CMOS Transistors Aspect Ratio		
Transistors	W(um)	L(um)
M1-M4	1.4	0.7
M5,M6	5.6	0.7
M7,M13-M15	14	0.7
M8	7	0.7
M9,M10	20.3	0.7
M12	29	0.7
M11,M16-M18	58.1	0.7