DEPARTMENT OF APPLIED PHYSICS

DELHI TECHNOLOGICAL UNIVERSITY, NEW DELHI

CERTIFICATE

This is to certify that Pradeep Duhan has done one year Research cum Project Work on the topic entitled **'SIMULATION OF DOUBLE GATE SOI FINFET'** under my supervision. The present research work is being submitted to Department of Applied Physics, Delhi Technological University, in partial fulfilment of the requirement for the award of the degree of Master of Technology in Nano Science and Technology. This work has not been submitted in part or full, for any other degree of Delhi Technological University or any other university.

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ABSTRACT

In the past few decades the minimum size of transistor has been downscaled according to the Moore's law. But now further downscaling of MOSFET is facing challenges like SCE(short channel effects), gate insulator tunnelling. To overcome these challenges FinFET, a type of multigate device, is the most promising device structure.

FinFET technology has the calibre to continue with the Moore's law. FinFET has started replacing conventional MOSFETs. The gate in FinFET is wrapped around a thin silicon fin for better control over the conducting channel i.e. fins. 3nm FinFET has been demonstrated in university labs.

This thesis analyses the effects of variation in fin width, fin height, oxide thickness on the various device parameters like drain current(Ion), leakage current(Ioff), threshold voltage(Vt), DIBL and subthreshold swing(S) of FinFET by using simulation tools 3D Silvaco ATLAS version5.16.3.R and Devedit version 2.6.0.R. Analysis has also been done by using high-k dielectric materials like Hafnium oxide(HfO_2), Silicon Nitride(Si_3N_4), and Aluminium oxide(Al_2O_3)for gate material instead of conventional gate material Silicon dioxide.

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Chapter 1

Introduction

1.1 CMOS Scaling and its Challenges

Scaling is the main thrust behind the advancement of CMOS technology. With the debut of MOSFET in the world of electronics, device performance and functionality enhancement both were mostly obtained by the down scaling methods made available by the industry with time. In the beginning downscaling methods worked well but now simple scaling has become more and more difficult and challenging.

As MOSFET's are scaled down much below in sub-half micron regime, the conventional bulk MOSFET starts behaving differently. It faces several challenges like higher DIBL, poor subthreshold swing(S) collectively known as Short Channel Effect(SCE)[1]. When the physical thickness of SiO_2 gate dielectric(Tox) is scaled beyond 1.2nm, quantum mechanical tunnelling current flowing from the gate into the channel becomes more dominant and significant[2]. Moreover, the gate oxide thickness has reached to its physical limit with the downscaling. With the reducing gate oxide thickness, the increase in gate leakage current has become one of the most challenging tasks for future scaling. Because of this increasing gate leakage it seems impossible to further scale down the gate oxide, also gate oxide can't be scaled beyond the inter-atomic distance. So if transistor downscaling is to be continued it requires new solutions to avoid above mentioned problems such as high-k gated dielectric materials or shallow, ultra low resistivity junctions[3] or development of innovative structures.

An innovative approach is needed to allow future reduction of channel length. The multi-gate structure is a promising candidate[4].

To overcome above limitations, several new multiple gate SOI structures have been proposed by various researchers such as Gate all around(GAA), Pi-gate MOSFET, FinFET. Double gate FinFET is one such promising candidate because of its quasiplanar structure, excellent roll-off characteristics, drive current and it is close to the conventional MOSFET in terms of layout and fabrication as it can be built using

standard bulk planar CMOS process[5,6]. Because of better gate control in FinFETs, the Short-channel effects are reduced as compared to a bulk MOSFET [7]. These devices have sharper subthreshold slopes which allow better switching in the device. FinFET can be used for both analog as well as digital applications. These are considered to be the best candidates for scaling of MOSFETs below 65 nm. FinFETs, with the physical gate length of 10 nm, have already been experimentally fabricated [8].

1.2 Silvaco ATLAS and DEVEDIT

This thesis uses DevEdit 3D version 2.6.0.R and Silvaco Atlas version 5.16.3.R to perform SOI FinFET simulation.

DevEdit is a device structure editor. It can be used to generate a new mesh on an existing structure or can be used to create or modify a device. DevEdit can be used as a simulator under DeckBuild or through a Graphical User Interface (GUI). DevEdit allows structures to be created or read into DevEdit in the form of SILVACO Standard Structure Files. ATLAS is a physically-based two and three dimensional device simulator. It predicts the electrical behaviour of specified semiconductor structures and provides insight into the internal physical mechanisms associated with device operation[9].

The DeckBuild run-time environment is used in this thesis. The DeckBuild run-time environment receives the input files. Within the input files, Silvaco Atlas is called to execute the code. And finally, TonyPlot is used to view the output or results of the simulation.

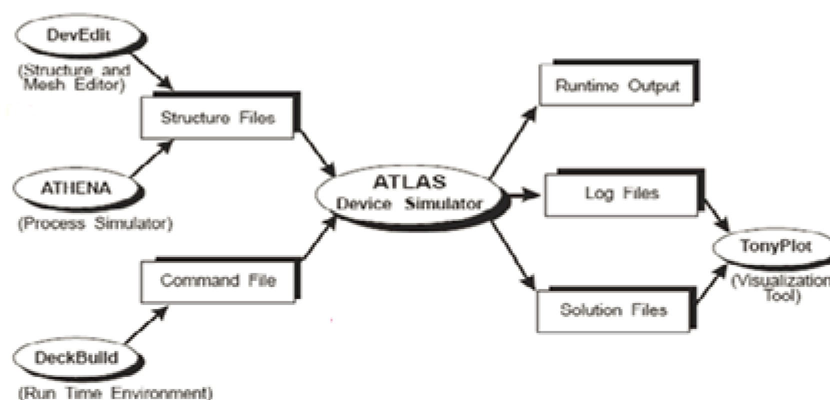


Figure 1.1 Data flow in ATLAS[9]

1.3 What is FinFET

FinFET is a non planar, double-gate transistor built on an SOI substrate, based on the earlier DELTA (single-gate) transistor design.[10] The term FinFET was coined by University of California, Berkeley researchers (Profs. Chenming Hu, Tsu-Jae King-Liu and Jeffrey Bokor). The distinguishing characteristic of the FinFET is that the conducting channel is wrapped by a thin silicon "fin", which forms the body of the device. The thickness of the fin determines the effective channel length of the device. Because of the vertically thin channel structure, it is referred to as a fin because it resembles a fish's fin; hence the name FinFET. If only side gates are effective then it is called a double gate FinFET. A gate can also be fabricated at the top of the fin, in which case it is a triple gate FinFET. Or optionally, the oxide above the fin can be made thick enough so that the gate above the fin is as good as not being present.

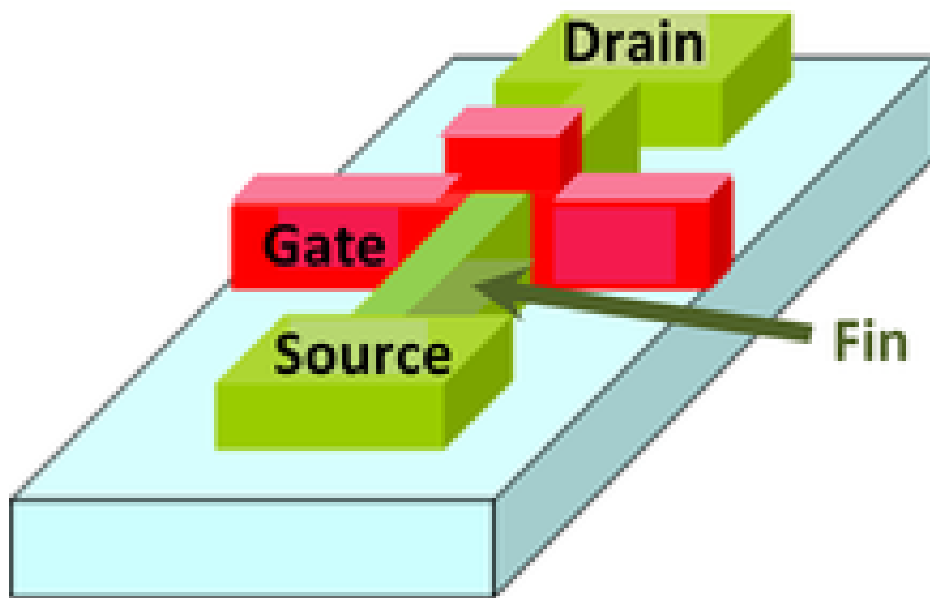


Figure 1.2 FinFET structure[10]

1.4 Research Objectives & Outline

The goal of this work is to investigate, through device simulations and a literature study, various device characteristics by varying various parameters of the SOI FinFET. The main advantage of the FinFET is that the leakage current and SCE are under control. There is also increase in the drain current. So FinFET is much better than conventional MOSFET. Because of better position of FinFET the analysis is done in

this work that how threshold voltage, leakage current and drive current are affected by varying various parameters of FinFET like fin width, fin height, oxide thickness, different oxide materials are varied and the effects are studied.

Outline

This thesis is outlined as follows:

Chapter 2 focuses on how and why downscaling was done, the adverse effects of downscaling and how these adverse effects can be handled.

Chapter 3 introduces the FinFET structure, its working, why it is better and what is the current status of FinFET.

Chapter 4 focuses on device simulation details and the various results of simulations carried out by altering various parameters of FinFET like Fin width, Fin height, oxide thickness, and different oxide materials.

Chapter 5 Finally conclusions are drawn.

Chapter 2

MOSFET Basics

The original MOSFET on a Si substrate using SiO_2 as the gate dielectric was built in 1960[11]. Although it was slower in process speed when compared with the bipolar transistor, but the advantage of this technology was a higher layout density and the fabrication process was much simpler then bipolar transistor.

The invention of the complementary MOS (CMOS) technology in 1963 was pioneering as this eased very large-scale integration (VLSI) of ICs which led to advanced memories and microprocessors. The downscaling of MOSFETs stimulated the growth of Si IC industry and information technology by constantly increasing the circuit speed, the integration level in the chip and reducing the manufacturing cost. The metal–oxide–semiconductor field-effect transistor (MOSFET) is a transistor used for amplifying or switching electronic signals. In this chapter, the basic theory of operation of the MOSFET is briefly presented, the dimensional downscaling is introduced, and the main challenges ahead are outlined. Finally, the promising advanced device structures and concepts for Si MOSFET are discussed.

2.1 Fundamentals of MOSFET

2.1.1 MOSFET STRUCTURE

A simple MOSFET is a three-terminal electronic switch. The energy barrier in the channel region is controlled by the vertical electric field of the gate electrode which adjusts the current flow from the source electrode to the drain electrode. A basic bulk n-channel MOSFET structure is shown in Figure 2.1. There are four terminals in this device: gate, source, drain, and substrate.

Normally the source and substrate terminals are grounded. The source and drain areas are heavily doped. Substrate doping is opposite of source and drain. For an n-MOSFET (i.e., n-type MOSFET), the source/drain electrodes are heavily doped with n-type, while the substrate is doped with p-type. The gate electrode is heavily doped with

n-type polycrystalline Si (poly-Si). A thin SiO_2 as the gate dielectric is placed between gate and channel. The SiO_2 is mostly fabricated by thermal oxidation process, and it works as an energy barrier between the gate electrode and the Si substrate.

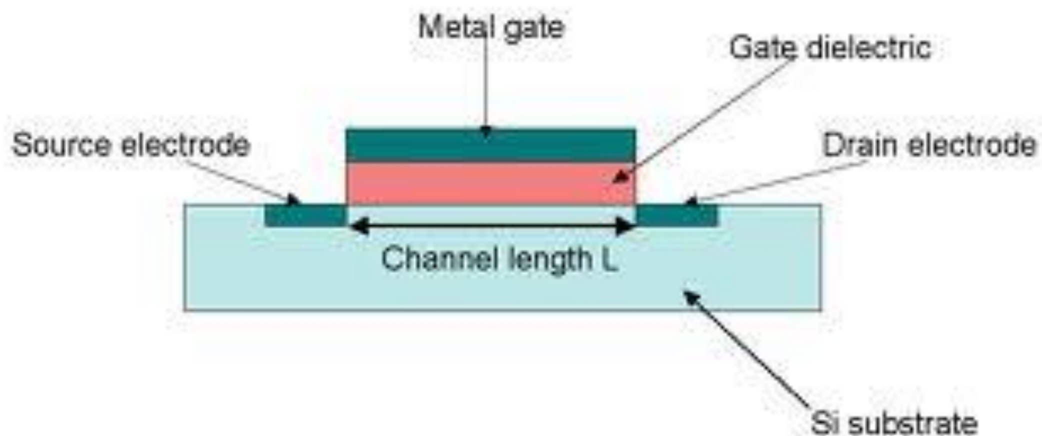


Figure 2.1 MOSFET structure [12]

2.1.2 n-channel MOSFET working

A metal–oxide–semiconductor field-effect transistor works on basis of modulation of charge concentration by the MOS capacitance between body electrode and gate electrode (which is located above the body electrode) and separated from rest of the device regions by a gate dielectric layer which is mostly an oxide, such as silicon dioxide or may some other high-k dielectric. When compared with the MOS capacitor, the MOSFET contains two more terminals (source and drain), each connected with individual highly doped regions that are separated by the body region(substrate). These regions can be either p or n type, depending on type of MOSFET but they must both be of the same type, and of opposite type to the body region. The source and drain (unlike the body) are highly doped which is denoted by a '+' sign after the type of doping.

If the MOSFET is an n-channel or n-MOSFET, then the source and drain are denoted by 'n+' regions and the body is denoted by 'p' region. If the MOSFET is a p-channel or p-MOSFET, then the source and drain are given by 'p+' regions and the body by 'n' region. The source is so called because it is the source of the charge carriers (electrons for n-channel, holes for p-channel) that passes through the channel to the drain which absorbs these charge carriers. For gate voltages less than the threshold

voltage, the channel is having very few charge carriers, and only a very small subthreshold leakage current can pass between the source and the drain.

When a negative gate-source voltage (positive source-gate) is applied, it creates a p-channel at and near the surface of the n region, compared to the n-channel case, but with opposite polarities of charges and voltages. When a voltage less negative than the threshold value (a negative voltage for p-channel) is applied between gate and source, the channel is vanished and only a very small subthreshold current can flow between the source and the drain.

The device may also have a Silicon On Insulator (SOI) structure in which a buried oxide (BOX) is formed under a thin semiconductor layer. If the channel region between the gate dielectric and BOX region is very thin, then this very thin channel region is referred to as an ultrathin channel (UTC) region with the source and drain sections formed on either side in and/or above the thin semiconductor layer. Another structure, the device may have is a semiconductor on insulator (SOI) structure in which silicon is not used but other semiconductors are used. When the source and drain regions are formed above the channel in part of fully, then they are called as elevated or raised source/drain (RSD) regions.

2.2 MOORE's LAW

Moore's law predicts about computing hardware scaling. It states that the quantity of transistors on integrated circuits(IC) doubles approximately every two years. This law is named after Intel co-founder Gordon E. Moore, who gave this law in his 1965 paper. The paper tells that the number of components in integrated circuits had doubled every year after the discovery of the integrated circuit in 1958 to 1965. On basis of this he predicted that this trend would continue "for at least ten years".

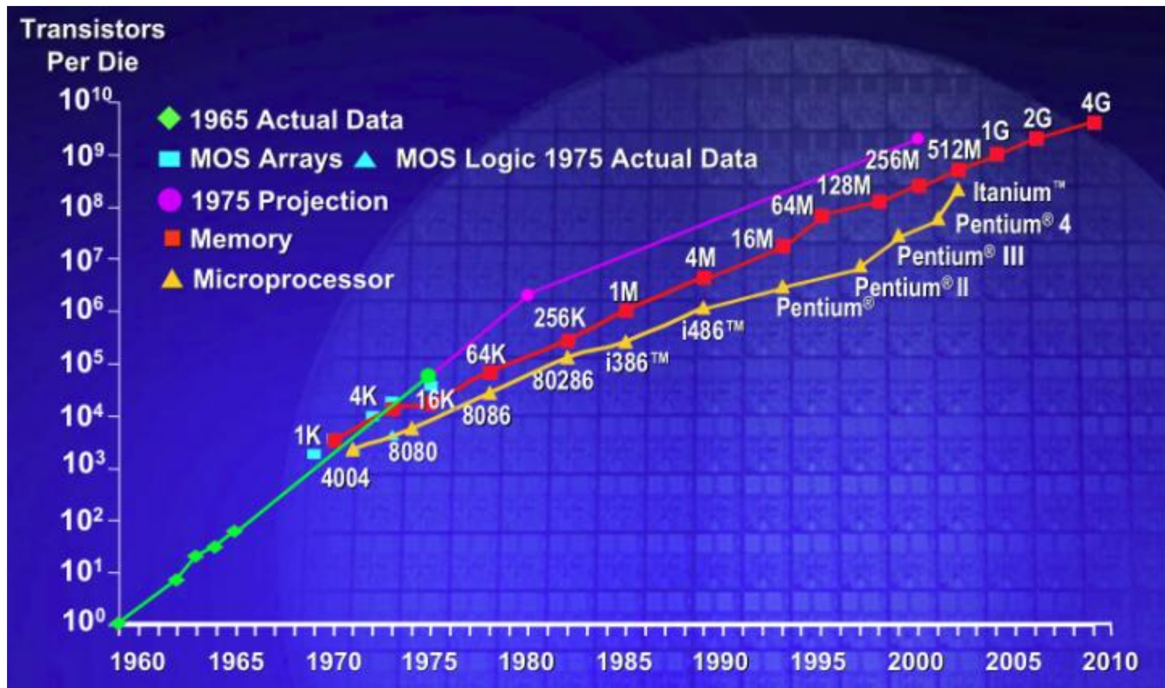


Figure 2.2 Number of transistors on a chip, as a function of the year of production[13]

The prediction by Moore has proved to be accurate, in part because the law is now used by the semiconductor industry to conduct long-term planning and to set targets for research and development.

Many features of almost all digital electronic devices are robustly correlated to Moore's law. These features are processing speed, memory capacity, sensors and even the number and size of pixels in digital cameras. All of these are improving almost at exponential rates as well. This exponential improvement has improved the impact of digital electronics in almost every section of the world economy. Moore's law describes the driving force of social and technological changes in the late 20th and early 21st century.

2.3 Downscaling- Why needed

Computing power has increased dramatically over the past few decades, because of the major advancements in silicon integrated circuit (IC) technology led by the continuous miniaturization in the size of MOS transistor. The fast progress in the semiconductor industry has been driven by improved circuit working and performance together with side by side reduction in the manufacturing costs. With the invent of the

MOS transistor its dimensions have been shrinking 30% for every 3 years, following Moore's law and scaling has in fact increased speedily.[14]

The main reason to make transistors smaller is to pack more and more devices in a specified chip area. This results in a chip with the same functionality in a smaller area, or chips with more functionality in the same area. Since fabrication costs for a semiconductor wafer are comparatively fixed, the cost per integrated circuits is mainly related to the number of chips that can be formed per wafer. As smaller ICs allow more chips per wafer, therefore there is a reduction in the price per chip. Reduction of the physical MOS device dimensions has improved both circuit speed and density in the following ways:

a) Circuit operational frequency increases with a reduction in gate length(Lg), allowing for faster circuits.
b) Chip area decreases therefore enabling higher transistor density and cheaper ICs.
c) Switching power density is almost constant; this allows lesser power per function or additional circuits at the same power.
d) Per transistor cost decreases

The classic scaling rule is called "constant-field scaling". It was planned by Dennard et al. in 1974 [15]. As the name implies this method was based on keeping a constant electric field throughout the channel length of the MOSFET by means of scaling down voltages and device dimensions by a definite factor k and conversely up scaling doping concentrations (Na,Nd) by that same factor. This allowed the power consumed per area (power density) to remain constant while the circuit delay went down by factor k. As a result, the circuit speeds up by the same factor k, and the power dissipation per circuit is decreased by factor of k^2.

Basically scaling can be made in two ways: constant voltage scaling and constant field scaling. In constant voltage scaling only lateral dimensions of the MOSFET are scaled i.e. gate length and gate width which may lead to dielectric breakdown. Constant voltage scaling is a simply geometrical route. To remove this drawback constant field scaling is done. In this lateral dimensions (gate length, gate width), perpendicular dimensions (oxide thickness), and voltages are scaled along with the doping levels.

2.3.1 Gate length scaling

Gate length scaling is directly related to the MOSFET scaling. Smaller gate length yields higher currents that result in consequently higher speed circuits. Smaller gate lengths are made possible by the advanced lithographic capability and this enhancement allows operation at lower voltages. At the same time higher packaging density is also achieved, due to the ability to pattern finer structures.

2.3.2 Gate oxide scaling

Higher drive current is achieved by scaling gate oxide to produce a higher gate capacitance so that extra inversion is induced at the same gate bias. Stronger capacitive coupling allows the gate to have superior control of the potential in the channel region and thus reducing short channel effects and maintaining good subthreshold turn-off slope. Gate oxide scaling is not restricted by manufacturing control. At very low dimensions of gate length, quantum mechanical(QM) tunnelling takes place leading to a gate leakage current. This leakage current increase exponentially with the reduction in oxide thickness and this in turn increases the chip standby power.

2.3.3 Voltage scaling

Main challenges for power voltage scaling (i.e. applied drain bias) have been the non-scaling character of threshold voltage. In scaling the MOSFET, the supply voltage has to be scaled along with the physical dimensions of the transistor to maintain a constant electric field across the source and drain called “constant field scaling”. The power supply voltage is usually reduced to minimize power dissipation and because of reliability reasons.

To maintain acceptable on-state performance, the device threshold voltage must also be scaled so that it can accommodate the reduced power supply. As threshold voltage is reduced, Ioff will be increased because the channel potential barrier height is reduced. So threshold voltage scaling is a limiting issue in transistor gate scaling.

2.4 Outcome of downscaling-SCE

A MOSFET device is considered to be short when the channel length is of the same magnitude as the depletion-layer widths of the source and drain junction. As the channel length L is reduced to boost both the operation speed and the quantity of components per chip, the Short Channel Effects arise. With the Short Channel Effects many important device characteristics are related, so it affects a lot.

2.4.1 Subthreshold Leakage

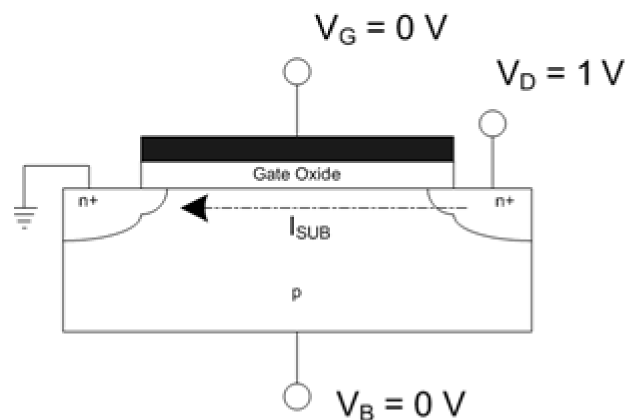


Figure 2.3 Subthreshold leakage in an nFET [16]

Subthreshold conduction or subthreshold leakage or subthreshold drain current is the current that flows between the source and drain of a MOSFET when the transistor is in subthreshold region, or weak-inversion region i.e., for gate-to-source voltages below the threshold voltage(Vgs<VT). Ideally this state is considered as the off-state but practically it is not. In digital circuits, subthreshold conduction is usually assumed as a parasitic leakage state that would ideally have no current. The subthreshold region is often referred to as the weak inversion region. This weak inversion region is the main component of the MOSFET off-state current, Ioff. Ioff is the Id(drain current) measured at Vgs=0 and Vds=Vdd. It is important to keep Ioff as low as possible to minimize the static power that a circuit consumes when it is in the standby mode.

Subthreshold conduction is only one contributor of leakage current, other contributors are gate-oxide leakage and junction leakage. In beginning, subthreshold conduction in transistors was very small, but with downscaling of transistors, leakage

from all sources increased their contribution. For a technology with threshold voltage of 0.2 V, leakage can exceed 50% of total power consumption.

The reason for the increasing importance of subthreshold conduction is that the supply voltage has continually scaled down, to reduce the dynamic power consumption of integrated circuits (the power that is consumed when the transistor is switching from an on-state to an off-state, which depends on the square of the supply voltage), and to carry on electric fields inside small devices low, to maintain device reliability. The value of subthreshold conduction is set by the threshold voltage, which sits between ground and the supply voltage, and therefore has to be reduced with the supply voltage. This reduction means less gate voltage swing below threshold to turn the device off, and as subthreshold conduction varies exponentially with gate voltage, it becomes more and more important as MOSFETs shrink in size.

At Vgs below Vt, the inversion electron concentration is small but it allow allow a small leakage current to flow between the source and the drain. For a given W and L, there are two ways to reduce leakage current. The first is to have a large Vt but this solution is not very good because a large Vt reduces Ion and which in turn increases the gate delays. The other good way is to reduce the subthreshold swing(S). S can be decreased by reducing oxide thickness(Tox). But again there is a loop in this as Tox is reduced gate leakage increases.[17]

2.4.2 Vt roll off

The threshold voltage of a long channel device is not affected by the channel length and the drain voltage. But when channel length size is reduced becomes shorter and shorter, the threshold voltage shows a greater reliance on the channel length and the drain voltage.

This dependence of the Vt is due to the loss of control by the gate of the depletion region underneath it. The gate voltage only controls a fraction of the depletion layer. Vt is lower for transistor with shorter gate length(Lg). This Vt roll-off is typically measured in mV/nm.

For digital applications, the Vt roll-off is the most undesirable SCE. One must ensure that Vt does not become too low for the minimum Lg devices on a chip. The

SCE is more prominent at higher drain bias. Vt drops with decreasing Lg. When Vt drops too much, Ioff becomes too large and that channel length is not tolerable.

The occurrence of Vt roll off can be understood as follows. In a short-channel device, the source drain distance is equal to the depletion width in the vertical direction in the channel region. The drain potential has a strong effect on the band bending over a significant fraction of the channel. Thus, the energy barrier which prevents carriers from flowing through under the "off" condition is deeply lowered by the drain field penetration. This causes a substantial increase of the subthreshold current, thus a reduced Vt. In a long-channel device, the source and drain are so far apart that their depletion regions have no effect on the energy barrier or the electric field pattern in most part of the channel. . Vertical dimensions in a MOSFET like oxide thickness, depletion width and junction depth must be reduced in order to support the reduction of gate length. To avoid threshold voltage roll-off, the substrate doping concentration should be chosen such that the minimum gate length is about 2-3 times Wdep.[18].

2.4.3 DIBL

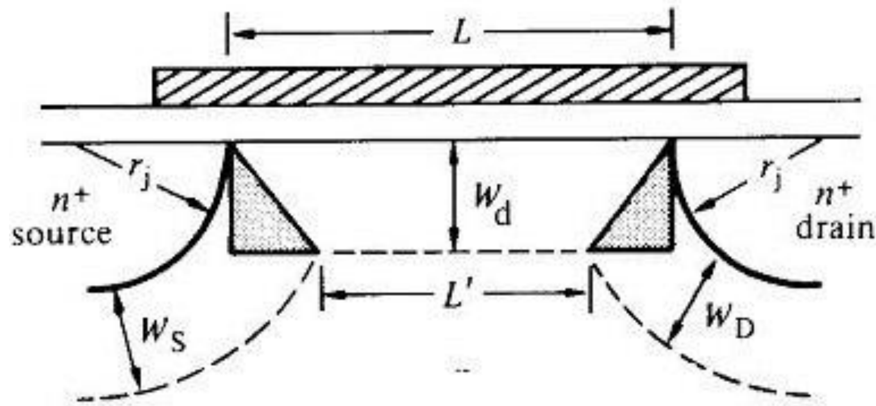


Figure 2.4 source/drain depletion region influence on the gate depletion region[19].

For a SC transistor, the depletion region of the source and drain enhance significantly resulting in reduction in Vt at higher drain bias. So threshold condition can be achieved at a lower gate bias. When the depletion regions surrounding the drain moves towards the source, the two depletion layers merge and punch through occurs. Punch through can be minimized with thinner oxides, larger substrate doping, shallower junctions, and with longer channels.

The current flow in the channel depends on creating and sustaining an inversion layer on the surface. If the gate bias voltage is not sufficient to invert the surface, the charge carriers in the channel face a potential barrier that blocks the flow. Increasing the gate voltage reduces this potential barrier and, eventually, allows the flow of carriers under the influence of the channel electric field. In small-geometry MOSFETs, the potential barrier is controlled by both the gate-to-source voltage and the drain-to-source voltage. If the drain voltage is increased, the potential barrier in the channel decreases, leading to drain-induced barrier lowering (DIBL). The reduction of the potential barrier eventually allows electron flow between the source and the drain, even if the gate-to-source voltage is lower than the threshold voltage. The channel current that flows under this conditions (i.e $V_{gs}<V_t$) is called the sub-threshold current.

In other words, the SCE gives a better depletion width with an increase in surface potential, making the channel more attractive for electrons and increasing the expected current for a given gate bias.

DIBL is therefore a measure of the short channel performance of transistor and can be measured by difference in threshold voltage between small drain bias(0.1V) and high drain bias(Vdd). It should be noted that a high DIBL or big difference between Vt does not imply poor transistor performance in a circuit operation since the transistor will not be operating at low drain bias. Rather a high DIBL indicates the presence of degraded device characteristics such as strong Vt roll-off and high Ioff.

2.5 Advantages of Multi-gate MOSFETs

As the size of MOSFET decreased, it increasingly suffered from the undesirable short-channel effect. So a alternate structure was required to control short channel effect in Mosfet, which came in the form of multigate devices. In a multigate device, the channel is surrounded by several gates on multiple surfaces. As the channel is surrounded by more than one gate and controlled electrostatically by multiple gates so there is better channel control by the gate than the conventional MOSFETs. The main advantage of the multi-gate devices is the improved short channel effects.

The second advantage of the multi-gate devices is the improved on-state drive current (Ion) and therefore faster circuit speed. Reduction of channel doping reduces

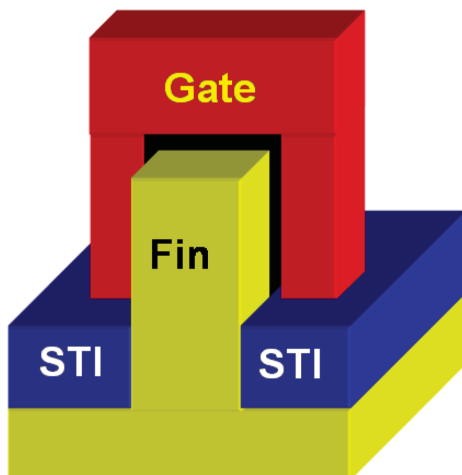
impurity Coulombic scattering. Reduced channel doping reduces the electric field normal to the SiO_2 interface and therefore reduces the surface roughness scattering.

The third advantage is the reduced manufacturing variation.

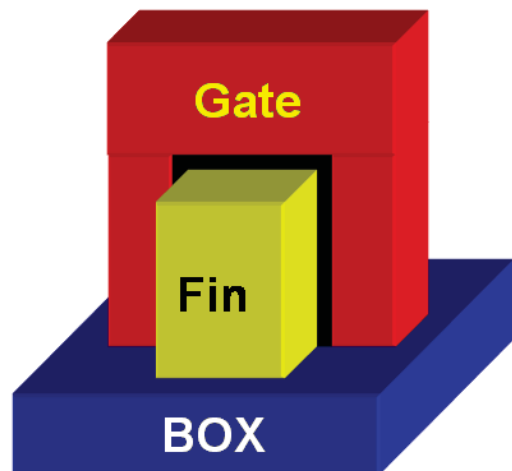
The fourth advantage is the more effective suppression of "off-state" leakage current which in turn leads to lower power consumption and improved device standby time.

Another advantage is that this technology is more compact than conventional planar transistors, improving transistor density which results to smaller overall microelectronics.

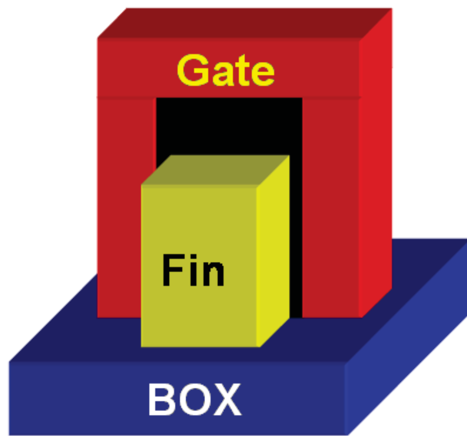
There are different types of multi-gate MOSFETs. Several examples are shown in Fig. 1. FinFETs (a type of Multigate device) can be made on either bulk or SOI substrates, forming bulk FinFET (Fig. 1(a)) or SOI FinFETs (Fig. 1(b)). (Fig. 1(c)). In double-gate FinFETs the top surface of the fin does not conduct current, whereas in triple-gate FinFETs (Figs. 1(a), (b)) the side surfaces and the top surface all conduct current. Another example of multi-gate MOSFET is the all-around gate device (Fig. 1(d)). It consists of a pillar-like body delimited by the gate dielectric and the gate. The nanowire MOSFET is one example of all-around gate devices.



(a) Triple-gate FinFET on Bulk Si

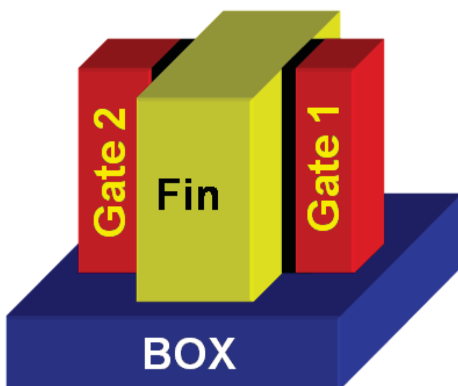


(b) Triple-gate FinFET on SOI



(c)Double-gate FinFET on SOI

(d) All-around Gate



(e) Independent Double-gate FinFET on SOI

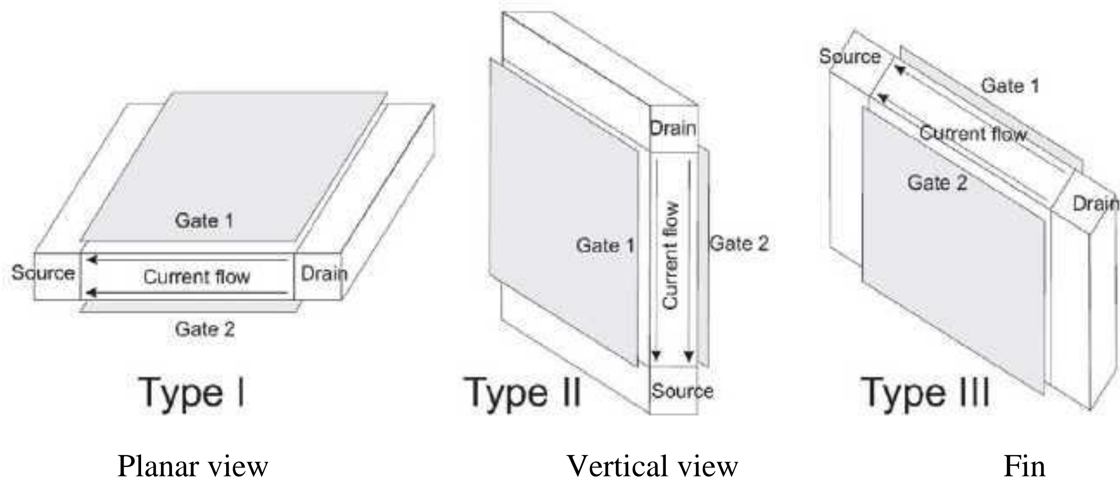
(f) Planar Double-gate SOI

Figure 2.5 Various Multi gate FETs(SOI-Semiconductor on insulator, BOX-Buried Oxide[20]

2.6 DG-MOSFET (Multi Gate Devices)

Double gate MOSFET (DG-FET) is a MOSFET that has two gates to control the channel. Its main advantage is improved gate-channel control. Because of its greater tolerance to SCE and with greater gate-channel control, the physical gate thickness can be increased (compared to planar MOSFET). Thus it also effectively controls the gate leakage current.

A DG-FET can be designed in three ways [21], labelled Types 1, 2 and 3 as shown in Fig. 3. Types 1 and 2 suffer mostly from fabrication problems, as it is hard to fabricate both gates of the same size and that too exactly aligned to each other. Also, it



Planar view Vertical view Fin

Figure 2.6: Three possible realizations of DGFETs[21]

is hard to align the source/drain regions exactly to the gate edges. More, in Type 1 DG-FETs, it is hard to provide a low-resistance, area-efficient contact at the bottom gate, as it is buried.

But the type 3 can be implemented easily and is in better position than the first two types. This type 3 led the way for double gate MOSFETs or multi-Gate MOSFETs. These type 3 structures are called FinFET.

Chapter 3

FinFET

The term FinFET was given by researchers of University of California, Berkeley(Profs. Chenming Hu, Tsu-Jae King-Liu and Jeffrey Bokor) to describe a nonplanar, double-gate transistor built on an SOI substrate, based on the earlier DELTA (single-gate) transistor design.[22] The distinguishing characteristic of the FinFET is that the conducting channel is wrapped by a thin silicon "fin", which forms the body of the device. The effective channel length of the device is depended on the thickness of the fin (measured in the direction from source to drain). It is an attractive successor of the single gate MOSFET because of its superior electrostatic properties and ease of manufacturability as compared to conventional MOSFETs.

3.1 Structure of FinFET

A Fully Depleted Lean Channel Transistor (DELTA) topology was introduced by D.Histamo in 1989. This DELTA topology was further developed for getting a better gate control. The shown DELTA structure is the predecessor of FinFET.[22]

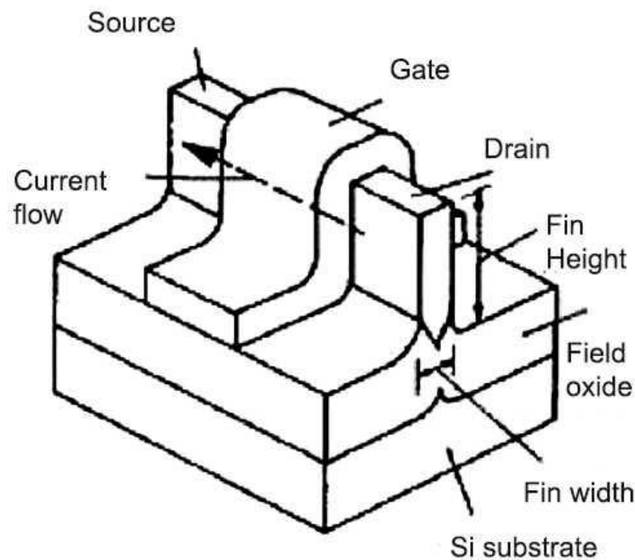


Figure 3.1: The DELTA structure[22]

The general FinFET structure is shown in Fig. 3.2. It is called so because of the thin channel region (body) stands vertically like the ‘fin’ of a fish between the source and drain regions. In the basic structure of the FinFET, the source, drain and fin are on a buried oxide layer(BOX). The fin is covered by dielectric material and this dielectric material is in turn covered by normally a polysilicon gate.

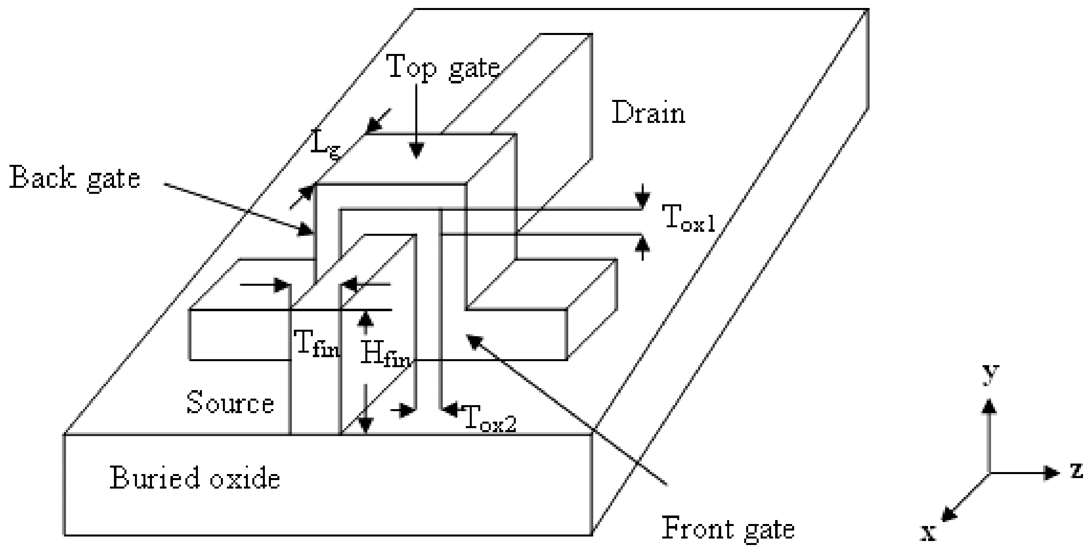


Figure 3.2 The FinFET structure[23]

The geometrical parameters of the FinFET are listed below:

(i) Gate length (*L*g): The physical gate length of FinFETs, or the printed gate length.
(ii) Fin height (*H*fin): The height of silicon fin, defined by the distance between
the top gate and buried oxide layer (BOX).
(iii) Fin Width (*T*fin): The thickness of silicon fin, defined between the front and back gates. Tfin is also referred as Tsi or Wfin.
(iv) Top gate thickness (*T*ox1): The thickness of the top gate oxide.
(v) Front or back gate thickness (*T*ox2): The thickness of the front or back gate
oxide.

3.2 Working of FinFET

In a FinFET the body or the fin is wrapped around by the gate in two/three sides, thus leading to higher gate-channel control and therefore reduced Short Channel

Effects. In strong inversion, conduction predominantly occurs close to the sidewalls, whereas in sub-threshold it occurs along the fin center (i.e. midway between the sidewalls). Even though current conduction is in the plane of the wafer, it is not strictly a planar device. It is rather referred to as a quasi-planar device, because its geometry in the vertical direction (viz. the fin height) also affects the behaviour of the device.

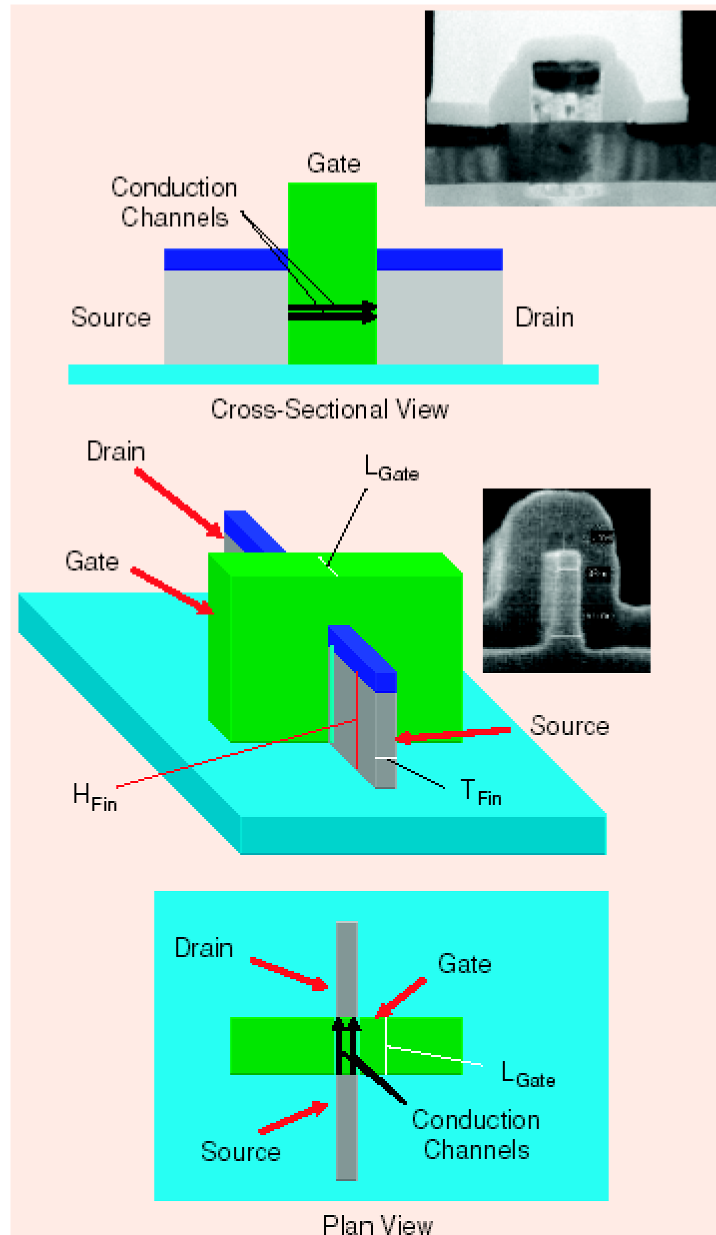


Figure 3.3 FinFET conduction path[24]

In a FinFET, the gate length L is the same as that in a conventional planar FET, whereas the device width W is quite different. W is defined as:

$$W = 2H_{fin} + T_{fin}$$

The above definition of device width is for a triple gate FinFET. If the gate above the fin is absent/ineffective, then the T_{fin} term in the above definition is taken out.

3.3 Fabrication of FinFET

The starting substrate for a FinFET is a SOI wafer with a buried oxide (BOX) thickness around 15-20 nm. The thickness of the silicon fin is about 8 nm, and the silicon is of lightly doped p-type with the dopant concentration of 1×1015 cm^{-3} which ensures fully depleted device operation. The main steps in a FinFET fabrication process are those related to fin formation, gate stack formation, and source/drain extension formation. The FinFET fabrication can be done by two routes, either a "gate-first" route, or a "gate-last" route. Both routes have fabricate well working FinFETs down to 20 nm gate lengths. FinFETs are fabricated with fin widths that are typically less than one-half of the minimum gate lengths. E-beam lithography can be used to pattern the fins directly; but in this technique cost of equipment used is very high and manufacturing output is low, therefore this route is not much preferred. Hence fin patterning needs to use creative techniques in order to pattern such very small dimensions, like resist-defined fin (RDF) patterning and spacer-defined fin (SDF) patterning. These are two main techniques for fin definition which are discussed below.

Resist-defined fin (RDF) patterning

A schematic flow of the RDF process is illustrated in figure 3.4.

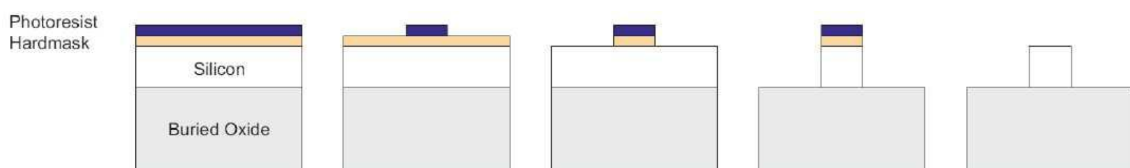


Figure 3.4 process flow for RDF Technology[25]

- First a thick hardmask is deposited on the silicon.
- Then there is deposition of positive photoresist and exposure using lithography to define the active areas.
- Unexposed areas of the photoresist are removed, which exposes the hardmask below, which is then etched using a HF-based etch process.
- Later trimming of the resist or hardmask stack is done to reduce the thickness down to the desired sublithographic dimension.
- Once again an aggressive, directional etch is done, this time etching into the silicon film, while the resist or hardmask combination serves to protect those areas that will eventually form the fins. This etch is continued till all the unprotected silicon has been etched away.
- Finally the hardmask on top of the silicon is also removed to show the fin areas.

The spacer-defined fin (SDF) patterning

A schematic of the SDF process is shown in Figure 3.5.

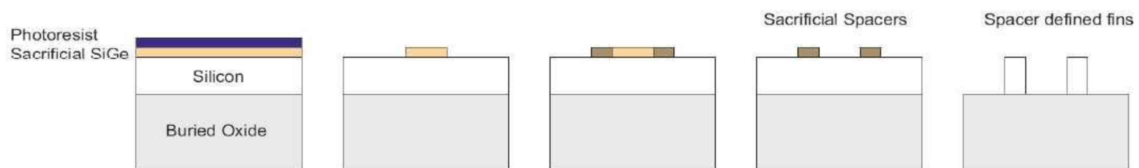


Figure 3.5 Process flow for SDF Technology[25]

- First a sacrificial SiGe film is deposited on top of the silicon film and patterned in a way that the width of the sacrificial SiGe will define the final fin-to-fin spacing.
- Then a thin nitride spacer along with the sidewalls of the SiGe is formed.
- After that SiGe film is removed, leaving behind the nitride spacers, which works as a hardmask during the subsequent etch of the silicon film.
- The thickness of the spacer turns into the resulting width of the fins.
- Depending on the process control and the desired fin widths, this process of sidewall spacer formation and etching can even be carried out one more time to result in even smaller fin widths.

- After fin width definition hydrogen annealing step takes place, to relax the stresses and defects at the surface which may have resulted due to aggressive etch chemistries employed for fin definition.

The next important section is of gate stack formation. There are two options: the "gate-first" approach and the "gate-last" approach.

- The gate-first approach:
    - First the gate dielectric is formed,
    - Then gate electrode is deposited on top.
    - Later the resist is deposited on top of this, and the stack having the gate dielectric, gate electrode, and the resist is patterned and subsequently trimmed to achieve the desired gate length.
    - Later the resist is removed.
- The gate-last approach:
    - In this source/drain is formed immediately after fin patterning.
    - Doped polysilicon or polycrystalline SiGe is deposited on the fin
    - Followed by a patterning which defines the source/drain extension regions.
    - Spacer is grown on the insides of this region, and is followed by gate stack deposition and patterning.

Using the SDF process high fin patterning densities can be obtained. The fin width is fixed in this technology, and it is not possible to use it for variable fin widths, since arbitrary fin widths are not supported in this technology.[25]

3.4 Current status of FinFET

Intel became the first company to adopt FinFET at 22 nm in 2011. The company is making its microprocessor using this new 3-D transistor.

Figure 3.6 shows a scanning electronic microscope (SEM) image of FinFET made using the new 22-nanometer manufacturing process by Intel. At a magnification of more than 100,000 times, the silicon fins are clearly visible as a series of walls projected above a flat surface.

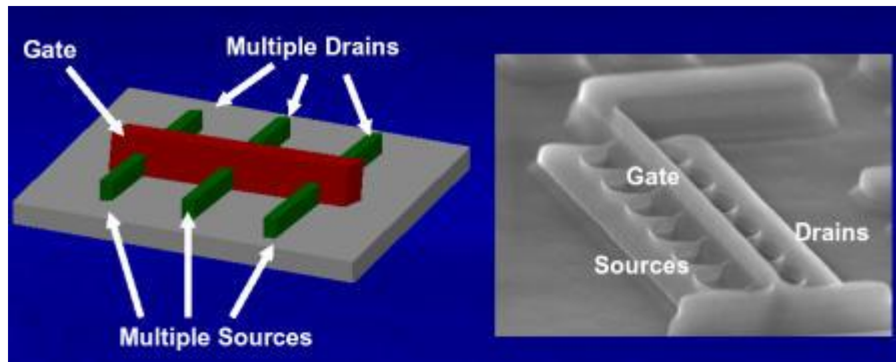


Figure 3.6 Schematic view (L) and SEM view (R) of Intel tri-gate transistors

In April 2012 Intel's Ivy Bridge processors were launched which uses 22nm process technology with Intel's tri-gate FinFET. This processor incorporated 1.4 billion transistors on a die size of 160 mm2. In this chip, at transistor level, each could produce upto 37 percent larger higher performance, while using 50 percent less power at the same performance.[26]

5nm FinFET has been demonstrated in industry fabrication and 3nm FinFET has been demonstrated in university lab.[27]

Chapter 4

Simulation

Device Simulations can give physical insight for explaining the effects observed through measurements. The simulations for this work are performed using a set of Silvaco tools, namely the Atlas Device simulator and DevEdit Device Structure Editor. The versions are 2.6.0.R for DevEdit 3D and 5.16.3.R. for Atlas 3D. Simulations are performed to know the effects of variation in fin width, fin height, oxide thickness and different materials for oxide in FinFETs. Interface effects, stress effects and quantum confinement were not taken into account.

To achieve accurate simulation results, the mesh should be denser in those regions of the device where the current density, electric field (depletion regions or interfaces) and charge generation are high. So the mesh is kept close to the Si-SiO_2 interface and the source and drain regions should be denser than other parts of the mesh. For device simulations the physical models used influence the electrical behaviour strongly. So the models should be chosen carefully. Because of the non-planar structure of FinFETs, 3D simulations are required to describe the full electric behaviour of the device. However, 3D simulations are time consuming.

4.1 Physical Parameters

The basic structure of the FinFET consists of a SiO_2 layer over which the silicon bar(Fin) and the source/drain are present. The fin is covered by a SiO_2 layer which again is covered by a polysilicon layer called the gate. The source and drain contacts are placed at the end of the source and drain junctions. The contacts source and drain are of aluminium. The temperature for simulation is set to 300 K.

Doping concentration in silicon bar is 1X15 cm^{-3} of p-type i.e. boron and the doping profile is uniform. Source and drain are heavily doped with 1X20 cm^{-3} of n-type i.e. phosphorus and the doping profile is gaussian for both the source and drain.

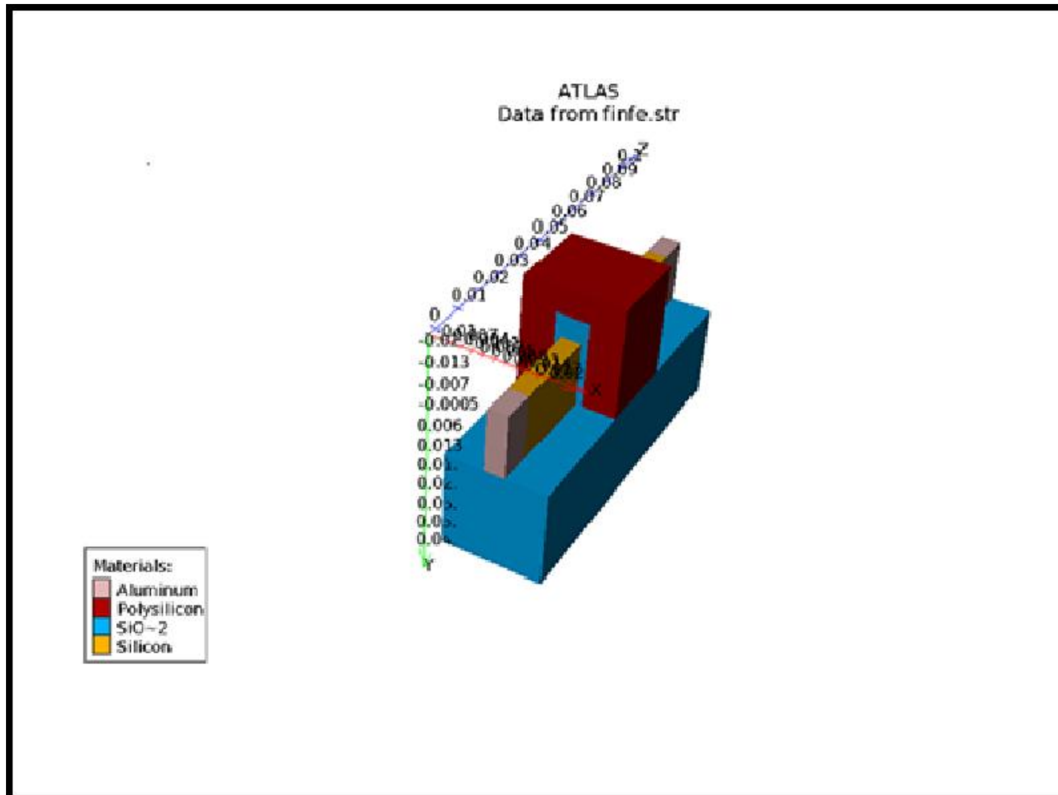
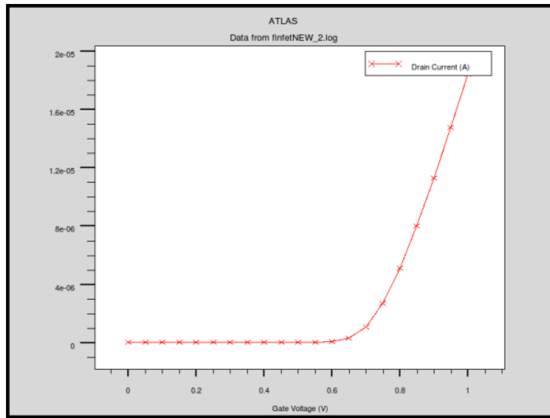


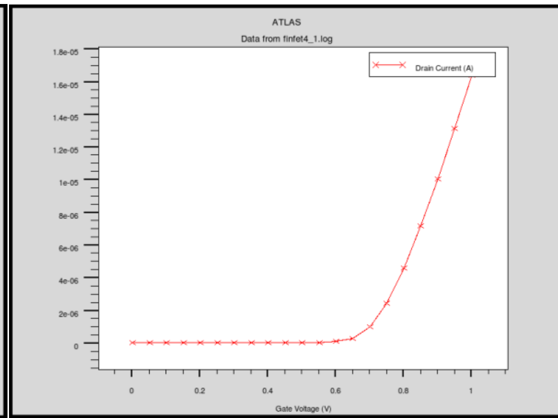
Figure 4.1 Basic FinFET structure.

The basic structure of FinFET have dimension for SiO_2 Buried Oxide Layer 100nmX30nmX30nm (LXBXH) respectively. The height of the fin is 20 nm and the breadth is 6 nm. The oxide thickness is 2 nm thick at sides and 8 nm thick at top of fin making it a double gate device. The workfunction is kept about 4.60 eV. The various models used are cvt, consrh, fermi, fldmob, bgn.

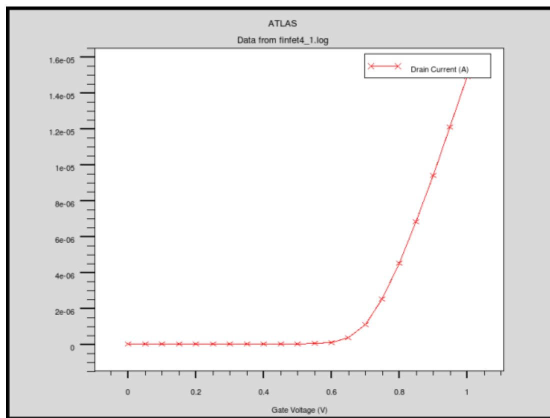
- CVT (Lombardi"s model) is good for non planar devices. The CVT model when activated will also, by default, apply the Parallel Electric Field Mobility Mode. It"s a mobility model.[28]
- Fldmob is a field dependent mobility model. It specifies transverse field degradation for electron.[28]
- CONSRH stands for Concentration dependent lifetime Shockley Read Hall. It is recommended for Si. This model is a recombination model.[28]
- Fermi model is used for carrier statistics.[28]
- BGN stands for Bandgap narrowing model. Recommended with SOI MOSFET.[28]



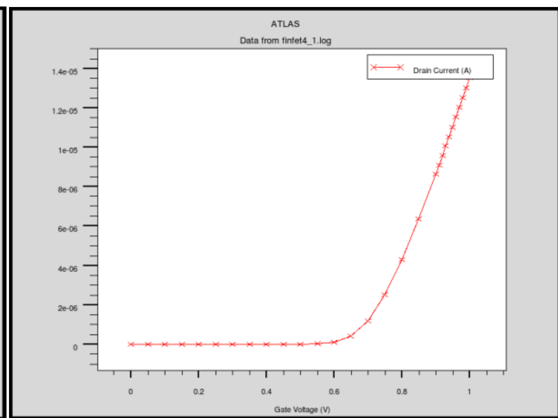
Oxide thickness 1 nm



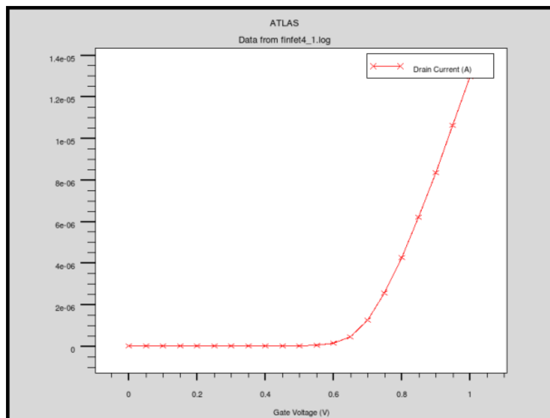
Oxide thickness 1.5 nm



Oxide thickness 2 nm



Oxide thickness 2.5 nm

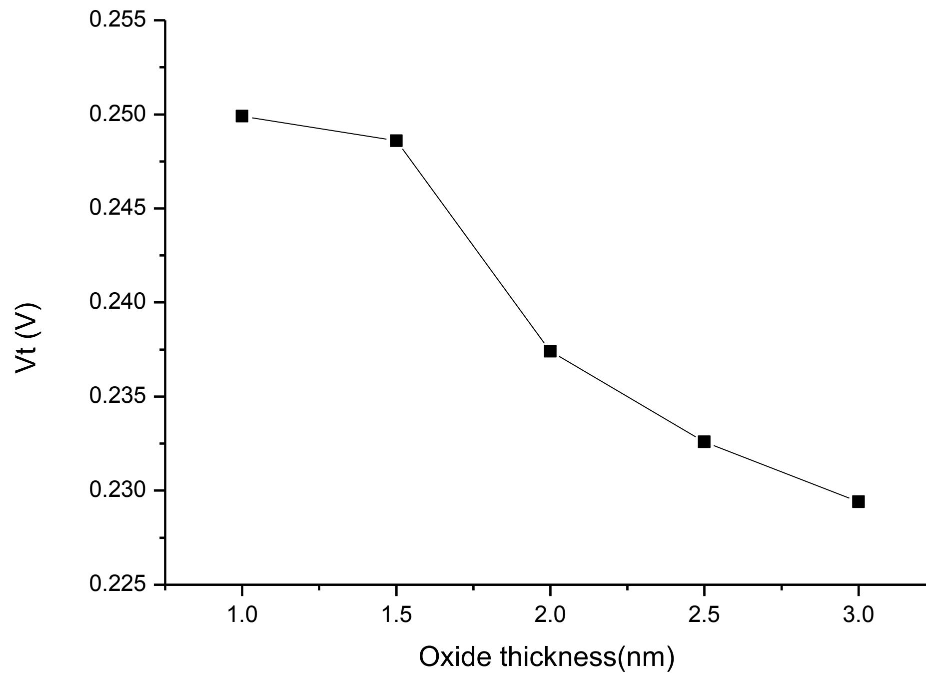


Oxide thickness 3 nm

Figure 4.2 Ion-Vgs curve for different oxide thickness

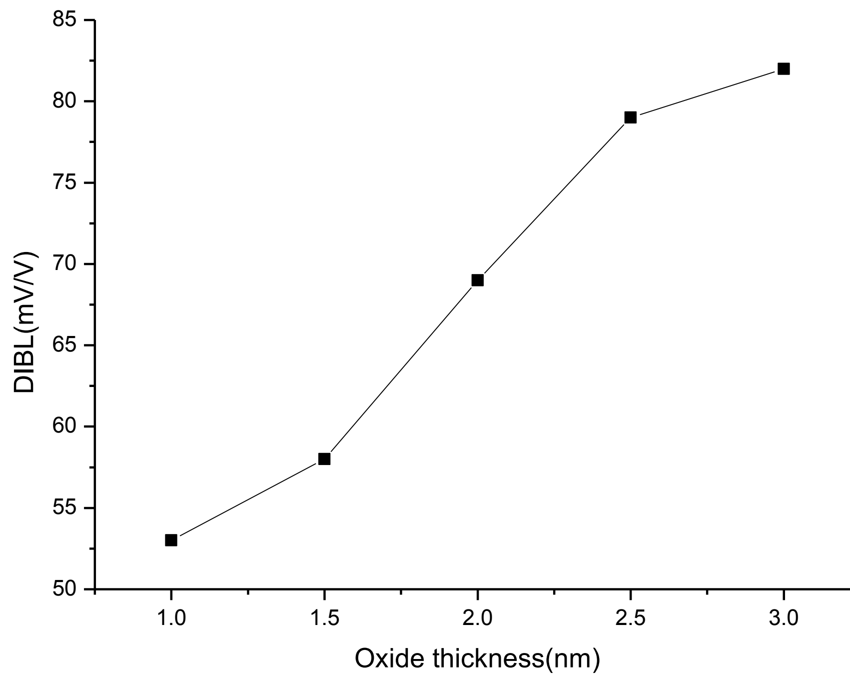
4.2 Oxide thickness variation in FinFET

4.2.1 Threshold Voltage(Vt) vs Oxide thickness



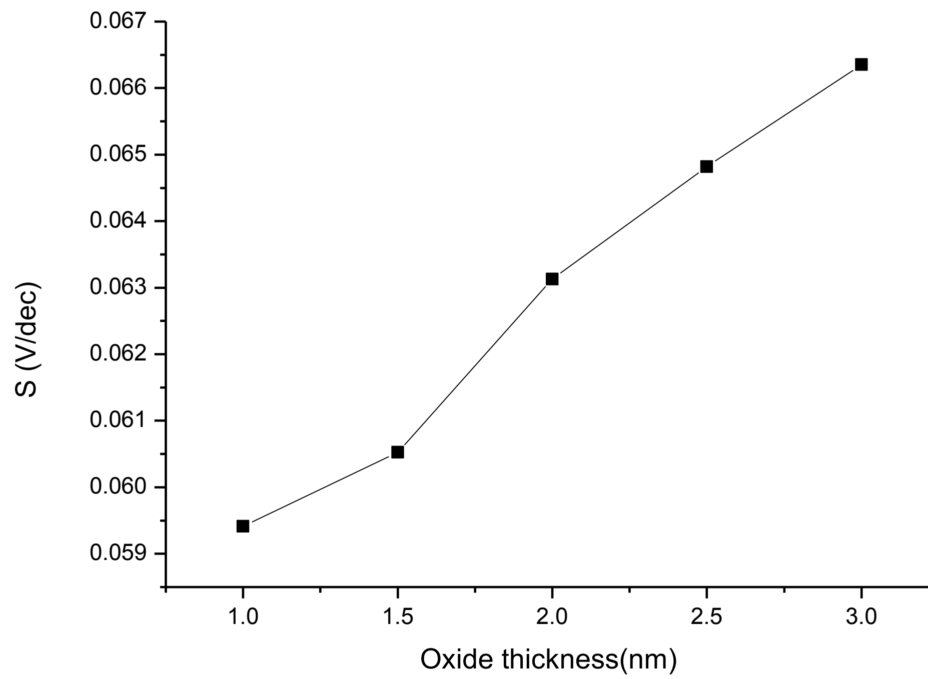
As the gate dielectric gets thinner, the gate voltage controls the channel more effectively. With the increasing oxide thickness there is a decrease in the threshold voltage[29].

4.2.2 DIBL vs Oxide thickness



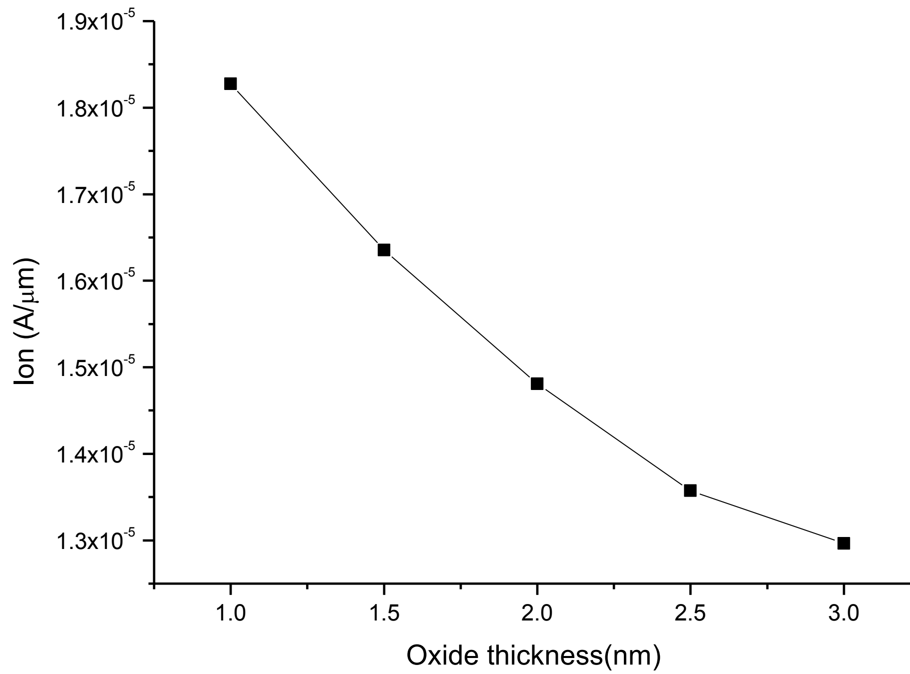
The gate voltage has a better control on channel as the oxide thickness reduces. Due to this better gate control on channel the effect of drain-induced barrier lower (DIBL) reduces.

4.2.3 Subthreshold swing(S) vs Oxide thickness



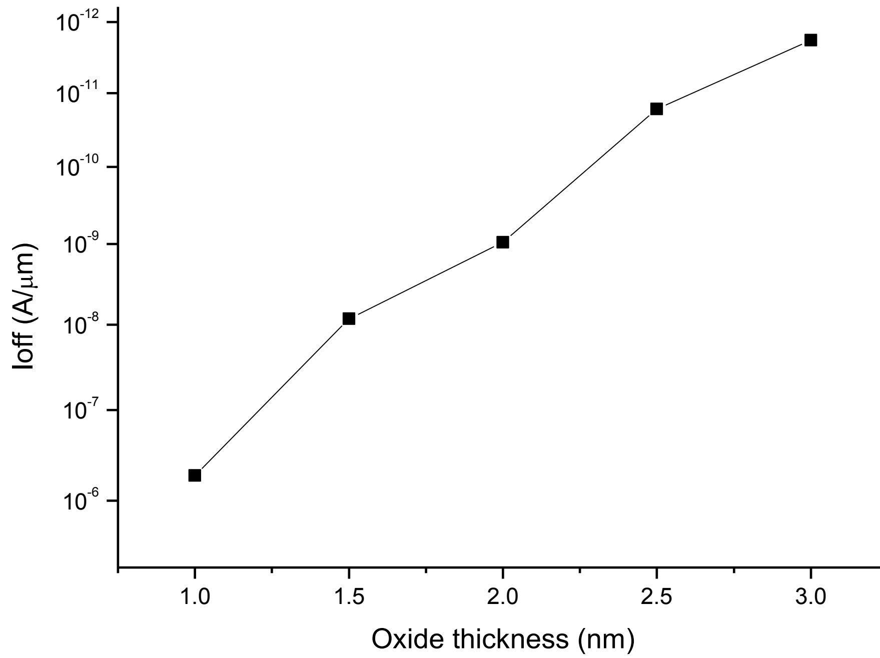
As can be observed from the above graph there is a increase in the subthreshold swing increases with the increase in the oxide thickness.

4.2.4 Drain current(Ion) vs Oxide thickness

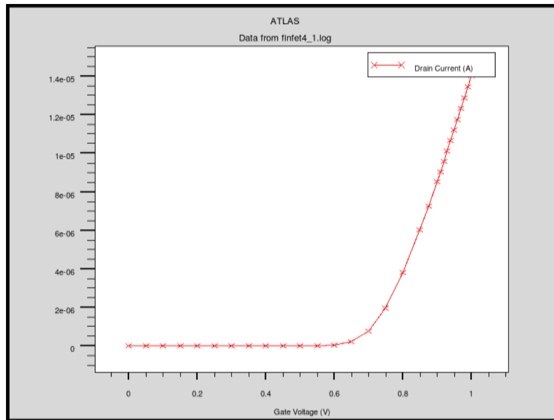


From the above figure it can be observed that Ion is affected with variation in oxide thickness. With the increase in oxide thickness the drain current(Ion) decreases.

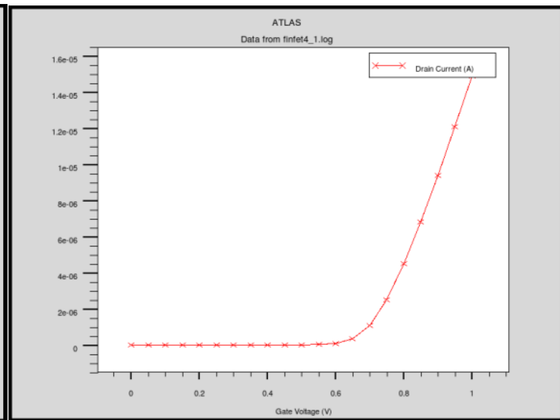
4.2.5 Leakage current(Ioff) vs Oxide thickness



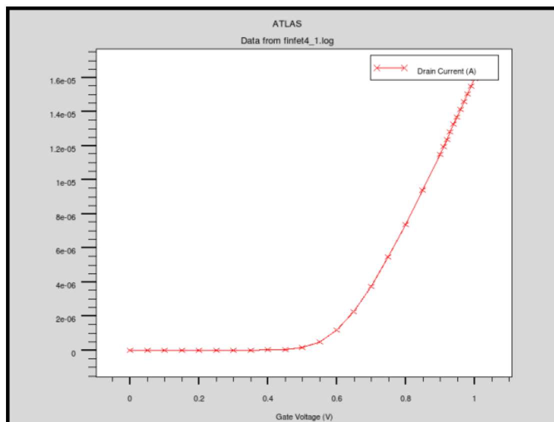
The leakage current was found to increase rapidly with decreasing oxide thickness. This is because of the dependence of the tunneling probability of charge carrier on the oxide thickness. The electric field across the SiO_2 layer increases on reducing its thickness, and as a result the tunneling probability increases.



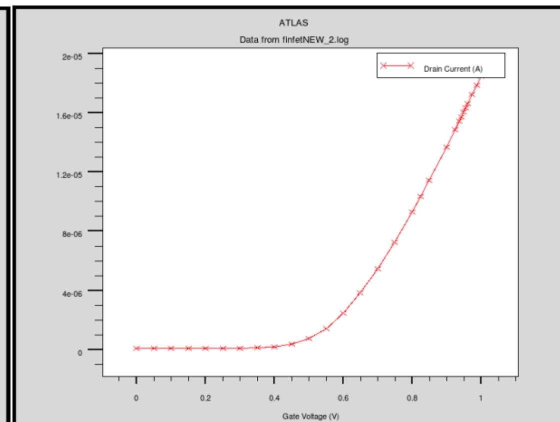
Fin width 4 nm



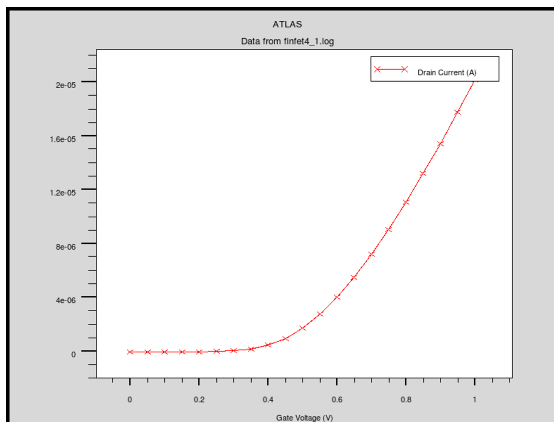
Fin width 6 nm



Fin width 8 nm



Fin width 10 nm

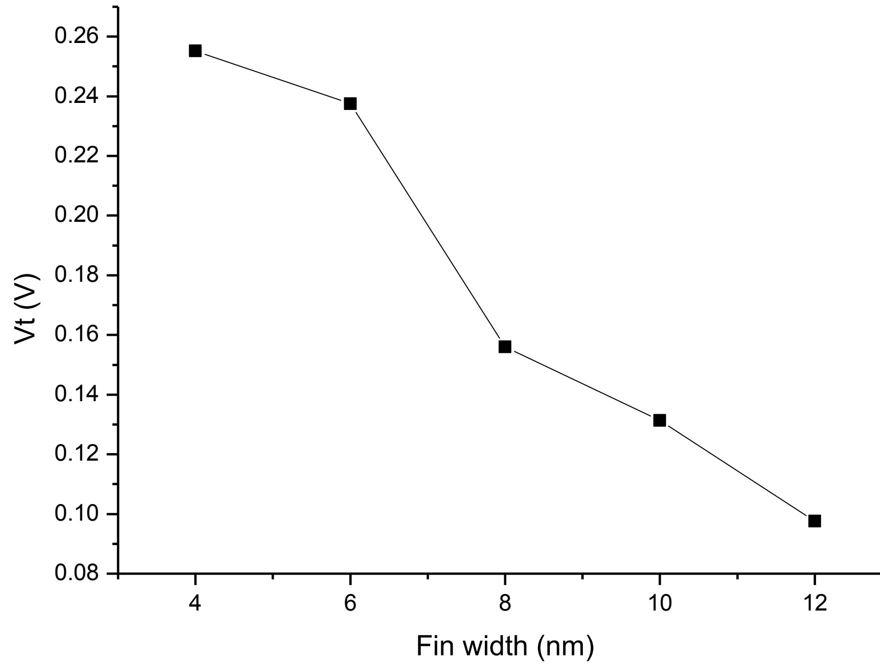


Fin width 12 nm

Figure 4.3 Ion-Vgs curve for Fin width variation

4.3 Fin Width variation

4.3.1 Threshold voltage(Vt) vs Fin width



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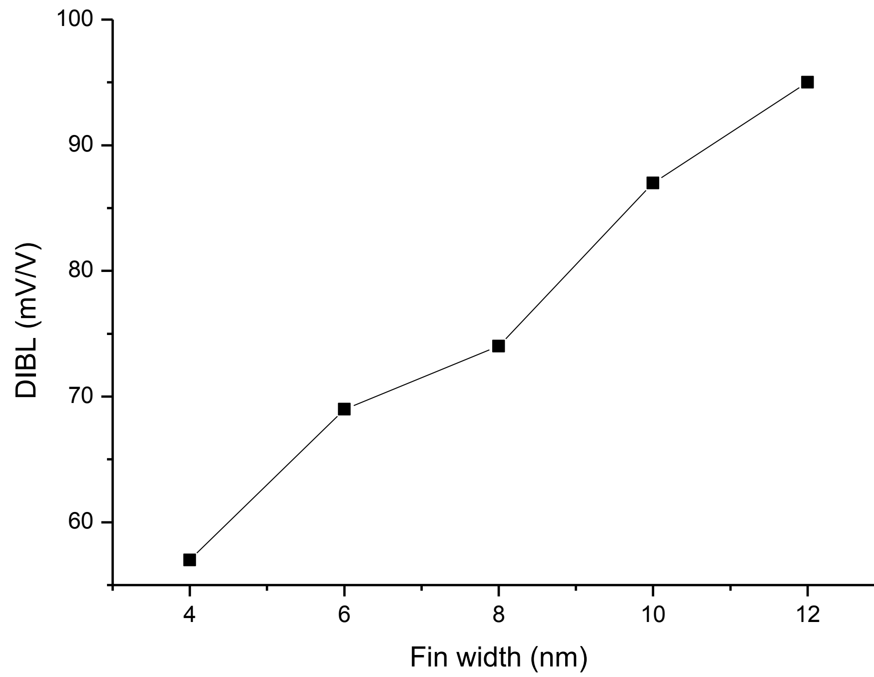
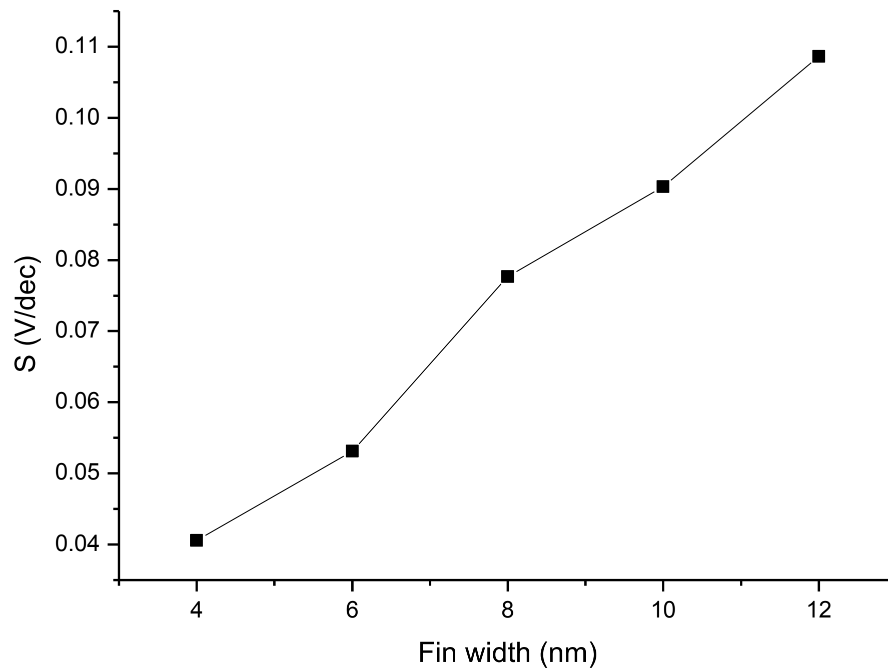
Vt increases significantly with decreasing body thickness This is because as the silicon body gets thinner, the two gates get closer and have better control over the channel, reducing short channel effect and Vt roll-off and hence the threshold voltage increases.[30]

4.3.2 DIBL vs Fin width



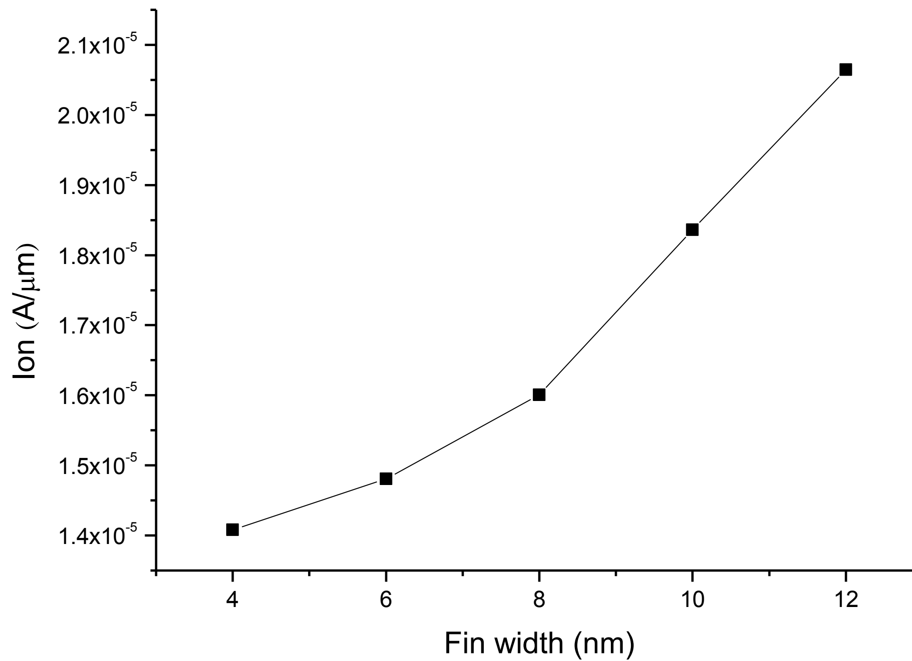
DIBL increases with increased fin-thickness because the drain electric field lowers the barrier of channel in case of thick silicon film devices because of reduced source/fin and drain/fin junction capacitances.

4.3.3 Subthreshold swing(S) vs Fin width



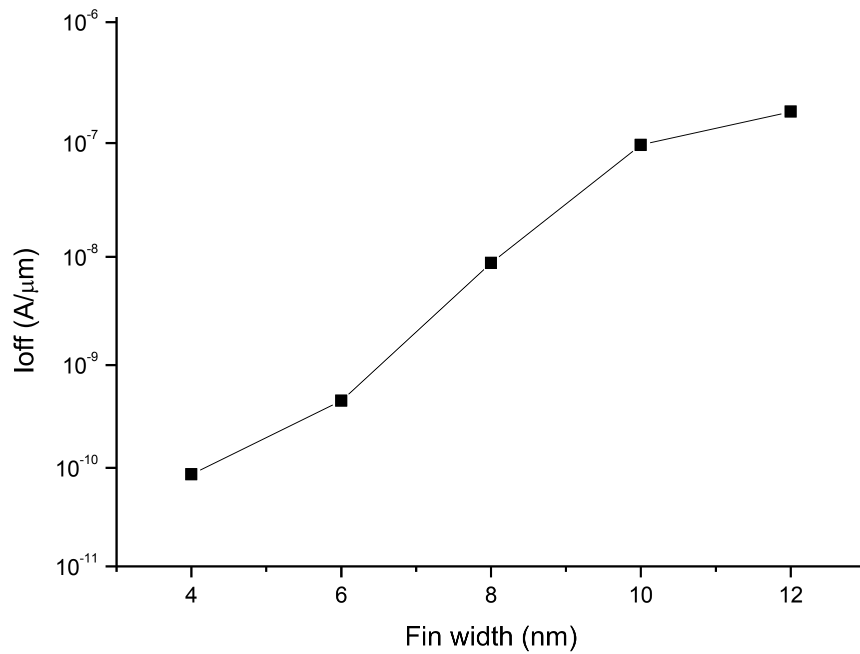
Subthreshold swing also increases with fin-thickness. The reason behind this is the gate control over channel region degrades with increased channel volume at constant drain and source proximity.

4.3.4 Drain current(Ion) vs Fin width

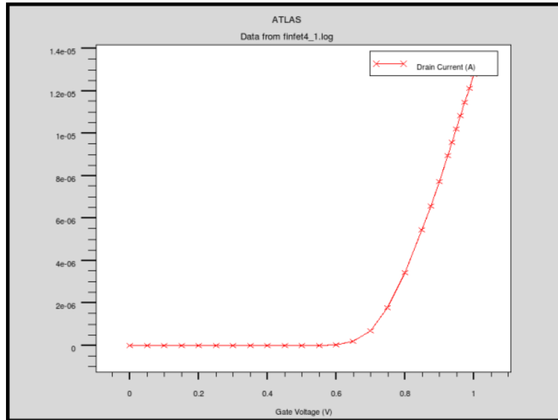


With the increase in the fin width the Ion increases. The degradation in the Ion with the decrease in fin width is because of the increase in the threshold voltage caused by quantum confinement and the effective gate capacitance decrease and the Ion also reduces due to the reduction in the number of charge carrier.

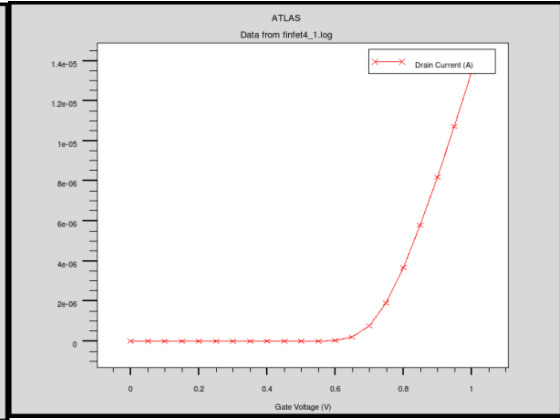
4.3.5 Leakage current(Ioff) vs Fin width



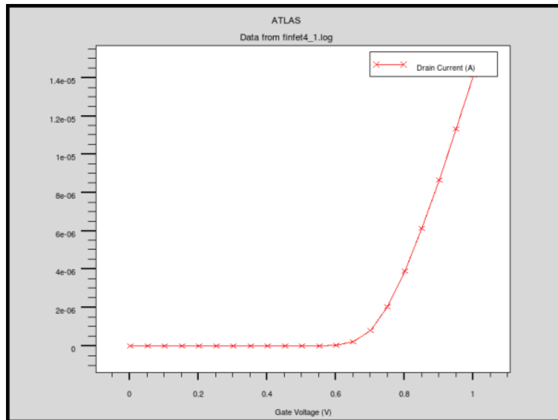
Leakage current increases with the decrease in the fin width. The change in the leakage current with the fin width is because of the change in the threshold voltage with different fin thickness.



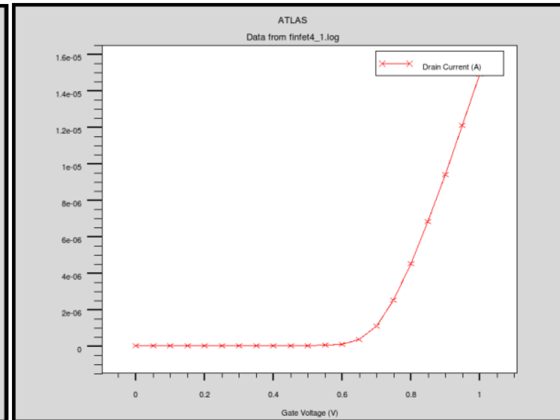
Fin height 12 nm



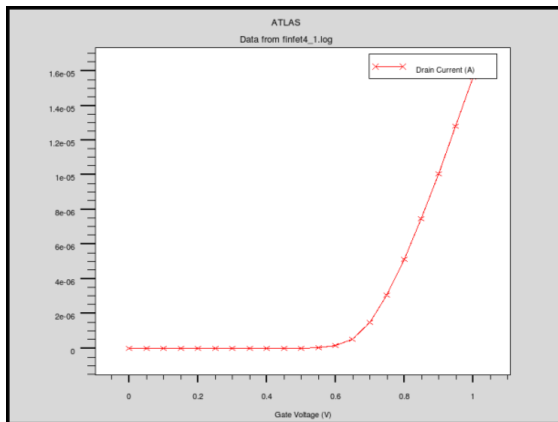
Fin height 14 nm



Fin height 16 nm



Fin height 18 nm

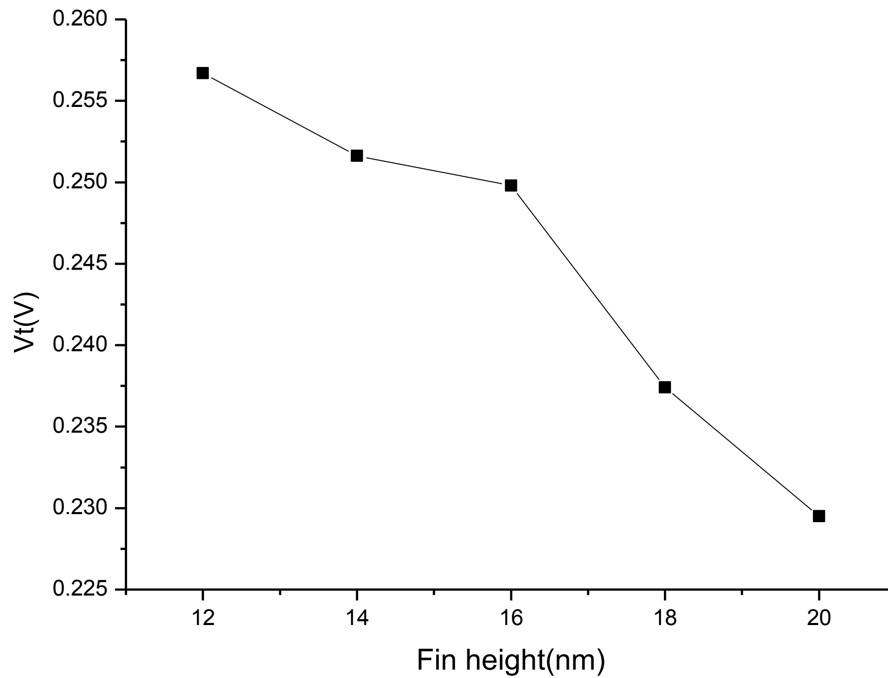


Fin height 20 nm

Figure 4.4 Ion-Vgs curve for variation in Fin height

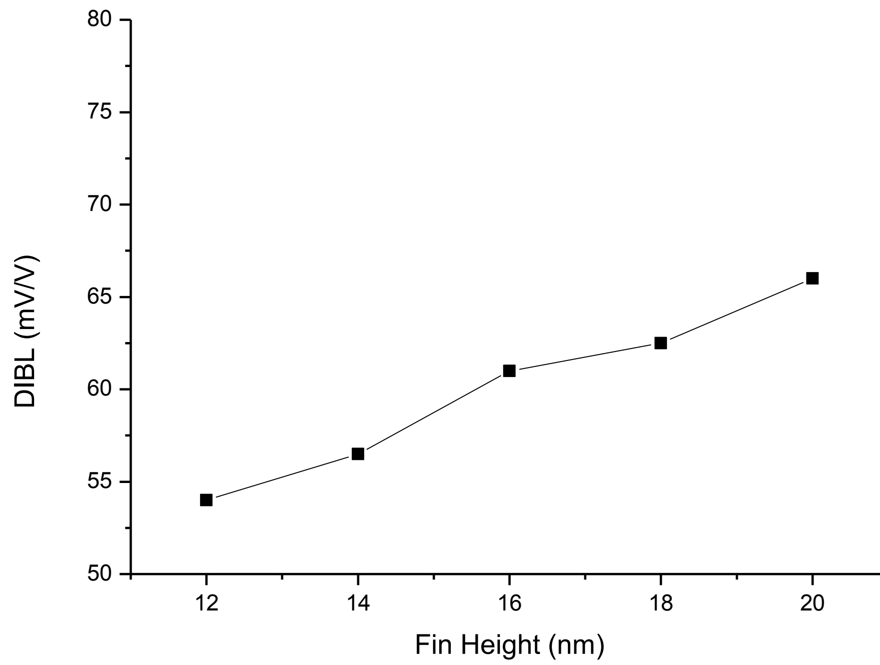
4.4 Fin height variation

4.4.1 Threshold voltage(Vt) vs Fin height



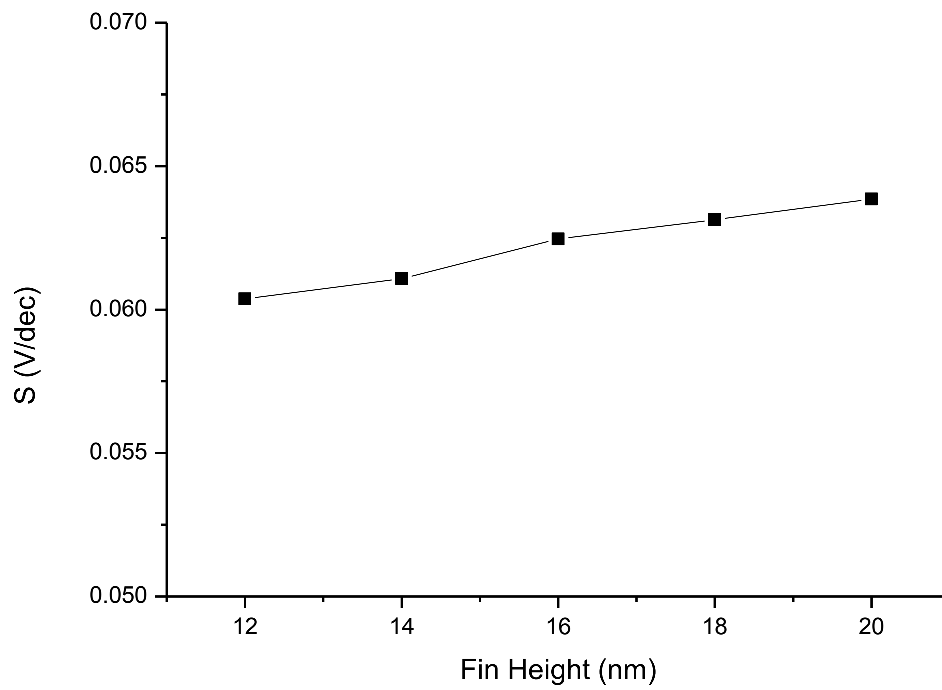
As the fin height increases, the width of the source/fin and drain/fin depletion region also increases, which decreases the source/fin and drain/fin junction capacitances, as a result the gate to surface potential coupling increases and hence the threshold voltage decreases with increased fin height[31].

4.4.2 DIBL vs Fin height



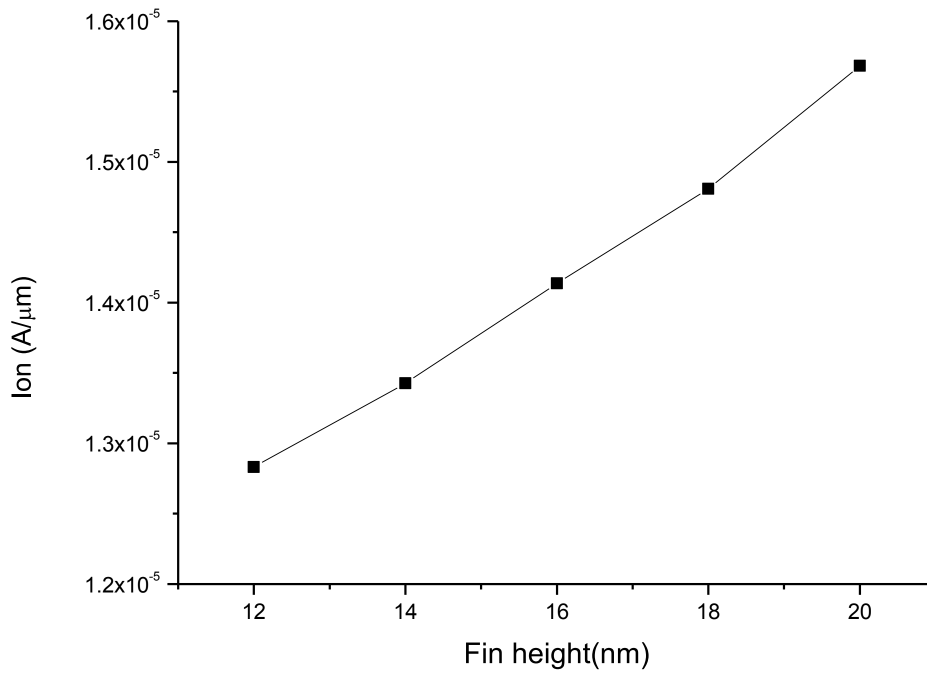
As can be observed from the above figure that DIBL increases with the increase in the fin height. The change in DIBL is not much influencing with the fin height change.

4.4.3 Subthreshold Swing(S) vs Fin height



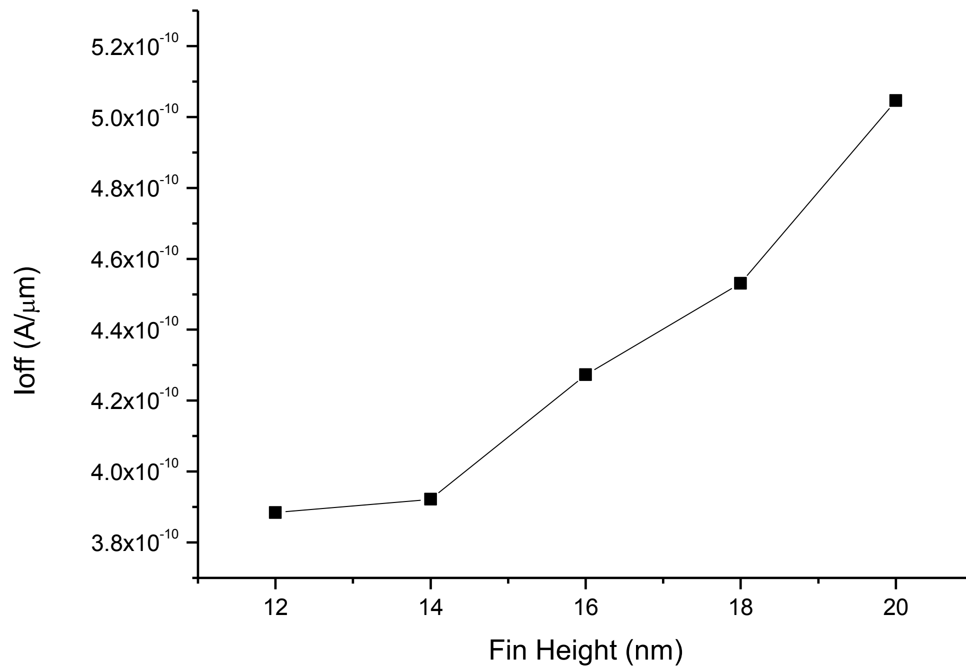
There is a minor change in the subthreshold swing with the change in the fin height. Subthreshold swing increases minutely with the increase in the fin height as the gate loses its control over the channel as fin height increases.[32]

4.4.4 Drain current(Ion) vs Fin height



The drain current increases with the increase in the fin height. One reason for decrease in the Ion with decreasing fin height is because of the reduction in number of charge carriers with decreasing fin height.

4.4.5 Leakage current(Ioff) vs Fin height



From the above graph it is observed that there is increase in the leakage current with the increase in the fin height. The leakage current increases rapidly as the fin height is increased.

4.5 FinFet simulation with high-k dielectric oxides

The term high-k dielectric refers to a material with a high dielectric constant k (as compared to silicon dioxide) used in semiconductor manufacturing processes instead of silicon dioxide. The high-k is needed to replace SiO_2 as the gate dielectric to reduce the gate leakage current. Silicon dioxide has been used as a gate oxide material for decades. As transistors have decreased in size, the thickness of the silicon dioxide gate dielectric has steadily decreased to increase the gate capacitance and thereby drive current, improving device performance. As the thickness scales below 2 nm, leakage currents due to tunnelling increase drastically, leading to high power consumption and reduced device reliability. Replacing the silicon dioxide gate dielectric with a high-k material allows increased gate capacitance and reduced gate leakage with high drive current.

As the physical thickness of SiO_2 based gate oxides reaches 2 nm, a number of fundamental problems arise. In this ultrathin regime, some key dielectric parameters degrade: gate leakage current, oxide breakdown, boron penetration from the polysilicon gate electrode [33]. So using SiO_2 based dielectrics below 1 nm becomes impractical. The solution is to replace conventional SiO_2 gate oxides with a material having higher dielectric constant. A high-k material with dielectric constant of 39 can be made ten times thicker than silicon oxide (taken dielectric constant 3.9). As the dielectric gate gets thicker the tunnelling of charge carriers through the gate reduces which helps to reduce the leakage current. High-k dielectrics materials can be used with physically thicker dimensions for the same electrical oxide thickness (EOT) thus offering significant gate leakage reduction. The effective oxide thickness of gate using high-k material can be calculated as:

$$T_{eff} = \frac{\varepsilon_2 \, high - k}{\varepsilon_1 \, SiO_2} \times t_{ox1} + t_{ox2}$$

Here ε_2 is the relative permittivity of High-k material

ε_1 is the relative permittivity of SiO_2

t_{ox1} is the oxide thickness of SiO_2

t_{ox2} is the oxide thickness of high-k dielectric

Below table shows the various parameters simulated with different dielectric materials. Normally with Al_2O_3 and HfO_2 a sacrificial SiO_2 layer is used.

Dielectric oxide (nm)	Vt (v)	DIBL (mV/V)	S (V/dec)	Ion (A/µm)	Ileak (A/µm)
Si_3N_4(2.5 nm)	0.248754	71	0.065136	2.26667e-5	4.70318e-12
Al_2O_3(2.5)/SiO_2(1)	0.273071	72.5	0.074925	3.74018e-5	6.92517e-12
HfO_2(3)/SiO_2(1)	0.351932	78	0.091472	5.38162e-5	1.49526e-13

From the simulation results it is clear that the leakage current decreases significantly with the increasing dielectric constant of the material. Threshold voltage is also increased. A high threshold voltage gives low leakage current in standby mode. DIBL shows a slight increment with the increment in gate dielectric constant.

5. Conclusion

Various parameters of FinFET i.e. oxide thickness, fin width and fin height were varied and studied. Despite the relatively thick gate oxide (2 nm) the FinFET shows very high drain current and good short-channel behaviour down to a gate length of 22 nm. This is because the FinFET structure, with its double gate and thin body, effectively suppresses DIBL and thus relaxes the gate oxide scaling requirement. This is a great advantage because oxide scaling has become one of the limiting factors in conventional MOSFET scaling, due to increasing gate leakage current.

It was seen that fin thickness reduction improves the SCEs and gate leakages at small gate lengths. But at the same time there is also decrease in drain current. Thus a compromise must be drawn between these two factors to optimise the device performance. DIBL is very sensitive for both fin width and oxide thickness variation. DIBL and Subthreshold Swing improved with thicker finwidth.

Fin height variation doesn’t affect much subthreshold swing. Threshold voltage decreases with the increase in fin height and drain current also increases with the increase in fin height.

The effects of high-k gate dielectric materials are also analyzed and found that high-k dielectric provides a considerable improvement in leakage current. The reason behind this is that the physical oxide thickness is increased by the effective oxide thickness is reduced. As the physical oxide thickness is improved therefore the tunnelling of charge carriers is reduced and this in turn reduces the gate leakage current. It also shows improvement in other device parameters and thus enhancing the overall device performance.

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