A Dissertation on

REALIZATION OF CONTINUOUS TIME FILTERS USING DDCCTA

Submitted in partial fulfillment of the requirement for the award of the degree of

MASTER OF TECHNOLOGY
(VLSI Design and Embedded System)

Submitted by :

JAYA CHAUDHARY

Roll No.: 04/VLS/2k10

Under the supervision and guidance of

Dr. NEETA PANDEY

ASSOCIATE PROFESSOR

Delhi Technological University

Department of Electronics and Communication Engineering

Delhi Technological University

(formerly DCE)

2010-2012

CERTIFICATE

This is to certify that the dissertation entitled "Realization of continuous time filters using DDCCTA" is the work of Ms. Jaya Chaudhary (Roll No.: 04/VLSI/2k10), a student of M.Tech (VLSI Design and Embedded System) in Delhi Technological University (Formerly DCE). This work is completed under my direct supervision and guidance and forms a part of Master of Technology (Electronics and Communication) course and curriculum. She has completed her work with utmost sincerity and diligence.

The work embodied in this major project has not been submitted to any other Institute/University for the award of any other degree to the best of my knowledge.

Dr. Neeta Pandey Date:_____

(Project Guide)

Associate Professor,

Department of Electronics and Communication,

Delhi Technological University (formerly DCE),

Delhi – 110042

ACKNOWLEDGEMENT

I am grateful to many people who supported and encouraged me during the work leading to this dissertation - guide, friends, and family.
First of all I would like to express my sincere gratitude to my guide, Asst.Prof. (Dr.) Neeta Pandey. She has been an excellent mentor and a constant source of knowledge, inspiration, and encouragement throughout my thesis/ M.Tech work.
I am extremely thankful to Prof. Asok Bhattacharya, former HOD of Electronics and Communication Deptt., Prof. Rajiv Kapoor, Head of Department, Electronics and Communication (ECE), Delhi Technological University, for their motivation and inspiration. I am also thankful to Mr.Rajendra Kumar, Mr. Baljeet, Mr.Pawan and all the non-teaching staff of ECE Department for providing unconditional access to resources.
I am grateful to my parents, brother and friends for their continuous support and encouragement during this work.

Jaya Chaudhary

M.Tech (VLSI Design and Embedded System)

Roll No.: 04/VLSI/2K10

Delhi Techological Univ., (formerly DCE)

Delhi – 110042

ABSTRACT

In this thesis DDCCTA has been studied and bi-quadratic filters have been realized using DDCCTA.The higher order filter may be realized using operational simulation (or leapfrog approach), topological simulation or wave active method. Both the methods has been discussed in brief here .The wave method is used for simulating reflected and incident wave for basic building block i.e. series inductor and configuring it for other passive element realization by making appropriate connection. A 4^{th} order lowpass filter has been realized using DDCCTA based wave equivalents and through operational simulation method. Its performance is evaluated through SPICE simulations using 0.25μm TSMC CMOS technology parameters. A new active building block , DDCCCTA has been proposed and port relationships are verified using SPICE simulations.

TABLE OF CONTENTS

Page no.

LIST OF FIGURES

LIST OF TABLES

Chapter 1

Introduction

Continuous time filters are well suited for high speed and low power applications as compared to switched capacitor or digital filters. In the last decade there was a great effort to integrate these filters using CMOS technology[1]. Continuous time filters offer certain advantages such as no oversampling required,less dissipation than digital filters, higher frequency capability than switched capacitor filters, no anti-aliasing filter required

There has been much effort to reduce the supply voltage of electronic circuits in last decade. This is due to the command for portable and battery-powered equipment. Since a low-voltage operating circuit becomes necessary, the current– mode technique is ideally suited for this purpose more than the voltage mode one. Consequently, there is a growing interest in synthesizing the current-mode circuits because of more their potential advantages such as larger dynamic range, higher signal bandwidth, greater linearity, simpler circuitry and lower power consumption. Many active elements able to function in current-mode such as OTA, current conveyor and current differencing buffered amplifier , have been introduced to response these demands. A number of current mode active elements such as operational transconductance amplifier (OTA) [2],current conveyors (CC)[3-5], differential voltage current conveyor (DVCC)[6], differential difference current conveyor (DDCC)[7], current feedback operational amplifier (CFOA) [8] are available in the literature. Recently some new analog building blocks, such as current conveyor transconductance amplifier (CCTA) [9,10], current controlled current conveyor transconductance amplifier (CCCCTA) [11], current controlled current difference transconductance amplifier (CCCDTA) [12], differential voltage current conveyor transconductance amplifier (DVCCTA) [13], differential voltage current

controlled conveyor transconductance amplifier (DVCCCTA) [14] and DDCCTA [15] are reported in the literature. All the good properties of CCTA, CCCCTA and DVCCTA including the possibility of inbuilt tuning of the parameters of the signal processing circuits to be implemented are included in DDCCTA and also all the versatile properties of DDCC such as easy implementation of differential and floating input circuits. In this thesis, DDCCTA has been used for implementing various filters. Also, a new block, differential difference current controlled conveyor transconductance amplifier (DDCCCTA) has been proposed.

For implementing higher order filter, there are mainly three approach- operational simulation or leapfrog approach, topological simulation or element replacement and wave active approach. In leapfrog approach , the voltage and current relationships of an LC ladder are written. From these equations corresponding Signal Flow Graph (SFG) is constructed. The number of the required equations for deriving the corresponding SFG increases correspondingly as the order of the filter increases. The resulted SFG is realized by employing lossy and loss less integrator configurations . In the topological simulation approach, the inductors of the passive prototype filters are replaced by appropriate configured active elements. An attractive approach for designing high-order filters is the wave method . According to this method, the corresponding LC ladder filter is split into two-port subnetworks which are fully described using the wave variables, defined as incident and reflected waves. An inductor in a series branch is chosen as the elementary building block, its wave equivalent includes an appropriately configured lossy integrator. The wave equivalents of the other passive elements are then derived by interchanging the terminals of the appropriate wave signals and performing signal inversion. Then each element of the passive prototype filter is substituted by its wave equivalent. The advantages of this approach are - the derived filter structures are modular and it use only lossy integrator. In this thesis the implementation of wave active filter using DDCCTA is presented.

This thesis is organised in 7 chapters.

Chapter-2 explains the operation of the DDCCTA. In chapter-3, realization of biquadratic filter using DDCCTA is explained. In Chapter-4 higher order filter is implemented using wave method.Wave equivalent of an inductor in a series branch is drawn, which is chosen to be the elementary building block. The wave equivalents of the

other reactive elements are also presented in this chapter. Chapter 5 shows the operational simulation or leapfrog approach of higher order filter. An active building block ,DDCCCTA has been proposed in Chapter 6. The thesis is concluded in chapter 7.

Chapter-2

DDCCTA

The Differential Difference Current Conveyor Transconductance Amplifier (DDCCTA) is an attractive active building block for analog signal processing. In this chapter DDCCTA has been discussed that consists of Differential Difference Current Conveyor (DDCC) and Transconductance amplifier (TA).

2.1 Differential Difference Current Conveyor (DDCC)

The differential difference current conveyor (DDCC) has the advantages of both the second-generation current conveyor (CCII) (such as large signal bandwidth, great linearity, wide dynamic range) and the differential difference amplifier (DDA) (such as high input impedance and arithmetic operation capability) [16]. This element as a building block has versatile and special properties, such as easy implementation of differential and floating input circuits, whose applications exist in the literature [17-23]. The DDCC, whose symbol is shown in Figure 2.1 is a six port building block.

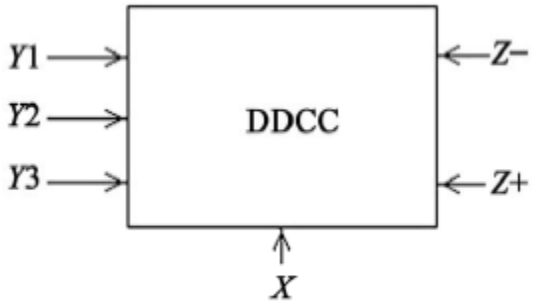


Fig. 2.1 Block diagram of DDCC

The DDCC is characterized by the following equations:

$V_X = V_{Y1} - V_{Y2} + V_{Y3}$ (2.1)

$I_{Z+} = I_X$ (2.2)

$I_{Z-} = - I_X$ (2.3)

$I_{Y1} = I_{Y2} = I_{Y3} = 0$ (2.4)

where, suffixes refer to the respective terminals.

The CMOS Differencial Difference Current Conveyor used in this work was introduced in 2004 [16]. The CMOS implementation of DDCC is shown in Figure 2.2. The input transconductance elements are realized with two differential stages (M1 and M2, M3 and M4). The high gain stage in the circuit composed of a current mirror (M7 and M8) which converts the differential current to a single ended output current. Transistors M9-M12 are used to reduce the current error due to different drain voltages of M7 and M8 between currents I_{D7} and I_{D8}. The transistors M9 and M13 provide negative feedback to make voltage V_X less dependent of the current drawn from X-terminal. The small intrinsic resistance at X terminal of DDCC, resistance R_X [16] is given as

$$R_X = \frac{(g_{d1}+g_{d4}+g_{d8})(g_{d1}+g_{d4}+g_{d8})}{g_{m4}g_{m9}g_{m13}} \quad (2.5)$$

The current through terminal X is conveyed to *Z*+ terminal by the current mirrors formed by transistors M13, M15 and M14, M16. Similarly, M17-M22 performs current inversion so as to provide Z− output [16].

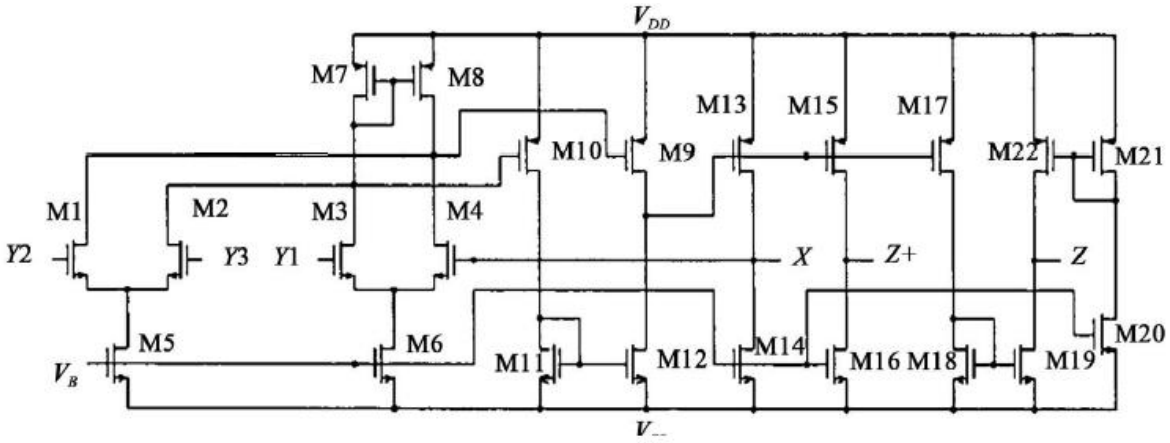


Fig. 2.2 CMOS implementation of DDCC

2.2 Transconductance Amplifier

The operational transconductance amplifier is a differential amplifier whose differential input voltage produces an output current. Thus, it is a voltage controlled current source (VCCS). The transconductance of the amplifier is proportional to the square root of bias current. This feature makes it useful for electronic control of amplifier gain. The block diagram and CMOS implementation of transconductance amplifier is shown in Fig. 2.3 and Fig. 2.4.

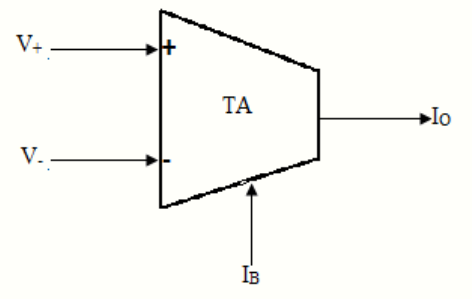


Fig. 2.3 Block diagram of Transconductance Amplifier

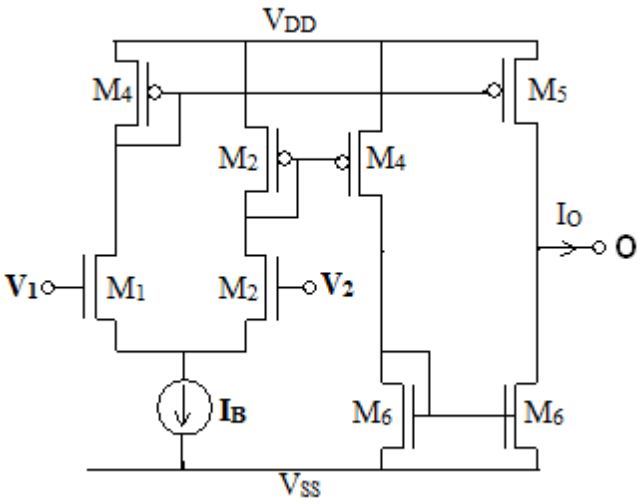


Fig. 2.4 CMOS Implementation of Transconductance Amplifier

The output current I_O may be given as

$I_O = g_m (V_1 - V_2)$ where $g_m = \sqrt{\mu_n C_{OX} I_B \left(\frac{W}{L}\right)_{1,2}}$

2.3 DDCCTA

Since DDCCTA comprises DDCC and Transconductance amplifier, so on combining the circuit diagram of Fig. 2.2 and Fig. 2.4, DDCCTA is obtained ,the block diagram and CMOS implementation of which is shown in Fig. 2.5 and Fig. 2.6

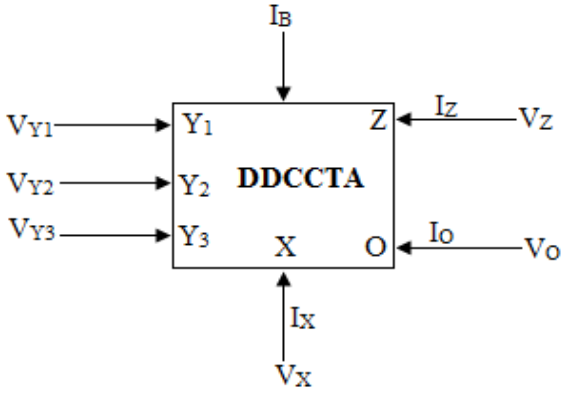


Fig. 2.5 Schematic Symbol of DDCCTA

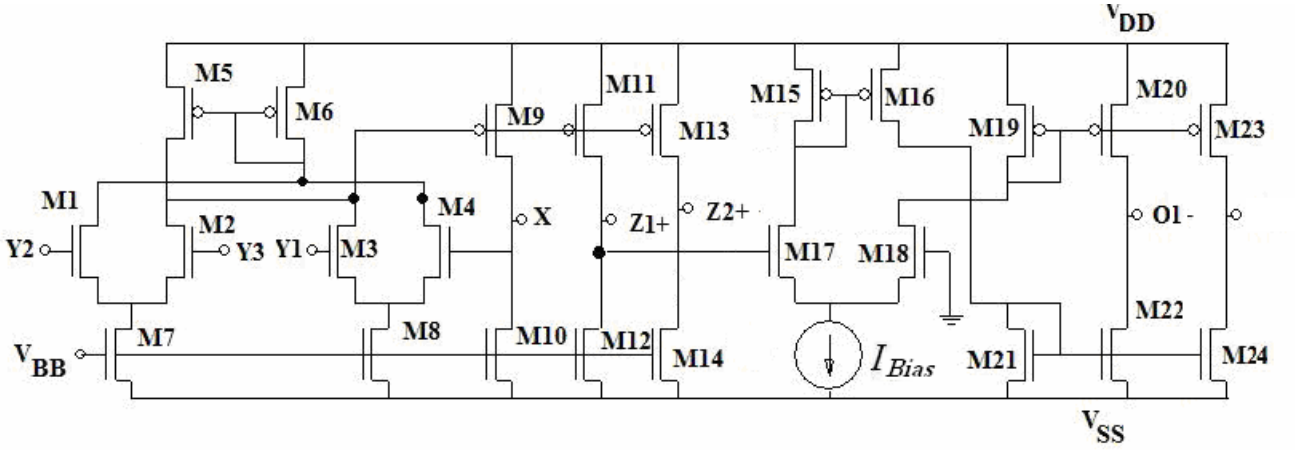


Fig. 2.6 CMOS implementation of DDCCTA.

In the Figure 2.6, the transistors from M_1 to M_{14} forms DDCC, the transistors from M_{15} to M_{24} form transconductance amplifier. The port relationships of the DDCCTA can be characterized by the following matrix :

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ V_X \\ I_Z \\ I_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & -g_m & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_X \\ V_Z \\ V_O \end{bmatrix}$$

where g_m is the transconductance from Z terminal to O terminal of the DDCCTA. The value of g_m depend on bias current I_B and may be expressed as

$$g_m = \sqrt{2\mu_n C_{ox}(W/L)_{13,14} I_B}$$

2.3.1 Simulation Result

PSPICE simulations have been carried out using TSMC 0.25μm CMOS process model parameters to validate the behaviour of the circuit. The supply voltages of VDD = -VSS = 1.25V and VBB = -0.8V are used. The DC transfer characteristics of the DDCCTA from Y1, Y2, Y3 terminals to X terminal are shown in the Figure 2.7(a) ,2.7 (b). The DC transfer characteristic for current transfer from X port to Z1+ and Z2+ ports is shown in figure 2.8 .

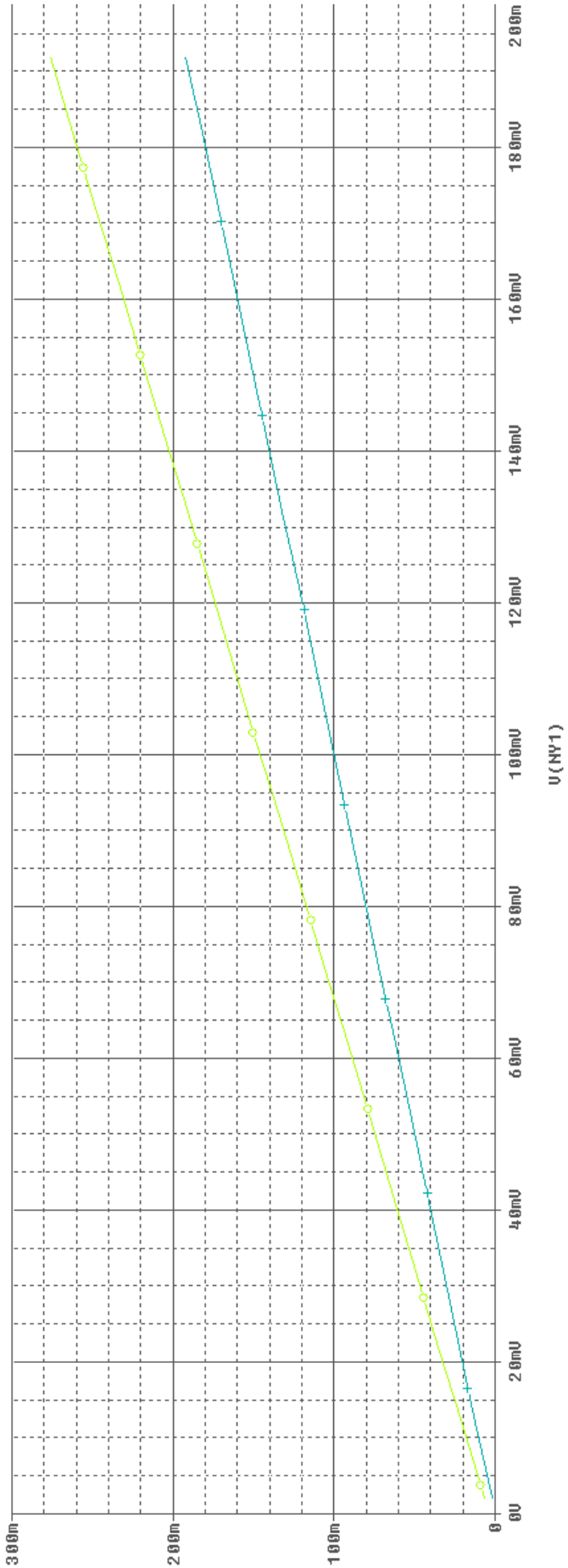


Fig. 2.7(a)DC transfer characteristic for voltage transfer from Y1 port to X port and Y2 port to X port

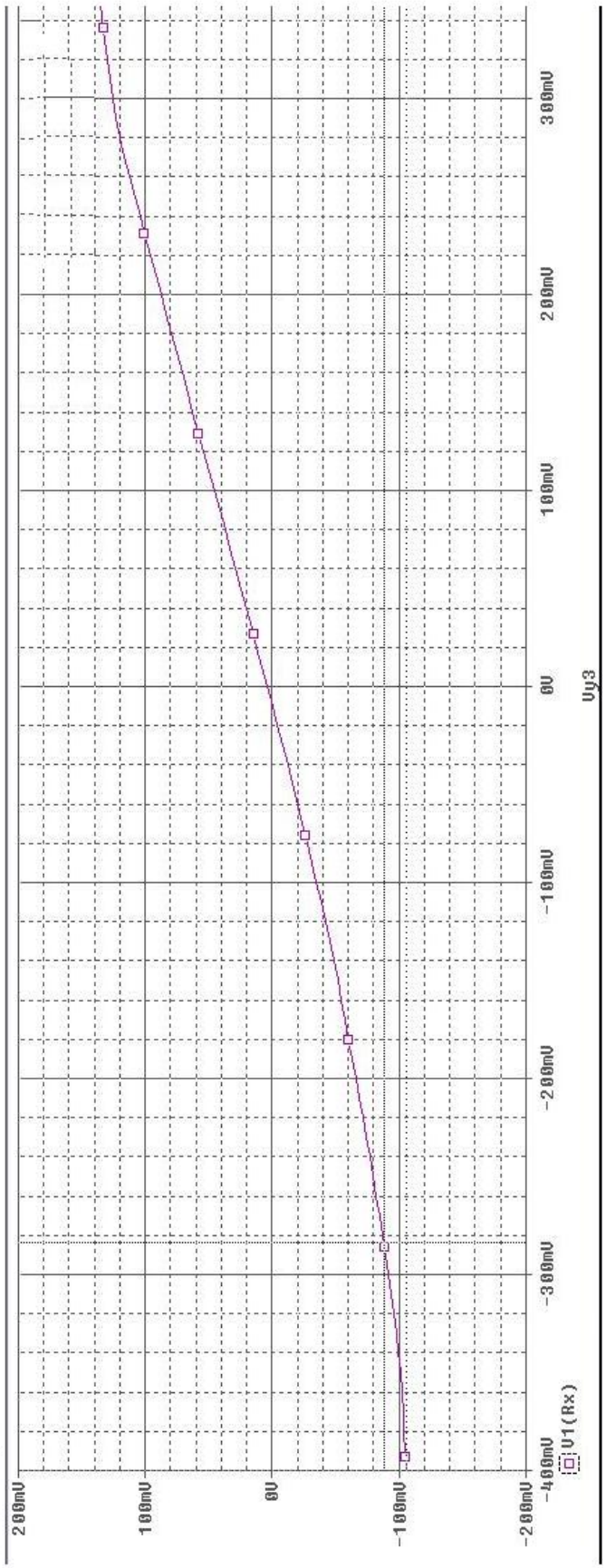


Fig. 2.7(b) DC transfer characteristic for voltage transfer from Y3 port to X port

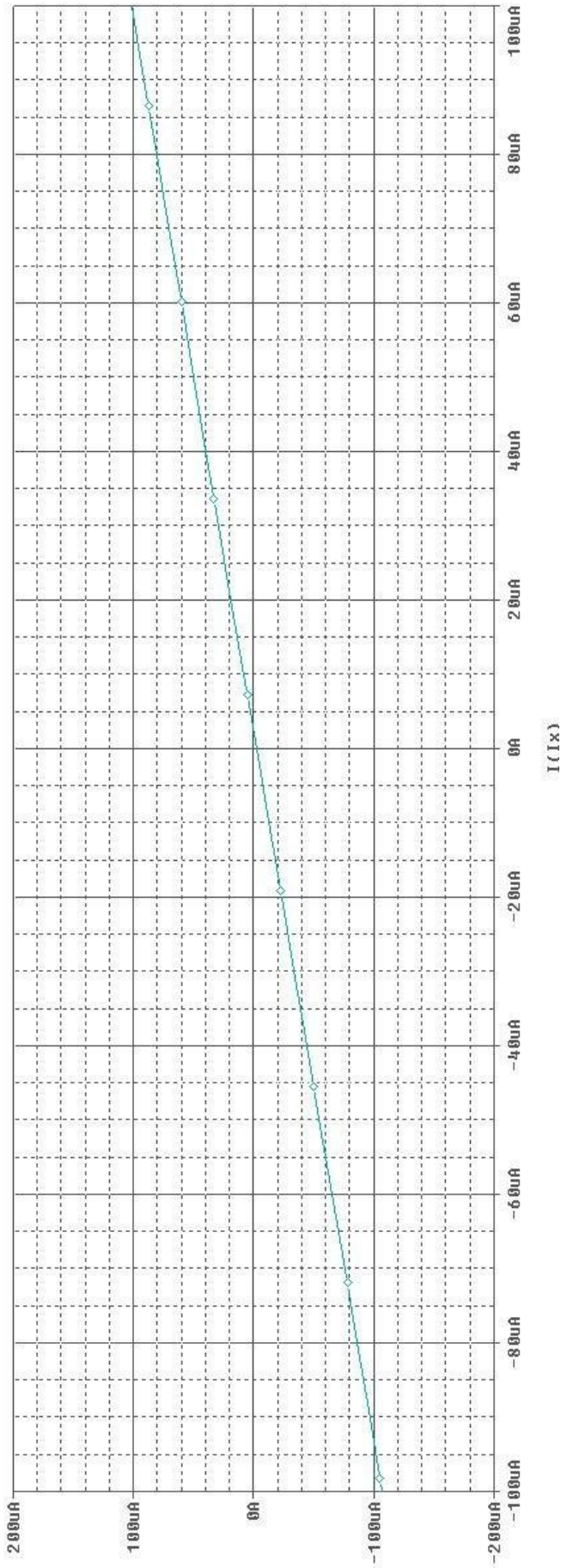


Fig. 2.8 DC transfer characteristic for current transfer from X port to Z1+ and Z2+ ports

Chapter-3

Biquadratic filter realization using DDCCTA

3.1. Multifuction voltage mode filter

In this section a multifunction voltage mode (VM) filter has been discussed. It consists of a single DDCCTA, two grounded capacitors and a grounded resistor [15]. The circuit of multifunction VM filter is shown in Fig. 3.1. The analysis of circuit yields the output voltages at various nodes as:

$$\frac{V_{out1}}{V_{in}} = \frac{s^2 C_1 C_2 R}{D(s)} \quad (3.1)$$

$$\frac{V_{out2}}{V_{in}} = \frac{s C_2}{D(s)} \quad (3.2)$$

$$\frac{V_{out3}}{V_{in}} = \frac{-g_m}{D(s)} \quad (3.3)$$

Where $D(s) = s^2C_1C_2R + sC_2 + g_m$

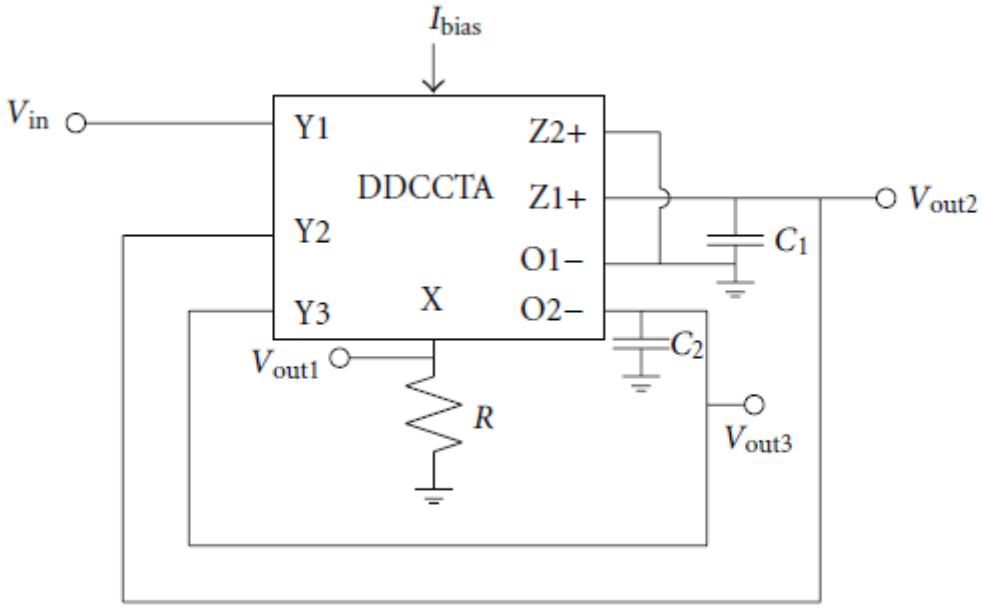


Fig. 3.1 Voltage mode filter

It can be seen from (3.1) to (3.3) that high pass, band pass and low pass responses are available simultaneously at V_{out1}, V_{out2} and V_{out3}. Thus the proposed structure is a single input and three output voltage mode filter. It may be noted that no component matching constraint is required. The responses are characterized by pole frequency (ω_o), bandwidth (ω_o /Q_o) and quality factor (Q_o) as

$$\omega_o = \sqrt[2]{\frac{g_m}{RC_1 C_2}} \qquad \frac{\omega_o}{Q_O} = \frac{1}{RC_1} \qquad Q_O = \sqrt[2]{\frac{g_m RC_1}{C_2}} \tag{3.4}$$

Equation (3.4) reveals that for high pass and band pass responses the pole frequency (ω_o) and quality factor (Q_o) can be adjusted by g_m , i.e. by bias current of DDCCTA, without disturbing (ω_o /Q_o). The ω_o and Q_o are orthogonally adjustable with simultaneous adjustment of g_m and R such that the product g_m R remains constant and the quotient g_m /R varies and vice versa**.**Since the resistance R is a grounded one,it may easily be implemented as a variable resistance using only two MOS [24]. Equation (3.4) also indicates that high values of Q-factor will be obtained from moderate values of

ratios of passive components i.e. from low component spread. These ratios can be chosen as $g_mR = \frac{C_1}{C_2} = Q_o$. So the spread of the component values becomes of the order of $\sqrt{Q_o}$. This feature of the filter related to the component spread allows the realization of high Q_o values more accurately compares to the topologies where the spread of passive components becomes Q_o or Q_o^2 . It can also be easily evaluated to show that the sensitivities of pole ω_o and pole Q_o are within unity in magnitude. Thus the discussed structures can be classified as insensitive. The proposed topology provides the availability of maximum number of simultaneous responses.

To verify the functionality of the single DDCCTA based voltage mode filter,
SPICE simulations have been carried out using TSMC 0.25μm CMOS process model parameters and supply voltages of VDD = -VSS = 1.25V and VBB = -0.8V. The aspect ratio of various transistors is provided in Table 1. The filter is designed for a pole frequency of f_o = 1.59 MHz, Q = 1, the component values are found to be C1 = C2 = 100 pF, R = 1 kΩ and bias current of DDCCTA equals to 100 μA. Figure 3.2 shows the simulation results for high pass (V_{out1}), bandpass (V_{out2}) and low pass (V_{out3}) filter responses which are available simultaneously.

Transistors	**Aspect ratio (W(μm)/L(μm))**
M_1-M_4	5/0.25
M_5, M_6	2.5/0.25
M_7 ,M_8	13.62/0.25
M_9, M_{11},M_{13}	4.25/0.25
M_{10},M_{12}, M_{14}	22/0.25
M_{15},M_{16},M_{19}-M_{24}	2.5/0.25
M_{17},M_{18}	13.5/0.25

Table 1 Aspect ratio of various transistors

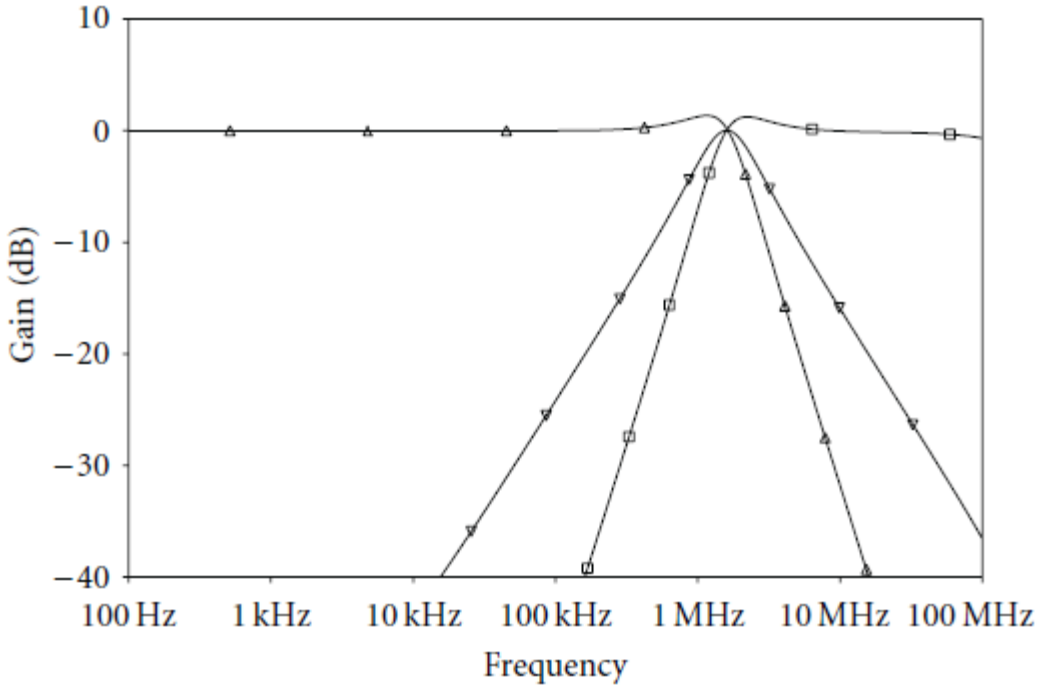


Fig. 3.2 Simulated responses of the voltage mode filter

3.2. MISO current mode universal filter

A multiple input single output (MISO) universal current mode (CM) filter has been shown in this section which is obtained by grounding voltage input in Fig. 3.1 and exciting it with current inputs as shown in Fig. 3.3. It employs a single DDCCTA, two grounded capacitors and a grounded resistor. Analysis of this circuit gives the output current as:

$$I_{out1} = \frac{-s^2 C_1 C_2 R I_{in1} - (sC_2 + g_m) I_{in2} + (sC_1) I_{in3}}{D(s)}$$

$$I_{out2} = \frac{-sg_m C_2 R (I_{in1} - I_{in2}) + g_m I_{in3} + D(s) I_{in4}}{D(s)}$$

Where $D(s) = s^2C_1C_2R + sC_2 + g_m$

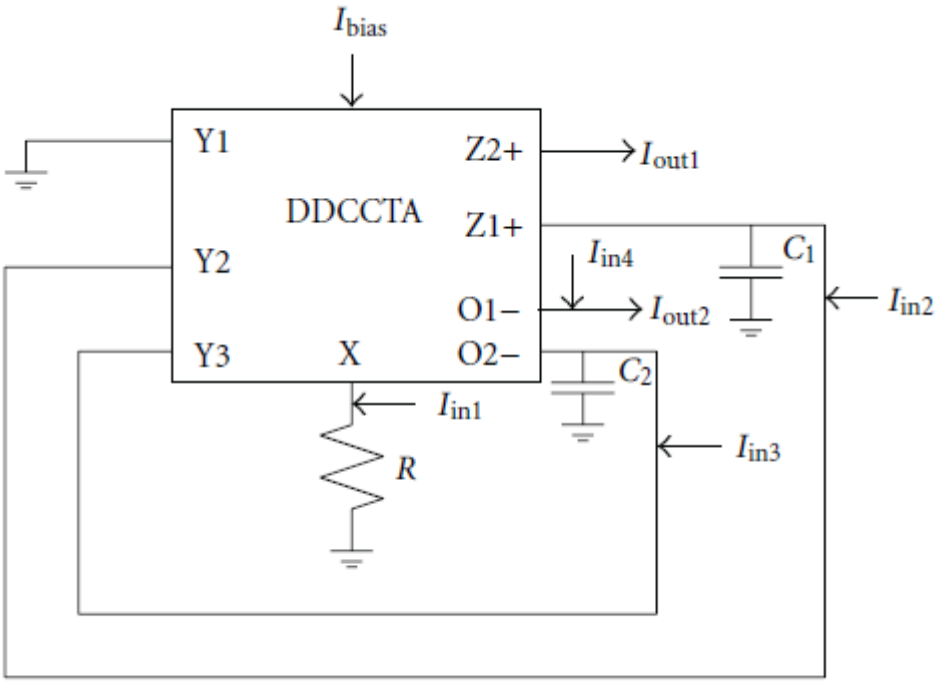


Fig. 3.3 Current mode universal filter

Table 2 shows the availability of each filter response and also the corresponding selection of input currents I_{in1}, I_{in2}, I_{in3} and I_{in4} . Thus the given structure is a four-input single output current mode filter. It may be noted that there is no component matching constraint for obtaining any filter response. The filter parameters are kept same as given in (3.4). The grounded resistance (R) may easily be implemented as variable one using only two MOS for full electronic control of filter parameters. The ω_o,Q_o and ω_o /Q_o can be adjusted orthogonally for low pass, high pass and band pass responses the way discussed in the previous section.

Filter responses	Inputs				Output
	I_{in1}	I_{in2}	I_{in3}	I_{in4}	
Low pass	0	0	1	0	I_{out2}
Band pass	0	0	1	0	I_{out1}
	1	0	0	0	I_{out2}
	0	1	0	0	I_{out2}
High pass	1	0	0	0	I_{out1}
Notch	0	1	0	1	I_{out2},$R = 1/g_m$
All pass	0	1	0	1	I_{out2},$R = 1/g_m$

Table 2 I_{in1}, I_{in2}, I_{in3} and I_{in4} values selection for each filter function response

The universal MISO current mode filter has been validated through SPICE simulations. The circuit of Fig.3.3 for a pole frequency of f_o = 1.59 MHz, Q = 1 has been designed with the component values of $C_1 = C_2$ = 100 pF, R = 1 kΩ and bias current of DDCCTA equals to 100 μA. Simulation results for band pass (I_{out1}) and low pass (I_{out2}) filter responses can be obtained simultaneously for $I_{in} = I_{in3}$, $I_{in1} = I_{in2} = I_{in4}$ = 0,shown in figure 3.4. Figure 3.5 shows the simulation results for band pass (I_{out2}) and high pass (I_{out1}) filter responses which are available simultaneously for $I_{in} = I_{in1}$, $I_{in2} = I_{in3}$=I_{in4}=0 and notch and all pass responses are available with $I_{in} = I_{in2} = I_{in4}$, I_{in1}= I_{in3}= 0 and R = 1 kΩ and 2 kΩ respectively.

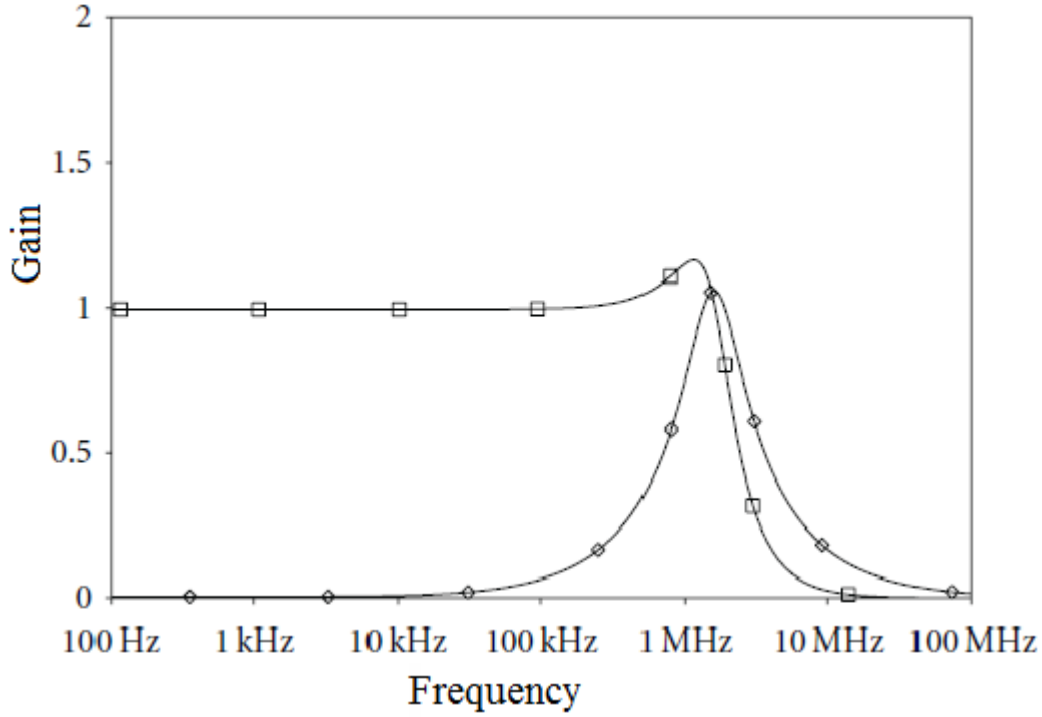


Fig.3.4 Simulated responses of the current mode universal filter: Low pass and Band pass

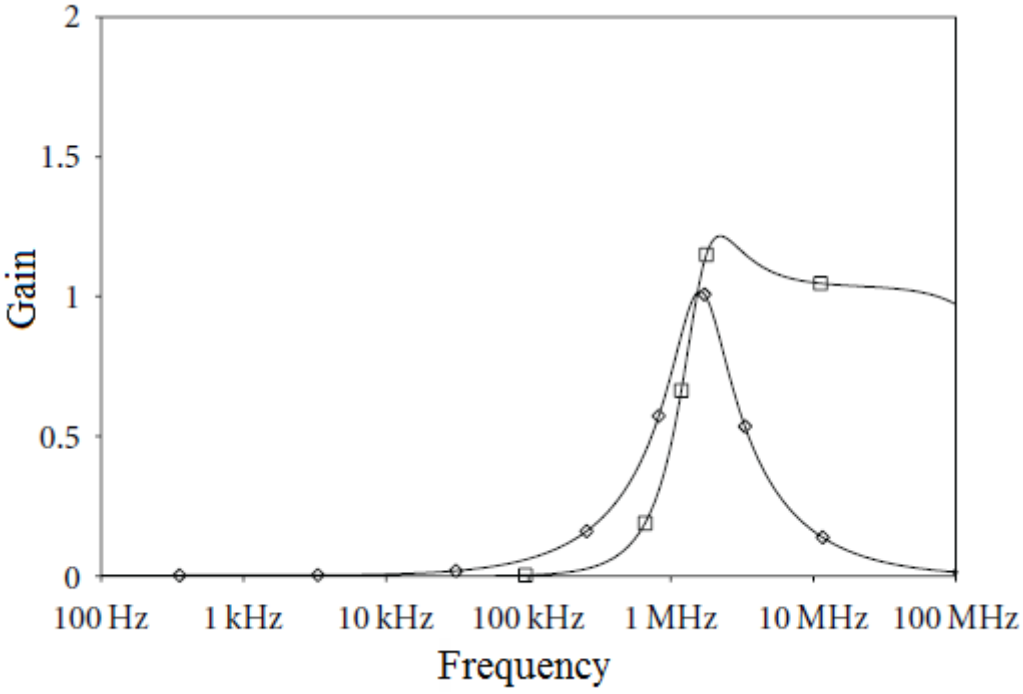


Fig.3.5 Simulated responses of the current mode universal filter: High pass and Band pass

Chapter 4

Realization of wave active filter using DDCCTA

4.1 Introduction

Higher order filter may be designed by mainly three approaches- topological simulation, operational simulation and wave active. In topological simulation or element replacement approach, the objective is to eliminate the inductor from the ladder filter. So the inductors of the LC ladder filters are replaced by appropriate configured active elements. The disadvantage of this approach is that a floating capacitor is used in active element and the floating passive elements are not good from the IC point of view as the parasitic are involve at high frequency.

In the operational simulation or leapfrog approach, the voltage and current relationships for each element of LC ladder filter are written. Then a Signal Flow Graph (SFG) is drawn using these equations and the resulted SFG is realized by lossy or lossless integrator. The drawback of this approach is that as we increase the order of filter, the number of the required equations for deriving the corresponding SFG increases. Another drawback is that, the realization of lossless integrators is not practically easy due to the imperfections imposed by the used active and passive elements.

An alternative approach for designing high-order filters is the wave method [25]-[31]. In this approach, we split the given filter into two port subnetworks. We draw the wave equivalent of the element of each subnetwork. For this first we draw the basic wave equivalent of series inductor, then the wave equivalent of other passive component can be drawn by interchanging the terminal and signal inversion. By interconnecting the

wave equivalents of each passive component we get the complete wave equivalent of the given filter. Wave active approach offers the following attractive feature.

a) The derived filter structures are modular, as the equivalents of the other passive components can be obtained from the wave equivalent of the elementary building block

b) In wave active approach there is no mathematical relationships related to the SFG representation as in the case of operational simulation approach. So the design procedure of high-order filters is much easier in compare to operational simulation approach

c) Realization of only lossy integrators using only grounded capacitors are required, instead of lossless integrators employed in the operational simulation or floating capacitors employed in the topological simulation.

4.2 Wave Active Filter

Wave active filter (WAF) design is an alternative approach to the simulation of resistively terminated LC ladder filter. According to this method, the corresponding passive prototype filter is split into two-port subnetworks which are fully described using the wave variables, defined as incident and reflected waves. The method to obtain wave equivalents of the two-port subnetworks is by using the scattering parameters matrix description. By choosing an inductor in a series branch as the elementary building block, its wave equivalent includes an appropriately configured lossy integrator. The wave equivalents of the other passive elements are derived by interchanging the terminals of the appropriate wave signals and signal inversion. As already mentioned, our approach to the synthesis of RC-active networks is based on the use of wave quantities rather than voltage-current quantities, hence the scattering matrix will play an important role in our concept. Usually, if scattering parameters are being used, as e.g., in microwave theory, they are derived for power waves; we could adopt this concept for our aim, too, but the use of voltage or current waves seems more convenient for our approach, since it leads sometimes to simpler circuits and, in addition, it simplifies the notation. For the approach presented in this report, we have decided to use voltage waves, which shall be introduced now. Consider the two-port N shown in Fig. 4.1, where the A1, A2 and B1, B2 denote the incident and reflected voltage waves at port one and two, respectively. To either port

we assign a port resistance (characteristic resistance) R1 and R2 respectively; the port resistances are assumed to be real positive constants.

The V, I port variables are related by means of a transmission matrix A as:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix}$$

The incident and reflected voltage waves are depicted as A_j (j=1,2) and B_j (j=1,2) respectively for two port network of Fig. 4.1 and are related with port resistance Rj (j=1,2) by the following relation:

$$A_j = V_j + I_j R_j \qquad B_j = V_j - I_j R_j$$

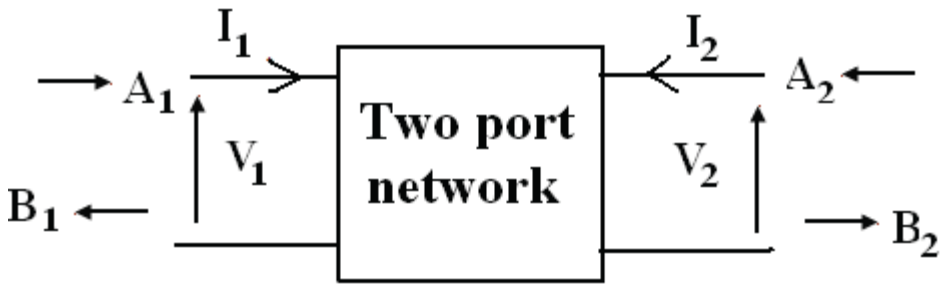


Fig. 4.1 Two port network

4.3 Realization of wave active filter

In wave method, the corresponding passive prototype filter is split into two-port subnetworks which are fully described using the wave variables, defined as incident and reflected waves. We use series inductor as a basic element for developing the wave active filter. The wave equivalent of an inductor in series branch is developed using differential difference current conveyor transconductance amplifier (DDCCTA), then

this basic wave equivalent can be used for other passive element realization by making appropriate connection. The results are verified through SPICE simulation using 0.25μm TSMC CMOS technology parameters.

4.3.1 Basic Wave Equivalent (Series Inductor)

In wave method, the forward and reflected voltage waves are used to define the functionality of the filter. The incident and reflected voltage waves are depicted as A_j and B_j respectively for two port network of Fig. 4.1 and are related by the following relation:

$$A_j = V_j + I_j R_j \qquad B_j = V_j - I_j R_j \tag{4.1}$$

Equation (3) can be expressed in terms of scattering matrix S as

$$\begin{bmatrix} B_1 \\ B_2 \end{bmatrix} = S \begin{bmatrix} A_1 \\ A_2 \end{bmatrix} \tag{4.2}$$

The basic element for the developing wave active filter is a series inductor L. It can be described in terms of scattering parameter as

$$S = \frac{1}{1+s\tau} \begin{bmatrix} s\tau & 1 \\ 1 & s\tau \end{bmatrix} \tag{4.3}$$

The relationship between incident (A_j, j=1,2) and the reflected wave (B_j. j=1,2) of a series inductor may be obtained from (4.2) and (4.3) as

$$B_1 = A_1 - \frac{1}{1+s\tau}(A_1 - A_2) \tag{4.4}$$

$$B_2 = A_2 + \frac{1}{1+s\tau}(A_1 - A_2) \tag{4.5}$$

Where $\tau = \frac{L}{2R}$ is time constant and R represents port resistance.

The implementation of (4.4) and (4.5) require three operations - lossy integration subtraction, summation and subtraction. These operations can easily be realized using DDCCTA as shown in Fig. 4.2.

In figure 4.2 ,block 1 represents lossy integration subtraction and provides output voltages V_1 as

$$V_1 = (A_1 - A_2)\frac{1}{1+s\tau} \tag{4.6}$$

Where $\tau = R_d C_d$ is time constant and $g_m R_d = 1$ .Using (4.4), (4.5) and (4.6), the value of C_d may be computed as

$$R_d C_d = \frac{L}{2R} \tag{4.7}$$

Assuming R = R_d, the value of capacitor C_d may be expressed as

$$C_d = \frac{L}{2R^2} \tag{4.8}$$

The block 2 in Fig. 4.2 performs the subtraction operation and presents output voltage as

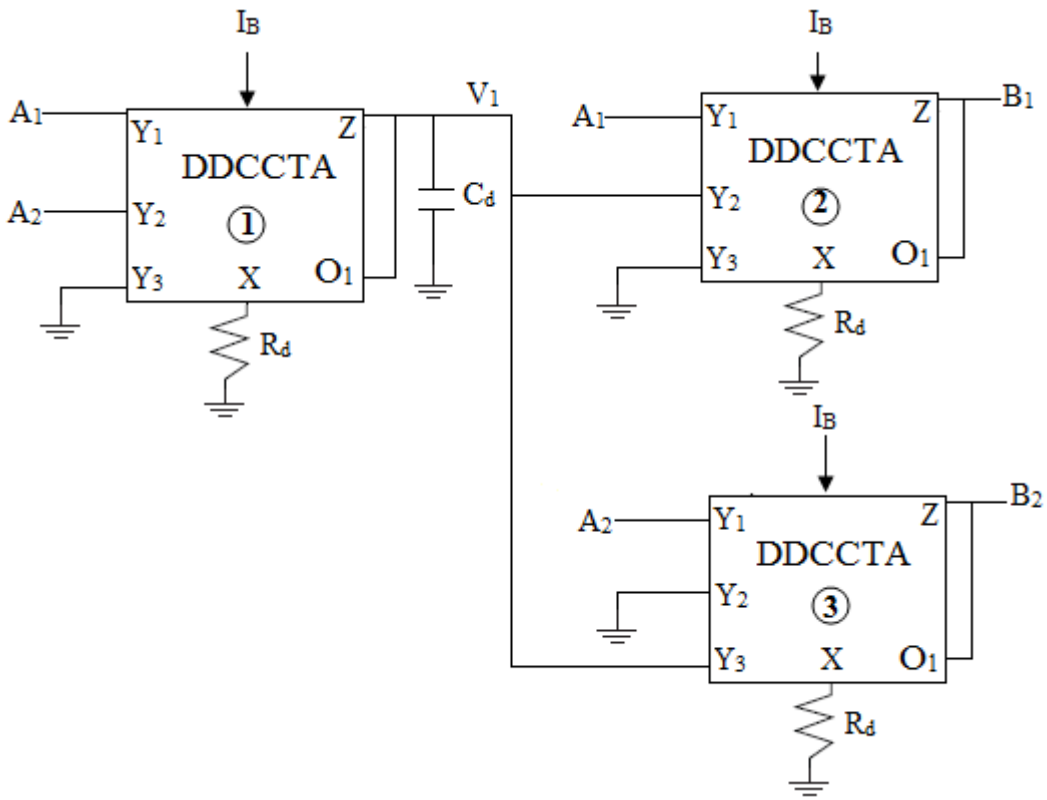
$$B_1 = A_1 - V_1 = A_1 - \frac{1}{1+s\tau}(A_1 - A_2) \quad \text{with} \quad g_m R_d = 1 \tag{4.9}$$

Summation operation is performed by block 3 of Fig.4.2. The output voltage of block 3 is

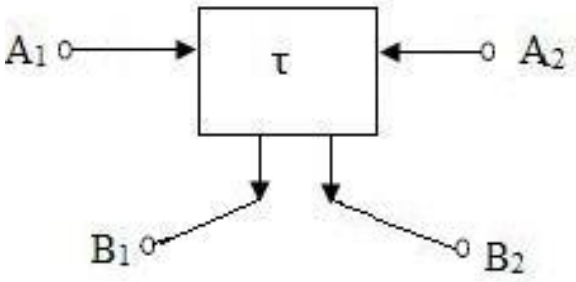
$$B_2 = A_2 + V_1 = A_2 + \frac{1}{1+s\tau}(A_1 - A_2) \text{ with } g_m R_d = 1 \tag{4.10}$$

It may be noted that the proposed realization uses significantly lesser number of resistor and active analog blocks than the earlier reported structures .

The complete schematic of wave equivalent for series inductor and its symbolic representation is shown in Fig 4.2(a) and 4.2(b).



(a)



(b)

Fig. 4.2 (a) Complete schematic of DDCCTA based wave equivalent of series inductor and (b) its symbolic representation

With the help of this basic wave equivalent of series inductor, the wave equivalent of other passive component can be obtained simply by swapping outputs and using signal inversion as shown in table 3 and table 4.

Table 3

Wave equivalent of Elementary Two Port consisting of series branch element

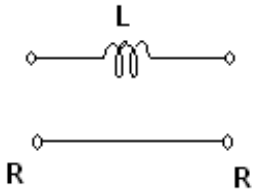
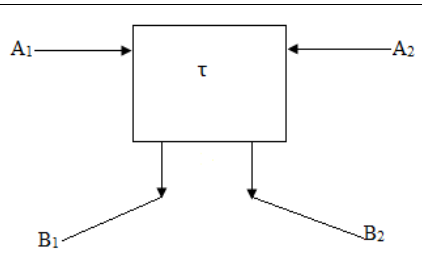
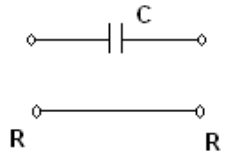
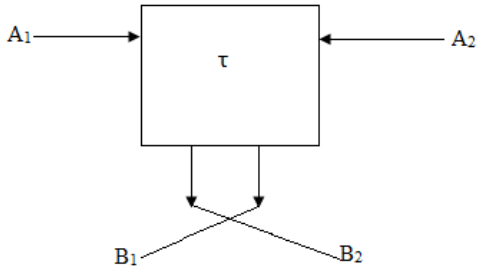
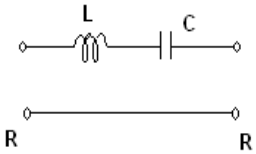
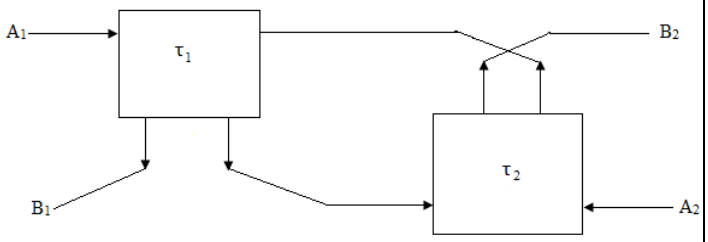
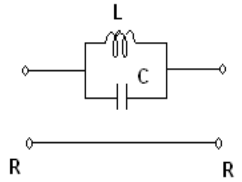
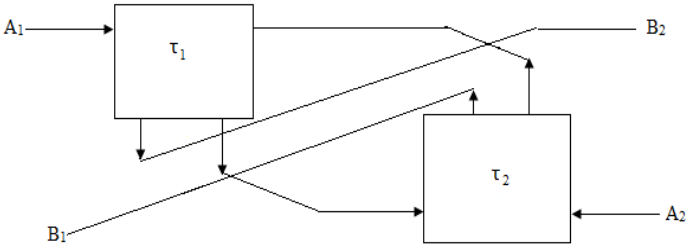
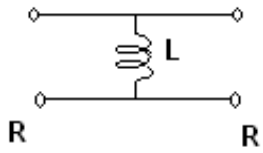
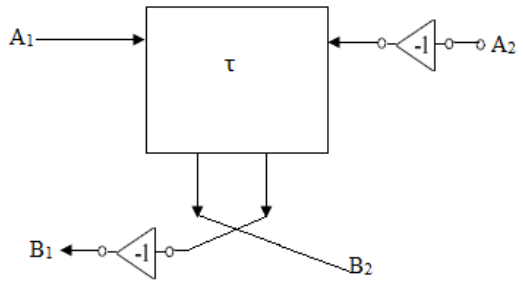
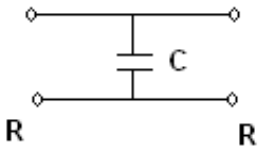
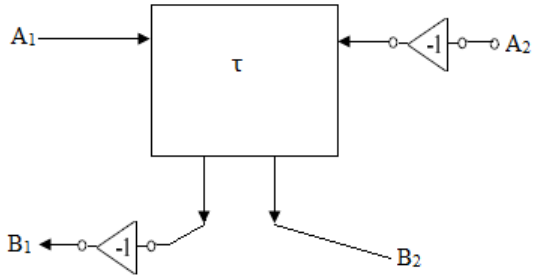
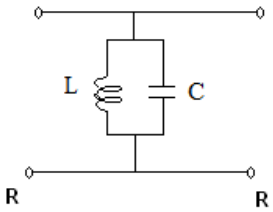
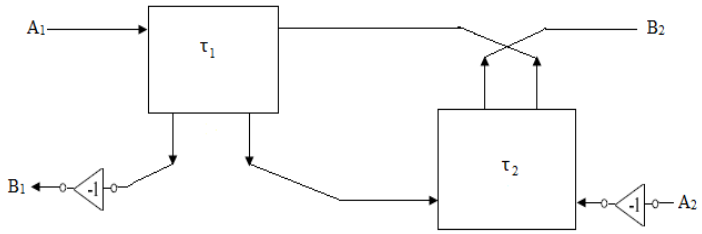
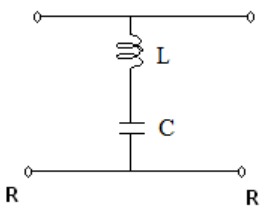
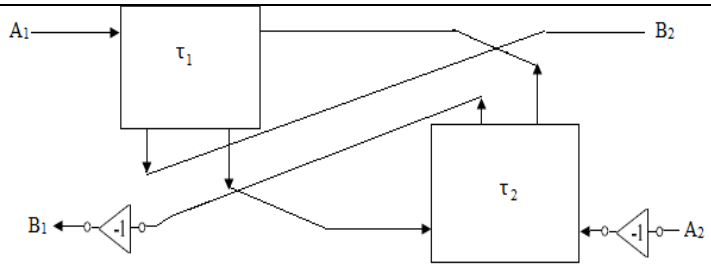
Elementary two port	Port Connection	Realized Time Constant; Capacitor value
		$\tau = L/2R$ $C_d = L/2R^2$
		$\tau = 2RC$ $C_d=2C$
		$\tau_1 = L/2R$ $\tau_2 = 2RC$ $C_{1d} = L/2R^2$ $C_{2d} = 2C$
		$\tau_2 = L/2R$ $\tau_1 = 2RC$ $C_{2d} = L/2R^2$ $C_{1d} = 2C$

Table 4

Wave equivalent of Elementary Two Port consisting of shunt branch element

Elementary two port	Port Connection	Time Constant; Capacitor value
		$\tau = 2L/R$ $C_d = 2L/R^2$
		$\tau = RC/2$ $C_d=C/2$
		$\tau_1 = RC/2$ $\tau_2 = 2L/R$ $C_{1d} = C/2$ $C_{2d} = 2L/R^2$
		$\tau_2 = 2L/R$ $\tau_1 = RC/2$ $C_{2d} = C/2$ $C_{1d} = 2L/R^2$

4.3.2 Realization of 4th order filter using wave active method

To demonstrate the wave active filter mentioned in the above section, a fourth order low pass butterworth filter of Fig. 4.3 has been taken as prototype. The normalized component values are given as R_s= 1, L_1 = .7654, L_2 = 1.8485, C_1 = 1.8485, C_2 = .7654 and R_L = 1 for maximally flat response. The wave equivalent topology of Fig. 4.3 may be obtained by replacing the series inductor and shunt capacitor by wave equivalent of Table 3 and table 4 and is shown in Fig. 4.4. For cut-off frequency f_o = 1 MHz, the bias current I_{B1} is taken as 200μA . The capacitor values for wave equivalent of series inductors (L_1, L_2) and shunt capacitors (C_1, C_2) are 40.83 pF, 100.45 pF and 100.45 pF, 40.83 pF respectively. The topology of 4^{th} order filter has been simulated using DDCCTA based wave equivalent as discussed in the above section using 0.25μm TSMC CMOS technology parameters and power supply of ±1.25V. Fig. 4.5 and 4.6 show the simulated low pass responses (V_{out}) and its complementary high pass response (V_{outc}) respectively.

The aspect ratios of various transistors of DDCCTA are listed in Table. 5

Table 5

Transistors	**Aspect ratio (W(μm)/L(μm))**
M_1, M_4, M_9, M_{11}, M_{19}	3/0.25
M_2, M_3, M_5, M_6	1/0.25
M_7 - M_8, M_{15}, M_{17}	5/0.25
M_{10}, M_{12}	12.5/0.25
M_{13} – M_{14},	5/0.25
M_{16}	4.6/0.25
M_{18}	4.7/0.25
M_{20}	2.7/0.25

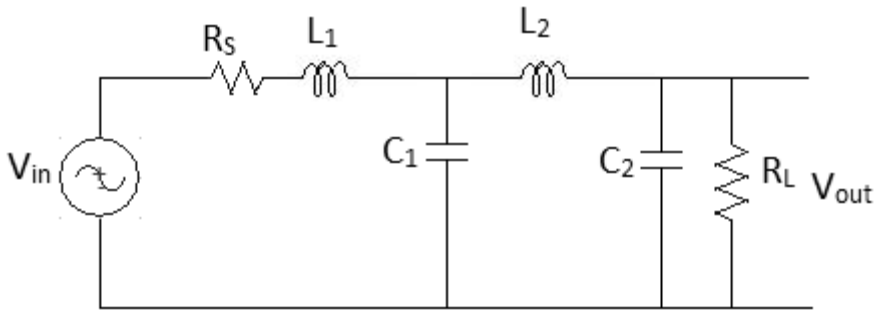


Fig.4.3 4th Order Butterworth Filter

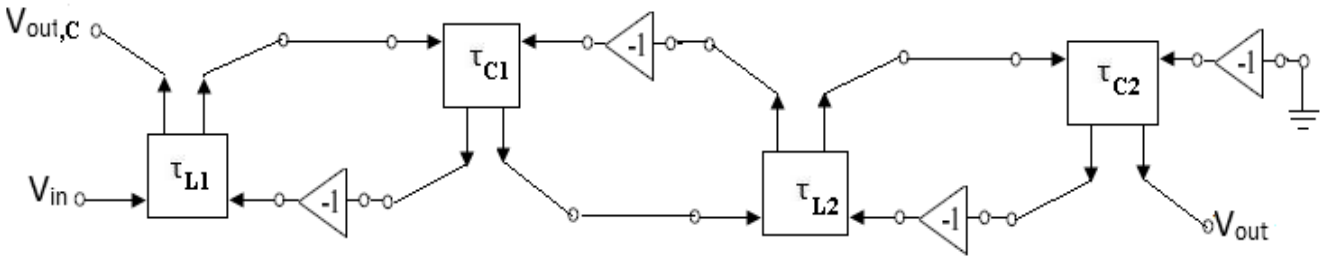


Fig. 4.4 Wave equivalent of 4th order low pass butterworth filter

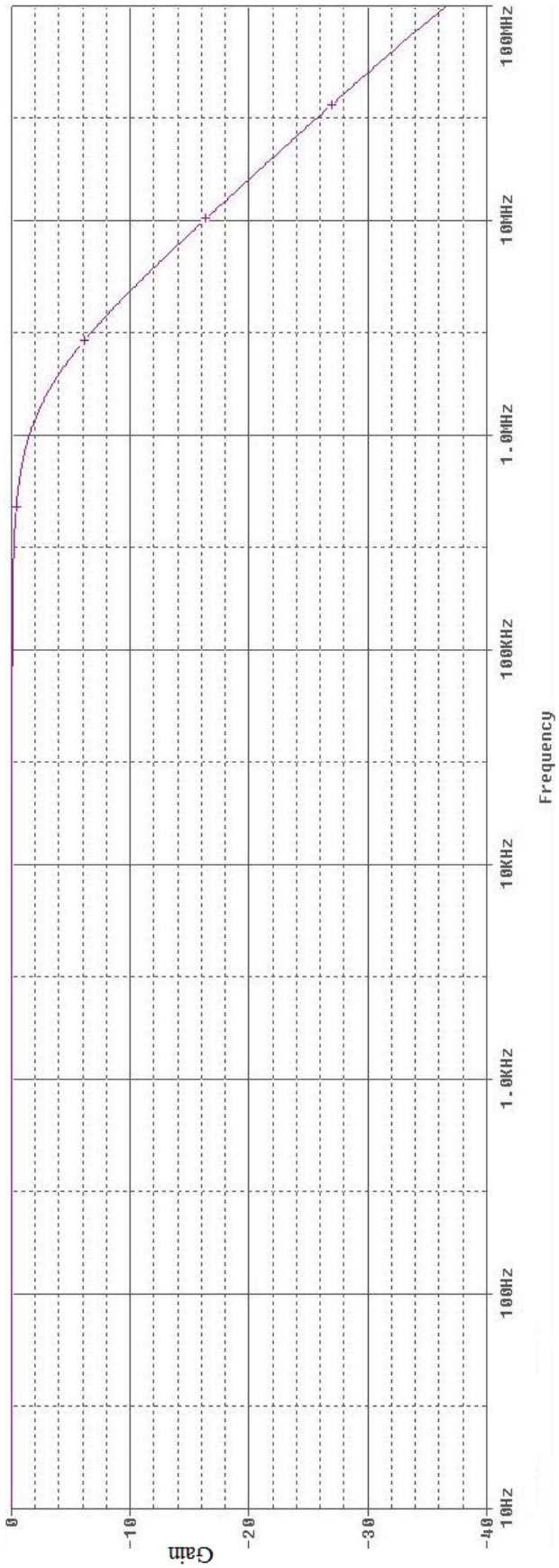


Fig. 4.5 Frequency Response of 4th order Low Pass Filter

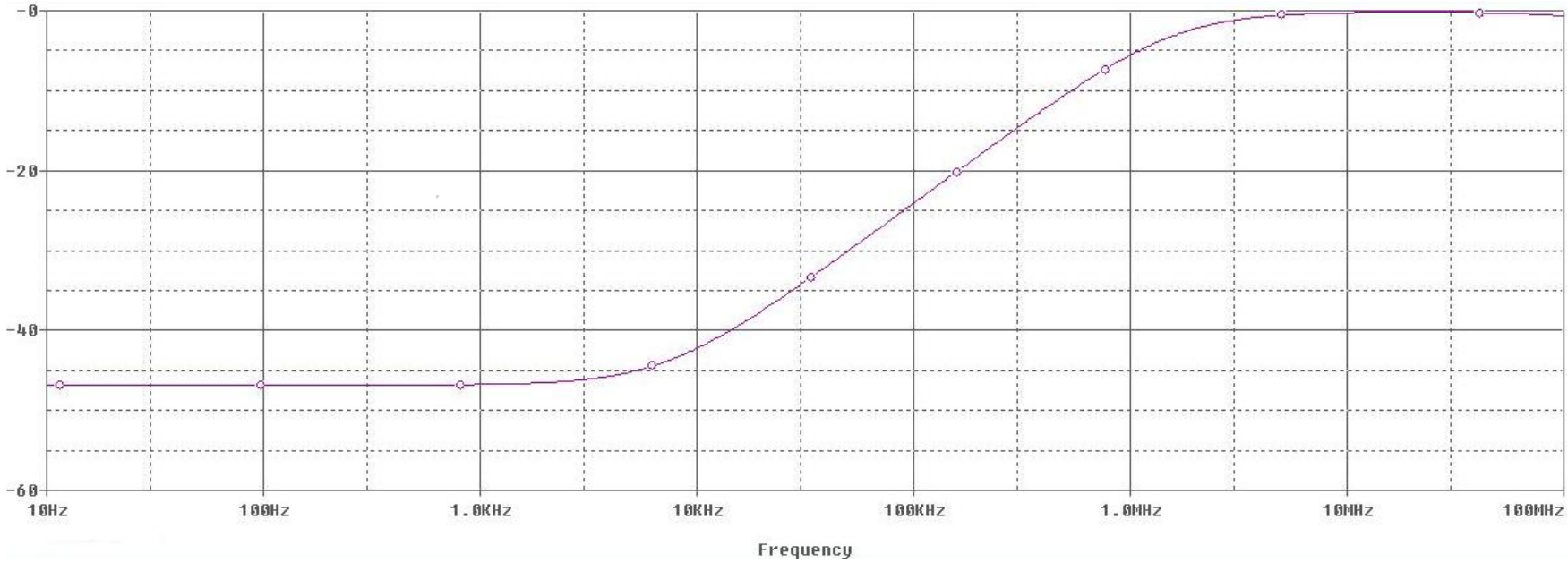


Fig. 4.6 Frequency Response of Complementary High Pass Filter

Chapter -5

Operational simulation

5.1 Introduction

The operational simulation method actually takes a different approach than topological simulation or wave active method, as in this approach we simulate operation of ladder rather than its component [25]. The circuit equations and voltage- current relationship of each element are written. Then these equations are represented either by block diagrams or by signal flow graph. Each block represents some analog operation, such as summation, integration etc. The process of simulating the operation of LC ladder is explained here by the following example from which the general design procedure become clear.

5.2 Operational simulation of 4th order low pass filter

To clarify the previous statement, consider the 4th order low pass filter as shown in Fig. 5.1 . Apply Kirchhoff's law in his circuit

$V_1 = V_{in} - V_2$ $\quad\quad$ $V_3 = V_2 - V_o$ $\quad\quad$ (5.1)

$I_2 = I_1 - I_3$ $\quad\quad$ $I_4 = I_3 - I_5 = I_3$ $\quad\quad$ (5.2)

Here we assumed that $I_5 = 0$

The V-I relationship for the series and shunt branch for the ladder

$$I_1 = \frac{V_1}{(sL_1 + R_S)} \qquad I_3 = \frac{V_3}{sL_2} \qquad (5.3)$$

$$V_2 = \frac{I_2}{sC_1} \qquad V_O = \frac{I_4}{(sC_2 + G_L)} \qquad (5.4)$$

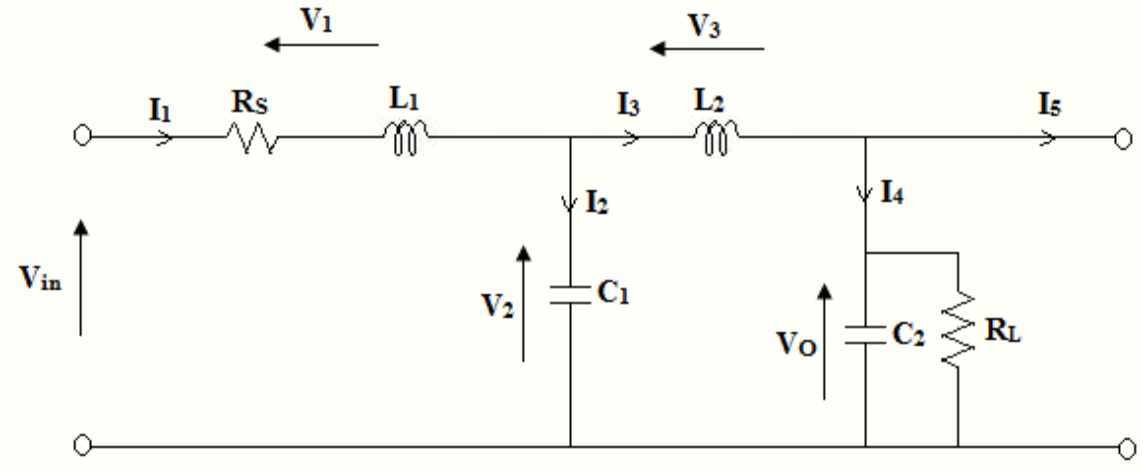


Fig. 5.1 4th order low pass butterworth filter

To simulate the equations from (5.1) to (5.4), we need the circuit which perform the differences of two voltage or currents, and those that perform the lossy and lossless integration. If we take these circuits and connect them appropriately, all the equation will be realized and the resulting structure will realized the given LC filter. To develop this process in a mathematical manner so that the results become generally valid, consider the general ladder of Fig. 5.2. The series branch element are labelled by admittance Y_i and the shunt branch by impedance Zi.

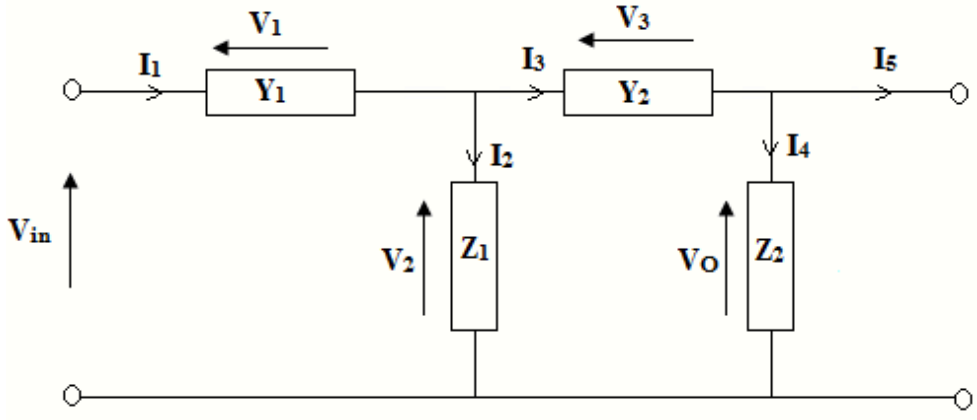


Fig. 5.2 The ladder of Fig. 5.1

The ladder is described by the equations

$I_1 = Y_1 (V_{in} - V_2)$ where $Y_1 = \left(\frac{1}{R_S + sL_1}\right)$ (5.5)

$V_2 = Z_1 (I_1 - I_3)$ where $Z_1 = \left(\frac{1}{sL_1}\right)$ (5.6)

$I_3 = Y_2 (V_2 - V_O)$ where $Y_2 = \left(\frac{1}{sL_2}\right)$ (5.7)

$V_O = Z_2 (I_3 - I_5) = Z_2 I_3$ where $Z_2 = \left(\frac{1}{\frac{1}{sR_L} + sC_2}\right)$ (5.8)

To implement the 4th order low pass filter we have to implement the above equations using DDCCTA.

Consider DDCCTA as arranged in the following configuration :

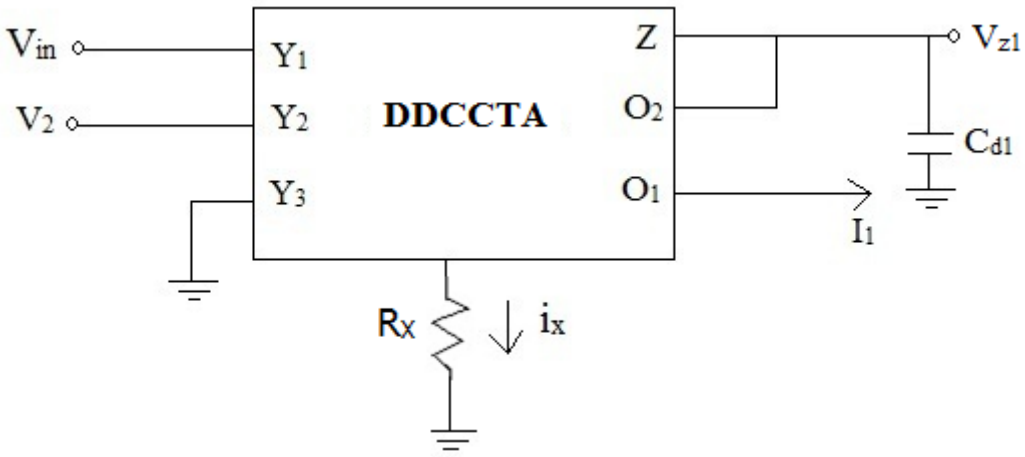


Fig. 5.3

$V_{z1} = [I_Z + (-g_m V_{z1})] \frac{1}{sC_{d1}}$

$sC_{d1}V_{z1} = \left(\frac{V_{in} - V_2}{R_x}\right) + (-g_m V_{z1})$

$$(sC_{d1} + gm)\, V_{z1} = \left(\frac{V_{in}-V_2}{R_x}\right)$$

$$V_{z1} = \left(\frac{V_{in}-V_2}{R_x\,(sC_{d1}+g_m)}\right)$$

$$I_{O1} = g_m\, V_{z1} = \frac{g_m(V_{in}-V_2)}{R_x\,(sC_{d1}+g_m)} \qquad (5.9)$$

Comparing (5.9) with equation (5.5)

$\frac{g_m}{R_x} = 1$ and $L_1 = C_{d1}$

Hence $g_m = R_X$ and $L_1 = C_{d1}$ (5.10)

Again consider DDCCTA in the following configuration :

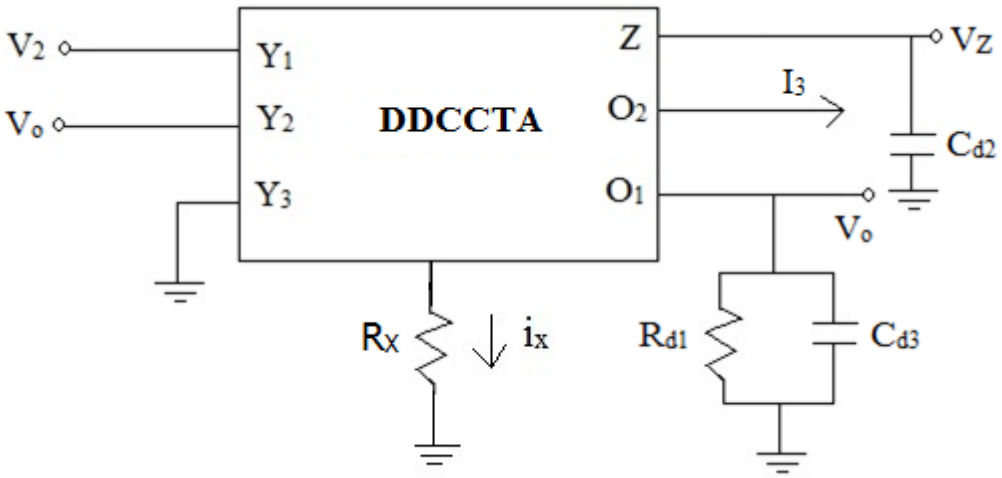


Fig. 5.4

$$V_Z = \left(\frac{V_2-V_O}{R_x}\right)\frac{1}{s\,C_{d2}}$$

$$I_{O1} = g_m\, V_z = \frac{g_m(V_2-V_o)}{R_x\,(sC_{d2})} \qquad (5.11)$$

Comparing (5.11) with equation (5.7)

$L_2 = C_{d2}$ since $g_m = R_X$ (5.12)

$$V_0 = I_{O1} \times \left(\frac{1}{\frac{1}{sR_{d1}} + sC_{d3}} \right) \quad (5.13)$$

Comparing (5.13) with equation (5.8)

$R_{d1} = R_L$ and $C_2 = C_{d3}$ (5.14)

Complete 4th order filter can be realized by combining above configured DDCCTA blocks in a manner so that equations from (5.5) to (5.8) can be realized.

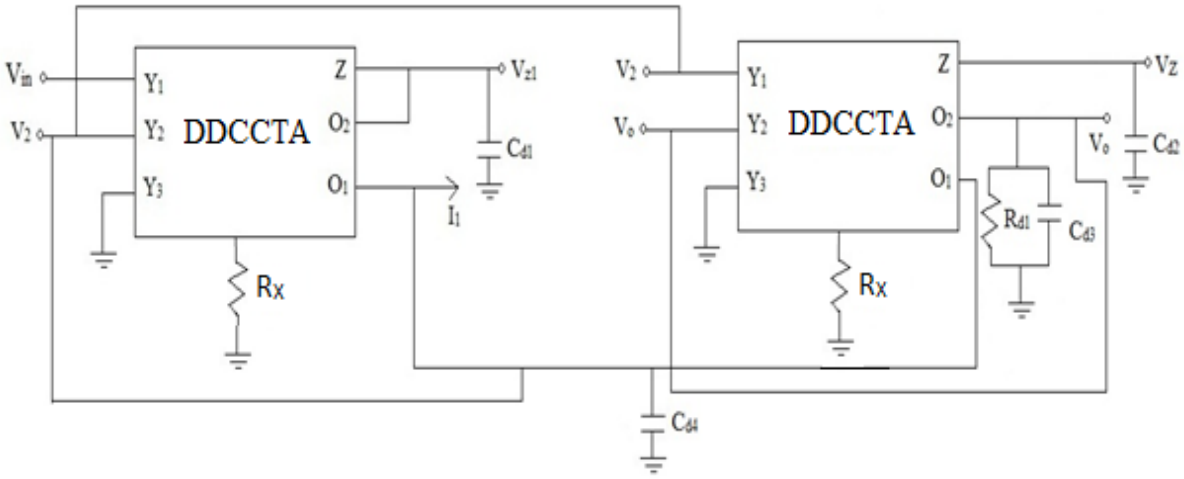


Fig. 5.5 Complete realization of 4th order low pass filter using DDCCTA

$$V_2 = \frac{1}{s\,C_{d3}} (I_1 - I_3) \quad (5.15)$$

Comparing (5.15) with equation (5.6)

$C_{d3} = L_1$ (5.16)

The normalized component values are given as R_s= 1, L_1 = .7654, L_2 = 1.8485, C_1 = 1.8485, C_2 = .7654 and R_L = 1. For cut-off frequency f_o = 1 MHz, the bias current I_{B1} is taken as 200μA .

The value of used capacitor in DDCCTA block can be calculated by the equation (5.10), (5.12), (5.14), (5.16) and the value of C_{d1}, C_{d2}, C_{d3}, C_{d4} are 44.7pf , 108.4pf, 108.4pf, 44.7pf respectively.

The simulation is carried out through 0.25μm TSMC CMOS technology parameters and the power supply of ±1.25V. The low pass filter response is shown in Fig. 5.6.

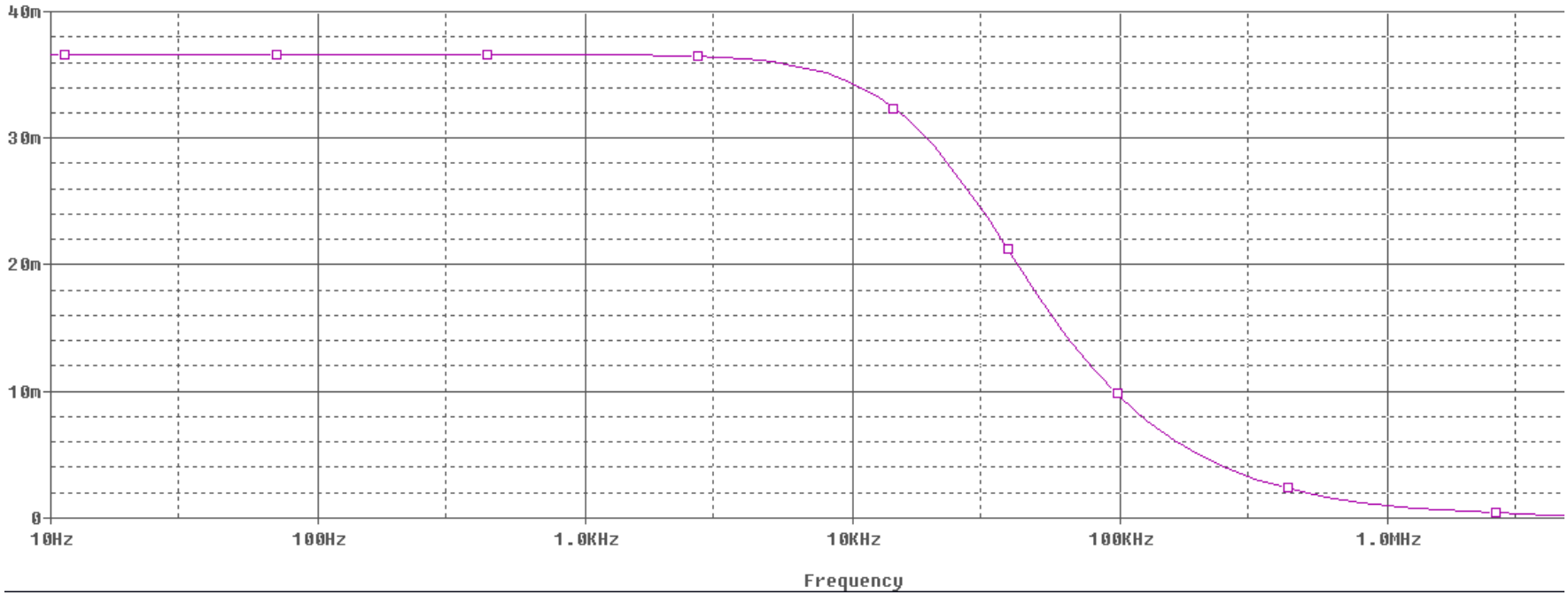


Fig. 5.6 Low pass response of 4th order filter

Chapter 6

Proposed DDCCCTA structure

6.1 Introduction

The Differential Difference Current Controlled Conveyor Transconductance Amplifier (DDCCCTA) is an attractive active building block for analog signal processing. In this chapter DDCCCTA has been discussed that consists of Differential Difference Current Conveyor (DDCC), Translinear loop and Transconductance amplifier (TA).

Differential Difference Current Conveyor (DDCC)

The differential difference current conveyor (DDCC), as a current-mode active device, has the advantages of both the second-generation current conveyor (CCII) (such as large signal bandwidth, great linearity, wide dynamic range) and the differential difference amplifier (DDA) (such as high input impedance and arithmetic operation capability) [16]. This element as a building block has versatile and special properties, such as easy implementation of differential and floating input circuits, whose applications exist in the literature [17–23]. The DDCC, whose symbol is shown in Figure 6.1 is a six port building block.

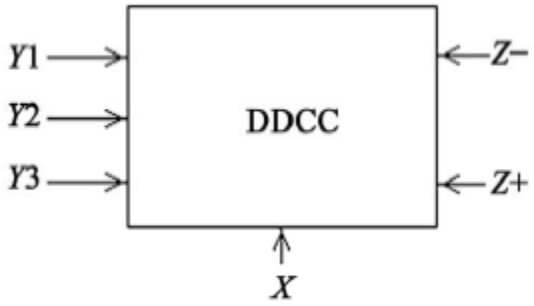


Fig. 6.1 Block diagram of DDCC

The DDCC is characterized by the following equations:

$$V_X = V_{Y1} - V_{Y2} + V_{Y3} \quad (6.1)$$

$$I_{Z+} = I_X \quad (6.2)$$

$$I_{Z-} = - I_X \quad (6.3)$$

$$I_{Y1} = I_{Y2} = I_{Y3} = 0 \quad (6.4)$$

where, suffixes refer to the respective terminals.

The CMOS implementation of DDCC is shown in Figure 6.2. The input transconductance elements are realized with two differential stages (M1 and M2, M3 and M4)

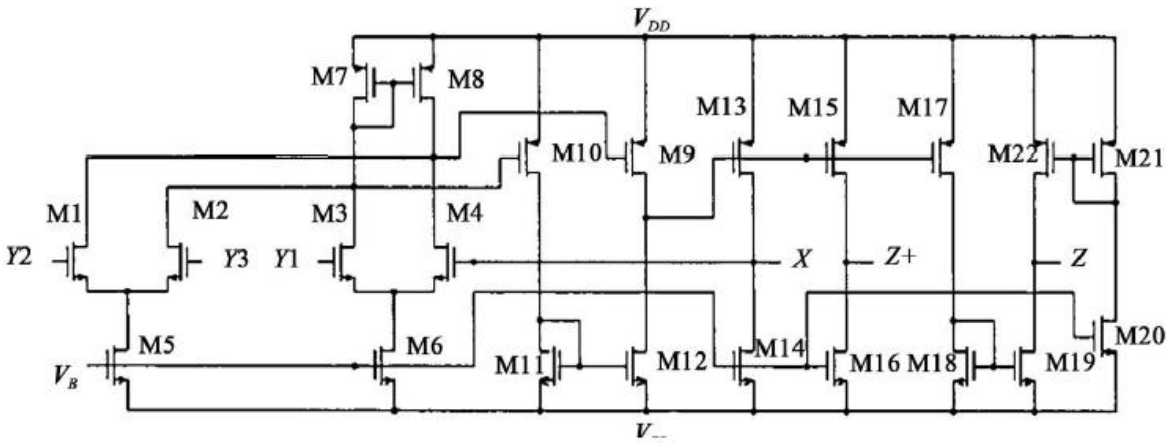


Fig. 6.2 CMOS implementation of DDCC

Translinear loop

This block is used to provide parasitic resistance in DDCCCTA and is shown in Fig. 6.3. The parasitic resistance is controlled by bias current.

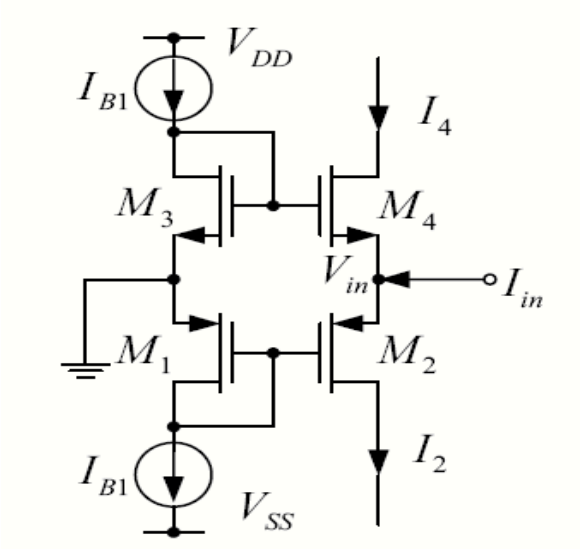


Fig. 6.3 Class AB Translinear Loop

Calculation of parasitic resistance:

Apply KCL at input node

$I_{in} = I_2 - I_4$ (6.5)

For small signal model the diode connected transistors M1 and M3 will be replaced by resistance of $1/gm_1$ and $1/gm_3$ where gm_i (i=1,3) is transconductance of i^{th} transistor. The currents I_2 and I_4 may be expressed as

$I_2 = g_{m2} V_{SG2}$

$I_4 = g_{m4} V_{GS4}$ (6.6)

$V_{SG2} = V_{S2} - V_{G2} = V_{in} - \left(-\frac{I_{B1}}{g_{m1}}\right)$

$$V_{GS4} = V_{G4} - V_{S4} = \left(\frac{I_{B1}}{g_{m3}}\right) - V_{in} \quad (6.7)$$

On putting the value of V_{SG2} and V_{GS4} in equation (6.6), we have

$$I_2 = g_{m2}\left[Vin + \left(\frac{I_{B1}}{g_{m1}}\right)\right] \text{ and } I_4 = g_{m4}\left[\left(\frac{I_{B1}}{g_{m3}}\right) - Vin\right] \quad (6.8)$$

Now put I_2 and I_4 in equation (6.5),

$$I_{in} = g_{m2}\left[Vin + \left(\frac{I_{B1}}{g_{m1}}\right)\right] - g_{m4}\left[\left(\frac{I_{B1}}{g_{m3}}\right) - Vin\right]$$

$$I_{in} = V_{in}\,(g_{m2} + g_{m4}) + I_{B1}\left(\frac{g_{m2}}{g_{m1}} - \frac{g_{m4}}{g_{m3}}\right)$$

$$1 = R_X\,(g_{m2} + g_{m4}) + \frac{I_{B1}}{I_{in}}\left(\frac{g_{m2}}{g_{m1}} - \frac{g_{m4}}{g_{m3}}\right) \text{ where } R_X = \frac{V_{in}}{I_{in}}$$

$$R_X = \frac{1}{g_{m2}+g_{m4}} - \frac{I_{B1}}{I_{in}(g_{m2} + g_{m4})}\left(\frac{g_{m2}}{g_{m1}} - \frac{g_{m4}}{g_{m3}}\right) \quad (6.9)$$

If $g_{m1} = g_{m3}$ and $g_{m2} = g_{m4} = g_m$, then

$$R_X = \frac{1}{g_{m2}+g_{m4}} = \frac{1}{2g_m} = \frac{1}{\sqrt{8kI_{B1}}} \quad (6.10)$$

Where transistors are assumed to be in saturation region and

$$K = \mu_n C_{OX}\left(\frac{W}{L}\right)_4 = \mu_p C_{OX}\left(\frac{W}{L}\right)_2 \quad (6.11)$$

Transconductance Amplifier

The operational transconductance amplifier is a differential amplifier whose differential input voltage produces an output current. Thus, it is a voltage controlled current source (VCCS). The transconductance of the amplifier is proportional to the square root of bias current. This feature makes it useful for electronic control of amplifier gain. The block

diagram and CMOS implementation of transconductance amplifier is shown in Fig. 6.4 and Fig. 6.5.

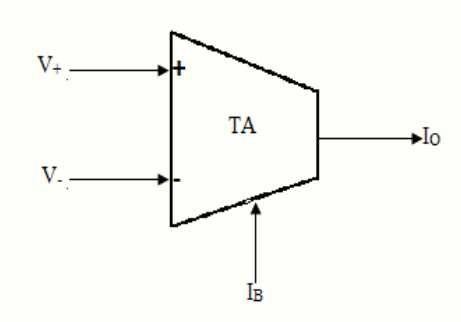


Fig. 6.4 Block diagram of Transconductance Amplifier

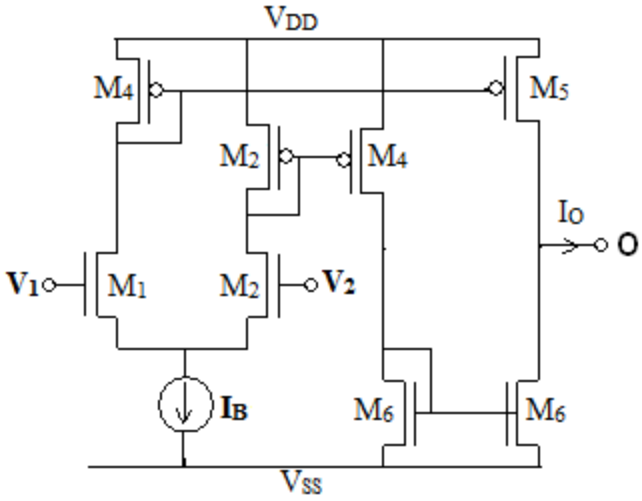


Fig. 6.5 CMOS Implementation of Transconductance Amplifier

The output current I_O may be given as

$$I_O = g_m (V_1 - V_2) \quad \text{where } g_m = \sqrt{\mu_n C_{OX} I_B \left(\frac{W}{L}\right)_{1,2}} \tag{6.12}$$

DDCCCTA

Since DDCCCTA comprises DDCC, translinear loop and Transconductance amplifier, so on combining the circuit diagram of Fig. 6.2, Fig. 6.3 and Fig. 6.5, the block diagram and CMOS implementation of DDCCCTA is obtained as shown in Figure 6.6 and Figure 6.7.

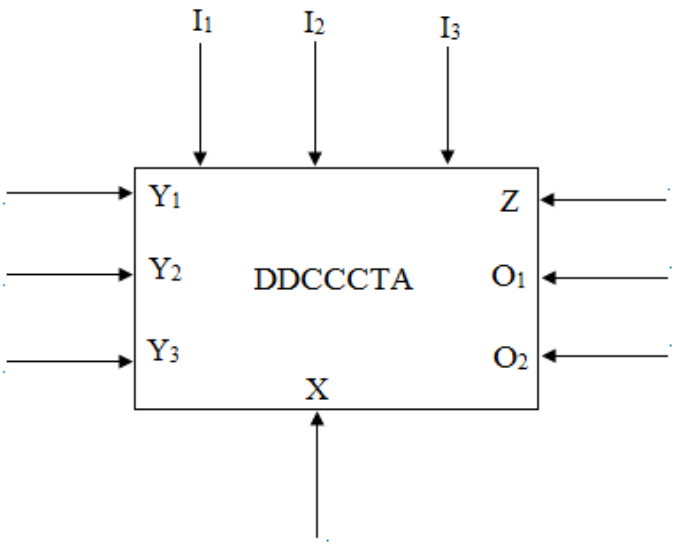


Fig. 6.6 Block diagram of DDCCCTA

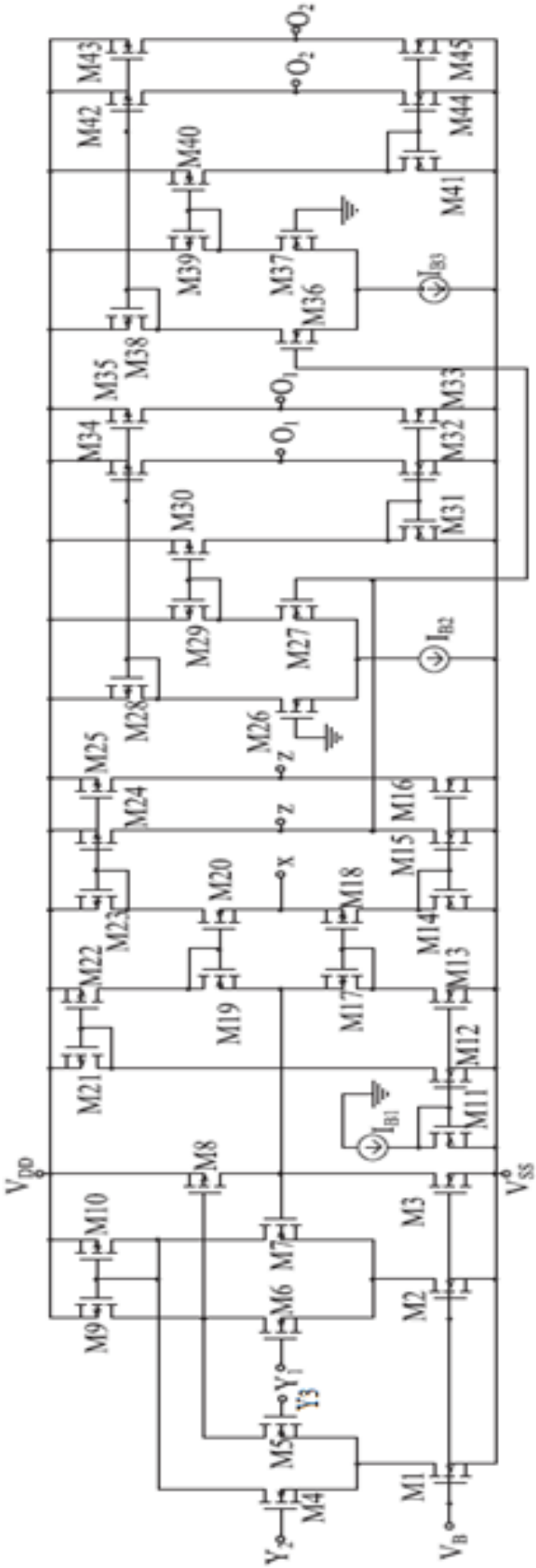


Fig. 6.7 CMOS implementation of DDCCCTA

The derivation of port relationships is given in sections 6.2 to 6.4 as per the method outlined in [12].

6.2 Relationship between voltages of X port and Y1, Y2, and Y3 ports

The voltage at X port may be found by analyzing the differential difference part (comprising of transistors M1 to M23) of the circuit of Fig.6.7 as follows:

$$V_X = \beta_1 V_{Y1} - \beta_2 V_{Y2} + \beta_3 V_{Y3} + \varepsilon_V + I_X R_X \tag{6.13}$$

Where $R_X = \dfrac{1}{g_{18}+g_{20}}$

And

Where

$$\beta_1 = \frac{1}{P1}\left(g_6 g_{10} + g_6 \frac{g_7 g_9 - g_6 g_{10}}{g_6+g_7}\right) \tag{6.14}$$

$$\beta_2 = \frac{1}{P1}\left(g_4 g_9 + g_4 \frac{g_4 g_9 - g_5 g_{10}}{g_6+g_7}\right) \tag{6.15}$$

$$\beta_3 = \frac{1}{P1}\left(g_5 g_{10} + g_5 \frac{g_4 g_9 - g_5 g_{10}}{g_6+g_7}\right) \tag{6.16}$$

$$\varepsilon_V = \frac{I_{B1}}{P1}\left(\frac{g_4 g_9 - g_5 g_{10}}{g_4+g_5} + \frac{g_7 g_9 - g_6 g_{10}}{g_6+g_7}\right) + I_{B1}\frac{1}{g_{18}+g_{20}}\left(\frac{g_{22} g_{12} g_{20}}{g_{11} g_{21} g_{19}} - \frac{g_{13} g_{18}}{g_{11} g_{17}}\right) \tag{6.17}$$

$$P_1 = \left(g_7 g_9 - g_7 \frac{g_7 g_9 - g_6 g_{10}}{g_6+g_7}\right) \tag{6.18}$$

With matched transconductances

$$V_X = V_{Y1} - V_{Y2} + V_{Y3} + I_X R_X \tag{6.19}$$

6.3 Relationship between currents at Z1+, Z2+ and X ports

The analysis of the portion of the circuit comprising of transistors M14 to M25 of the circuit of Fig.6.7 gives

$$I_Z = \alpha I_X + \varepsilon \tag{6.20}$$

Where

$$\alpha = \frac{1}{g_{20}+g_{18}}\left[\frac{g_{20}g_{24}}{g_{23}} + \frac{g_{15}g_{18}}{g_{14}}\right] \tag{6.21}$$

$$\varepsilon = \left(\frac{g_{22}g_{12}g_{20}\,g_{24}}{g_{19}g_{23}g_{21}g_{11}} - \frac{g_{13}g_{15}g_{18}}{g_{17}g_{11}g_{14}}\right) + \frac{1}{g_{20}+g_{18}}\left(\frac{g_{20}g_{24}}{g_{23}} + \frac{g_{15}g_{18}}{g_{14}}\right)\left(\frac{-g_{20}g_{22}g_{12}}{g_{19}g_{21}g_{11}} + \frac{g_{13}g_{18}}{g_{17}g_{11}}\right)I_{B1} \tag{6.22}$$

for matched transistors , equation (6.20) reduces to

$$I_Z = I_X \tag{6.23}$$

6.4 Relation for currents at O1, O2 ports

Assuming gate voltages of transistors M_{26} and M_{27} as V_{T1} and V_{T2} , the output currents I_{01} and I_{02} may be found respectively as

$$I_{01} = \gamma_1 V_{T1} - \gamma_2 V_{T2} + \varepsilon_2 \tag{6.24}$$

Where $$\gamma_1 = \frac{-1}{g_{26}+g_{27}}\left[\frac{g_{26}g_{27}g_{34}}{g_{28}} + \frac{g_{26}g_{27}g_{30}g_{32}}{g_{29}g_{31}}\right] \tag{6.25}$$

$$\gamma_2 = \frac{-1}{g_{26}+g_{27}}\left[\frac{g_{26}g_{27}g_{34}}{g_{28}} + \frac{g_{26}g_{27}g_{30}g_{32}}{g_{29}g_{31}}\right] \tag{6.26}$$

$$\varepsilon_2 = \frac{I_{B2}}{g_{26}+g_{27}}\left[\frac{-g_{26}g_{34}}{g_{28}} + \frac{g_{27}g_{30}g_{32}}{g_{29}g_{31}}\right] \tag{6.27}$$

and $$I_{02} = \frac{g_{42}g_{36}}{g_{38}(g_{36}+g_{27})}[g_{37}(V_{T2} - V_{G37}) + I_{B3}] + \frac{g_{40}g_{44}g_{37}}{g_{39}g_{41}(g_{36}+g_{27})}[g_{36}(V_{G37} - V_{T2}) + I_{B3}] \tag{6.28}$$

Here gate voltage of M_{27} be V_{G27} which is same as V_{G36} that is V_{T2}.

6.5 Simulation Results

PSPICE simulations have been carried out using TSMC 0.25μm CMOS process model parameters to validate the behaviour of the circuit. The supply voltages of VDD = -VSS = 1.25V and VBB = -0.8V are used. The DC transfer characteristics of the proposed DDCCCTA from Y1, Y2, Y3 terminals to X terminal are shown in the Figure 6.8(a) , 6.8 (b), figure 6.8 (c). The DC transfer characteristic for current transfer from X port to Z port is shown in figure 6.9 .The other circuit performance parameters of the DDCCCTA are summarised in Table 6.

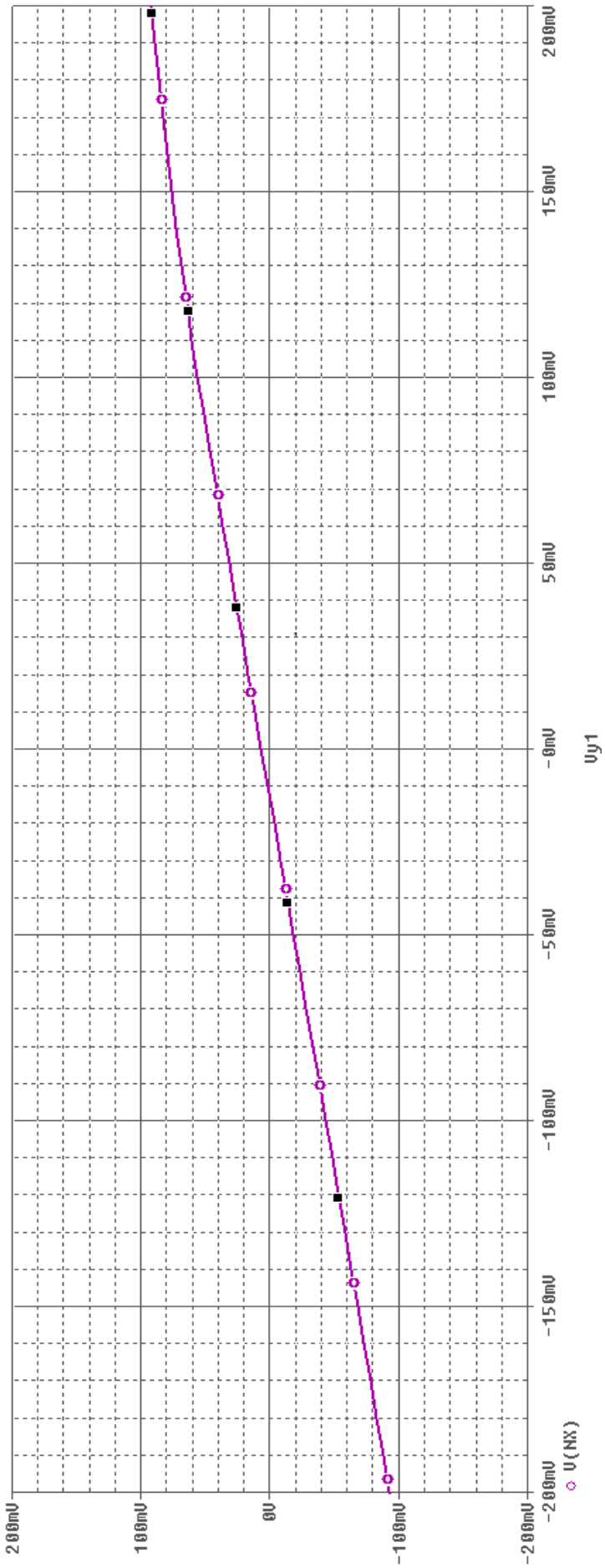


Fig. 6.8 (a) DC transfer characteristic for voltage transfer from Y1 port to X port

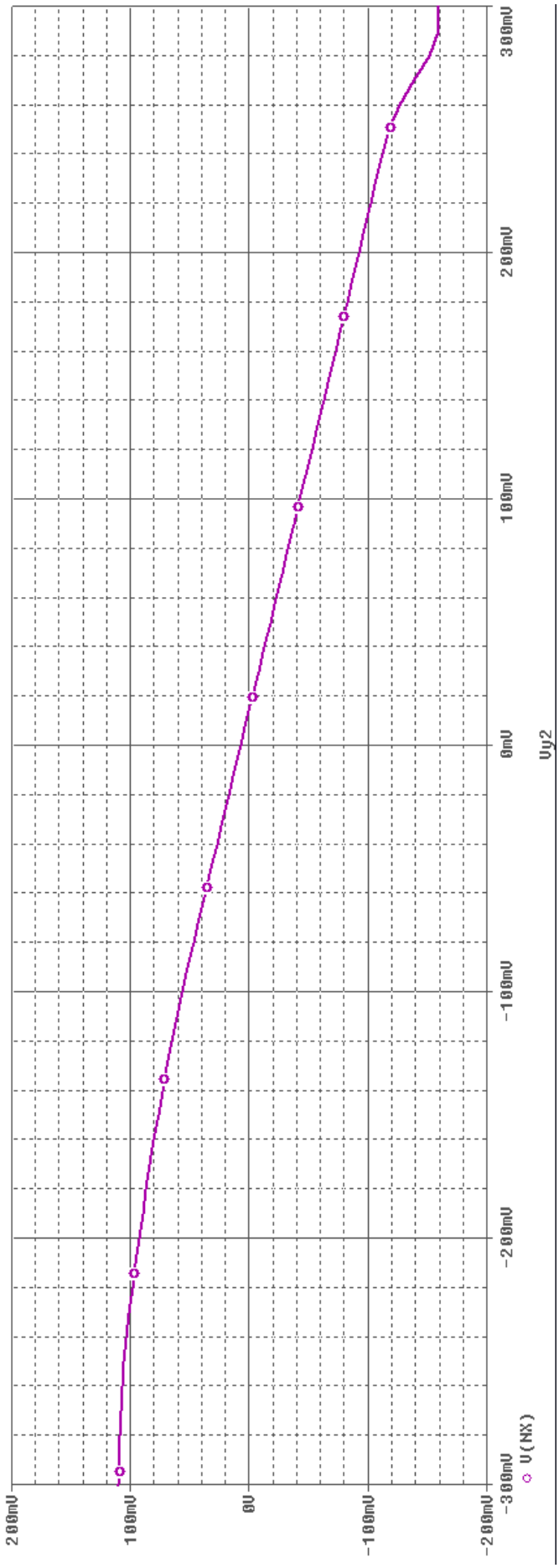


Fig. 6.8 (b) DC transfer characteristic for voltage transfer from Y2 port to X port

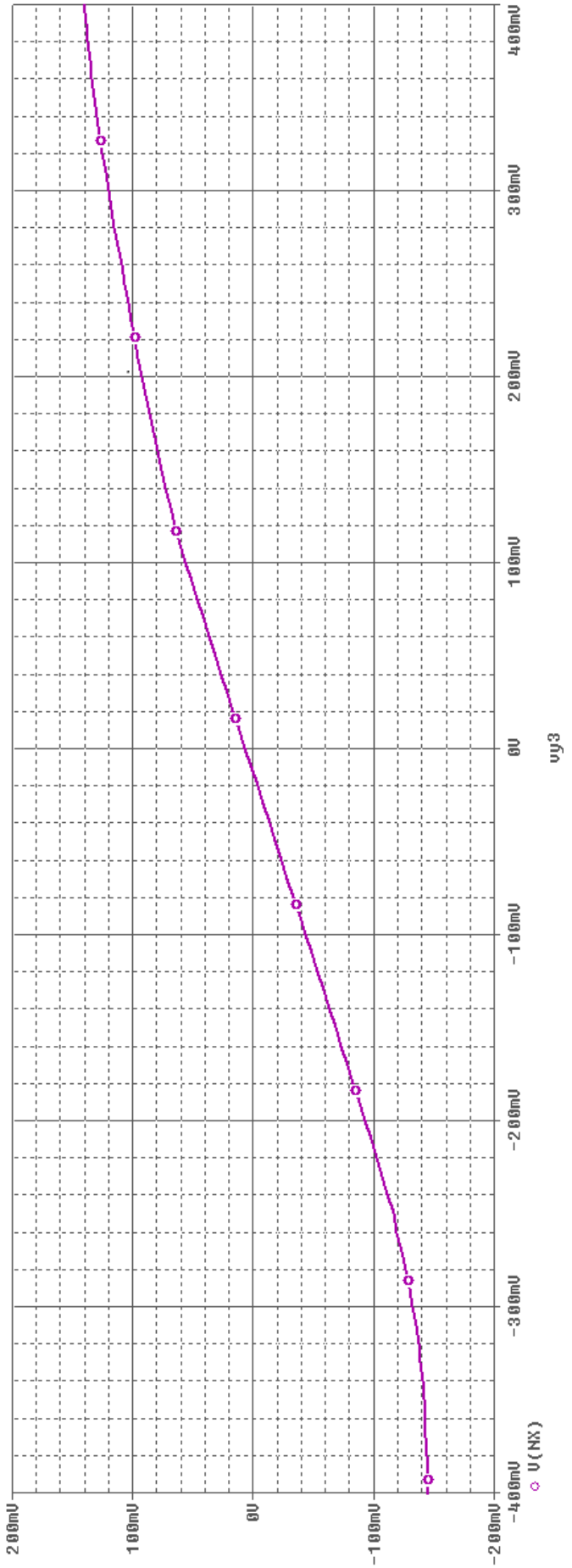


fig. 6. 8(c) DC transfer characteristic for voltage transfer from Y3 port to X port

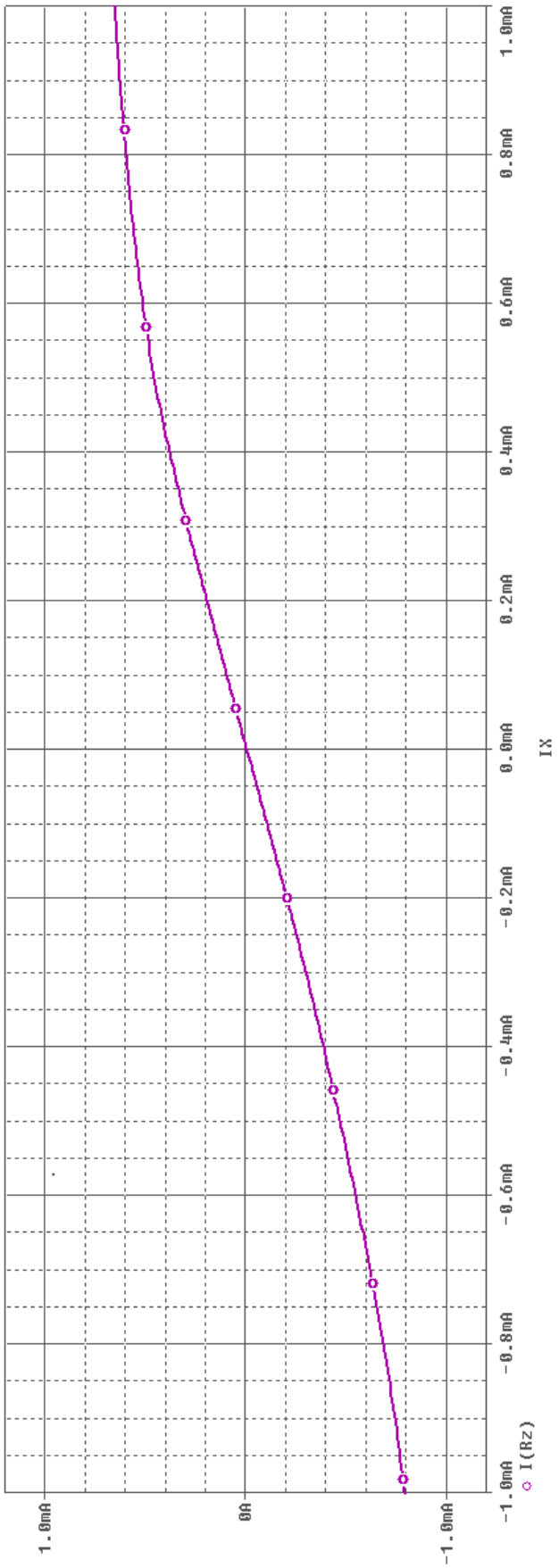


Fig. 6.9 DC transfer characteristic for current transfer from X port to Z port

Table 6. Circuit performance parameters of the DDCCCTA

input voltage linear range (voltage inputs)	-200mV to +200mV
input current linear range (current input)	-600μA to 400 μA
parasitic at Yports (R_Y, C_Y)	very high, 20fF
parasitic at Z ports (R_Z, C_Z)	220kΩ,
parasitic at O ports (R_o, C_o)	324 kΩ, 20fF
−3 dB Bandwidth (I0=100μA)	85.5 MHz for V_x/V_y
	90.75 MHz for I_z/I_x
	90 MHz for I_o/V_z

6.6 Grounded inductor using DDCCCTA

The proposed DDCCCTA may also be configured for grounded inductor simulator as shown in Fig. 6.10 . It may be noted that the gain of amplifiers and inductance can be adjusted by gm i.e. by varying bias current of DDCCTA**.**The transfer functions may be expressed as follows:

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{sCR}{g_m}$$

The circuit of inductor has been verified by carrying out PSPICE simulations using TSMC 0.25μm CMOS process model parameters. Results are shown in figure 6.11 .

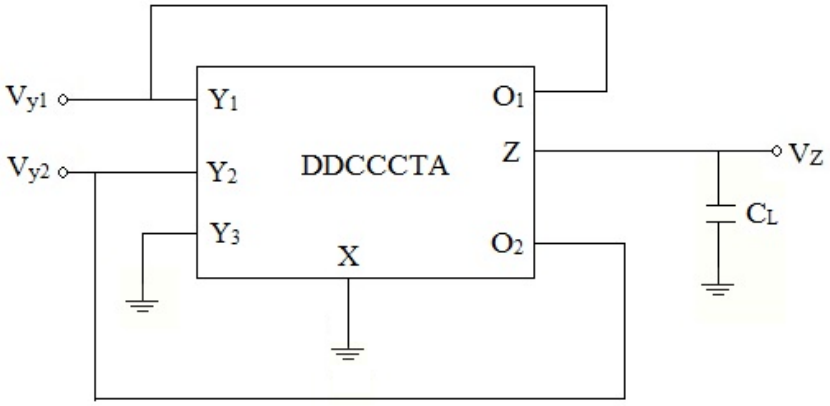


Fig. 6.10 Grounded inductor simulator

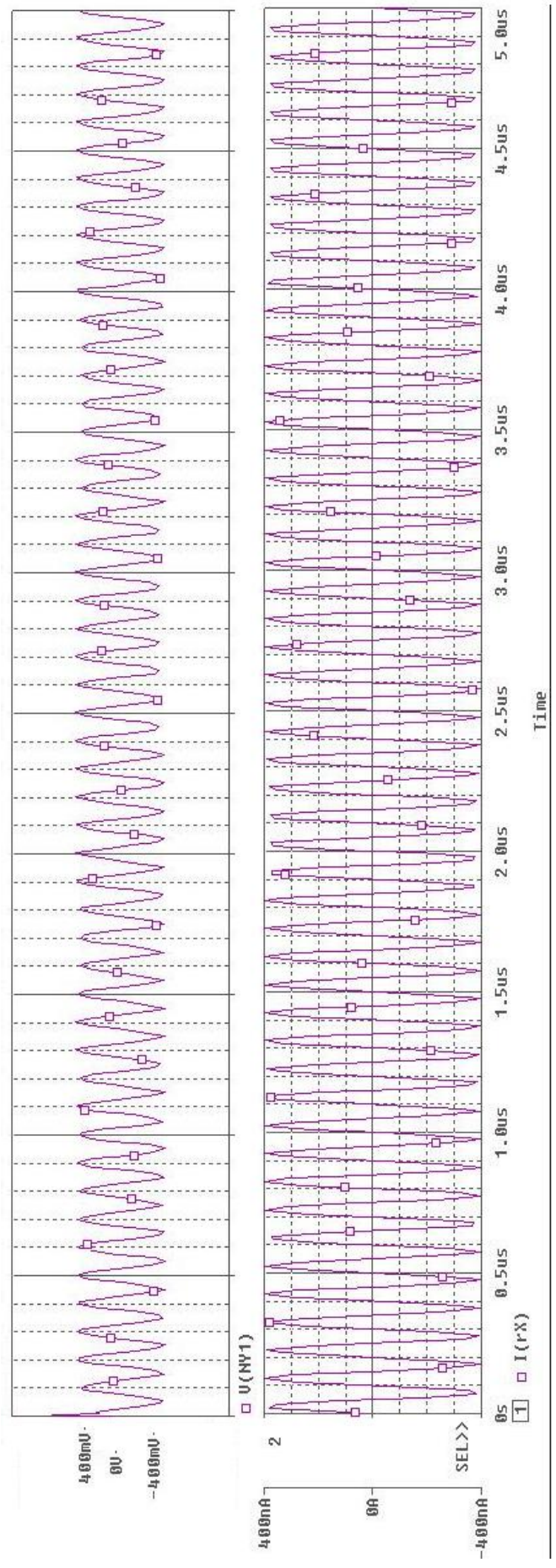


Fig. 6.11 current and voltage waveforms of the corresponding inductor

Chapter 7

Conclusion

In this thesis a detail study of differential difference current conveyor transconductance amplifier (DDCCTA) is presented in Chapter 2. Biquadratic voltage and current mode filters are realized using DDCCTA in chapter 3. Higher order filters can be easily designed using the wave method and operational simulation (leapfrog) method. DDCCTA based high order filter based on wave method is presented in chapter 4 and based on operational simulation is presented in chapter 5. In wave method DDCCTA based series inductor wave equivalent is realized as it is basic building block which is then configured for other passive element realization by making appropriate connections. The approach is verified for a 4th order low pass filter through SPICE simulation using 0.25μm CMOS technology parameters. A new active building block , differential difference current controlled conveyor transconductance amplifier (DDCCCTA) is proposed in chapter 6.

References

[1] M. Banu , Y. Tsividis : “Continuous-time MOSFET-C filters in VLSI ”,IEEE Trans., Circuit and Systems-33 ,pp. 125-139,1986.

[2] R. L. Geiger, E. Sanchez-Sinencio, “Active filter design using operational transconductance amplifiers: A tutorial,” *IEEE Circuits and Devices Magazine*, 1, pp. 20 – 23, 1985.

[3] A. S. Sedra, K. C. Smith, “A second generation current conveyor its application,” *IEEE Transactions on Circuit Theory,* 17, pp. 132-134, 1970.

[4] A. Fabre, O. Saaid , F. Wiest, C. Boucheron, “High frequency applications based on a new current controlled conveyor,” *IEEE Transactions on Circuit and Systems I,* 43, pp. 82-91, 1996.

[5] I. A. Awad, A. M. Soliman, “Inverting second generation current conveyors: the missing building blocks, CMOS realizations and applications ,” *International Journal of Electronics*, 86, 413-432, 1999.

[6] H. O. Elwan, A. M. Soliman, “Novel CMOS differential voltage current conveyor and its applications,” *IEE Proceedings - Circuits Devices Systems,* 144, 195-200, 1997.

[7] W. Chiu, S. I. Liu, H. W. Tsao, J. J. Chen, “CMOS differential difference current conveyor and their applications,” *IEE Proceedings - Circuits Devices Systems,* 143, pp. 91 – 96, 1996.

[8] C. Toumazou , A. Payne, “Current feedback opamp: A blessing in disguise?,” *IEEE Circuits and Devices Magazine,* 10, pp. 43 – 47, 1994.

[9] R. Prokop, V. Musil, “CCTA-a new modern circuit block and its internal realization,” *Proceedings of International Conference on Electronic devices and systems (IMAPSCZ),* (89–93),2005.

[10] W. Jaikla, P. Silapan, C. Chanapromma, M. Siripruchyanun, “Practical Implementation of CCTA Based on Commercial CCII and OTA,” *Proceedings of International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS2008).*

[11] M. Siripruchyanun, W. Jaikla, “Current controlled current conveyor transconductance amplifier (CCCCTA): a building block for analog signal processing,” *Electrical Engineering*, 90, pp. 443–453, 2008.

[12] Siripruchyanun M., W. Jaikla, “CMOS current-controlled current differencing transconductance amplifier and applications to analog signal processing,” *International Journal of Electronics and Communication (AEU)*, 62, pp. 277 – 287, 2008.

[13] A. Jantakun, N. Pisutthipong, M. Siripruchyanun, “A Synthesis of Temperature Insensitive/Electronically Controllable floating simulators based on DV-CCTAs,” *Proceedings of 6th International Conference on electrical engineering/ electronics, computer, telecommunications, and information technology (ECTI-CON 2009)* (560–563).

[14] W. Jaikla, M. Siripruchyanun, A. Lahiri, “Resistorless dual-mode quadrature sinusoidal oscillator using a single active building block,” *Microelectronics Journal*, doi:10.1016/j.mejo.2010.08.017 ,(2010).

[15] N. Pandey, S. K. Paul, “Differential Difference Current Conveyor Transconductance Amplifier (DDCCTA):A new analog building block for signal processing”, J*ournal of Electrical and Computer Engineering,* doi:10.1155/2011/361384, (2011).

[16] J. Hu, Y. Xia, T. Xu and H. Dong, “A New CMOS Differential Difference Current Conveyor and Its Applications,” *International Conference on Communications, Circuits and Systems*, Vol. 2, pp. 1156-1160. doi:10.1109/ICCCAS.2004.1346380,2004.

[17] W. Chiu, S. I. Liu, H.W. Tsao, and J. J. Chen, “CMOS differential difference current conveyors and their applications,” *IEE* Active and Passive Electronic Components 5 *Proceeding—Circuits Devices and Systems*, vol. 143, no. 2, pp.91–96, 1996.

[18] C.-M. Chang and H.-P. Chen, “Universal capacitor-grounded voltage-mode filter with three inputs and a single output,” *International Journal of Electronics*, vol. 90, no. 6, pp. 401–406 ,2003.

[19] J.-W. Horng, W.-Y. Chiu, and H.-Y. Wei, “Voltage-mode highpass, bandpass and lowpass filters using two DDCCs,” *International Journal of Electronics*, vol. 91, no. 8, pp. 461–464,2004.

[20] M. A. Ibrahim, H. Kuntman, and O. Cicekoglu, "Single DDCC biquads with high input impedance and minimum number of passive elements," *Analog Integrated Circuits and Signal Processing*, vol. 43, no. 1, pp. 71–79, 2005.

[21] W. Y. Chiu and J.-W. Horng, "High-input impedance voltagemode universal biquadratic filter using three plus-type CCIIs," *IEEE Transactions on Circuits and Systems II*, vol. 54, no. 8, pp. 649–652, 2007.

[22] H.-P. Chen, "Universal voltage-mode filter using only plustype DDCCs," *Analog Integrated Circuits and Signal Processing*, vol. 50, no. 2, pp. 137–139, 2007.

[23] J.-W. Horng, "High input impedance voltage-mode universal biquadratic filter with three inputs using DDCCs," *Circuits, Systems, and Signal Processing*, vol. 27, no. 4, pp. 553–562, 2008.

[24] H. P. Chen, High-Input Impedance Voltage-Mode Multifunction Filter with Four Grounded Components and Only Two Plus-Type DDCCs, Active and Passive Electronic Components Volume 2010, Article ID 362516, 5 pages doi:10.1155/2010/362516, 2010.

[25] S. Rolf, Valkenburg. Design of analog filter, *Oxford University Press*.

[26]A. Soliman, Applications of the current feedback amplifiers. *Analog Integrated Circuits and Signal Processing*, vol. 11, no. 3, p. 265-302 ,1996.

[27]H. Wupper, K.Meerkotter, New active filter synthesis based on scattering parameters. *IEEE Transactions on Circuits and Systems*, vol. 22, no. 7, p. 594-602, 1975.

[28] I. Haritantis, A. Constantinides, T. Deliyannis. Wave active filters. *IEE Proceedings*, vol. 123, no. 7, p. 676-682 ,1976.

[29] K. Georgia, P. Costas. Modular filter structures using CFOA. *Radio engineering*, vol.19, no. 4, p. 662-666 , 2010.

[30] A. Spanidou, and C. Psychalinos, Current Amplifier based Wave Filter. *IEEE Trans. Circuit Systems Signal Processing*, vol. 24, No. 3, P.303-313, 2005.

[31] N. Pandey, P. Kumar, " Differential Voltage Current Conveyor Transconductance Amplifier based Wave active filters", *Journal of Electron devices*, vol. 10, p. 429-432 , 2011 .

Appendix-B

.25µm TSMC CMOS Technology Parameter

```
.MODEL NMOS NMOS  (LEVEL = 3

+ TOX = 5.7E-9              NSUB = 1E17              GAMMA = 0.4317311
+ PHI = 0.7                 VTO = 0.4238252          DELTA = 0
+ UO = 425.6466519          ETA = 0                  THETA = 0.1754054
+ KP = 2.501048E-4          VMAX = 8.287851E4        KAPPA = 0.1686779
+ RSH = 4.062439E- 3        NFS = 1E12               TPG = 1
+ XJ = 3E- 7                LD = 3.162278E-11        WD = 1.232881E-8
+ CGDO = 6.2E-10            CGSO = 6.2E-10           CGBO = 1E- 10
+ CJ = 1.81211E-3           PB = 0.5                 MJ = 0.3282553
+ CJSW = 5.341337E-10       MJSW = 0.5 )

.MODEL PMOS PMOS (LEVEL = 3
+ TOX = 5.7E-9              NSUB = 1E17              GAMMA = 0.6348369
+ PHI = 0.7                 VTO = -0.5536085         DELTA = 0
+ UO = 250                  ETA = 0                  THETA = 0.1573195
+ KP = 5.194153E-5          VMAX = 2.295325E5        KAPPA = 0.7448494
+ RSH = 30.0776952          NFS = 1E12               TPG = - 1
+ XJ = 2E- 7                LD = 9.968346E-13        WD = 5.475113E-9
+ CGDO = 6.66E-10           CGSO = 6.66E-10          CGBO = 1E- 10
+ CJ = 1.893569E-3          PB = 0.9906013           MJ = 0.4664287
+ CJSW = 3.625544E-10       MJSW = 0.5 )
*
```