Design and Implementation of PID Controllers Using CM Building Blocks

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CERTIFICATE

This is to certify that **Mr. Rakesh Verma**, **Roll No. 06/C&I/2K10**, student of **M.Tech, Control & Instrumentation, Department of Electrical Engineering, Delhi Technological University,** has submitted the dissertation entitled **"Design and Implementation of PID Controllers Using CM Building Blocks"** under my supervision in partial fulfillment of the requirements for the award of the degree of Master of Technology in Electrical Engineering (Control & Instrumentation). This dissertation is a record of his work carried out by him under my guidance and supervision and has not been presented earlier for the award of any degree/diploma.

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Rakesh Verma
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LIST OF SYMBOLS

S.No.	Symbols	Descriptions
1	t_r	Rise Time
2	t_s	Settling Time
3	e_{ss}	Steady State Error
4	A_o	Open Loop Gain
5	α	Current Gain
6	ω_o	Cut Off Frequency (in radian/sec.)
7	β	Voltage Gain in Active Blocks
8	A_{closed}	Closed Loop Gain
9	ζ	Damping Factor
10	T	Time Constant
11	K_P	Proportional Coefficient
12	K_I	Integral Coefficient
13	K_D	Derivative Coefficient
14	g_m	Transconductance
15	Z_i	Input Impedance
16	Z_o	Output Impedance
17	V_{SS}	Source Supply Voltage
18	V_{DD}	Drain Supply Voltage
19	I_o	Bias Current
20	I_b	Bias Current

21	w.r.t.	With respect to
22	OTA	Operational Transconductance Amplifier
23	CC	Current Conveyor
24	DOCC	Dual Output Current Conveyor
25	CFA	Current Feedback Amplifier
26	CFOA	Current Feedback Operational Amplifier
27	CDBA	Current Differencing Buffer Amplifier
28	FTFN	Four Terminal Floating Nullors
29	CMOS	Complementary Metal Oxide Semiconductor
30	OA	Operational Amplifier
31	Op amp	Operational Amplifier
32	SFG	Signal Flow Graph
33	SCSM	Supply Current Sensing Method
34	VLSI	Very Large Scale Integration
35	VCO	Voltage Controlled Oscillators
36	WTA	Wideband transconductance amplifier
37	VCVS	Voltage Controlled Voltage Source
38	VCCS	Voltage Controlled Current Source

39	CCVS	Current Controlled Voltage Source
40	CCCS	Current Controlled Current Source
41	P	Proportional
42	I	Integral
43	D	Derivative

44	W/L	Transistor Aspect Ratio
45	μ_n	Mobility of NMOS
46	C_{ox}	Gate oxide capacitance per unit area
47	BJT	Bipolar Junction Transistor
48	CCCII	Second Generation Current Controlled Current Conveyor
49	$H_v(s)$	Transfer Function for Voltage Mode
50	$H_{i(s)}$	Transfer Function for current Mode
51	T_{ii}	Integral Time Constant for Current Mode
52	T_{iv}	Integral Time Constant for Voltage Mode
53	T_{di}	Derivative Time Constant for Current Mode
54	T_{dv}	Derivative Time Constant for Voltage Mode

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ABSRACT

Proportional plus Integral plus Derivative (PID) controllers are the mainstay of most of the control systems employed in different process industries. Traditional PID controllers have been implemented using the voltage mode operational amplifiers (VOA). Performance of these VOA based PID controller is limited by the performance of the traditional VOA.

In this dissertation, current mode (CM) and voltage mode (VM) analog PID controllers have been studied & implemented. The CM and VM building blocks chosen for study and implementation of the PID controllers are (i) OTA, (ii) DOCC-II, (iii) CFA and (iv) CDBA. The PID controllers have been implemented in PSPICE and closed loop performances of some prototype second order system have been studied to establish the workability of these PID controllers.

A novel fully differential current- mode PID controller has also been designed and implemented which uses a fully differential implementation of proportional, integral and differential terms.

CONTENTS

CHAPTER I

INTRODUCTION

1.1 Introduction

This dissertation presents a study on designing and implementation of PID controllers using CM/VM active building blocks. The proportional-integral-derivative (PID) controller is one of the most important control elements used in the process control industry. A PID controller is composed of three terms namely: (1) proportional, (2) integral, and (3) derivative [1]. The proportional term adjusts the speed of response of the system; the integral term adjusts the steady-state error of the system, but may introduce instability in the system while the derivative term adjusts the degree of stability of the system, but might increase errors. By carefully tuning the various gains the closed- loop performance of a system can be improved significantly.

Traditionally, voltage operational amplifiers are largely used in analogue PID controllers. These op-amps (operational amplifiers) based controller have large number of active and passive components required for tuning the performance of closed loop control system [2]. Operational amplifiers have two major limitations viz. slew rate and constant product of gain & bandwidth. In the most traditional industrial problems, requirements on the selection of active components is not necessary, it depends on the general synthesis procedures [3]- [6] to perform operations of PID controller, so reduced number of parameters are required to be tuned for the closed loop control system.

1.2 PID controllers using a new class of current mode active blocks

Generally, there are two modes to perform operations in any electronic circuit, they are: (i) voltage mode, and (ii) current mode operations. Several voltage and current mode continuous-time filters, oscillators, analog multipliers, inductance simulators and PID controllers have been developed using a new current mode active blocks in which circuits are driven by current carrying signals.

Current-mode signal processing techniques have received a wide attention due to wide bandwidth, low-voltage operation, better linearity and stability properties and simple implementations of signal operations such as addition and subtraction, and are often preferable to voltage-mode counterparts [2]. These components, such as current conveyors (CCs) [7], operational transconductance amplifiers (OTAs) [8], current feedback operational amplifiers (CFOAs) [9] and current differencing buffer amplifier (CDBAs) [10] are considered for PID applications where speed and/or large bandwidth are required.

1.3 Current mode active blocks

The building blocks used for implementation of PID controllers can be implemented in both Bipolar as well as CMOS technology. These blocks in general fall into the categories of voltage controlled voltage source (VCVS), voltage controlled current source (VCCS), current controlled voltage source (CCCS) & current controlled current source (CCVS), or many a times into a combination of more than one of these blocks. The basic design of a voltage mode or current mode building block is guided by the signal processing functions it is supposed to perform. Nevertheless certain common features which may be found in most of the CM/VM building blocks are the presence of

i. Voltage/Current differencing circuits
ii. Current source biasing arrangements
iii. Minimum number of passive components
iv. Current mirrors of different types for copying of signal currents and/or bias currents from one part of the circuit to the other part.

OTA is a differential VCCS (Voltage Controlled Current Source) in which output current is controlled by input voltage source [8] and it is characterized by transconductance (g_m). The second-generation current-conveyor [11] is a voltage-follower with input Y and output voltage terminal X, and a current-follower (or current-inverter) with a current input X and output Z. In third generation current conveyor [11], the input current flows into the Y-terminal and out from the X-terminal, it is assumed that a differential current input fed output in voltage form. A current feedback amplifier is equivalent to a plus type second-generation current conveyor with a voltage buffer [9]. The term current feedback is used because the signal entering at the feedback

node of op-amp is in the form of current signal. CDBA is a newly introduce active circuit; it is a combination of two fundamental building blocks i.e., current differencing block and voltage follower block. FTFN is a more general and flexible building block compared to other active elements. They are used to function more successfully in both voltage mode and current mode e.g., voltage mode op-amps and current conveyors.

The basic current-mode circuit of OTA configuration is obtained from a second-order integrator loop structure consisting of the loss-less integrators [8]. An implementation of the second generation current conveyor is done by using a mixed (NMOS and PMOS) translinear loop [12]. The circuit of CFOA allows almost a rail-to-rail input and output operation. The configuration of CDBA is same as that of a CMOS second-generation current conveyor (CCII) [7]. With the help of these devices several filters and oscillators are built. Generally most of these devices are made for current controlling operations in such a way that it provides a better performance by using biasing current.

1.4 Organization of the Dissertation

In chapter II, a brief study of the characteristics, implementation and applications of various CM/VM active building blocks used for synthesizing PID controller has been presented. In chapter III, PID controllers are built through a general synthesis procedure with the help of signal flow graph (SFG). In order to test these PID controllers, implementation of CM/VM PID controller are done. In chapter IV, a new fully differential PID controller is made with the help of DO-CCII. In chapter V summary of the project has been presented along with suggestions for some future work on this topic.

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CHAPTER II

CM/VM ACTIVE BUILDING BLOCKS USED FOR SYNTHESIS OF PID CONTROLLER

In the present chapter, we present a brief description of various active building blocks used for implementation of the PID controllers. Though, a very large number of active building blocks have been proposed by various research groups in recent part [1]. In the present chapter, we have studied only those active building blocks which have been directly used for PID controller implementation.

2.1 Operational Transconductance Amplifier (OTA)

2.1.1 History

In 1969, RCA produced an integrated circuit, called OTA (Operational Transconductance Amplifier) for the purpose of commercial needs. The first publications with OTA came out in 1985, when the [4] presented to the new CMOS based OTA architectures and new filter realizations.

2.1.2 Symbol and Characteristic Equation

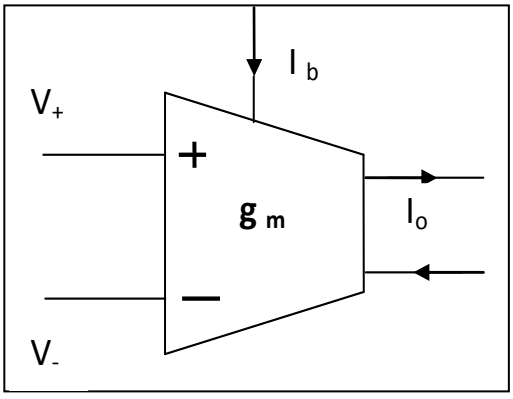

Fig. 2.1.1 OTA Block-Diagram

OTA is a differential VCCS (Voltage Controlled Current Source) in which output current is controlled by input voltage source and it is characterized by transconductance[1] (g_m). The output current of the OTA is given as follows [4]

$$I_o = g_m (V_+ - V_-),$$

where V_+ and V_- are voltages on non-inverting and inverting input terminal of OTA.

Characteristics of ideal OTA can be summarized as below

Input impedance (Z_{in}) = ∞ , Output Impedance (Z_0) = ∞ , Bandwidth = ∞ .

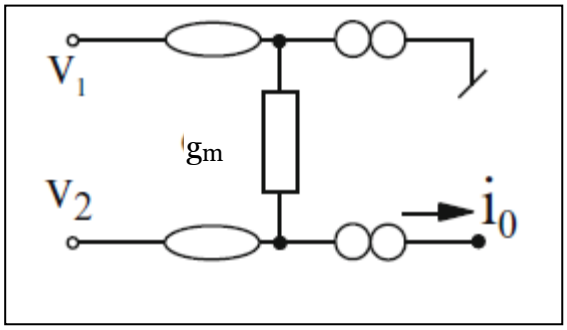

Fig. 2.1.2: Nullor model of OTA [3]

Nullor model of the OTA is given above in fig. 2.1.2 [3].

2.1.3 CMOS/Bipolar Implementation

The Operational transconductance amplifier is basically a differential voltage controlled current source and several bipolar as well as CMOS implementations have appeared in literature. In the following we present a CMOS implementation of differential input differential output OTA given in [5].The transconductance is taken as follows

$$g_m = \sqrt[2]{(\mu_n C_{ox} \frac{W}{L} I_b)}$$

[1]The term "transconductance" (g_m) comes because it is the ratio of the output current over the input voltage. Transconductance of an OTA is electronically tunable through an external DC bias voltage/ current.

Where μ_n, C_{ox}, W/L and I_b are the electron mobility of NMOS, gate oxide capacitance per unit area, transistor aspect ratio and bias current of the OTA, respectively. In above equation, it can observe that the transconductance g_m is adjustable by a supplied bias current I_b.

Fig. 2.1.3 shows the complete CMOS realization of OTA using MOS transistors [5].

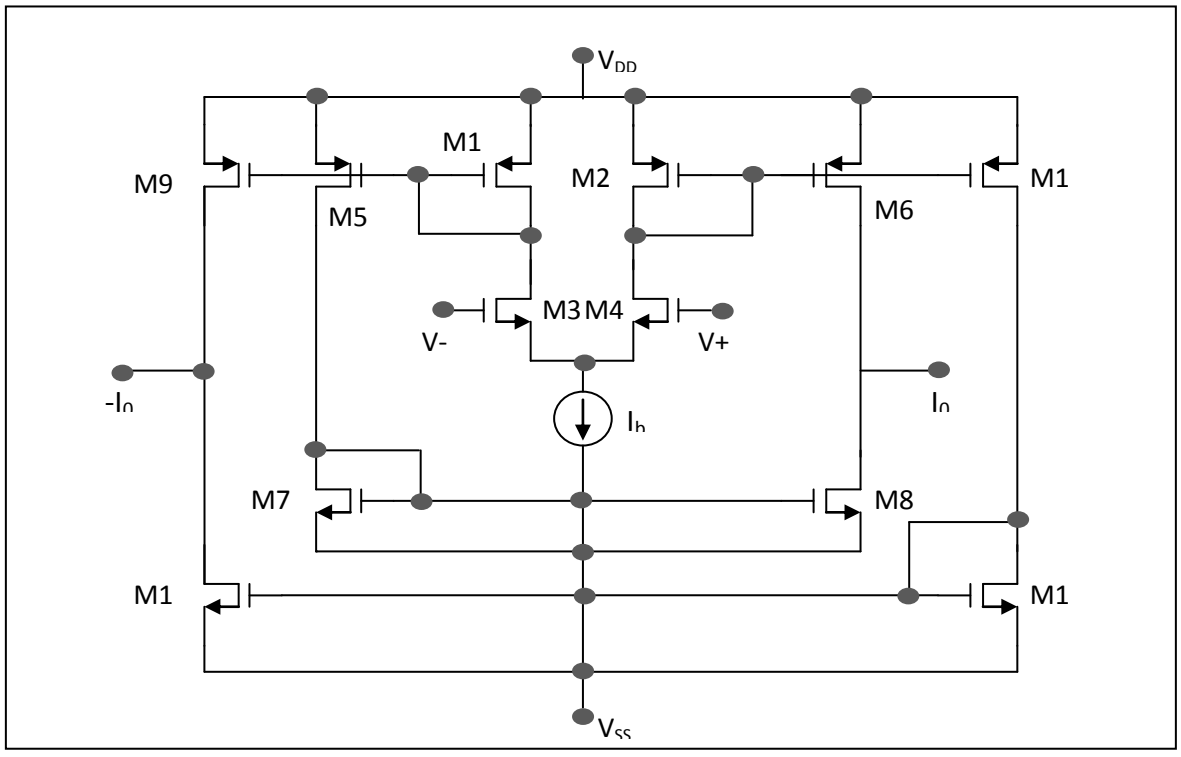

Fig. 2.1.3: CMOS realization of OTA [5]

In [5], electronically tunable multiple-mode universal biquadratic circuits are introduced using some highly linear operational transconductance amplifiers (OTAs) and grounded capacitors. For realization of higher order circuit transfer function, a second-order function of biquadratic circuit is a very useful block. The basic current-mode circuit configuration is obtained from a second-order integrator loop structure consisting of loss-less integrators. The multiple-mode biquadratic circuits are constructed with additional OTAs to the current-mode one.

2.1.4 Applications

In recent few years, OTA-C attracts more than OA (Operational Amplifier) IC, because it has several advantages e.g., it has a wider operational linear range, and this may possible with tuning of its transconductance (g_m) also, it requires just a few or even no resistors for its circuitry and in addition, it is more reliable in high frequency operations as it imposes a current mode active circuitry. OTAs, have been used for the realization of OTA-C based filters [6]-[15], oscillators [16]-[18] in battery operated equipments. Currently, OTA elements are available in the market by many manufacturers [6]. A commercially available OTA element is the circuit LT1228 (Linear Technology) or MAX435 (MAXIM-Dallas Semiconductor), which is a high-speed wideband transconductance amplifier (WTA) with high-impedance inputs and output. The OTA is popular for implementing voltage controlled oscillators (VCO) and filters (VCF) for analog music synthesizers.

2.2 Current Conveyor (CC)

2.2.1 History

Sedra and Smith introduced the first generation[2] and the second generation current conveyor[3]. The current-conveyor was presented in 1968 [23] and further developed a second-generation current-conveyor in 1970 [24]. The third generation current conveyor[4] was proposed in 1995 [25].

2.2.2 First Generation Current Conveyor (CCI)

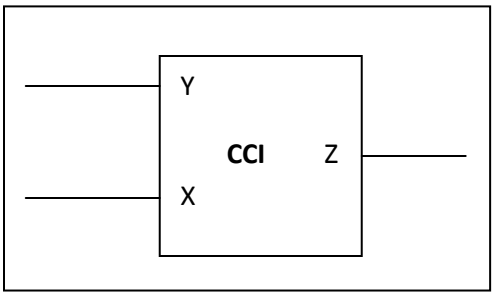

Fig. 2.2.1: Block-diagram of the first generation current-conveyor

[2, 3 & 4] are popularly known as CCI, CCII and CCIII respectively.

Current-conveyor which is characterized by a three-port network has terminals X, Y and Z, as shown in fig. 2.2.1. The first generation current-conveyor CCI has been expressed in a matrix form as follows [23]

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} . \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix}$$

The first generation current conveyor (CCI) employs both currents and voltages in ports X and Y to be equal and a replica of the currents is conveyed to the output port Z.

2.2.3 Second Generation Current Conveyor (CCII)

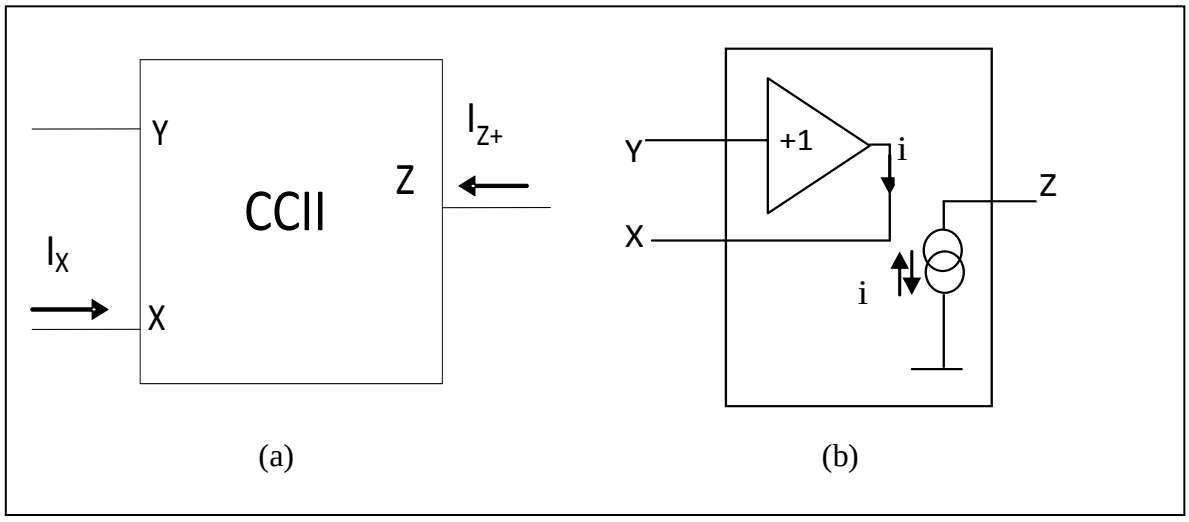

Fig. 2.2.2: CCII: (a) Block-diagram **(b)** Principle of operations: $i_{z+}=i_x$ [24]

The principle of operation of CCII+ is shown in fig. 2.2.2(b). The + sign indicates its positive gain. CCII is described in matrix form as follows [24]

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} . \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix}$$

The second-generation current-conveyor is a voltage-follower with input voltage terminal Y and output voltage terminal X, and a current-follower (or current-inverter) with a current input X and a current output Z connected together. The second generation current conveyor has a high input impedance terminal in which no current is flowing in terminal Y, so it is used in many

applications by increasing the versatility of the current conveyor-I [24]. For these reasons, the second generation current-conveyor was developed. It has one high and one low impedance input rather than the two low impedance inputs of the CCI.

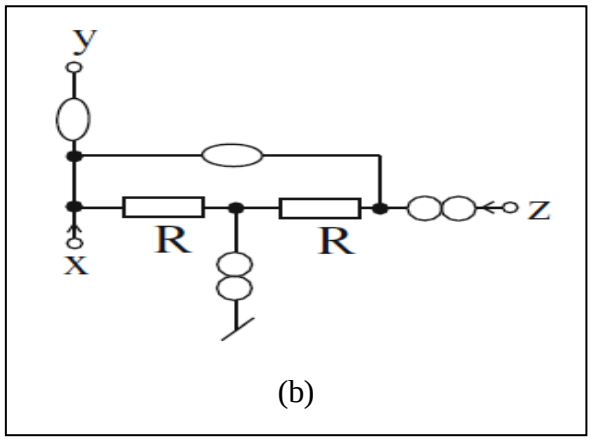

Fig. 2.2.3: Nullator-norator model of CCII [3]

CCII+ can be represented by nullators, norators and resistors; it requires two resistors in addition as shown in fig. 2.2.3 [3].

A variety of current conveyors (CCs) are implemented by Senani in [26]. The circuit configuration is shown in fig. 2.2.3-1. Here, the working applications of CCs viz. CCI+/- and CCII+/- depend on the proper connection adjustment of R_1 & R_2.

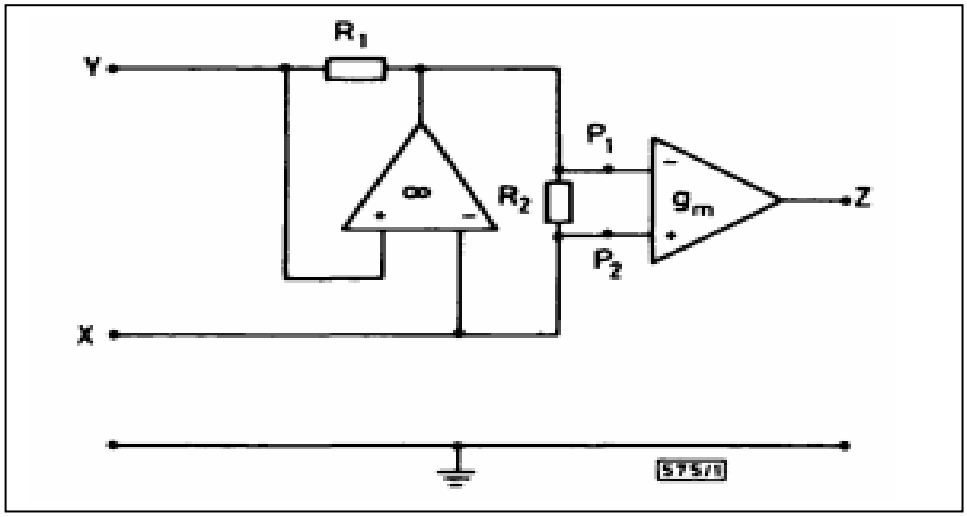

Fig. 2.2.3-1: Novel circuit implementation of four forms of current conveyor, namely CCI +, CCI-, CCll+ & CCll- based on OA and OTA [26]

2.2.4 Third Generation Current Conveyor (CCIII)

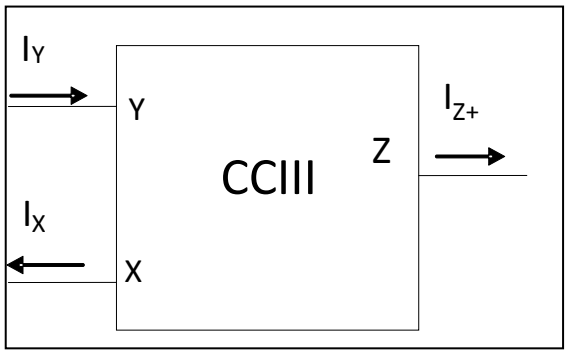

Fig. 2.2.4: Block-Diagram of CCIII

CCIII is similar to CCI except there is opposite current transfer between X and Y terminal. The third generation current-conveyor CCIII is formulated in a matrix form as follows [25]

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} . \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix}$$

The input current flows into the Y-terminal and out from the X-terminal, it is assumed that a differential current input could be realized with this amplifier. However, the CCIII has high input impedance with common-mode current signals, i.e. identical currents are fed both to terminal-Y and terminal-X.

2.2.5 Current Controlled Current Conveyor (CCCII)

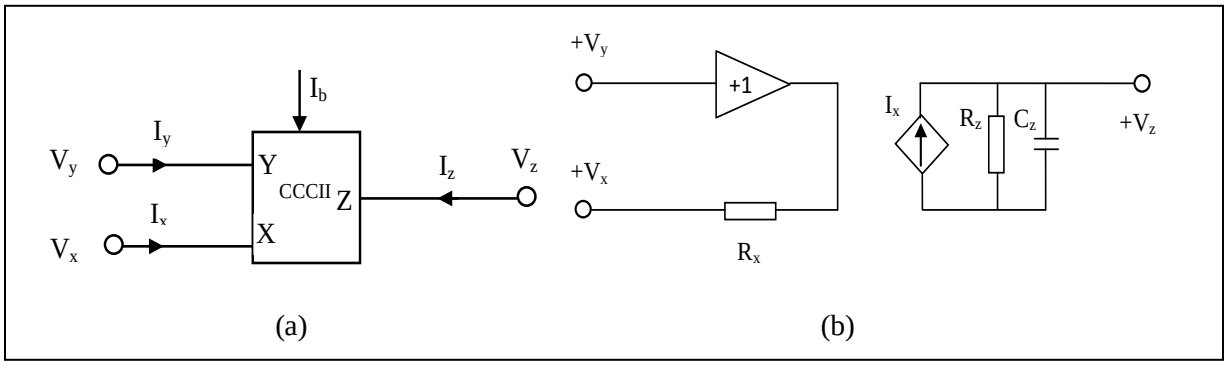

Fig. 2.2.5: (a) Symbol of CCCII (b) Equivalent circuit of CCCII

The ideal CCCII can be described as below [27]

$$I_y = 0, \qquad V_x = V_y + R_x I_x, \qquad I_z = \pm k I_x$$

where V_y & V_x are the input terminal voltages and I_y & I_x are the input terminal currents of non-inverting and inverting input nodes, respectively. V_z and I_z are the voltage and current at output terminal respectively.

The positive k denotes a positive CCCII (CCCII+) and the negative k denotes a negative CCCII (CCCII-), and k=1-ε, |ε|<<1 represents the current tracking error.

R_x is the input resistance at port X, which value is

$$R_x = \frac{V_T}{2I_b}$$

where V_T is the thermal voltage (25.8 mV at 27 °C) and I_b is the bias current of the CCCII. The equivalent circuit of CCCII is shown in fig. 2.2.5 (b), where R_x is the output resistance of the equivalent Thevenin generator seen from port X. R_z and C_z are the resistance and the capacitance of z-output, respectively.

2.2.6 Dual Output CCII/CCIII (DOCCII/DOCCIII)

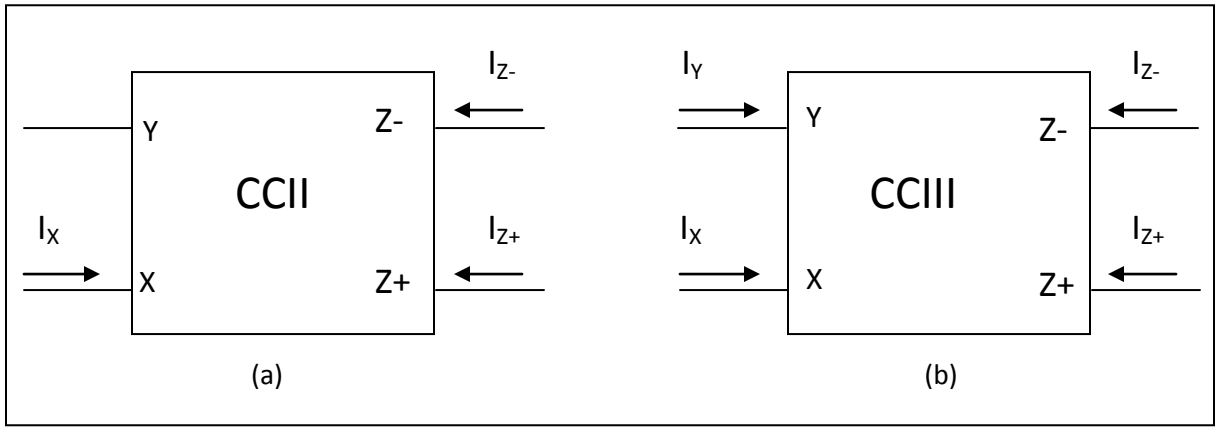

Fig. 2.2.6: Block-Diagram of (a) DOCCII (b) DOCCIII

Inputs and output terminals voltage and current relationship of DOCCII and DOCCIII are described in the following matrix form as described as bellow [28]

$$\begin{bmatrix} I_Y \\ V_X \\ I_{Z\pm} \end{bmatrix} = \begin{bmatrix} 0 & a & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} . \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix},$$

where I_{Z+} is the positive-type and I_{Z-} is the negative-type output current for both CCII± and CCIII±. For *a=0*, the circuit is called second generation current conveyor (CCII±). For *a=-1*, the circuit is called third generation current conveyor (CCIII±).

An implementation of the second generation current conveyor using a mixed (NMOS and PMOS) translinear loop is shown in fig. 2.2.6 [28], [29] & [30]. Nadhamia and Dorra proposed a multi-input multi-output filter, which contains two dual-output second-generation current conveyors (CCII±s) and one dual-output third-generation current conveyor (CCIII±) [28]. PSPICE simulations using CMOS 0.35μm technology parameters are included to demonstrate the results. Here it can be noticed that the bias current I_0 directly affects the values of parasitic resistances R_X, R_Y and R_Z.

Fig. 2.2.7 and 2.2.8 show CMOS realization of CCII and CCIII respectively, using translinear loop from [28].

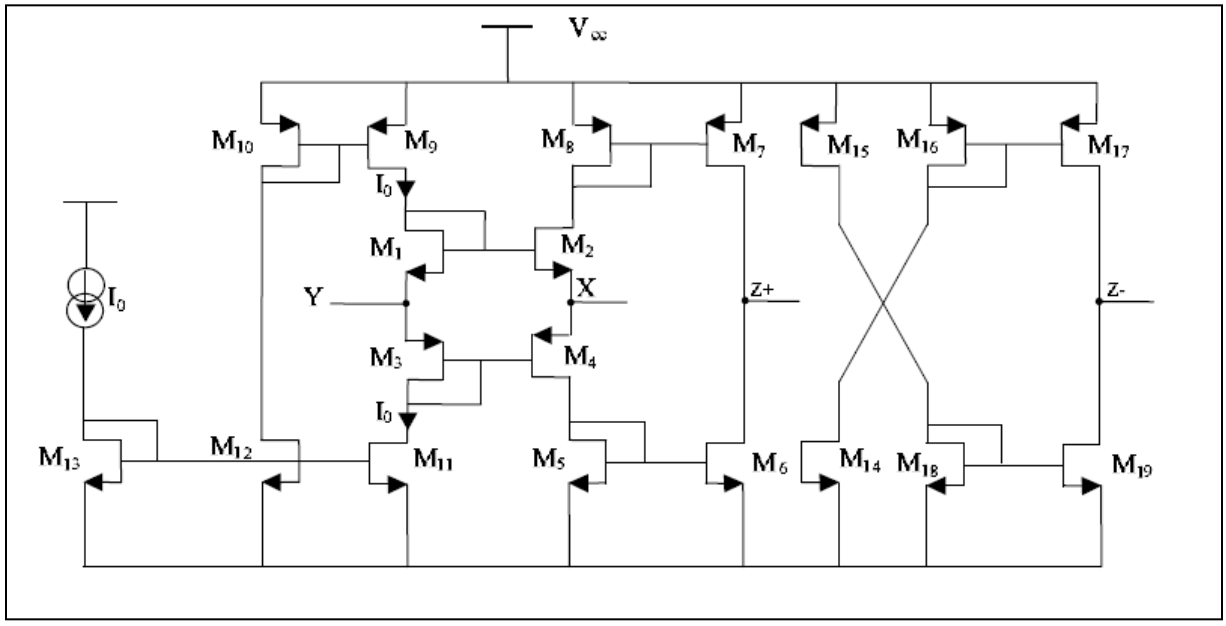

Fig. 2.2.7: CCII circuit realization using CMOS vlsi process [28]

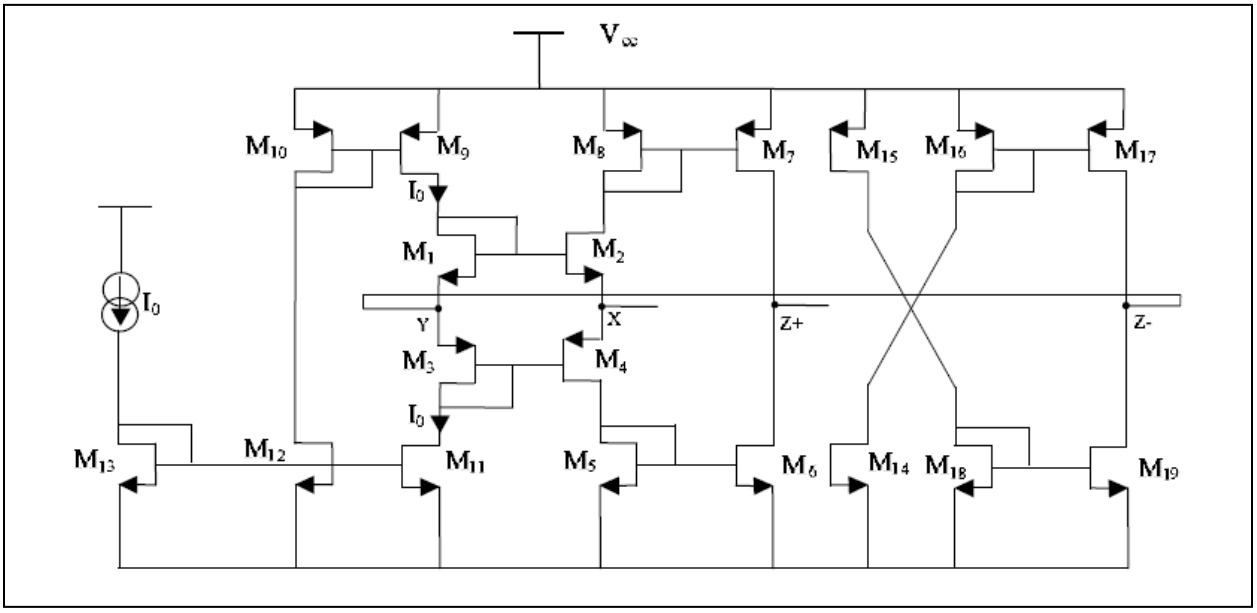

Fig. 2.2.8: CCIII circuit diagram using CMOS vlsi process [28]

2.2.7 Applications

There are several applications of current conveyor since it has greater linearity and wider bandwidth over the voltage mode counterparts, op-amps [31]. Some applications are described in [24], [31], [37]. Despite, there is a lot of research papers published in as filters realizations [39]-[50], oscillatory circuit [38] (current mode Wein model oscillator) and in some papers some mathematical operations, like multiplication/division are introduced [35], [38]. The current conveyor active block derives several bipolar/cmos implemented circuits e.g., second generation current controlled current conveyor i.e., CCCII [32], dual output current conveyor i.e., DOCCII/DOCCIII± [28], differential voltage i.e. DVCCII [32], [33], dual X current conveyor i.e., DXCC in which it has two X- terminals, these are non-inverting terminal X_p and inverting terminal X_n [34] reference cited therein.

2.3 Current Feedback Operational Amplifier (CFOA)

2.3.1 History

The CFA was invented by David Nelson at Comlinear Corporation, and first sold in 1982 as a hybrid amplifier, the CLC103. Now recently in few years, there are several CMOS realizations

for the CFOA which have been reported in the literature [52]-[58]. From beginning of the implementation of CFOA came out in existence with using only bipolar processes technology. It is well known for the current sensitivity so the techniques are intrinsically well suited to processing signals in the form of current which is given by the high bipolar junction transistor (BJT) transconductance.

2.3.2 Symbol and Characteristic equation

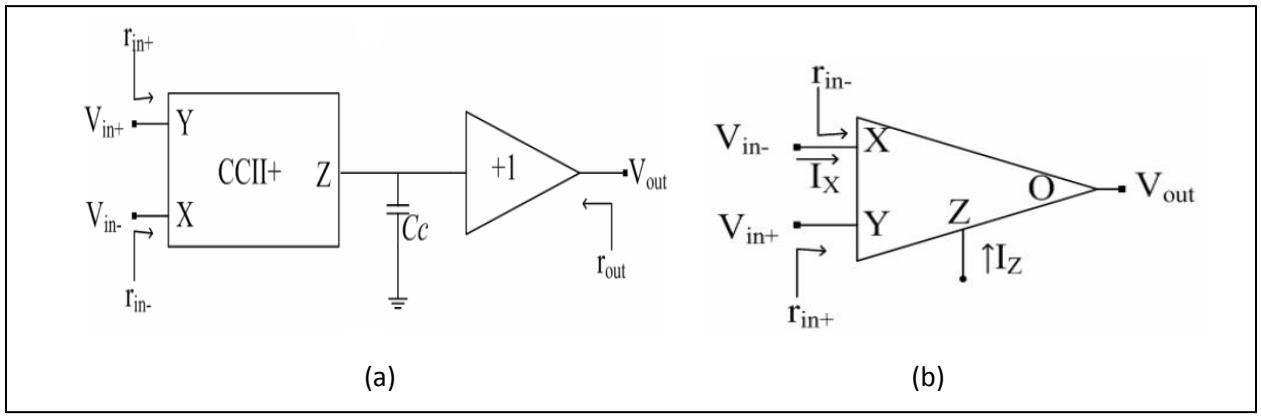

Fig. 2.3.1 (a) Equivalent Block Diagram of CFOA using current conveyor followed by a buffer

Fig. 2.3.1 (b) Schematic symbol of CFOA

CFOA can be expressed in matrix form, given as below

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \\ v_W \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_Y \\ i_X \\ v_Z \\ i_W \end{bmatrix}$$

A current feedback amplifier is equivalent to a plus type second-generation current conveyor with a voltage buffer as shown in fig. 2.3.1(a) [59]. The term current feedback is used because the signal entering at the feedback node of op-amp is in the form of current signal.

2.3.3 CMOS/Bipolar Implementation

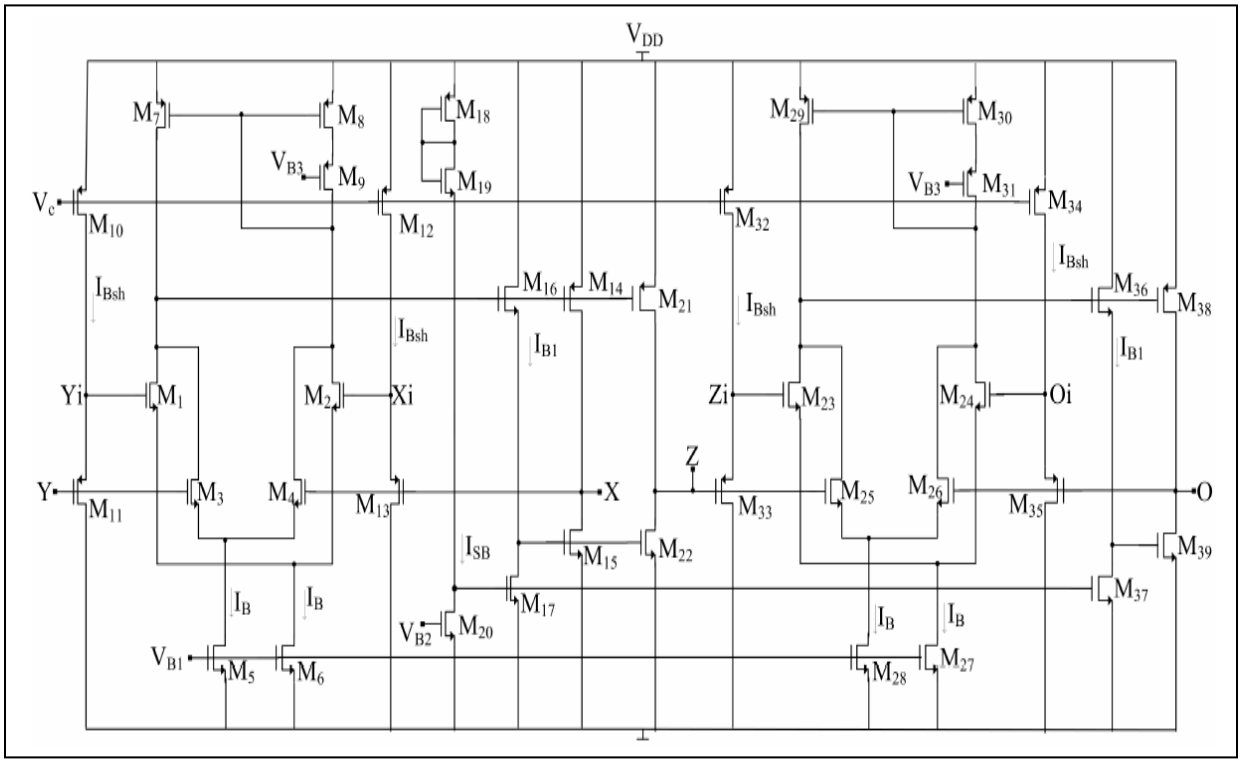

Fig. 2.3.2: CFOA circuit diagram using CMOS-bipolar technology [59]

In [59], a CMOS low-voltage current feedback operational amplifier (CFOA) is introduced. The design of this circuit is based on the MOS- transistor technology. The circuit allows almost a rail-to-rail input and output operation; also, it reduces the offset voltage and provides high driving current capabilities. The CFOA has been always seen as an extension of the CCII, therefore, the design approach was to cascade a CCII+ with a voltage follower to realize the complete circuit [60]. Fig. 2.3.2 shows the complete schematic circuit diagram of CFOA, using mos-bipolar technology.

2.3.4 Circuit Descriptions: Characteristics

The X- terminal has low input impedance since the input stage of CFOA is a voltage follower. Transistors (M14-M20) designed to provide a buffering action with a rail-to-rail swing capability. Transistors M14 and M15 form the push pull output stage at the X terminal, so that they reduce the power dissipation in fig. 2.3.2. To prevent the cross over distortion, both transistors M14 and M15 must be ON when no current is withdrawn from the X terminal

(standby mode), this current should be small and controllable. This is achieved by using a suitable gate voltage of M20, which sets the voltage level shift between the gates of M14 and M15. The standby power consumption of the overall circuit for dual power supply is given by:

$$P_{SB} = 2V_{DD}(4I_{SB} + 4I_B + 4I_{Bsh} + 2I_{B1})$$

In above equation, this is observed that power consumption can be reduced by varying I_{B1} as shown in fig. 2.3.2 and this current can be kept small by choosing small aspect ratio for transistors (M16 and M17). The proposed CFOA has a lot of advantages; the class AB output stage enables the circuit to drive the heavy resistive and capacitive load with low standby power dissipation and no slewing. There is important point that smaller miller compensation capacitors can be connected between the gate and drain of transistors M14 and M21 to ensure good transient response under all loads.

$$I_{M1} + I_{M3} = I_{M2} + I_{M4}$$

Since, transistors M7 and M8 force transistors M1 and M3 to equal currents in transistors M2 and M4. From above relation, the matched differential pair transistors are carrying equal currents. Therefore, it can be seen that,

$$V_X = V_Y$$

In Fig. 2.3.2, it can be seen that, transistors (M21, M22) are used to build a current follower stage. They are conveyed the X terminal current into the Z terminal current. Therefore,

$$I_Z = I_X$$

Finally, transistors M23 to M39 build a buffer between the Z and O terminals. It is similar to the buffer between the Y and X terminals. This buffer yields,

$$V_O = V_Z$$

Terminal-Y and terminal-X represent the non-inverting and inverting input terminals. Terminal-Z controls current in such a way producing equal voltage on terminal-W. The CFOA is capable to reduce the power dissipation and it can operate under a minimum supply voltage of ($|V_{Tp}| + V_{Tn} + V_{DS,sat}$) [59]. It has also a high current drive capability and good power conversion

efficiency since it adds a new circuit design including a class AB output stage. In [59], also remarks one of things that a rail to rail input and output voltage operation is also achieved.

2.3.5 Applications

One of the most popular CFOA namely, the AD844 from Analog Devices, is a 4-terminal building block. There is a growing interest employing CFOAs for the realization of active filters, immittance simulators, single frequency as well as single element controlled variable frequency sinusoidal oscillators and single/multiphase oscillators using CFOA pole. Recently, several current conveyor based and CFOA based [61], [62]–[64] oscillators are proposed in the literature.

2.4 Current Differencing Buffered Amplifier (CDBA)

2.4.1 History

The current differencing buffered amplifier is initially introduced by Acar and Ozoguz [65]. It is a newly introduce active circuit that is a combination of two fundamental building blocks i.e., current differencing block and voltage follower block.

2.4.2 Symbol and Characteristic Equation

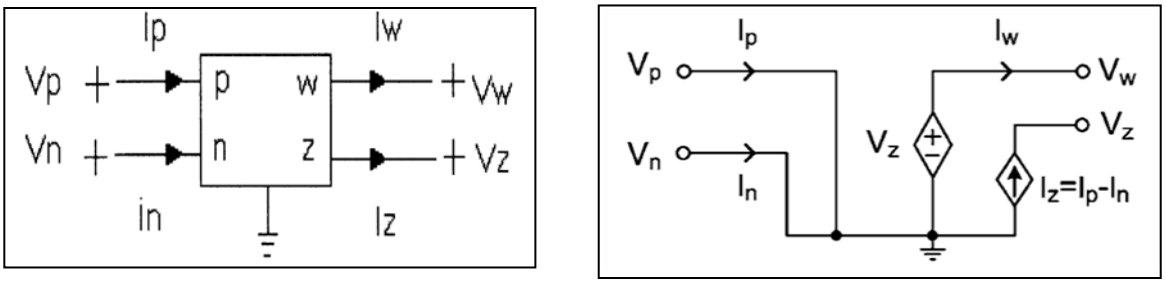

Fig. 2.4.1: (a) CDBA Block- Diagram (b) CDBA equivalent circuit [65]

It is a four terminal device; input terminals are assigned with p and n-terminal, and output terminals are assigned with w and z-terminal. The p-terminal shows, its non-inverting terminal and the n-terminal shows, its inverting terminal. The block-diagram of CDBA is shown in the

fig. 2.4.1 (a). CDBA equivalent circuit is shown in the fig. 2.4.1 (b.). It describes the conversion of the difference of input currents to the output voltage.

It can operate in both current-mode as well as voltage-mode, which provide flexibility and enable to have a variety of circuit design. Moreover, it is free from many parasitic capacitances and appropriate for high frequency operation.

The circuit can be described as under in matrix form,

$$\begin{bmatrix} I_z \\ V_w \\ V_p \\ V_n \end{bmatrix} = \begin{bmatrix} 0 & 0 & \alpha_p & -\alpha_n \\ \beta & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_z \\ I_w \\ I_p \\ I_n \end{bmatrix}$$

Where current gains assigned by α_p & α_n and voltage gain β are ideally equal to one. Here, p and n-terminals are internally grounded.

The CDBA can be considered as a transimpedance amplifier that converts the difference of input currents I_p and I_n at the terminals p and n, respectively, into the output voltage V_w at the terminal w through an impedance connected at the terminal z.

Here, p and n terminals have ideally zero impedance and the current output at terminal-z which has ideally infinite impedance. Moreover, the voltage of terminal-w follows that of terminal-z. Hence, terminal-w is the voltage output that should have zero impedance.

2.4.3 CMOS/Bipolar Implementation

In [66], Keskin and Hancioglu presented a current mode multi function using two CDBAs. In this paper they realized CDBA with the help of CMOS- bipolar technology.

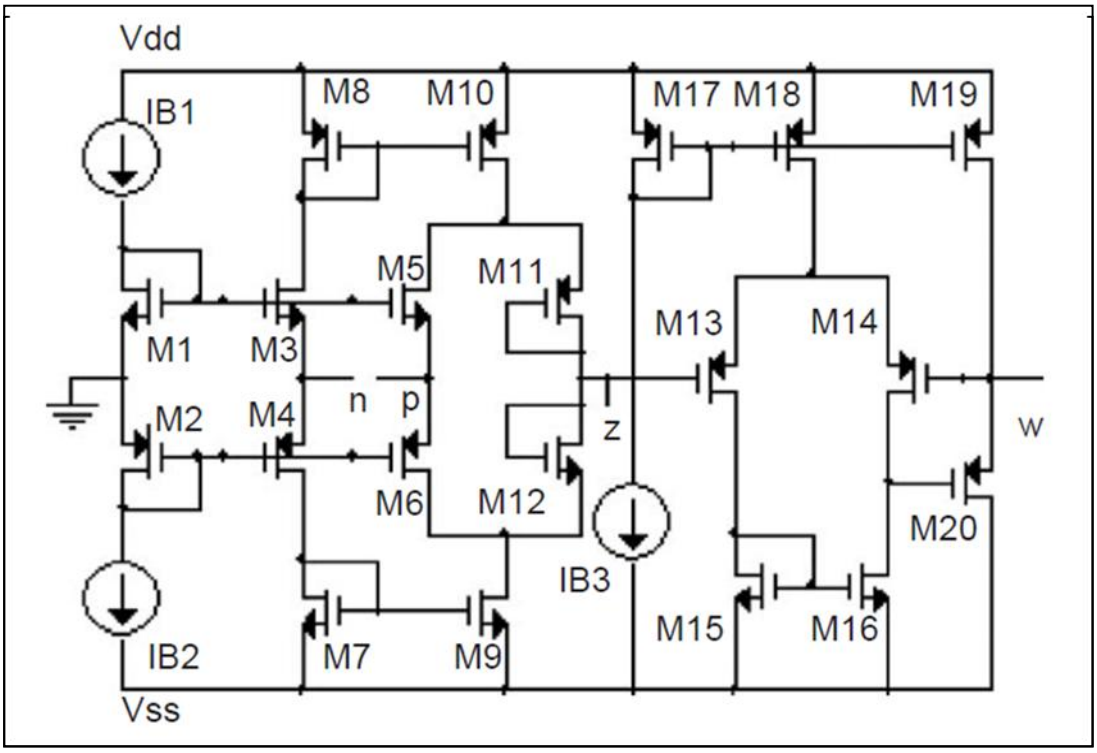

Fig. 2.4.2: CMOS realization of CDBA [66]

The CDBA used in this design is realized with CMOS technology using the topology illustrated in fig. 2.4.2 with supply voltages of $V_{DD} = 2.5V$ and $V_{SS} = -2.5\ V$ and biasing currents of $I_{B1}=I_{B2}=I_{B3} = 30\mu A$. Fig. 2.4.2 shows the complete schematic of proposed CDBA, which is based on the use of current differencing circuit (M1-M12) and the voltage buffer circuit (M13-M20). The circuit simulation is done using 0.5µ MIETEC level- 3 real transistor model parameters for all transistors in the circuit.

2.5 Conclusion

In this chapter, history, characteristics, applications and CMOS/bipolar implementation of the current mode active building blocks used for implementation of PID controllers are briefly discussed. The devices described are

(i) OTA-C

(ii) DOCCII

(iii)CFOA

(iv)CDBA.

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CHAPTER III

DESIGN AND IMPLEMENTATION OF SINGLE ENDED PID CONTROLLER

3.0 Introduction

In the present chapter, we present a review of the design of single ended PID controllers using current mode/voltage mode active building blocks. These controllers have been designed, based on the signal flow graph of a PID controller given in [2]-[5]. The current mode/voltage mode active building blocks used are OTA, CCCII, CFA and CDBA. The terminal equations characterizing these blocks have been used for designing a single ended PID controller. Detailed simulation results for OTA and DOCCII-based PID controllers are also presented.

3.1 Traditional PID controller design based on operational-amplifier

Before we present the detailed design and simulation results of the single ended PID controllers based on other devices it is worthwhile to have a look at the traditional op-amp based PID controller which is presented in fig. 3.1.1[1].

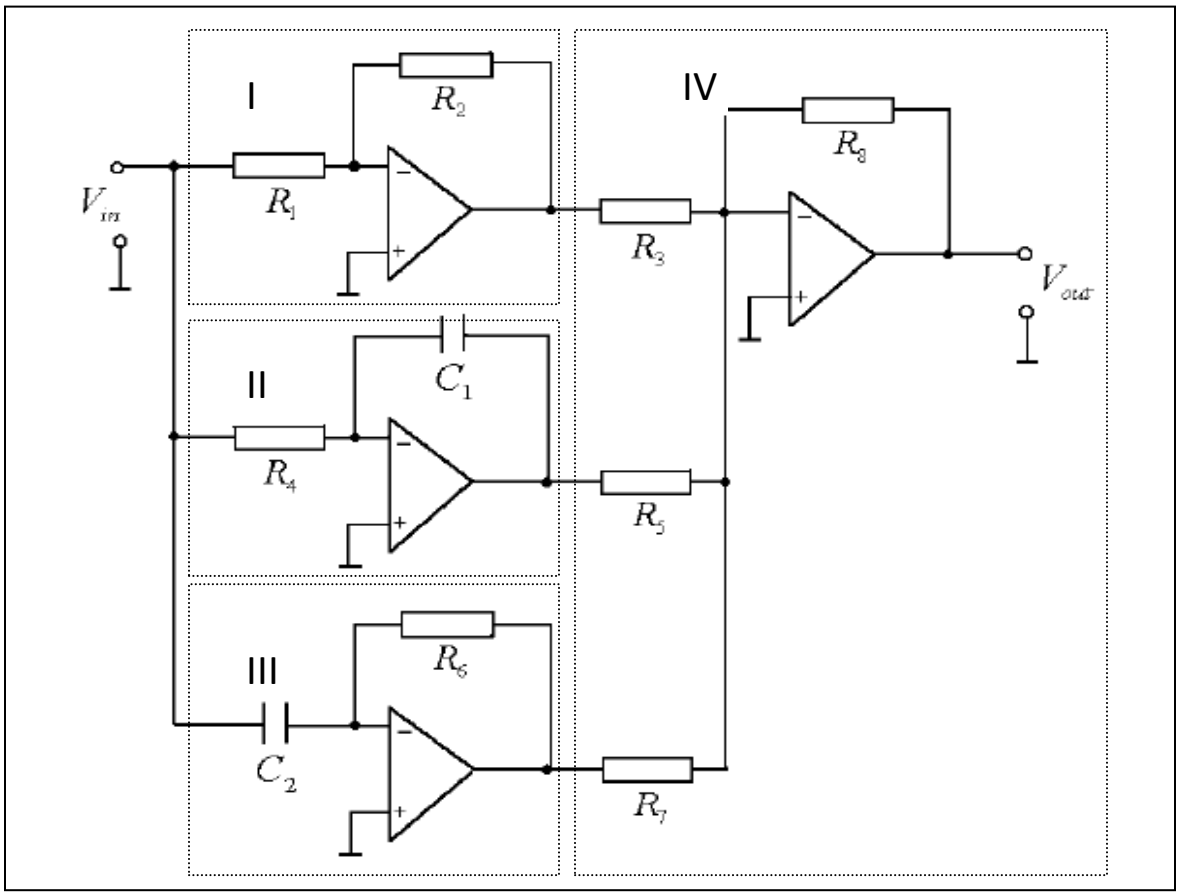

Fig. 3.1.1: Traditional PID controller constructed with op-amps

In this figure, P, I, D and summer operations are recognized by I, II, III and IV respectively. It can be seen that the circuit employs four op-amps and ten floating passive elements.

The transfer function of a PID controller can be written as follows (given in [1])

$$\frac{V_O(s)}{V_I(s)} = K_P + \frac{K_I}{s} + sK_D = \frac{K_D s^2 + K_P s + K_I}{s}$$

Here,

Proportional constant,

$$K_p = \frac{R_2 R_8}{R_1 R_3}$$

Integral constant,

$$K_I = \frac{R_8}{C_1 R_4 R_5}$$

Derivative constant,

$$K_D = \frac{R_6 C_2 R_8}{R_7}$$

The signal flow graph representation of above equation is given in fig. 3.1.2 which is consisting of the sub-graphs for proportional, integral and derivative parts of the controllers.

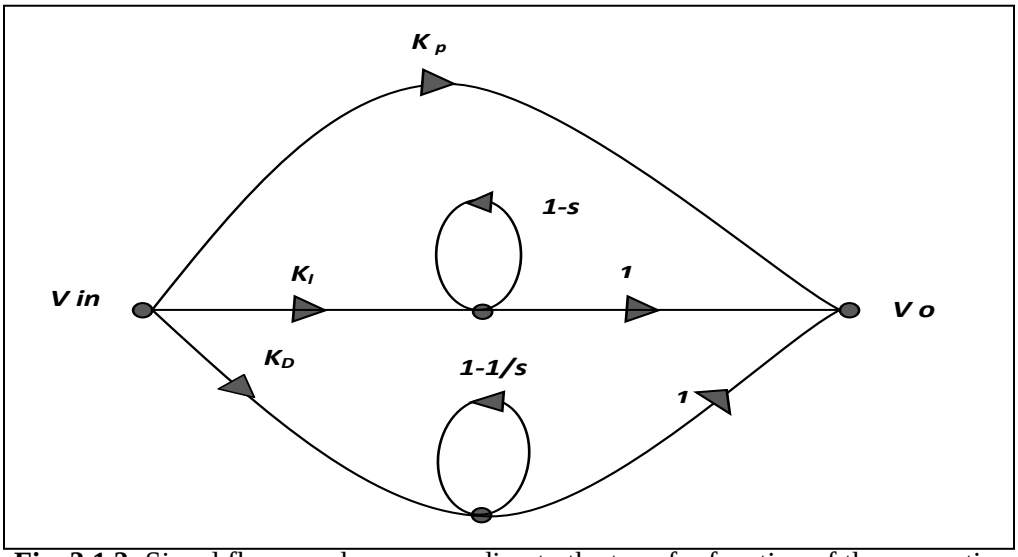

Fig. 3.1.2: Signal flow graph corresponding to the transfer function of the proportional-integral-derivative (PID) Controller

3.2 OTA-C based PID controller

Based on the signal flow graph shown in fig. 3.1.2, the subgraphs and their corresponding blocks, using OTA-Cs are shown in following fig. 3.2.1 [2]. The circuit details of OTA-C are discussed in chapter 2. With the help of characteristics of the OTA-C circuit (defined in chapter 2), a voltage mode integrator is shown in fig. 3.2.1(a) and a voltage mode differentiator containing an inductor is shown in fig. 3.2.1(b), which is used for the realization of differentiator circuit as given in fig. 3.2.1(c). A summer circuit can be represented as shown in fig. 3.2.1(d) [2].

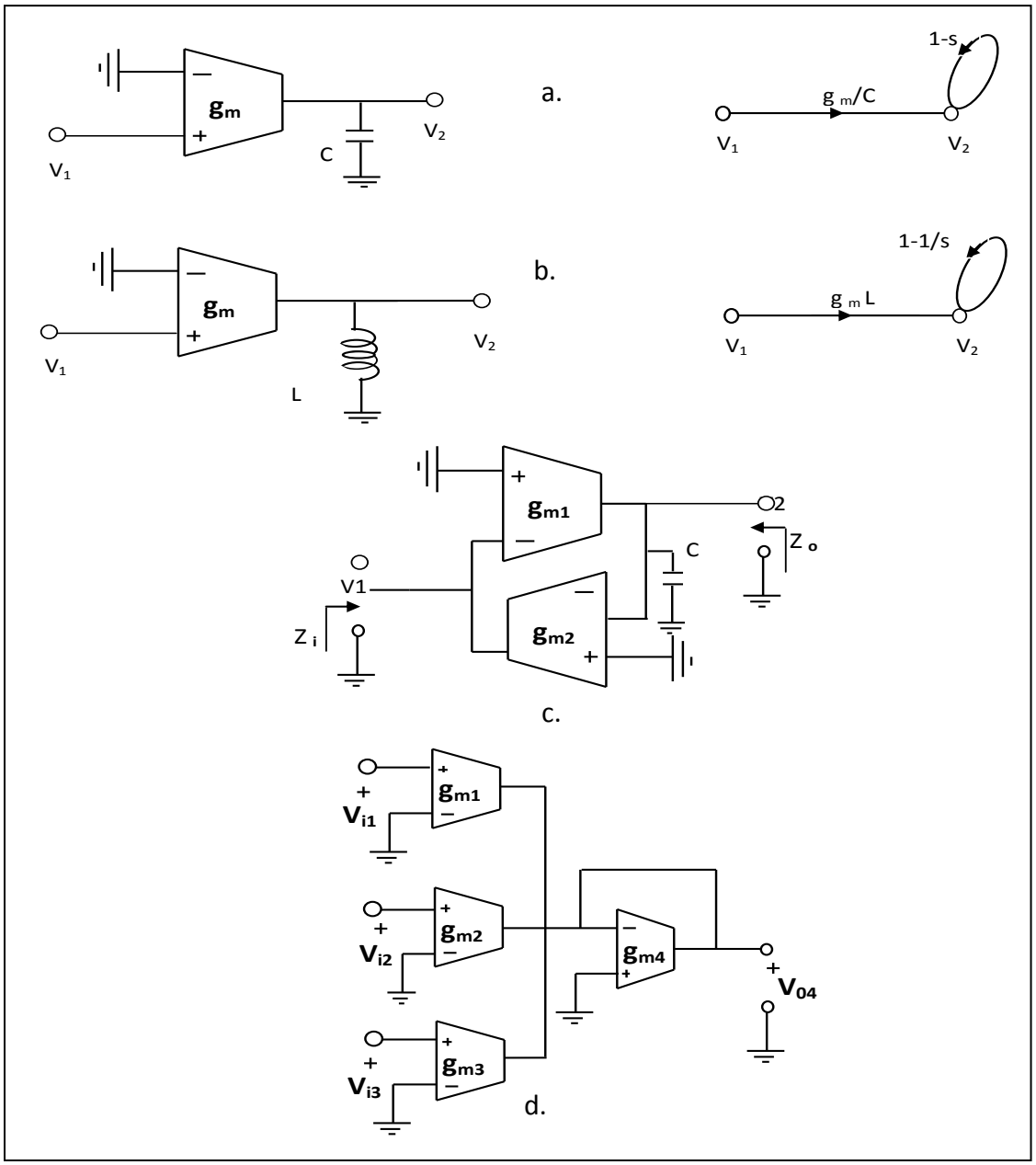

Fig. 3.2.1: Basic building blocks using OTAs and grounded capacitors together with corresponding signal flow graphs (a) Integrator circuit (b) Derivative circuit (c) Inductance element (d) Summing circuit

In fig. 3.2.1(c), OTA-C based gyrator circuit gives input impedance

$$Z_i = 1/g_{m1}g_{m2}Z_o = sC/g_{m1}g_{m2}$$

From above equation, it can be observed that Z_i is proportional to s, so this circuit behaves as an inductor. This inductance and the OTA build a derivative circuit. The capacitor C, together with the OTA (see fig. 3.2.1(a.)) forms the integration circuit. The OTAs, shown in above fig. 3.2.1(d), form the weighted summing circuit.

Connecting all these sub-circuits as shown in above fig. 3.2.1, into a single block as shown in fig. 3.2.2, performs the operation of a PID controller.

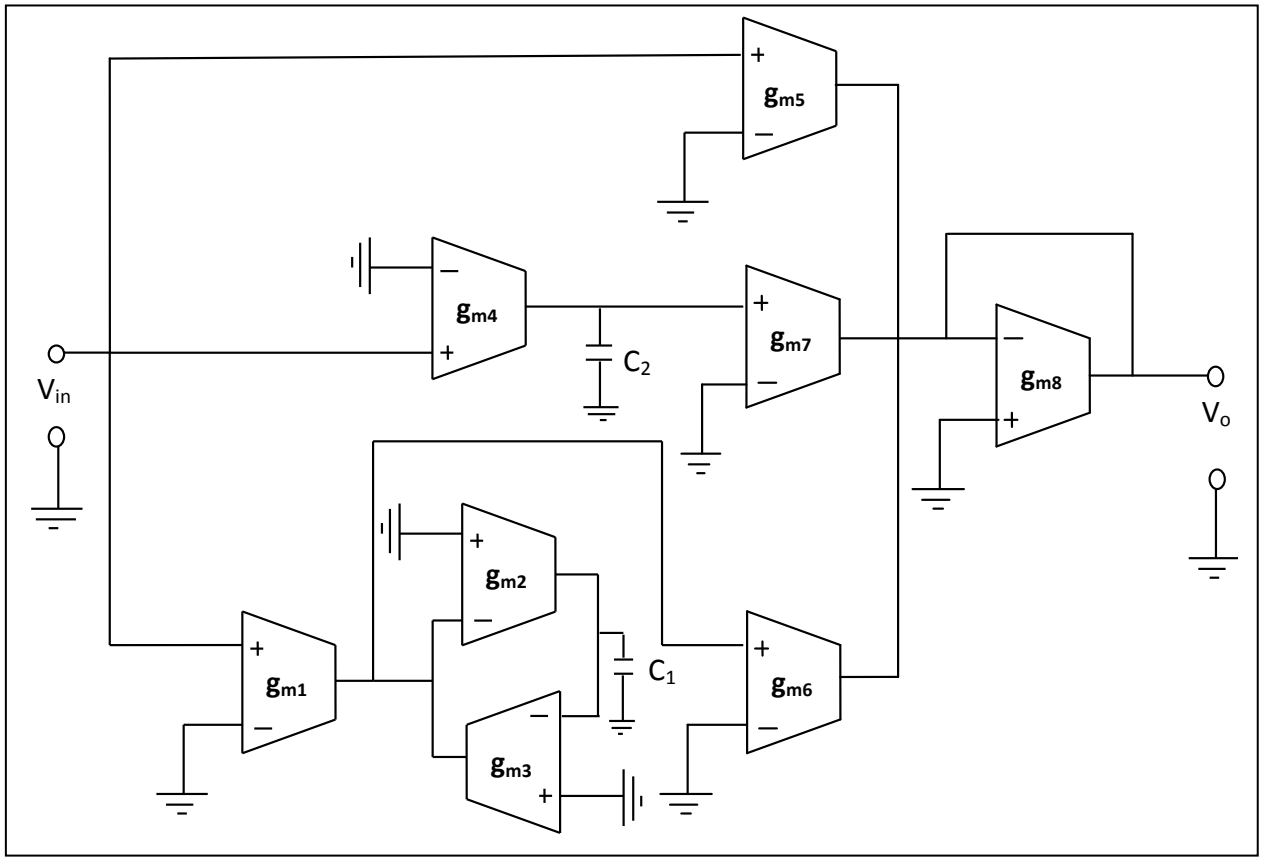

Fig. 3.2.2: An OTA-C based proportional-integral-derivative (PID) controller realization from [2] corresponding to the signal flow graph in Fig. 3.1.2.

In fig. 3.2.2, the derivative circuit is configured by simulation of gyrator which is introduced by connecting two OTAs g_{m2} and g_{m3}, together with the capacitor C1 shown in fig. 3.2.2. The capacitor C2 and OTA g_{m4} form the integration circuit. The OTAs g_{m5}, g_{m6}, g_{m7} and g_{m8} form the weighted summing circuit. OTAs g_{m5} and g_{m8} form the proportional gain.

$$K_P = g_{m5}/g_{m8}$$

$$K_I = \frac{g_{m4}}{C_2}\frac{g_{m7}}{g_{m8}}$$

$$K_D = \frac{g_{m1}C_1}{g_{m2}g_{m3}}\frac{g_{m6}}{g_{m8}}$$

The controller gain can be assigned to the prescribed values by adjusting OTAs' transconductances, g_{mi}; i = (1- 8), by DC control voltages.

3. 3 Current-Controlled Conveyor based PID controller

Based on the signal flow graph as shown in fig. 3.1.2, the subgraphs and their corresponding blocks using current controlled current conveyors (CCCIIs) are shown in following fig. 3.3.1 [3]. The circuit details of CCCII are discussed in chapter 2. In fig. 3.3.1(a), block-diagram and signal flow graph of an amplifier circuit is shown. Fig. 3.3.1(b) and 3.3.1(c) represent the signal flow graphs and blocks of an integration circuit and of a derivative circuit, respectively. From the fig. 3.3.1(c), the value of derivative time constant is equal to L/R_x where Inductance L is realized through a routine analysis [3] and it gives the value of impedance for inductance simulation

$$Z_i = sR_{X1}R_{X2}C_D$$

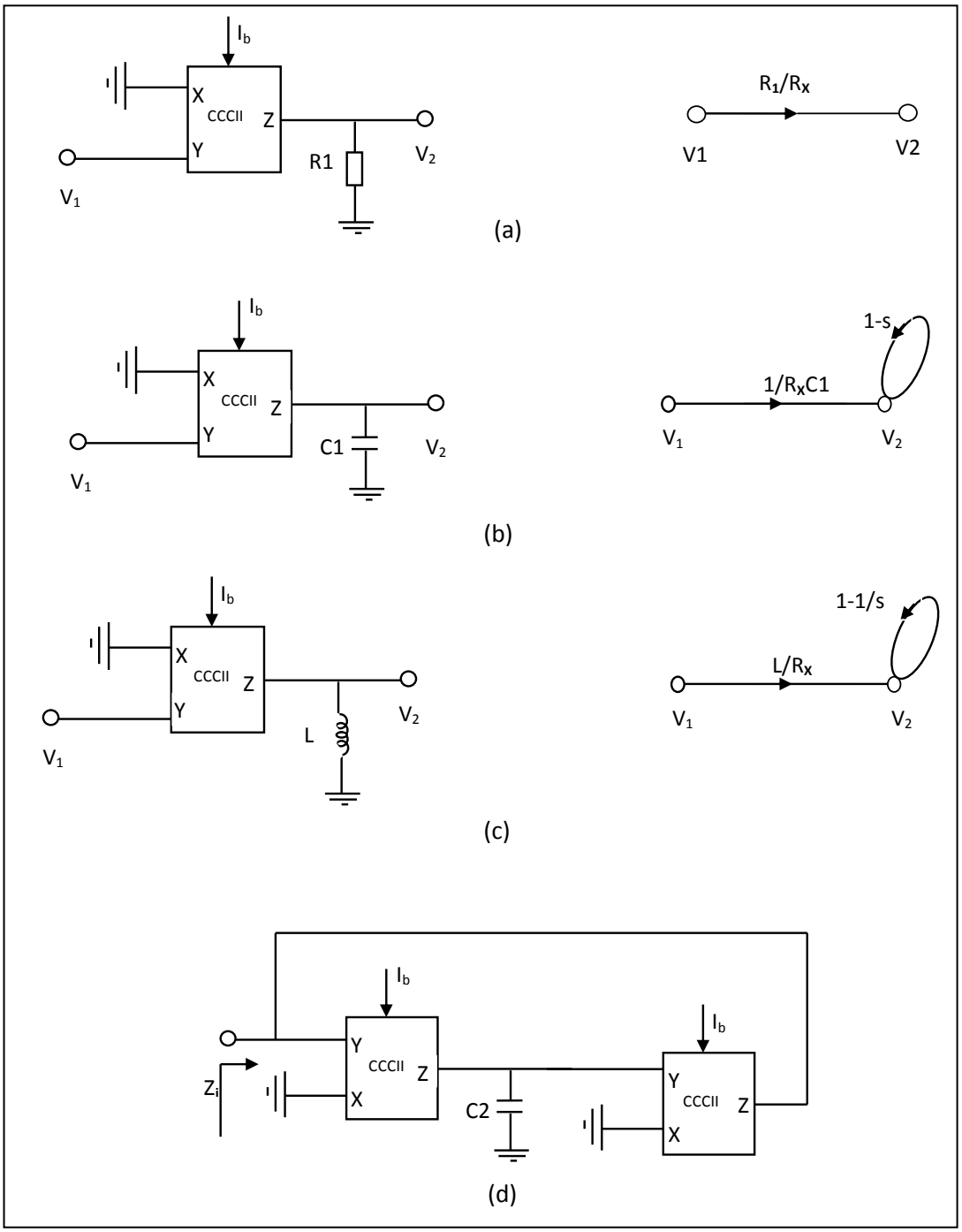

Fig. 3.3.1: Sub-graphs and corresponding active sub-circuits involve CCCII (a) Amplifier, (b) integrator, (c) derivative circuit, (d) inductance simulation

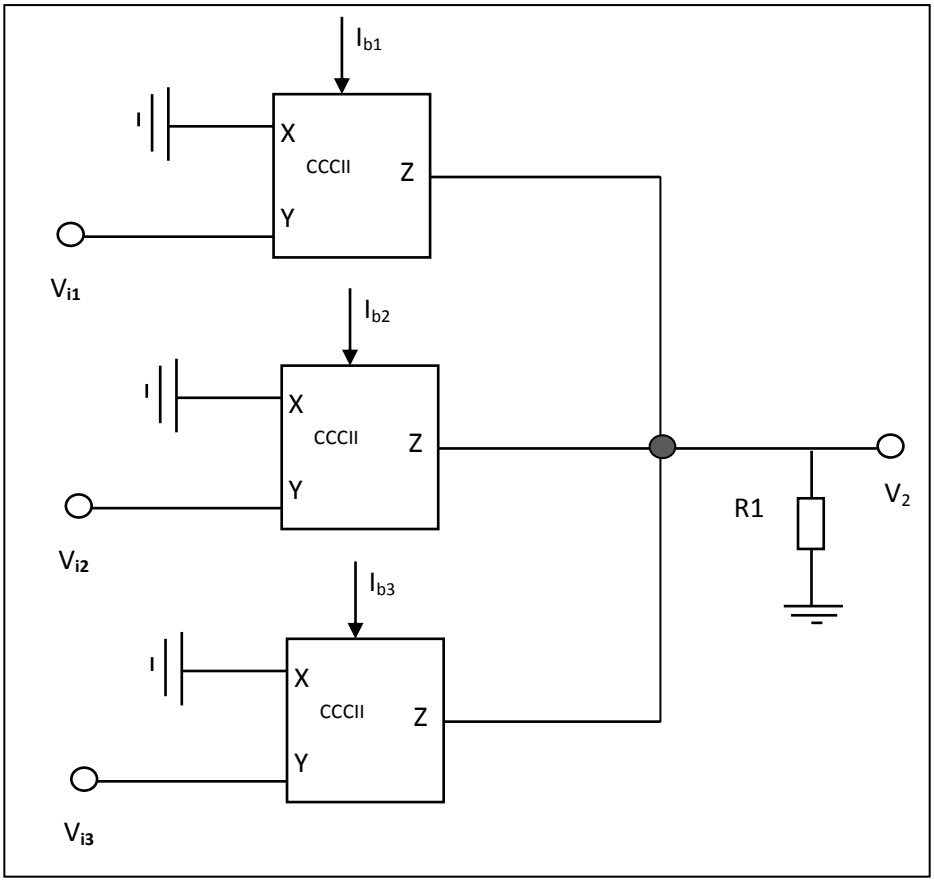

Fig. 3.3.1(e): summing circuit using CCCII

For the proportional gain in a PID controller, the CCCII is connected together with a resistor R1 as shown in the fig. 3.3.1(a). For the integration circuit, the CCCII is connected together with the capacitor C1 as shown in the fig. 3.3.1(b). For the derivative term in a PID controller, an inductance is connected together with the CCCII. This inductance, having a value of $L=R_{x1}R_{x2}C_2$ is simulated through two CCCIIs (see fig. 3.3.1(c)), which is connected together with the capacitor C_2 (see fig. 3.3.1(d)). In fig. 3.3.1(e), the weighted summing circuit is represented by three CCCIIs.

Connecting all these sub-circuits as shown in above fig. 3.3.1, into a single block as shown in fig. 3.3.2, gives the operation of a PID controller.

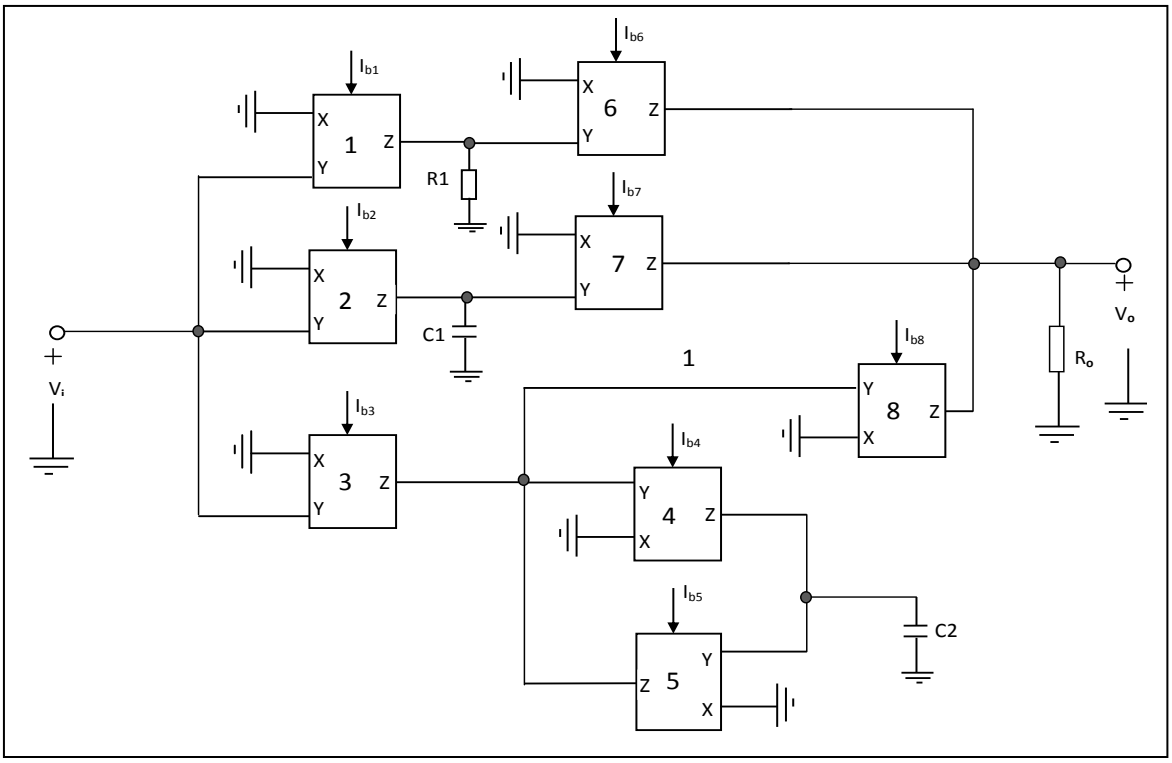

Fig. 3.3.2: Proposed CCCII-based PID controller realization from [3] corresponding to the signal-flow graph shown in fig. 3.1.2.

Taking ideal values, the circuit in fig. 3.3.2 gives the values of controller gains as follows

$$K_P = \frac{R_0 R_1}{R_{X1} R_{X6}}$$

$$K_I = \frac{R_0}{R_{X2} R_{X7} C_1}$$

$$K_D = \frac{R_{X4} R_{X5} R_0 C_2}{R_{X3} R_{X8}}$$

R_{Xi} is the input resistance of i^{th} CCCII active element, here i=1; 2:::; 8. From above equations, it can be seen that the controller gains associated with X input resistances of CCCIIs and this can be adjusted by the control current, I_{bi} of a selected CCCII.

3.4 CFA based PID controller

Based on the signal flow graphs as shown in fig. 3.4.1, the subgraphs and their corresponding blocks using active building blocks of CFAs, are shown in fig. 3.4.2 [4]. The circuit configuration of CFA is discussed in chapter 2. In fig. 3.4.2(a), block and signal flow graph of an amplifier circuit is shown. Fig. 3.4.2(b) and 3.4.2(c) represent the signal flow graph and block of

an integration circuit and of a derivative circuit, respectively. Fig. 3.4.2(d) represents block with corresponding signal flow graph of a summing circuit.

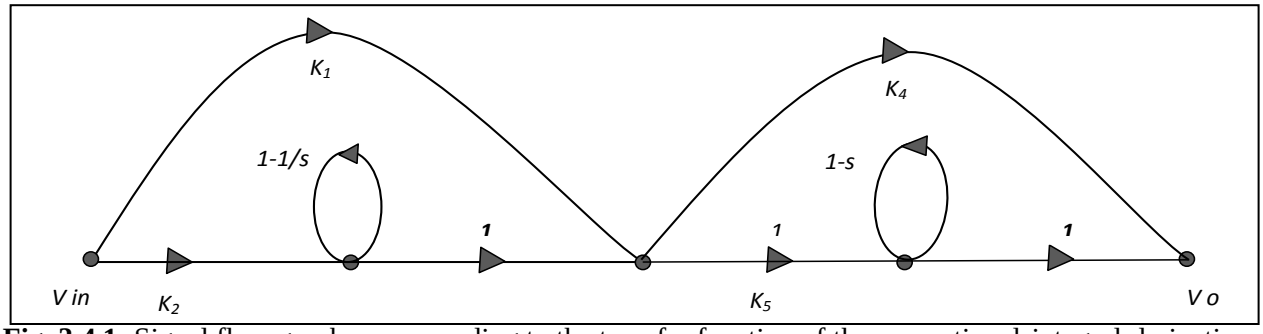

Fig. 3.4.1: Signal flow graph corresponding to the transfer function of the proportional-integral-derivative (PID) Controller

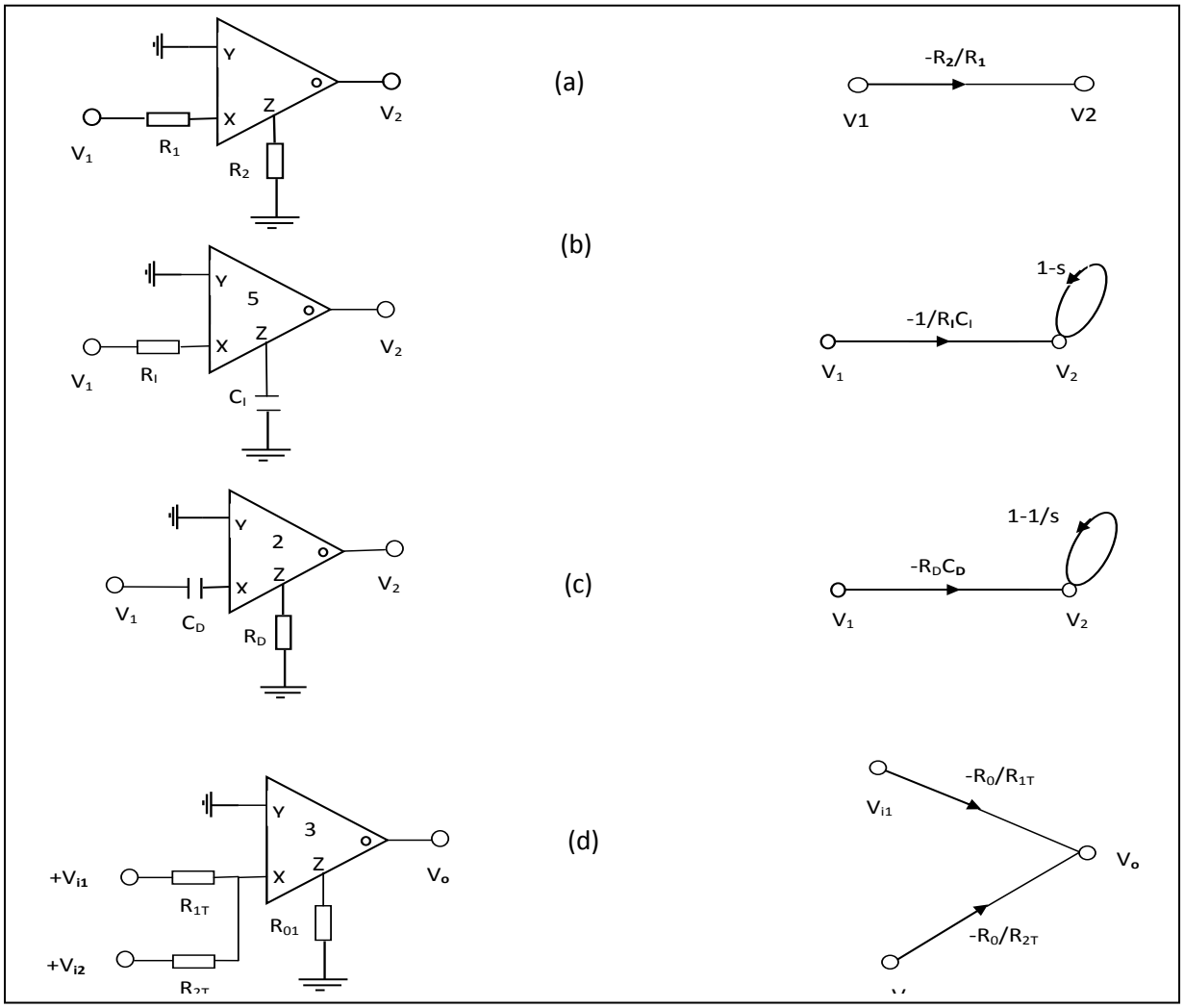

Fig. 3.4.2: Basic building blocks using CFOAs together with corresponding sub-graphs (a) Amplifier, (b) integrator, (c) derivative circuit, (d) summing circuit.

Fig. 3.4.2 (a) gives a value of $-R_2/R_1$ for the proportional gain, fig. 3.4.2(b) & (c) give the value of $1/R_IC_I$ for the time constant in the integrator circuit and of R_DC_D for the derivative time constant, respectively. Connecting all these blocks as shown in fig. 3.4.2, in such a way they can perform the operation of a PID controller as shown in fig. 3.4.3.

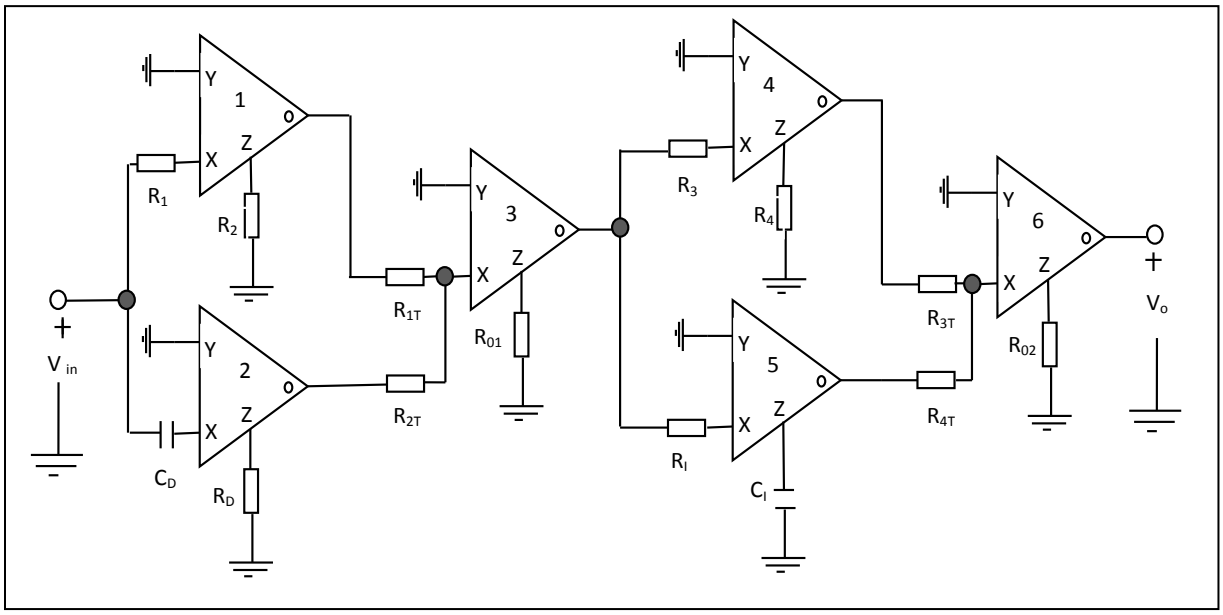

Fig. 3.4.3: A CFA based PID controller from [4] corresponding to the signal flow graph in fig. 3.4.1

Considering all ideal cases to adjust all gains as unity, the controller coefficients are given below

$$K_P = \frac{R_2R_4}{R_1R_3} + \frac{R_DC_D}{R_IC_I}$$

$$K_I = \frac{R_2}{R_1C_IR_I}$$

$$K_D = \frac{R_DC_DR_4}{R_3}$$

3.5 CDBA based PID Controller:

On the basis of a signal-flow graph as shown in fig. 3.1.2, the subgraphs and their corresponding blocks using CDBAs are shown in fig. 3.5.1 [5]. The circuit's details of CDBAs are discussed in chapter 2.

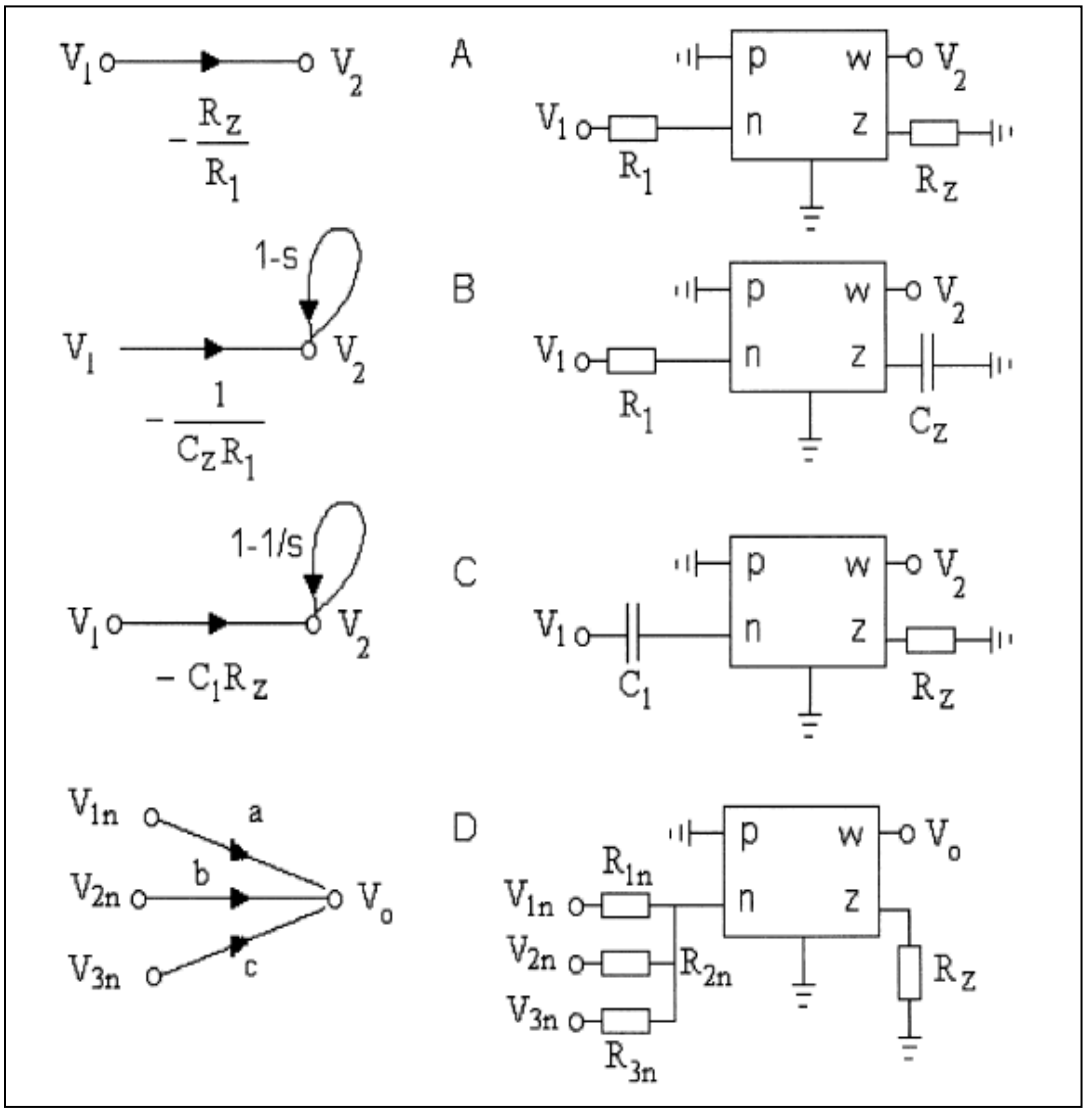

Fig. 3.5.1: Sub-graphs for the PID controller and their corresponding CDBA based sub-circuits. The coefficients in sub-graph D are $a = -R_Z/R_{1n}$, $b = -R_Z/R_{2n}$, $c = -R_Z/R_{3n}$.

Connecting all these blocks as shown in fig. 3.5.1, into a single block as shown in fig. 3.5.2, they perform the operation of a PID controller.

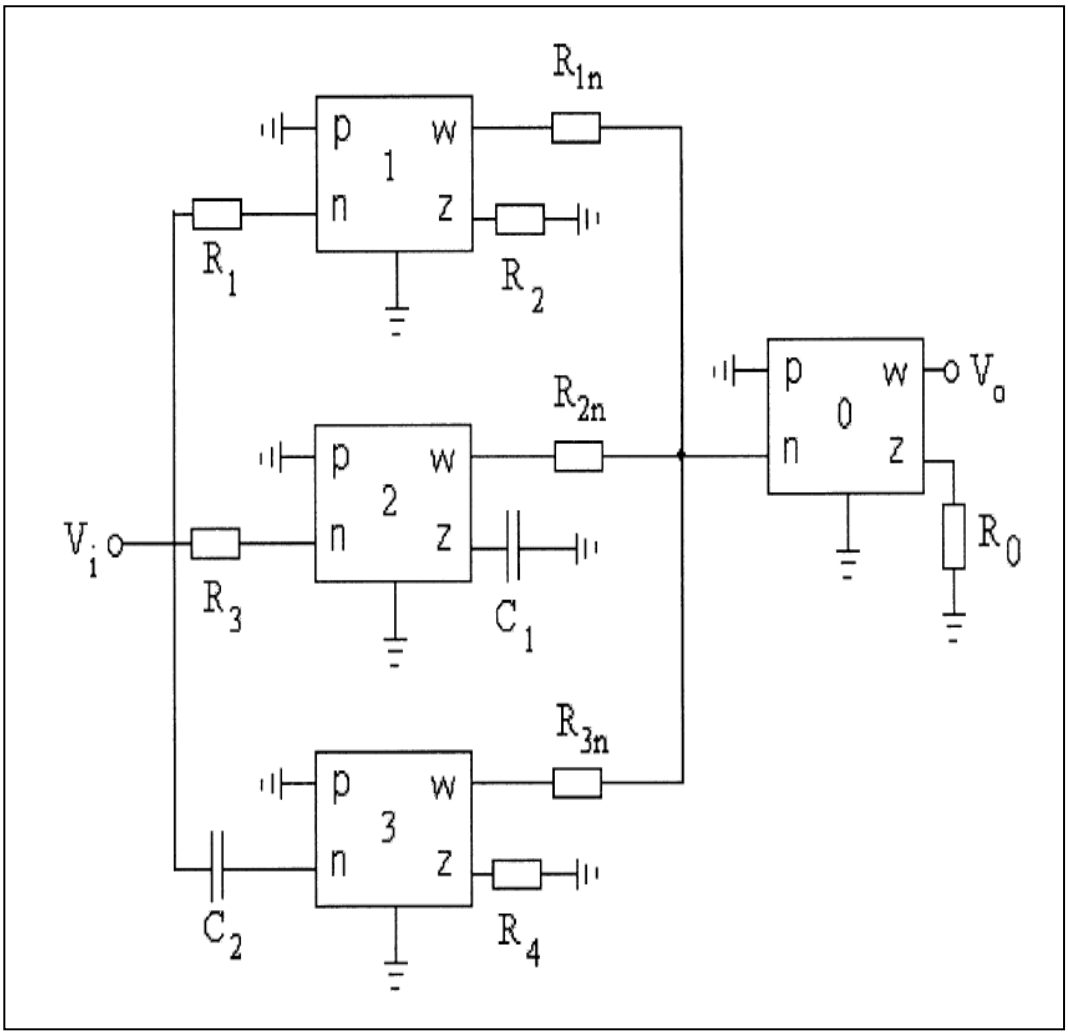

Fig. 3.5.2: CDBA-based PID controller circuit from [5]. All voltages are referred to ground.

Taking all ideal values, the coefficients of PID controllers are given below [5]

$$K_P = \frac{R_0 R_2}{R_1 R_{1n}}$$

$$K_I = \frac{R_0}{R_3 C_1 R_{2n}}$$

$$K_D = \frac{R_0 C_2 R_4}{R_{3n}}$$

3.6 Simulation

3.6.1 Implementation of OTA-C based PID controller

The voltage mode PID controller as shown in fig 3.2.2, was used to implement a closed loop system by cascading it with the following second order system and its open loop (without controller) and closed loop time (without/with controller) response was simulated in PSPICE. The details of the simulation results are presented below.

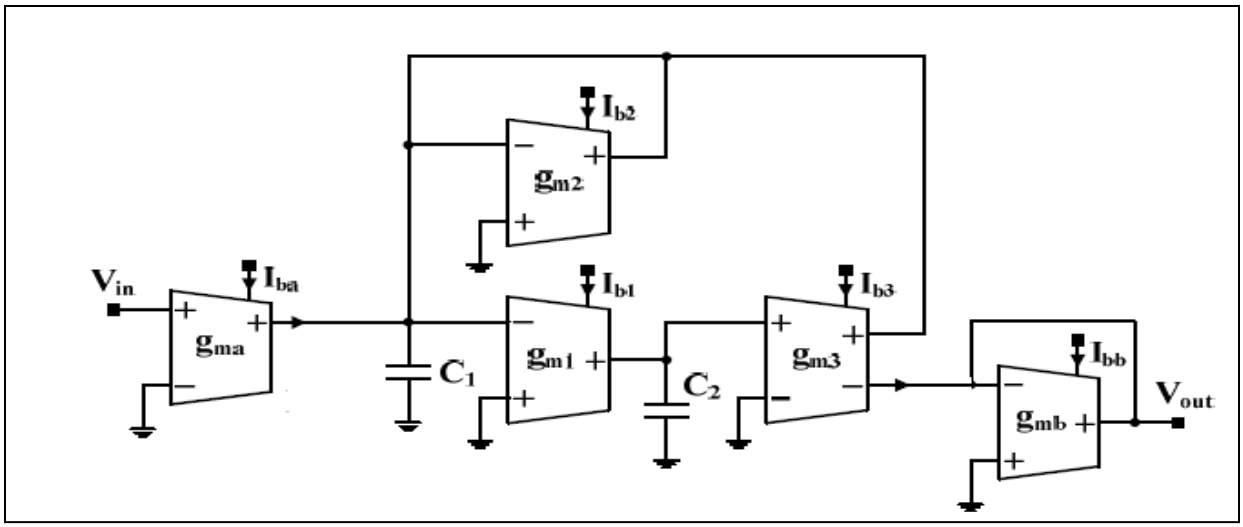

Fig. 3.6.1-1: OTA-C based voltage mode second order system [10]

The second order system [10] shown in fig. 3.6.1-1 gives the following transfer function

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{g_{m1}g_{m3}/C_1C_2}{s^2 + sg_{m2}/C_1 + g_{m1}g_{m3}/C_1C_2}$$

Taking values of $g_{m1}= g_{m3}= g_{m4}= g_{m5}= g_{m6}=165\mu A/V$ and $g_{m2}=58.345\mu A$, so that it gives damping ratio $\zeta=0.177$ and cut off frequency $f_c=8.758$ KHz. Simulation of this system gives open loop gain= 0.958.

Step response of this system without applying any controller in open loop structure is shown in fig. 3.6.1-2. Step response of the uncompensated closed loop system i.e., negative feedback without any controller is shown in fig. 3.6.1-3. Here the gain decreases by a factor of 0.477 from open loop gain.

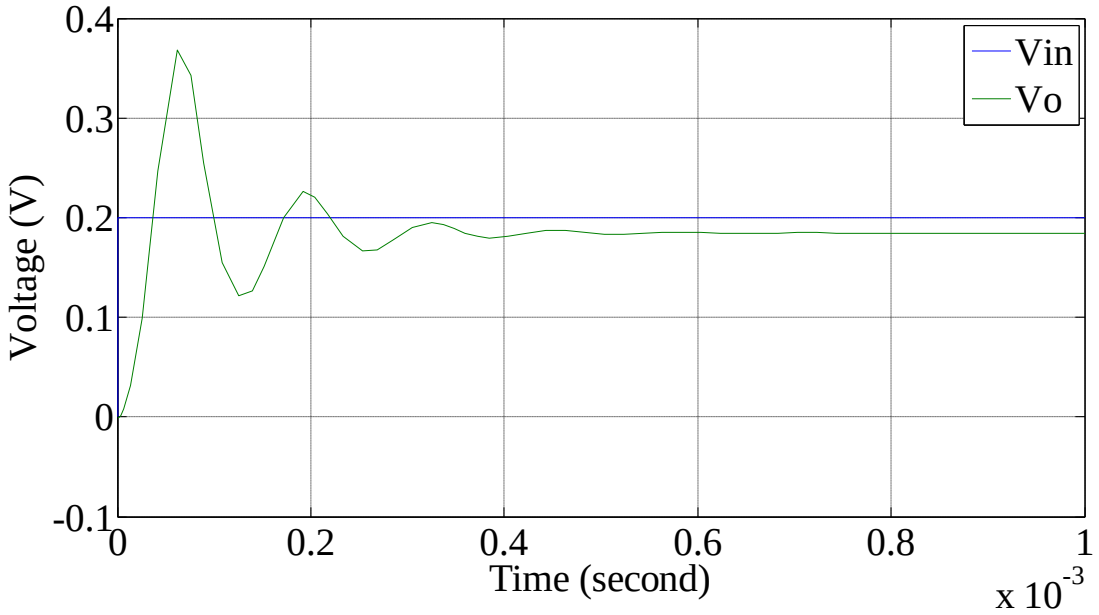

Fig. 3.6.1-2: Step response of uncompensated open loop system in voltage mode operation

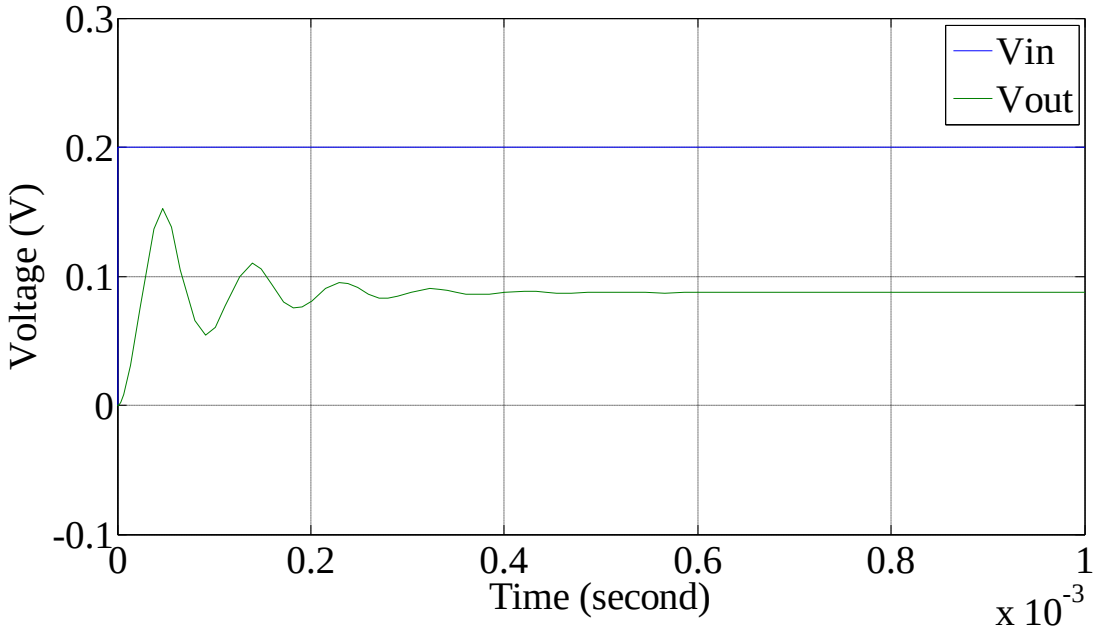

Fig. 3.6.1-3: Step response of uncompensated closed loop system in voltage mode operation

Now the implementation of PID controller is done, for (a) $K_p=0.1$, $K_I=1.625*10^4$, $K_D=0.595$ as shown in fig. 3.6.1-4, (b) $K_p=1$, $K_I=1.625*10^4$, $K_D=0.595$ as shown in fig. 3.6.1-5 and (c) $K_p=10$, $K_I=1.625*10^5$, $K_D=5.95$ as shown in fig. 3.6.1-6

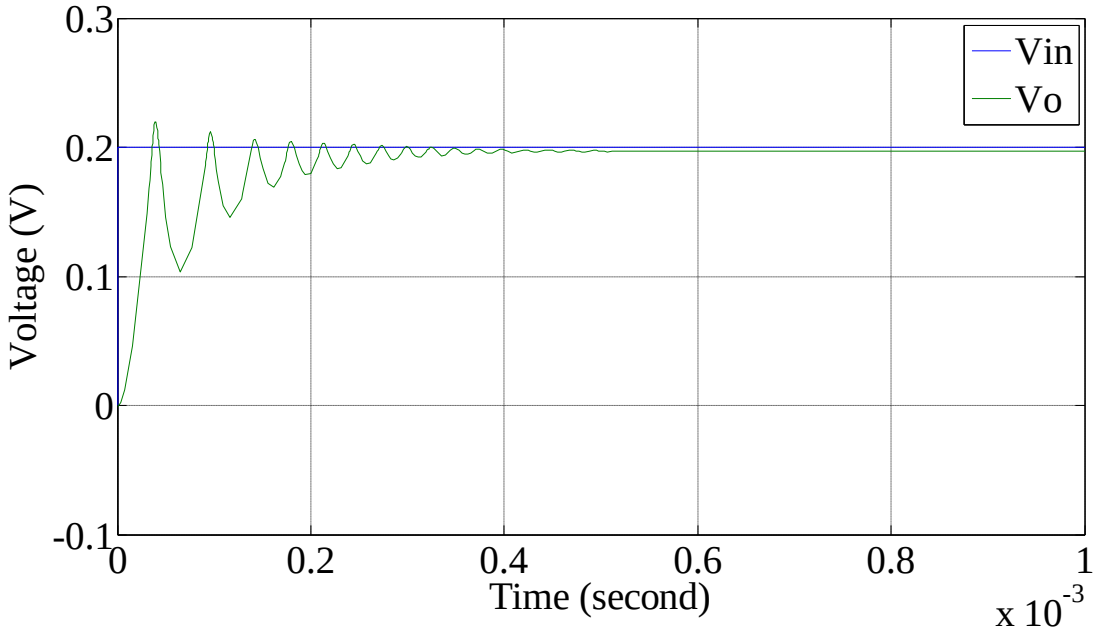

Fig. 3.6.1-4: Step response of compensated closed loop system for $K_P=0.1$, $K_I=1.625*10^4$, $K_D=0.595$

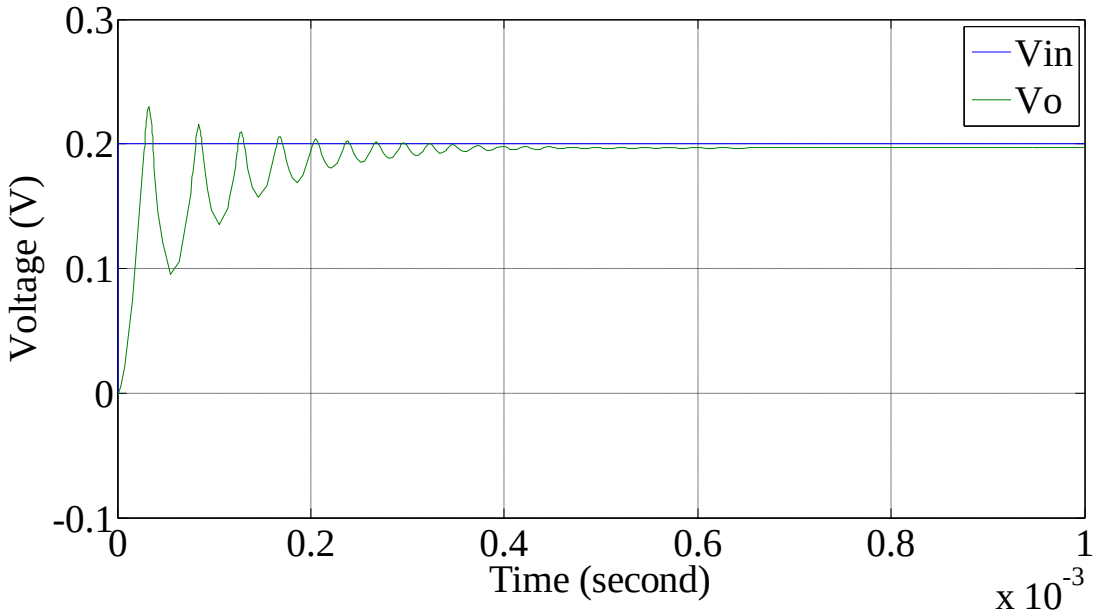

Fig. 3.6.1-5: Step response of compensated closed loop system for $K_P=1$, $K_I=1.625*10^4$, $K_D=0.595$

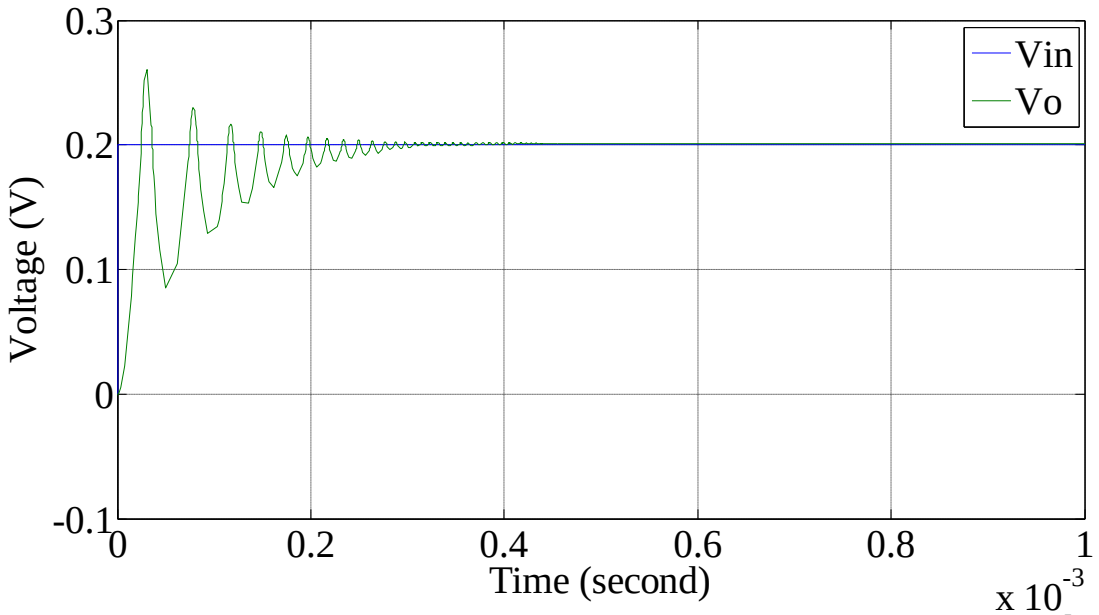

Fig. 3.6.1-6: Step response of compensated closed loop system for $K_P=10$, $K_I=1.625*10^5$, $K_D=5.95$

Table 3.0: Observation from the step response of the system operating in voltage mode

S.No.	Various System Configuration	Rise Time t_r (µs)	Overshoot (%)
1.	*Open loop uncompensated*	43	99
2.	*Closed loop uncompensated*	30	74.7
3.	*Closed loop compensated*		
	$K_p=0.1$, $K_I=1.625*10^4$, $K_D=0.595$	26	11.69
	$K_p=1$, $K_I=1.625*10^4$, $K_D=0.595$	21	16.73
	$K_p=10$, $K_I=1.625*10^5$, $K_D=5.95$	19	31

3.6.2 Implementation of DOCCII based PID controller

The voltage mode and current mode PID controller was used to implement a closed loop system by cascading it with the following second order system and its open loop (without controller) and closed loop time (without/with controller) response was simulated in PSPICE. The details of the simulation results are presented below.

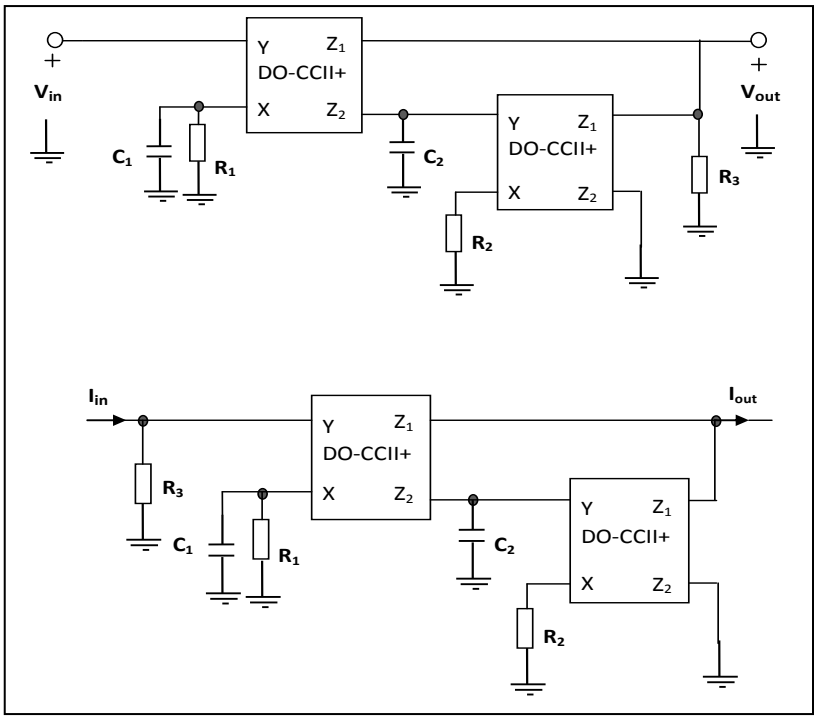

Fig. 3.6.2-1: PID Controller: (a) Voltage Mode (b) Current Mode [6]

Analysis of the PID controller circuits from fig. 3.6.2-1 gives the following voltage and current transfer functions:

$$H_v(s) = \frac{V_{out}(s)}{V_{in}(s)} = K_{pv} + \frac{1}{sT_{iv}} + sT_{dv}$$

$$H_i(s) = \frac{I_{out}(s)}{I_{in}(s)} = K_{pi} + \frac{1}{sT_{ii}} + sT_{di}$$

Coefficients for both voltage as well as current mode are written as follow

$$K_p = K_{pv} = K_{pi} = \alpha_1\beta_1\frac{R_3}{R_1} + \alpha_2\beta_1\beta_2\Upsilon_1\frac{C_1R_3}{C_2R_2}$$

$$K_I = K_{Iv} = K_{Ii}\frac{\alpha_2\beta_1\beta_2\Upsilon_1R_3}{C_2R_1R_2}$$

$$K_D = K_{Dv} = K_{Di} = \alpha_1\beta_1C_1R_3$$

Where, $\alpha_1, \beta_1, \alpha_2, \beta_2$ and Υ_1 are in form of multiplier constants for the parameters.

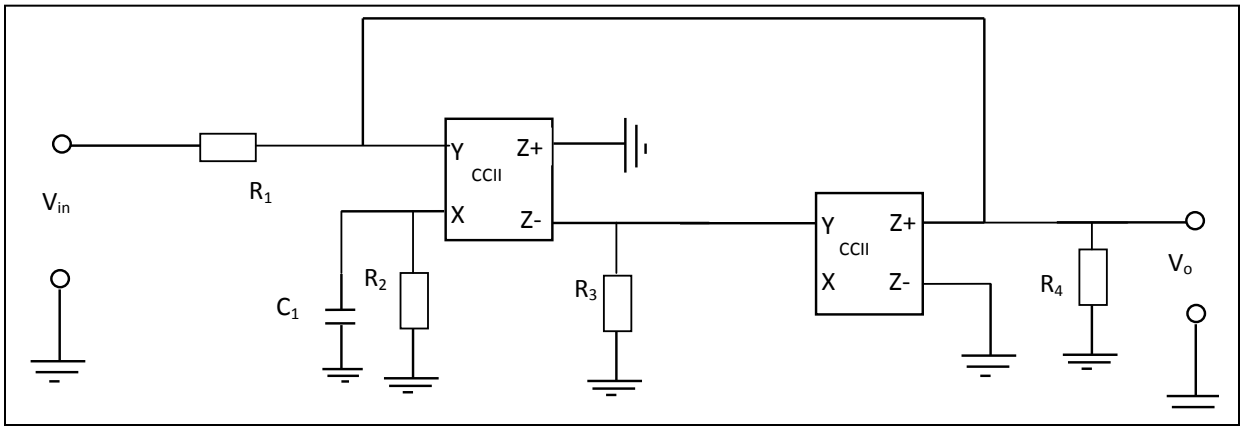

Fig. 3.6.2-2: Block- diagram of a voltage- mode second order system [7]

The above fig. 3.6.2-2 gives the voltage transfer function as given below

$$H_{lpv}(s) = \frac{V_o}{V_{in}} = \frac{\frac{1}{C_1 C_2 R_1 R_3}}{s^2 + \frac{s}{C_1 R_2} + \frac{1}{C_1 C_2}\left(\frac{1}{R_3 R_4} + \frac{1}{R_1 R_2}\right)}$$

Taking R_1=5KΩ, R_2=600KΩ, R_3=100KΩ, R_4=50KΩ C_1=10pF and C_2=70pF, so that the above transfer function gives the following results

Damping factor $\zeta = 0.047$,

Results from mathematical analysis:	Results after simulation:
Cut off frequency f_c= 280 KHz	Cut off frequency f_c= 300 KHz
Gain K=0.9	Gain K=0.905

The step response of the second order system is shown in the fig. 3.6.2-3. This is the step response of the system without applying any controller. Step response of the uncompensated closed loop system i.e., negative feedback without any controller is shown in fig. 3.6.2-4. Here the gain decreases by a factor of 0.656 from open loop gain.

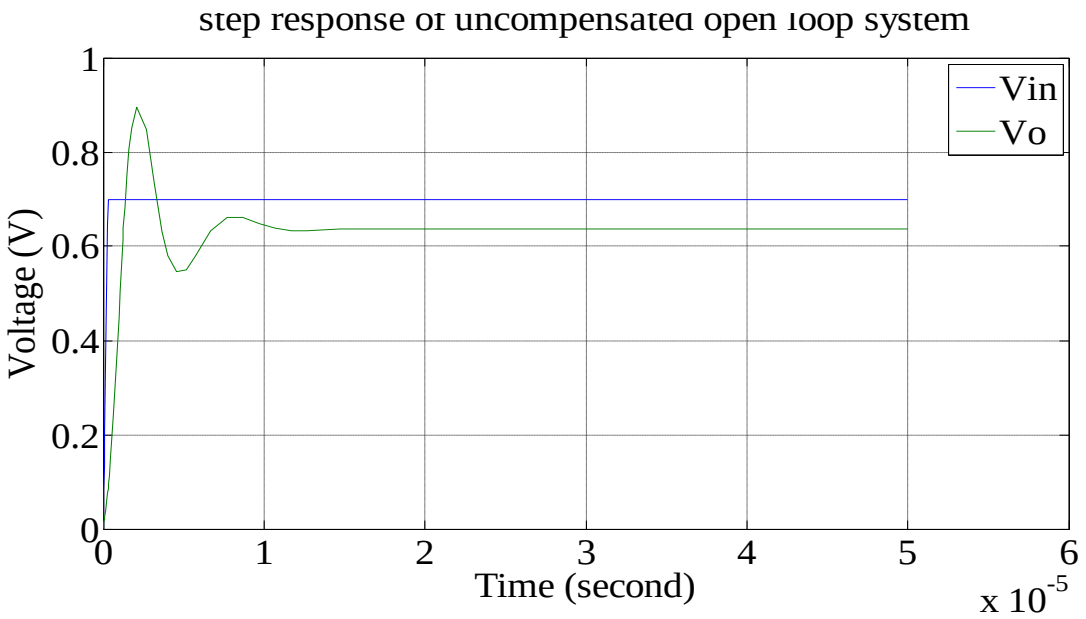

Fig. 3.6.2-3: STEP response of uncompensated open loop system operating in voltage mode

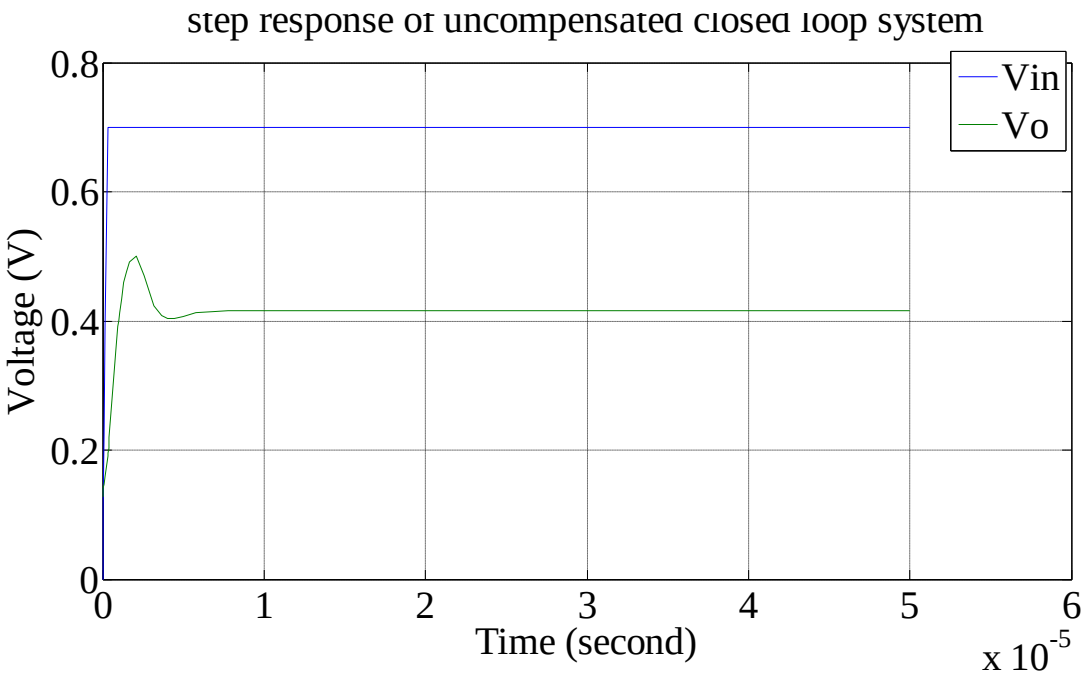

Fig. 3.6.2-4: STEP response of uncompensated closed loop system operating in voltage mode

Now the implementation of PID controller is done, for (a) $K_P=100$, $K_I=50*10^6$, $K_D=50*10^{-6}$ as shown in fig. 3.6.2-5, (b) $K_P=20$, $K_I=10*10^7$ & $K_D=10^{-6}$ as shown in fig. 3.6.2-6 and (c) $K_P=200$, $K_I=10*10^9$ & $K_D=10^{-6}$ as shown in fig. 3.6.2-7.

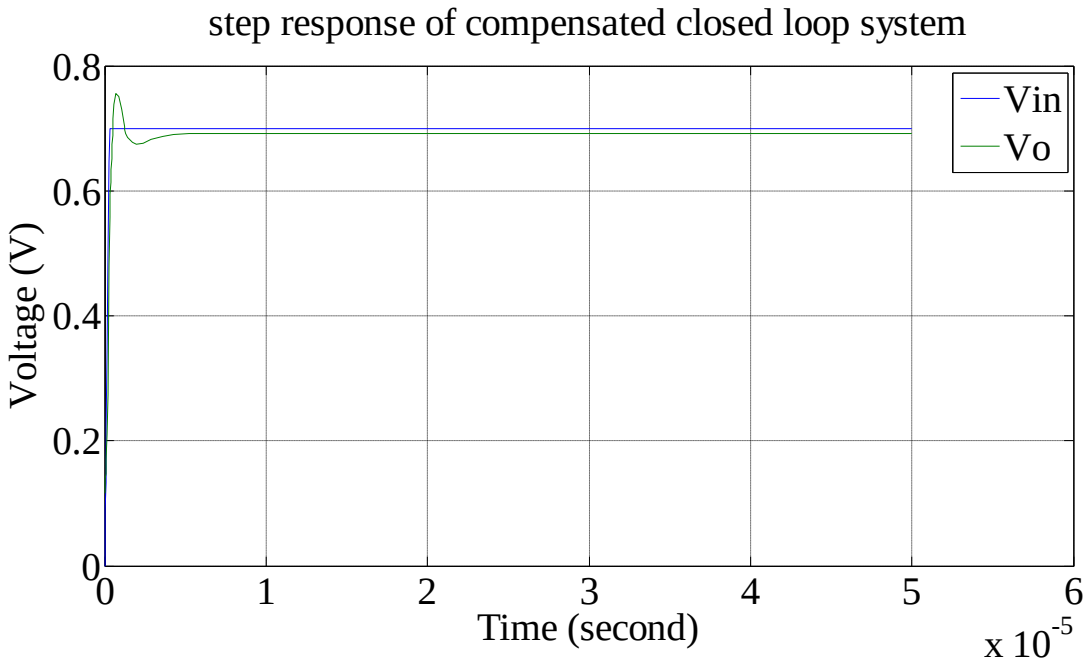

Fig. 3.6.2-5: Step response of compensated closed loop system for $K_P=100$, $K_I=50*10^{6}$, $K_D=50*10^{-6}$

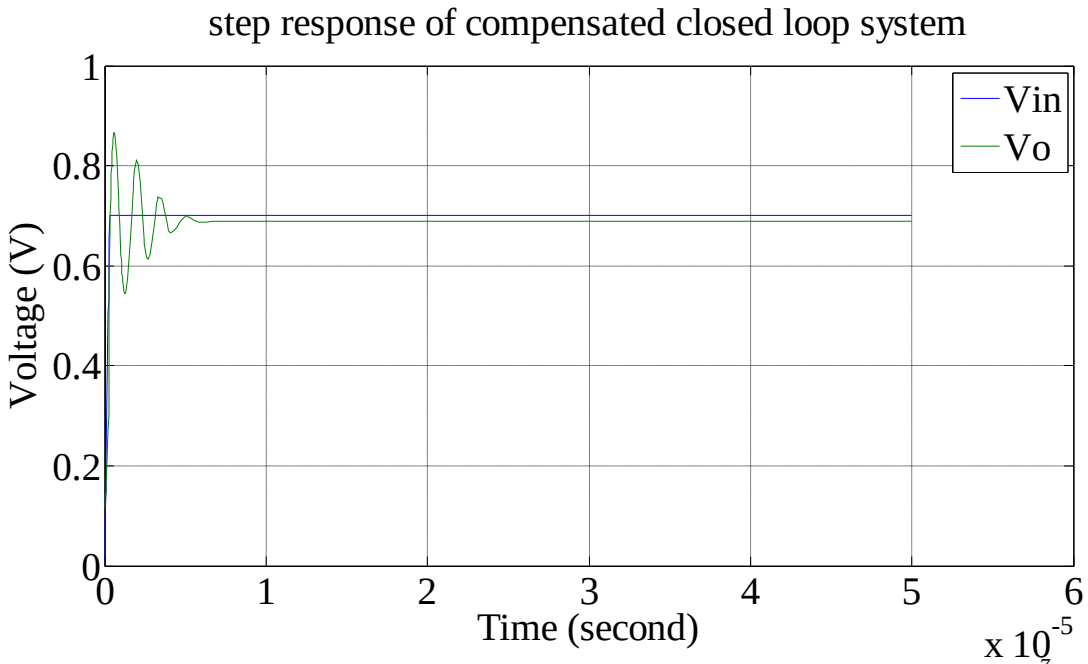

Fig. 3.6.2-6: Step response of compensated closed loop system for $K_P=20$, $K_I=10*10^{7}$ & $K_D=10^{-6}$

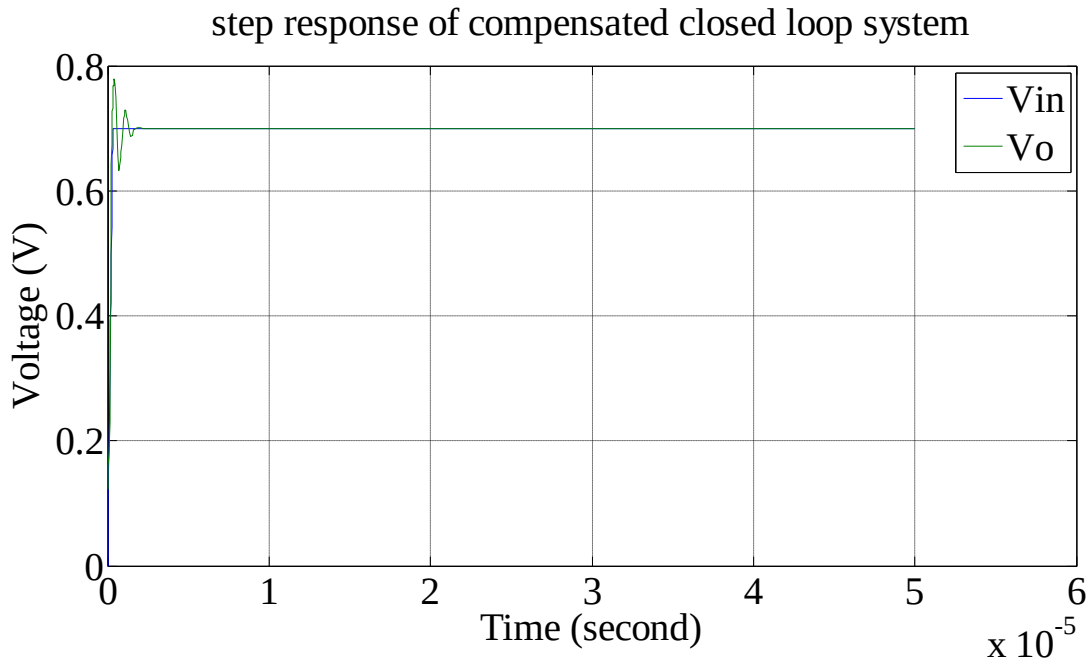

Fig. 3.6.2-7: Step response of compensated closed loop system for $K_P=200$, $K_I=10*10^9$ & $K_D=10^{-6}$

Here some important parameters are measured in table 3.1 from above all graphs as shown in fig. 3.6.2-3, 3.6.2-4 & 3.6.2-7

Table 3.1: Observation from the step response of the system operating in voltage mode

S.N.	Parameters Measured	Uncompensated Open Loop System	Uncompensated closed Loop System	Compensated closed Loop System
1.	*Rise Time* t_r	1.3µs	1.15 µs	0.19 µs
2.	*Overshoot (in %)*	40	20	11

Current mode PID controller as shown in fig. 3.6.2-1(b)), was cascaded with a second order system given below fig. 3.6.2-8 and its open loop (without controller) and closed loop time (without/with controller) response was simulated in PSPICE. The details of the simulation results are presented below.

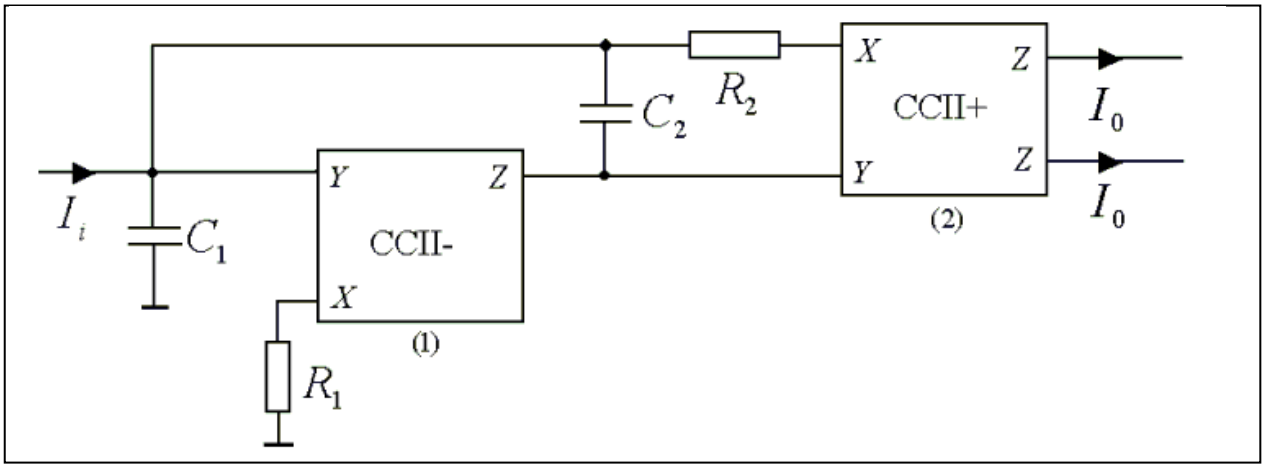

Fig. 3.6.2-8: Block- diagram of a current- mode second order system

The above fig. 3.6.2-8 gives the current transfer function, as below

$$H_{lpi}(s) = \frac{I_o}{I_i} = \frac{\frac{1}{C_1 C_2 R_1 R_2}}{s^2 + \frac{s}{C_1 R_1} + \frac{1}{C_1 C_2 R_1 R_2}}$$

Taking R_1=5KΩ, R_2=0.1KΩ, C_1=10nF and C_2=2nF, so that the above transfer function gives the following results

Damping factor ζ= 0.14, cut off frequency f_c= 50 KHz

The ramp response of the second order system without applying any controller is shown in the following fig. 3.6.2-9. Here slope of ramp input signal is set at 170 for this system. Response of system shows oscillatory nature to some time extent.

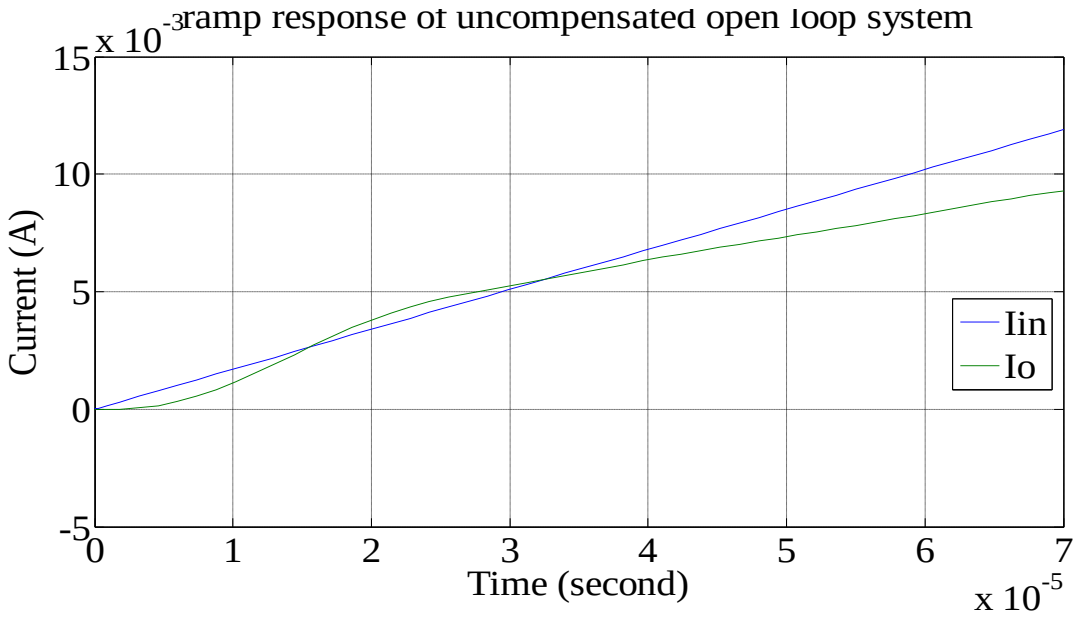

Fig. 3.6.2-9: RAMP response of uncompensated open loop system operating in current mode

In fig. 3.6.2-10, it can be observed that uncompensated closed loop system has faster response, lesser oscillatory nature and more instability in comparison to the open loop system (without controller).

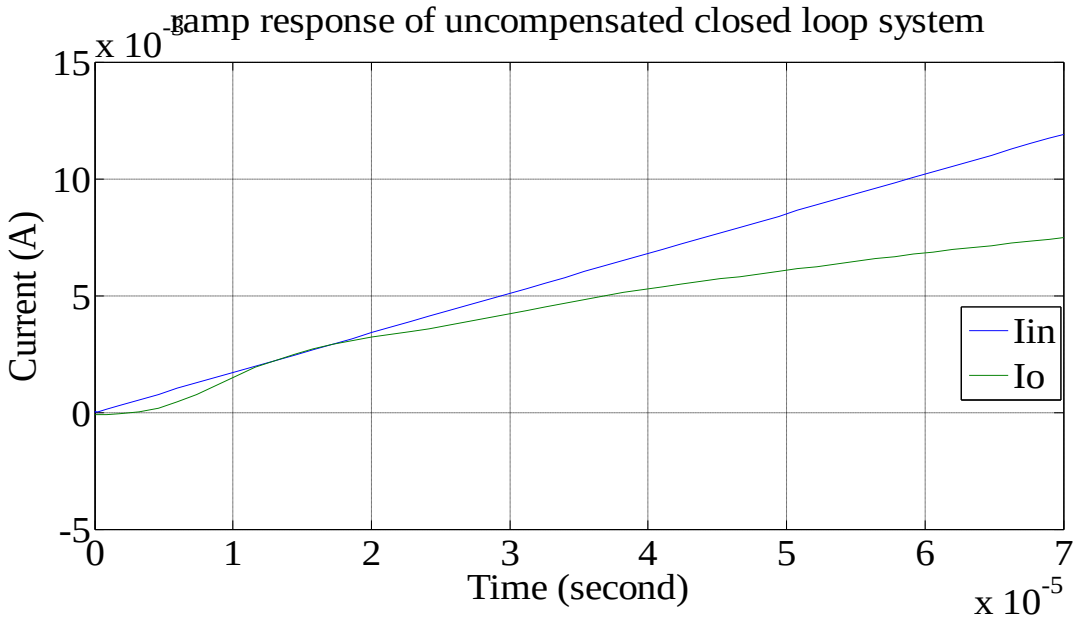

Fig. 3.6.2-10: RAMP response of uncompensated closed loop system operating in current mode

Here the implementation of current mode PID controller (fig. 3.6.2-1(b)) is done and for $K_p = 20$, $K_I = 10*10^6$, $K_D = 1*10^{-5}$ the simulation result is shown in following fig. 3.6.2-11.

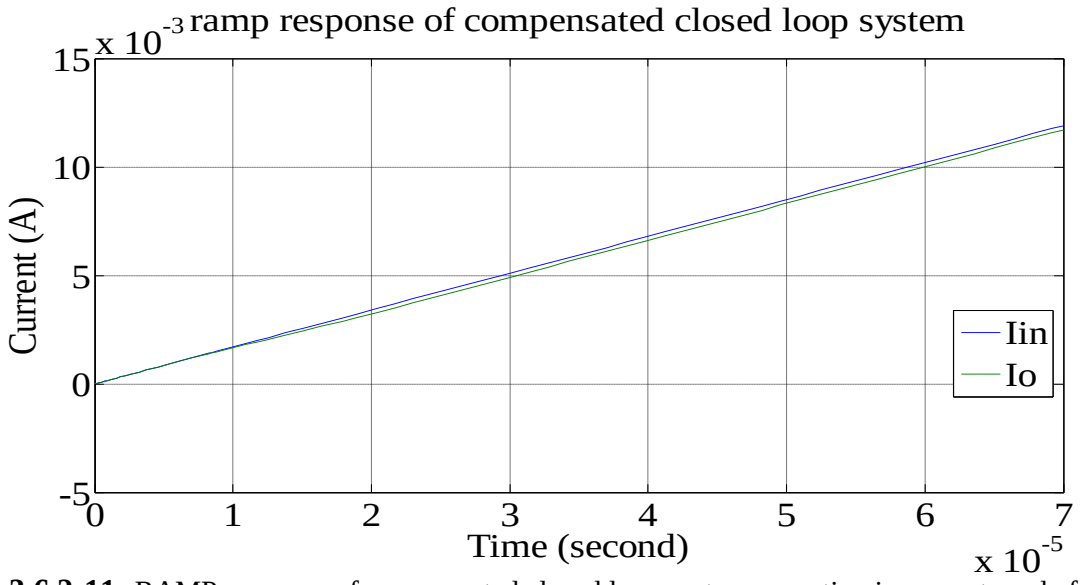

Fig. 3.6.2-11: RAMP response of compensated closed loop system operating in current mode for $K_P = 20$, $K_I = 10*10^6$, $K_D = 1*10^{-5}$

With the step input (step input of 500µA) signal, it gives response as shown in fig. 3.6.2-12.

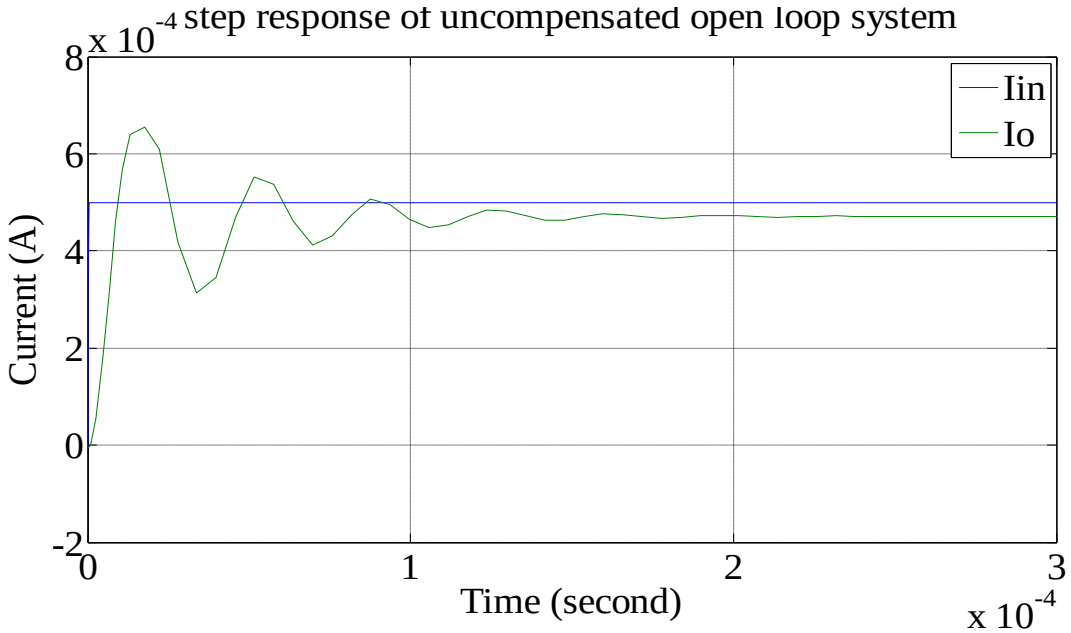

Fig. 3.6.2-12: STEP response of uncompensated open loop system operating in current mode

This is the step response of the system without applying any controller. Step response of the uncompensated closed loop system i.e., negative feedback without controller is shown in fig. 3.6.2-13. Here the gain decreases by a factor of 0.75 from open loop gain.

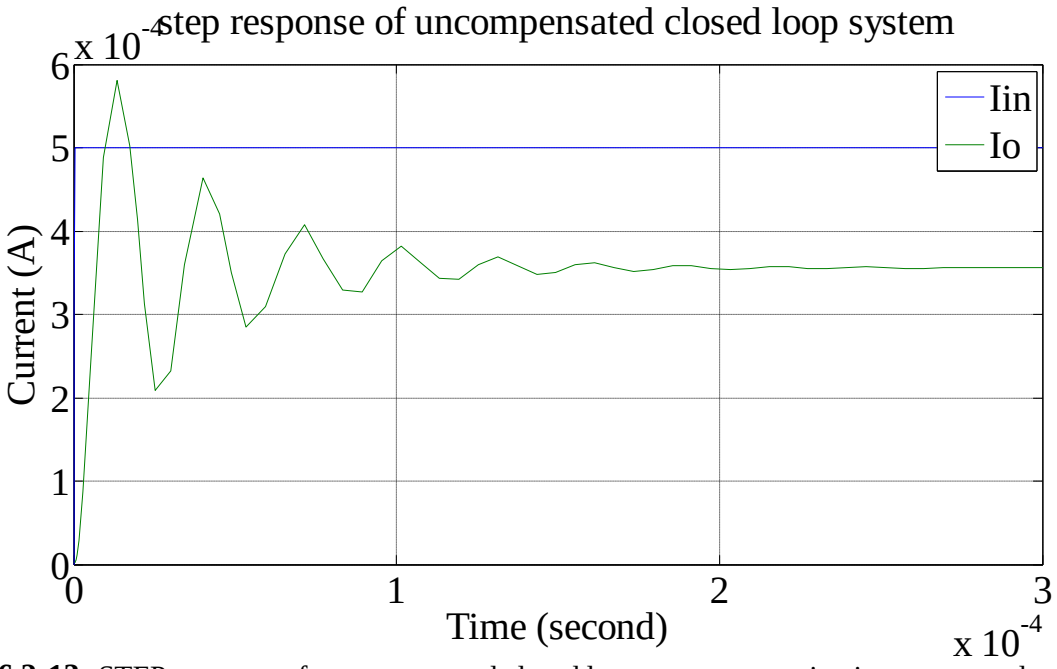

Fig. 3.6.2-13: STEP response of uncompensated closed loop system operating in current mode

Now the implementation of PID controller is done for different values of K_P, K_I and K_D. Fig. 3.6.2-14, 3.6.2-15, 3.6.2-16, and 3.6.2-17 are step responses of compensated closed loop system for

(a) $K_P=4$, $K_I=2*10^{-6}$ and $K_D=2*10^{6}$,

(b) $K_P=40$, $K_I=20*10^{-6}$ and $K_D=2*10^{6}$,

(c) $K_P=200$, $K_I=100*10^{-6}$ and $K_D=100*10^{6}$,

(d) $K_P=1000$, $K_I=500*10^{-6}$ and $K_D=500*10^{6}$, respectively.

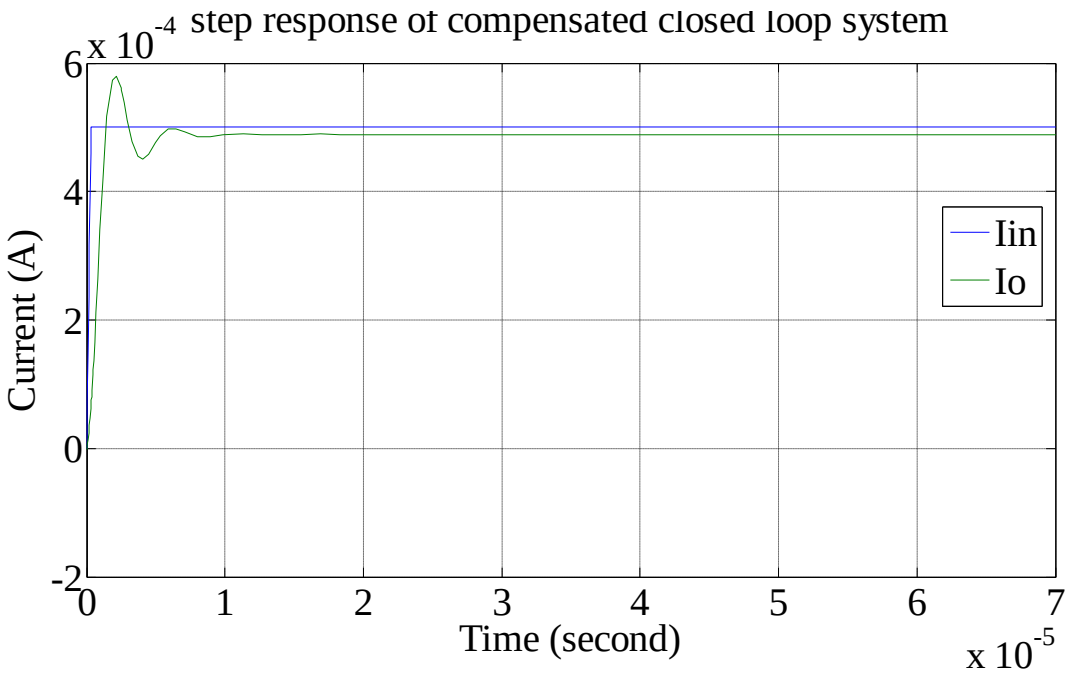

Fig. 3.6.2-14: STEP response of compensated closed loop system operating in current mode for $K_P=4$, $K_I=2*10^{-6}$ and $K_D=2*10^{6}$

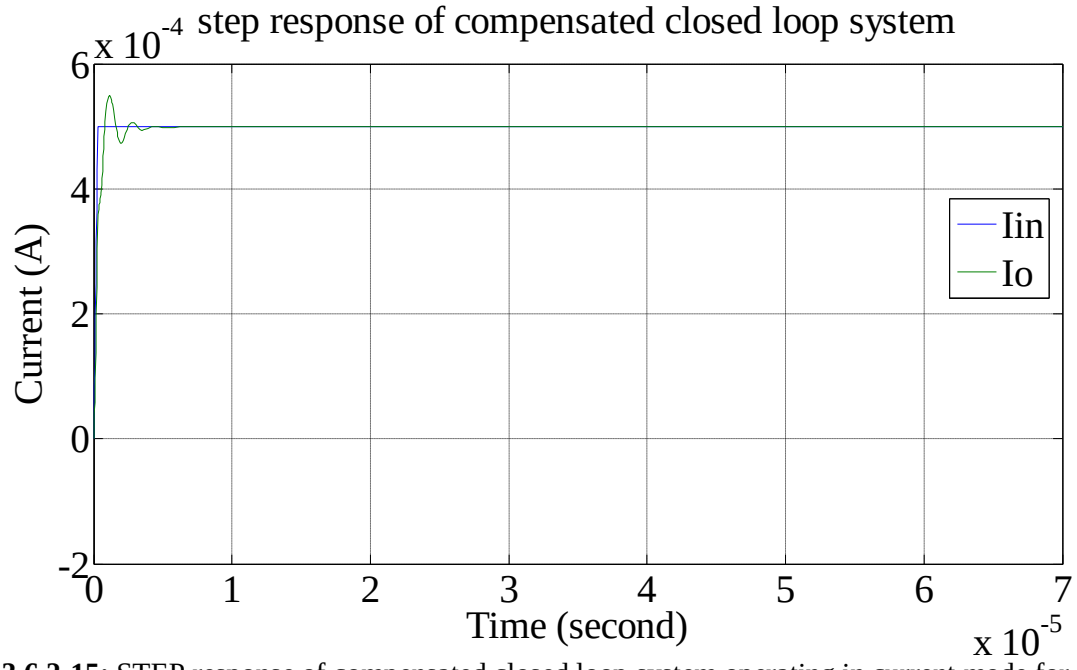

Fig. 3.6.2-15: STEP response of compensated closed loop system operating in current mode for $K_P=40$, $K_I=20*10^{-6}$ and $K_D=2*10^{6}$

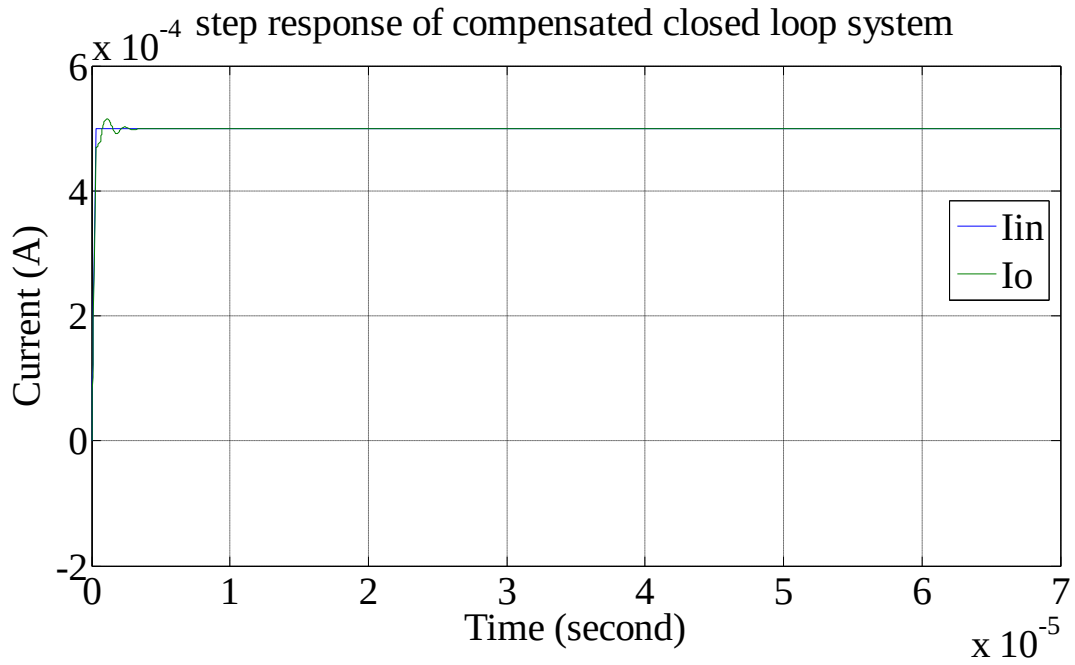

Fig. 3.6.2-16: STEP response of compensated closed loop system operating in current mode for $K_P=200$, $K_I=100*10^{-6}$ and $K_D=100*10^{6}$

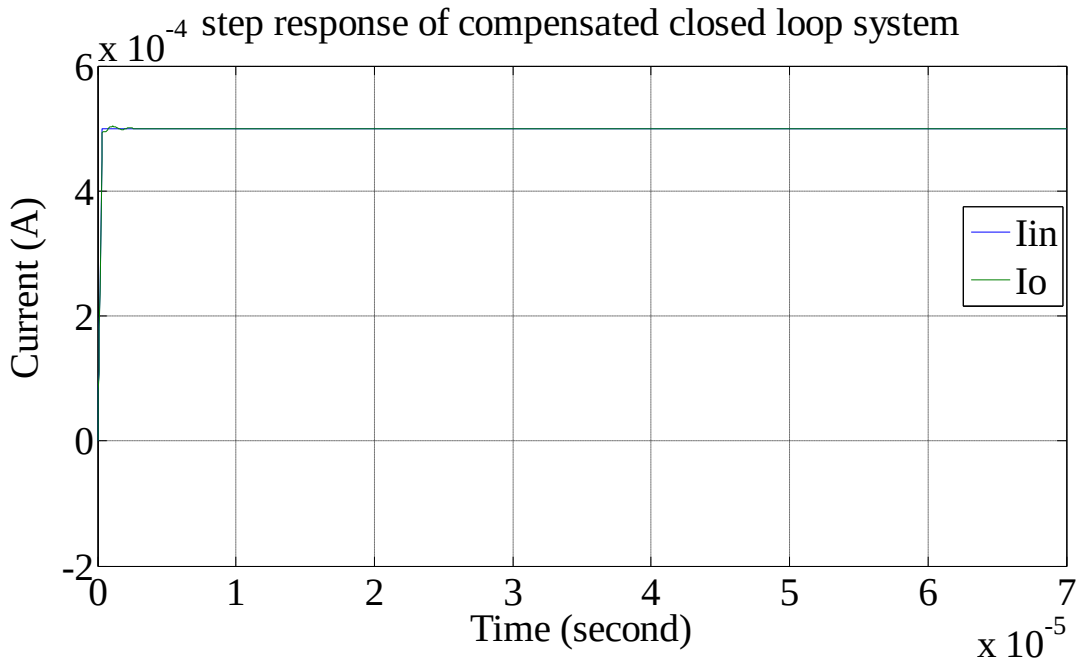

Fig. 3.6.2-17: STEP response of compensated closed loop system operating in current mode for $K_P=1000$, $K_I=500*10^{-6}$ and $K_D=500*10^{6}$

Table 3.2: Observation from the step response of the system operating in current mode

S.No.	Various System Configuration	Rise Time t_r (µs)	Overshoot (%)
1.	*Open loop uncompensated*	8.9	100
2.	*Closed loop uncompensated*	7.6	62.87
3.	*Closed loop compensated*		
	$K_p=4, K_I=2*10^{-6}, K_D=2*10^6$	1.23	18
	$K_p=40, K_I=2*10^{-5}, K_D=2*10^7$	0.726	10
	$K_p=200, K_I=1*10^{-4}, K_D=1*10^8$	0.276	3
	$K_p=1000, K_I=5*10^{-4}, K_D=5*10^8$	0.26	0.68

3.7 Conclusion

In this chapter, a brief discussion on the synthesis methods for analog PID controller using different current mode active blocks are described, with the help of signal flow graph techniques and their corresponding blocks. Design of OTA based, DOCCII based, CFA based and CDBA based PID controllers has been presented. The detailed simulation results on the time response studies on a OTA-based voltage mode PID controller and a DOCCII based voltage mode as well as current mode PID controller has been presented.

3.8 References

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CHAPTER IV

CURRENT MODE FULLY DIFFERENTIAL PID (FDPID) CONTROLLER REALIZATION

4.1 Introduction

The conventional PID controller has a very simple structure (which is its main advantage) and is used in a variety of process control system for control of various process parameters [1]. The conventional PID controllers have been realized with traditional voltage mode operational amplifiers and thus suffer from many disadvantages viz. low speed, low bandwidth , low dynamic range, as well as gain bandwidth conflict. Current-mode active devices are getting wide attention due to their wider bandwidth, lower-voltage operation and better linearity and stability properties in comparison to voltage- mode devices. Many of these devices such as current conveyors [2], operational transconductance amplifiers [3], current feedback operational amplifiers [4] and current differencing buffer amplifier [5] have been used to realize PID controllers. All these controllers have been realized as single ended controller where the output of the controller is always ground referred. Fully differential signal processing has started receiving attention in recent past because of inherent advantages such as increased dynamic range, lower harmonic distortion and better noise performance in presence of common mode noise etc [6]. In the following we present a fully differential current mode PID controller which uses dual output current conveyors to realize a fully differential current mode PID controller and is based on the formulation of a fully differential current mode building block using nullors [6].

4.2 Synthesis of Fully Differential Current Mode Active Block

The fully differential PID controller is synthesized with the help of a fully differential generalized building block described in terms of nullors [6]. Before we discuss the synthesis procedure in detail it is worthwhile to revise very briefly the properties of the nullor element [7].

Nullor is the combination of nullator and norator [6]. Nullator is a two terminal element which does not allow current flow through it, and the voltage across its terminals is zero under all conditions as shown in fig. 4.2-1 (a), while in norator, voltage V and current I have any arbitrary value as shown in fig. 4.2-1 (b).

Fig. 4.2-1: (a) Nullator symbol representation (b) Norator symbol representation

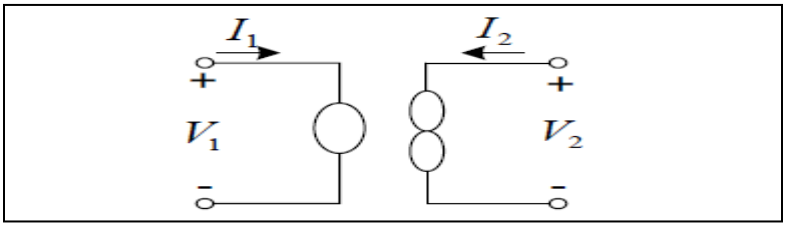

Fig. 4.2-2: Two-port nullor symbol [6]

These two one- ports, do not have independent existence but when combined to constitute a two port, have a transmission matrix which is a null matrix given below. The symbolic representation of the nullor is given in fig. 4.2-2.

$$\begin{bmatrix} V_1(s) \\ \mathrm{I}_1(s) \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_2(s) \\ -I_2(s) \end{bmatrix}$$

Nullors have been used for analysis, synthesis and design of various types of active circuits and their equivalents [8]. The fully-differential formulation shown in fig. 4.2-3, is constructed with the help of two three- terminal nullors, which can be very easily implemented using current conveyors [9].

By routine analysis, the output currents of the configuration are given by

$$i_o = -i_o{}' = \frac{Z_1}{Z_2}(i_{in} - i_{in}{}')$$

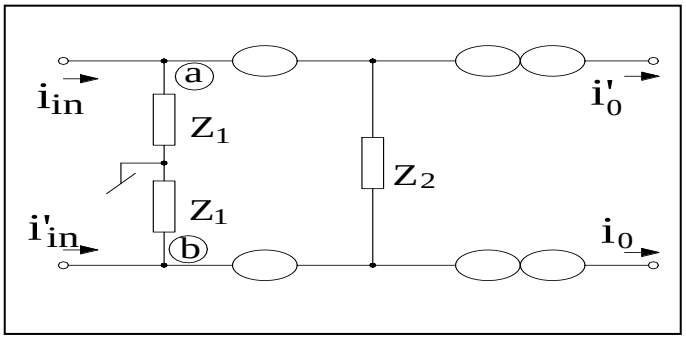

Fig. 4.2-3: Fully differential CM building block [6]

4.2.1 Synthesis of a fully differential PID (FDPID) controller

In a PID controller circuit, four mathematical functions viz. constant multiplication, integration, differentiation and summation, need to be implemented [1]. For a current mode PID controller we must implement the following current transfer function

$$H_i(s) = \frac{I_{out}(s)}{I_{in}(s)} = K_P + \frac{K_I}{s} + sK_D$$

By appropriately choosing the type of Z_i (in fig. 4.2-3) as resistor and/or capacitor so that a fully differential constant multiplier, a fully differential integrator, a fully differential differentiator and a fully differential summer (whose nullor representation is given in Fig. 4.2.1-1) can be realized with the nullors being replaced with CCIIs (with dual/multiple outputs). Fig. 4.2.1-2 gives a DOCCII based realization of these fully differential blocks.

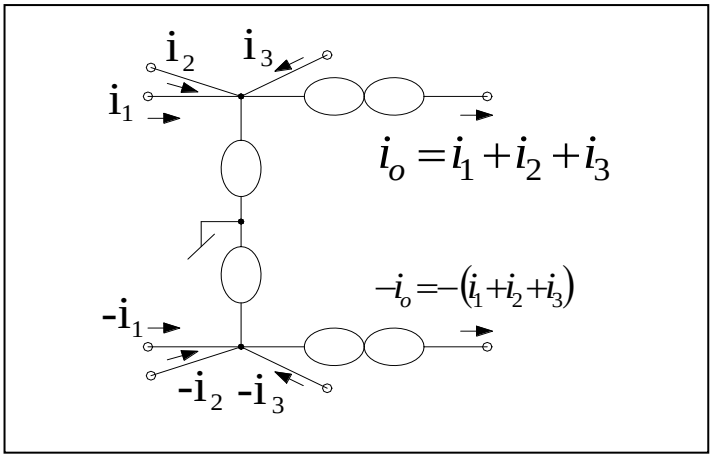

Fig. 4.2.1-1: Summing operation of PID controller with complementary CM outputs [6]

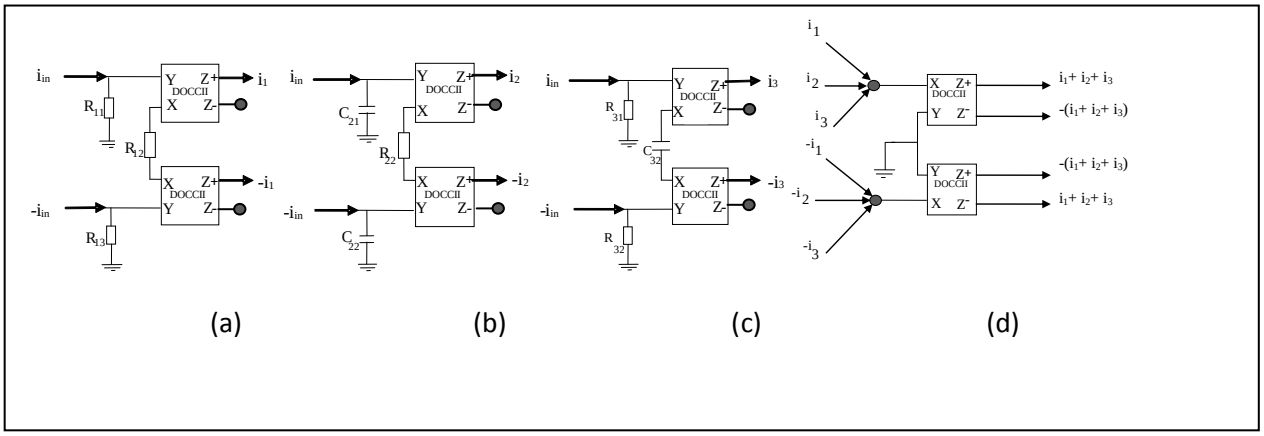

Fig. 4.2.1-2: CCII-based implementation of the sub-blocks of PID controller (a) constant multiplication, (b) integration and (c) differentiation.

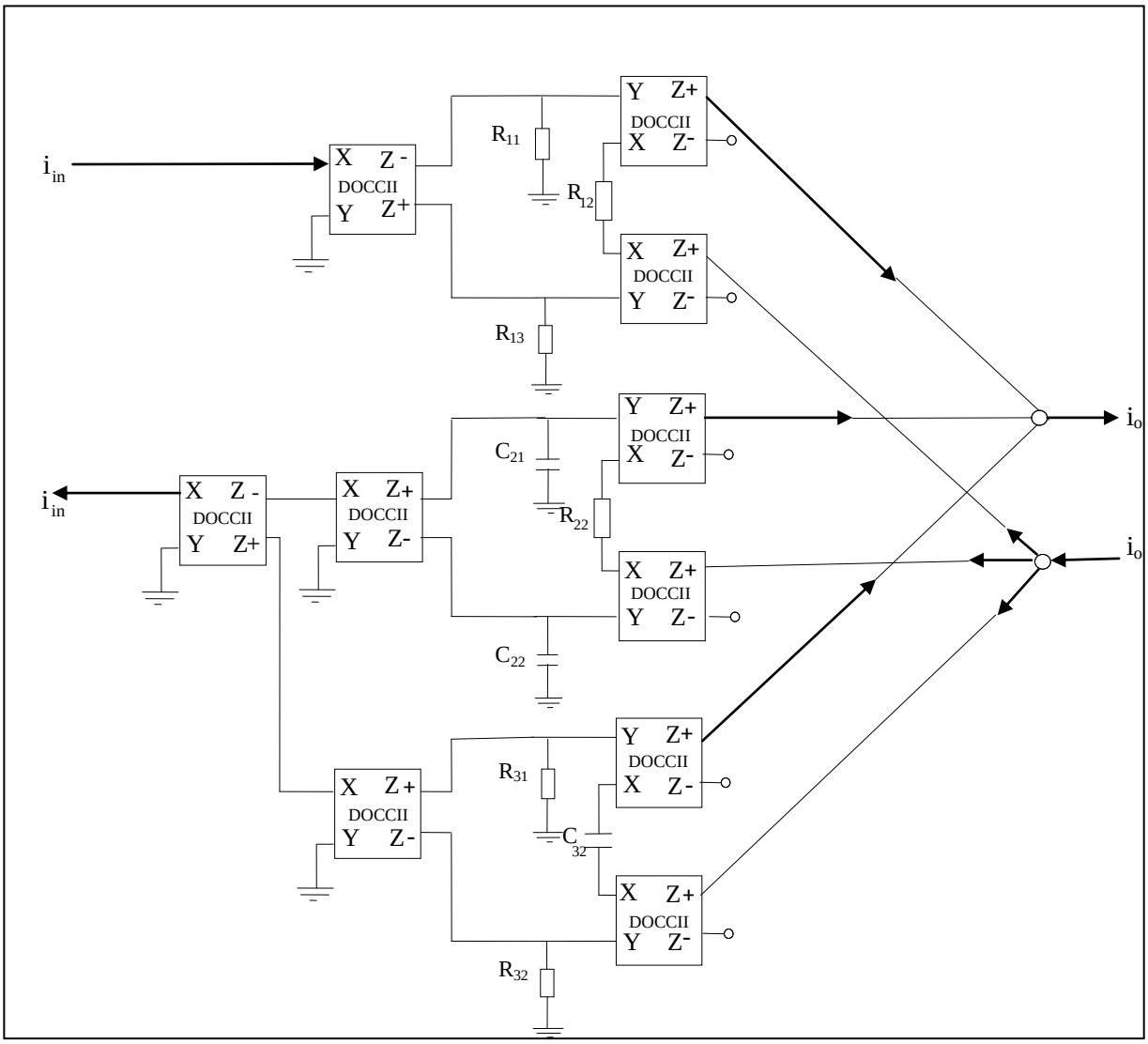

Fig. 4.2.1-3: A fully differential PID controller operating in current mode

Finally the circuit implementation of fully differential current mode PID controller is given in Fig. 4.2.1-3. The various tuning constants of the PID controller are given by

Proportional coefficient,

$$K_P = \frac{R_{11}}{R_{12}} + \frac{R_{13}}{R_{12}}$$

Integral coefficient,

$$K_I = \frac{1}{R_{22}}\left(\frac{1}{C_{21}} + \frac{1}{C_{22}}\right)$$

Derivative coefficient,

$$K_D = C_{32}(R_{31} + R_{32})$$

4.2.2 Fully differential second order open loop system

To test the workability of the fully differential current mode PID controller we have carried out the time response system analysis of a fully differential second order system given in [6], as shown in Fig. 4.2.2, in PSPICE with the PID controller put in cascade and closing the loop.

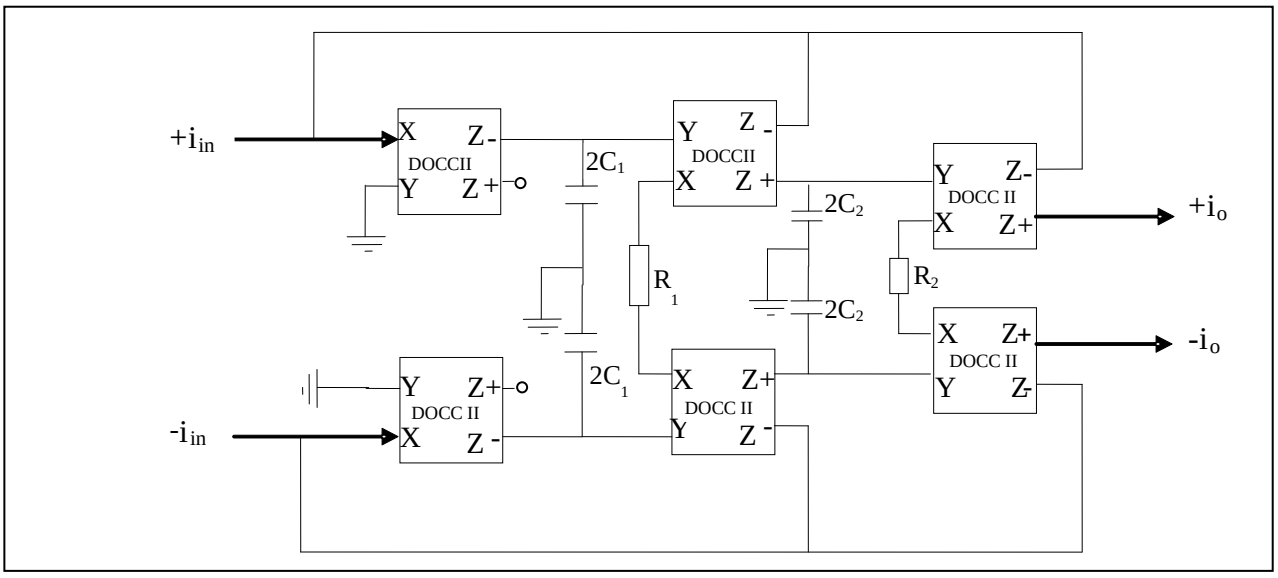

Fig. 4.2.2: A fully differential second order system employing DOCCII

The transfer function of this filter is given as

$$\frac{I_o(s)}{I_{in}(s)} = \frac{\frac{1}{R_1 R_2 C_1 C_2}}{s^2 + \frac{s}{R_1 C_1} + \frac{1}{R_1 R_2 C_1 C_2}}$$

Comparing the above equation with the general equation of a second order low pass filter, as given below

$$H(s) = \frac{\omega_0^2}{s^2 + 2\zeta\omega_0 s + \omega_0^2}$$

Here $\omega_0 = \sqrt{\frac{1}{R_1 R_2 C_1 C_2}}$ is the cut off frequency in radian/sec and $\zeta = \sqrt{\frac{R_2 C_2}{R_1 C_1}}$ is the damping factor.

4.3 Simulation:

The following values were taken to give a value of ζ=0.028, ω_o=14.14*10^3radian/sec: R_1=*50KΩ*, R_2=*1KΩ*, $2C_1$= *25nF* and $2C_2$=*1nF*. To establish the workability of the fully differential PID controller; the PID controller and the fully differential second order system given above in Fig. 4.2.2 were simulated using a DOCCII given below in Fig. 4.3.1. Design details of this circuit is given [10], and are also given in appendix,

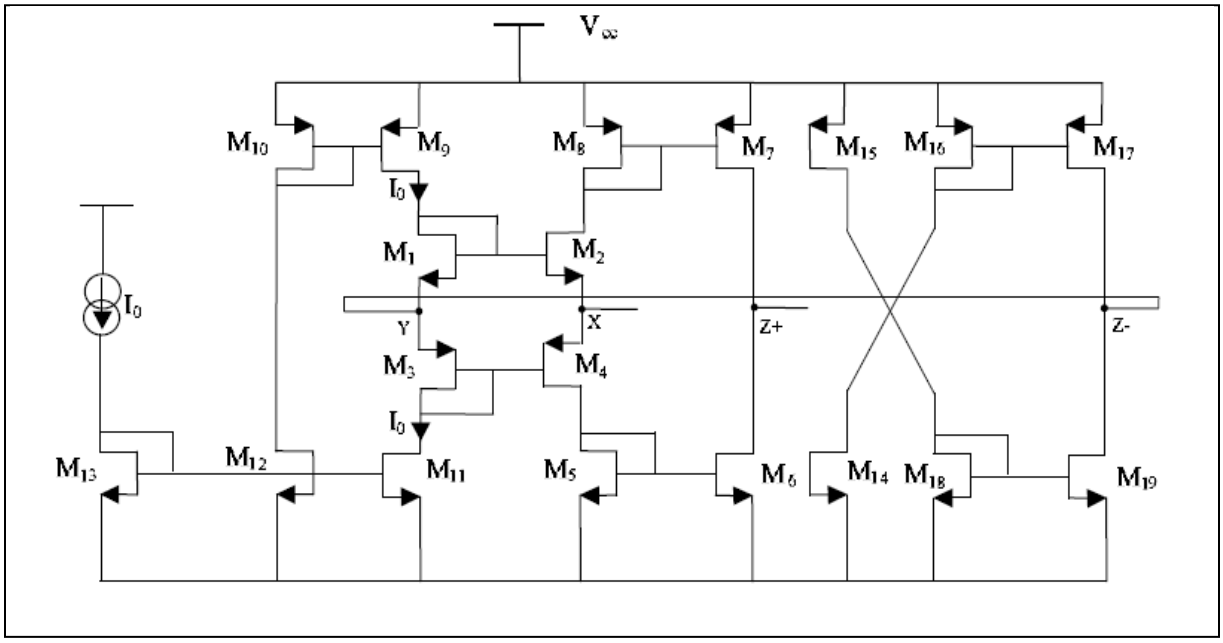

Fig. 4.3.1: CMOS implementation of DOCCII [10]

In order to test the performance of a fully differential second order system in open loop without introducing any controller, as shown in fig. 4.3.2, the step response (assuming input current is 400μA) of the system is shown in fig. 4.3.3. This figure shows that oscillations are damped in nature to some extent and reached steady state position afterwards. When the system is operating in closed loop without introducing any controller, as shown in fig. 4.3.4, the step response is shown in Fig. 4.3.5, the gain of the system decreases by $1/(1 + A_0\beta)$ in comparison to open loop which value is equal to 187.

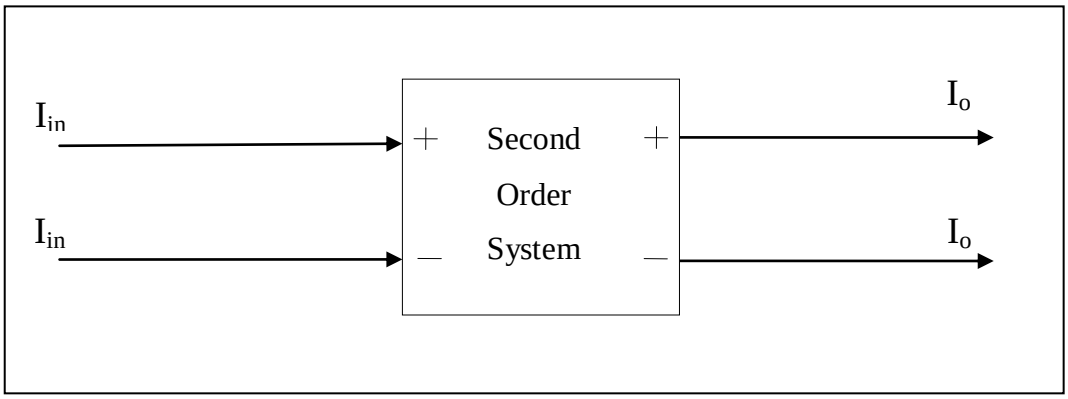

Fig. 4.3.2: Block-diagram of uncompensated closed loop system

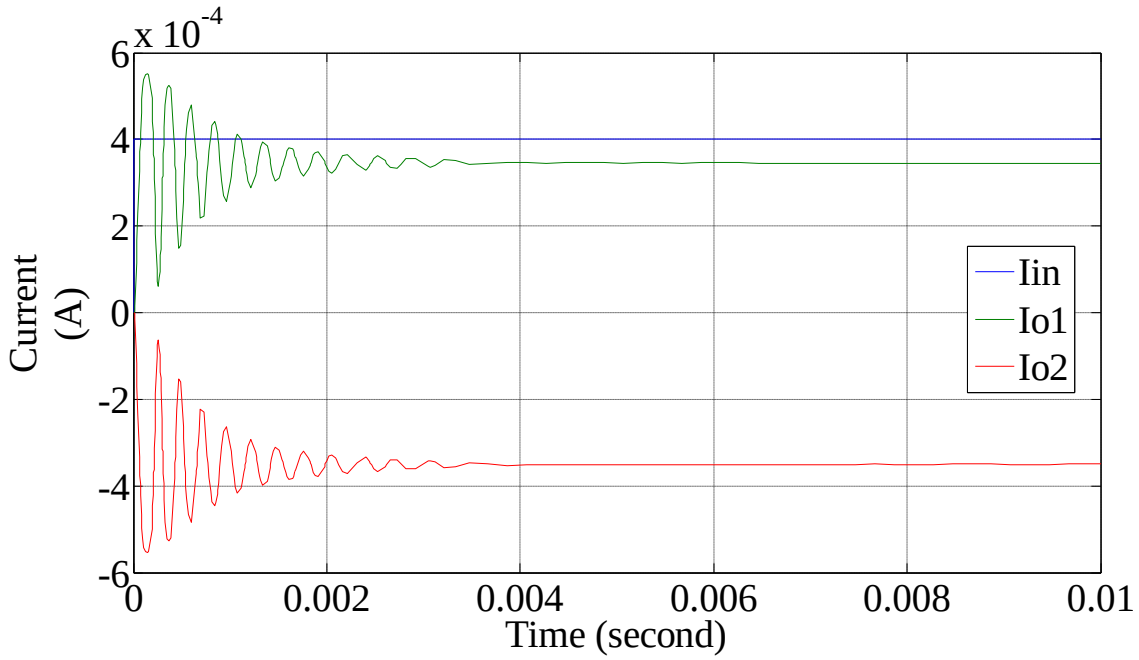

Fig. 4.3.3: Step response of an uncompensated open loop fully differential second order low pass filter

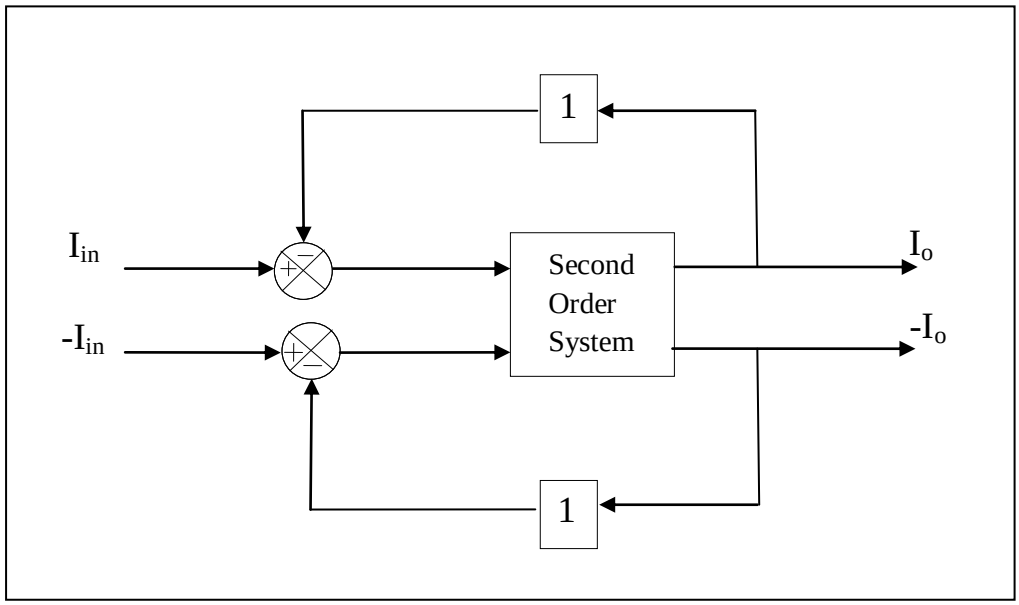

Fig. 4.3.4: Block-diagram of uncompensated closed loop system

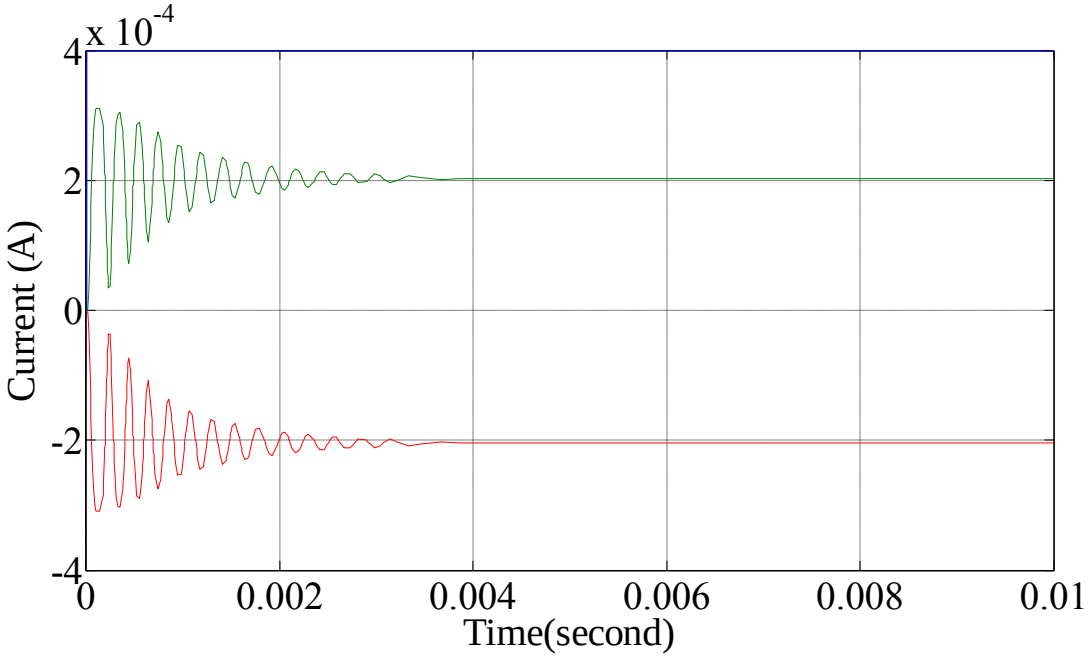

Fig. 4.3.5: Step response of uncompensated closed loop second order low pass filter

When a PID controller is employing to the system as shown in fig. 4.3.6, some parameters are varied for getting a good performance of the system. Fig. 4.3.7 & 4.3.8, show step response of the system for different values of K_P, K_I & K_D.

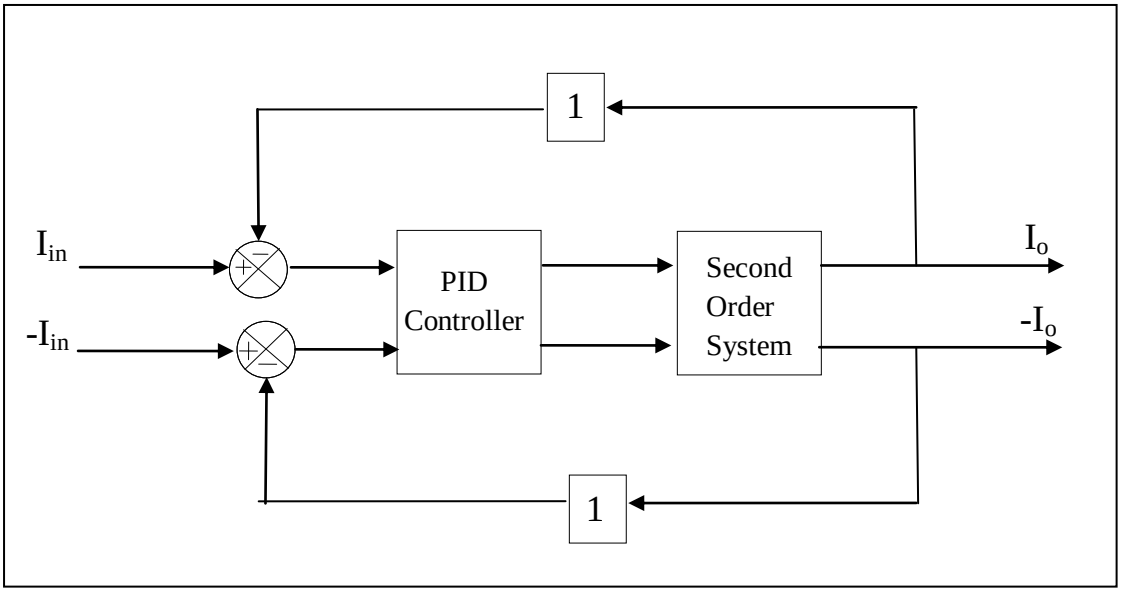

Fig. 4.3.6: Block-diagram of a compensated fully differential low pass filter (LPF) with PID controller

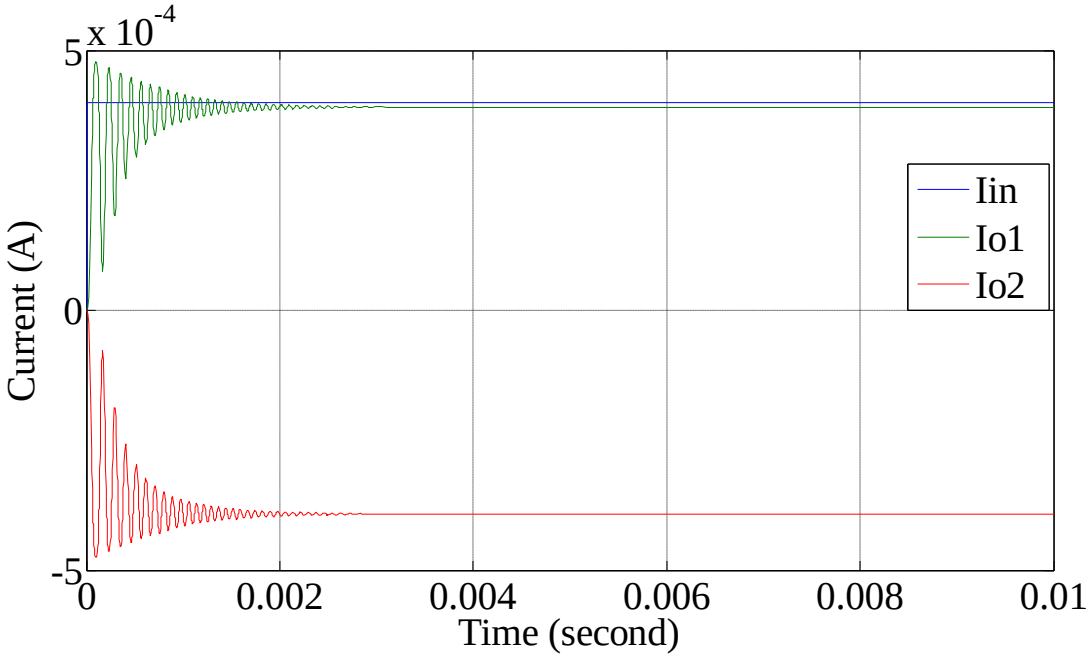

Fig. 4.3.7: Step response of a compensated fully differential second order low pass filter for $K_P=40$, $K_I=20{,}000$ and $K_D=10^{-5}$

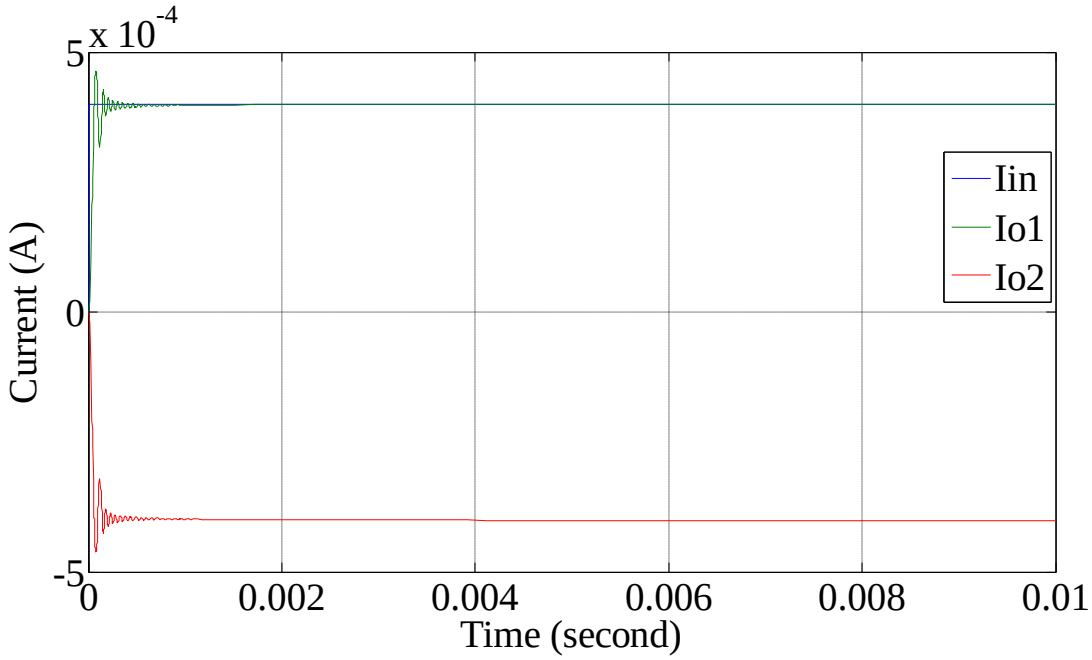

Fig. 4.3.8: Step response of a compensated fully differential second order low pass filter for $K_P=80$, $K_I=2000$ and $K_D=10^{-3}$.

Table 4.1: Observation from the step response of a fully differential system

Parameters	**Various System Configuration**			
	Open Loop Uncompensated System	***Closed Loop Uncompensated System***	***Closed Loop Compensated System for $K_P=40$, $K_I=2*10^4$, $K_D=10^{-5}$***	***Closed loop compensated System for $K_P=80$, $K_I=2*10^3$, $K_D=10^{-3}$***
Overshoot (in percentage)	59.6	53.25	21.5	15.88
Rise Time (in µs)	0.65	0.51	0.47	0.42

Without applying controller in open loop system, the error is $50\mu A$ at time= $3\mu s$. With controller the close loop system gives error $11\mu A$ at time= $1.5\mu s$ for $K_P=40$, $K_I=2*10^4$, $K_D=10^{-5}$ and $4\mu A$ at time= $0.5\mu s$ for $K_P=80$, $K_I=2*10^3$, $K_D=10^{-3}$.

4.4 Conclusion

In this chapter, a new fully differential current mode PID controller based on the nullor representation of a generalized fully differential block has been developed. The develop controller has been tested on a fully differential second order system whose open loop and closed loop time response study in PSPICE has been presented. The PID controller has been implemented using a DOCCII.

4.5 References

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CHAPTER V

SUMMARY AND CONCLUSION

5.1 SUMMARY

In this dissertation we have presented a study on designing and implementation of PID controllers using CM/VM active building blocks. The proportional-integral-derivative (PID) controller is one of the most important control elements used in the process control industry. In the following we present a summary of the work done in this project.

In Chapter I, the general description of the PID controller has been presented. Some background material on various current mode and voltage mode active building blocks used for the implementation of PID controllers has also been presented.

In Chapter II, history, characteristics, applications and CMOS/bipolar implementation of the current mode active building blocks used for implementation of PID controllers are briefly discussed. The devices described are OTA-C, DOCCII, CFOA, and CDBA.

In Chapter III, a brief discussion on the synthesis methods for analog PID controller using different current mode active blocks are described, with the help of signal flow graph techniques and their corresponding blocks. Design of OTA based, DOCCII based, CFA based and CDBA based PID controllers has been presented. The detailed simulation results on the time response studies on a OTA-based voltage mode PID controller and a DOCCII based voltage mode as well as current mode PID controller has been presented.

In Chapter IV, a new fully differential current mode PID controller based on the nullor representation of a generalized fully differential block has been developed. The develop controller has been tested on a fully differential second order system whose open loop and closed loop time response study in PSPICE has been presented. The PID controller has been implemented using a DOCCII.

5.2 FUTURE SCOPE

In this project emphasis was on using those blocks for implementation of PID controllers which could be implemented with off-the shelf available components. The work presented in this project may be extended to include the transistor level design of PID controllers. Furthermore we have not carried out frequency domain analysis of the closed loop systems. These studies may be carried out to give the complete quantitative characterization of the PID controller. Thus there is ample scope for extending this work.

CHAPTER VI

APPENDIXES

Appendix A

PSpice model files used for Process and electrical parameters CMOS 0.5um from MOSIS Technology

*Mosis Technology
*Valid range for n channel and p channel models‟ >= 0.4um, W >= 0.53um.
*AMI Semiconductor Barcelona
*Spice Level3 Parameters

.MODEL NMOS NMOS LEVEL=3 PHI=0.7 TOX=9.5E-09 XJ=0.2U TPG=1
+ VTO=0.7 DELTA=8.8E-01 LD=5E-08 KP=1.56E-04
+ UO=420 THETA=2.3E-01 RSH=2.0E+00 GAMMA=0.62
+ NSUB=1.40E+17 NFS=7.20E+11 VMAX=1.8E+05 ETA=2.125E-02
+ KAPPA=1E-01 CGDO=3.0E-10 CGSO=3.0E-10
+ CGBO=4.5E-10 CJ=5.50E-04 MJ=0.6 CJSW=3E-10
+ MJSW=0.35 PB=1.1

*SPICE LEVEL3 PARAMETERS
.MODEL PMOS PMOS LEVEL=3 PHI=0.7 TOX=9.5E-09 XJ=0.2U TPG=-1
+ VTO=-0.95 DELTA=2.5E-01 LD=7E-08 KP=4.8E-05
+ UO=130 THETA=2.0E-01 RSH=2.5E+00 GAMMA=0.52
+ NSUB=1.0E+17 NFS=6.50E+11 VMAX=3.0E+05 ETA=2.5E-02
+ KAPPA=8.0E+00 CGDO=3.5E-10 CGSO=3.5E-10
+ CGBO=4.5E-10 CJ=9.50E-04 MJ=0.5 CJSW=2E-10
+ MJSW=0.25 PB=1

PSpice model files used for Process and electrical parameters CMOS 0.35um from TSMC process

*TSMC 0.35um CMOS, code SCN4ME_SUBM
* Spice Level3 Parameters

.MODEL CMOSN NMOS (LEVEL = 3
+TOX = 7.9E-9 NSUB = 1E17 GAMMA = 0.5827871
+PHI = 0.7 VTO = 0.5445549 DELTA = 0
+UO = 436.256147 ETA = 0 THETA = 0.1749684

+KP = 2.055786E-4 VMAX = 8.309444E4 KAPPA = 0.2574081
+RSH = 0.0559398 NFS = 1E12 TPG = 1
+XJ = 3E-7 LD = 3.162278E-11 WD = 7.046724E-8
+CGDO = 2.82E-10 CGSO = 2.82E-10 CGBO = 1E-10
+CJ = 1E-3 PB = 0.9758533 MJ = 0.3448504
+CJSW = 3.777852E-10 MJSW = 0.3508721)
.MODEL CMOSP PMOS (LEVEL = 3
+ TOX = 7.9E-9 NSUB = 1E17 GAMMA = 0.4083894
+ PHI = 0.7 VTO = -0.7140674 DELTA = 0
+ UO = 212.2319801 ETA = 9.999762E-4 THETA = 0.2020774
+ KP = 6.733755E-5 VMAX = 1.181551E5 KAPPA = 1.5
+ RSH = 30.0712458 NFS = 1E12 TPG = -1
+ XJ = 2E-7 LD = 5.000001E-13 WD = 1.249872E-7
+ CGDO = 3.09E-10 CGSO = 3.09E-10 CGBO = 1E-10
+ CJ = 1.419508E-3 PB = 0.8152753 MJ = 0.5
+ CJSW = 4.813504E-10 MJSW = 0.5)

Appendix B

Dimensions of CMOS Transistors Used

Fig. 2.1.3: W=3µm and L=1.5µm for all CMOS (M1-M12)

Fig. 2.2.7: All transistors dimensions are given belows

Transistors	**W(µm)**	**L(µm)**
M1, M2	12	0.35
M3, M4	36	0.35
M_{xx} (in PMOS current mirrors)	18	0.35
M_{xx} (in NMOS current mirrors)	6	0.35