CHAPTER 1

Introduction

1.1 Motivation

In the present world wireless personal communication market has been growing explosively due to ever emerging new applications and dropping prices. A low cost, small, long-battery-life solution has been the dream for decades. Tremendous efforts have been made to the integration of such circuits in desirable low-cost technology in order to reach the goal. The applications of wireless communication devices include pagers, cordless phones, cellular phones, global positioning systems and wireless local area networks, transmitting either voice or data. A standard tells how devices talk to each other.

Numerous standards exist which are optimized for different implementations. For voice, examples include GSM, DCS, PCS, CDMA, and so on. For data, there are WLAN, Bluetooth, HomeRF and so on. Costs have been driven down by technology improvement and better design. The rapidly growing market and ever emerging new applications create a high demand for a low cost, low power, high portability transceiver solution.

A frequency synthesizer (FS) is a device that generates one or many frequencies from one or a few frequency sources. The output of an FS is characterized by its frequency tuning range, frequency resolution, and frequency purity. Ideally, the synthesized signal is a pure sinusoidal waveform. But in reality, its power spectrum features a peak at the desired frequency and tails on both sides. The uncertainty of a synthesizer's output is characterized by its phase noise (or spur level) at a certain frequency offset from the desired carrier frequency in unit of dBc/Hz.

Current commercial approaches utilize several high quality discrete components to provide high performance required by transceiver. High component counts and multiple chips in various technologies increase the cost and form factor. A higher integration level is required to lower the cost and form factor. Many efforts are underway to increase the integration level of the transceiver. The ultimate goal would be a single chip transceiver in a single technology with a minimum number of off-chip components, that is, an antenna to receive or transmit the RF signal, a power supply, and a crystal reference to provide a clean frequency reference. This single chip would act as an interface between the analog RF world and the digital baseband world. With high integration level, cost and form factor is reduced. However, many difficulties remain in the process of integration due to the lack of high quality components on chip. In a conventional double conversion receiver, the received signal spectrum is shifted down to the baseband in two steps.

During the first step, a local oscillator signal at RF is mixed with the RF signal, shifting the signal to a fixed IF frequency. To achieve this, the RF LO needs to be tunable and the minimum frequency step must be smaller or equal to the channel spacing of the standard.

Then a fixed local oscillator at IF is used to shift the mixed down version of the received signal to baseband.

The RF LO utilizes a low-phase-noise VCO which is coupled to a reference oscillator by a synthesizer loop of low bandwidth. The low bandwidth is desirable in order to minimize the spurious tones in the output frequency spectrum that result from the frequency comparison process. One consequence of the low synthesizer control bandwidth is that the phase noise of the overall synthesizer is dominated by the phase noise of the VCO. This makes the narrow loop bandwidth approach suitable for the implementation with discrete high Q components that is needed by the low phase noise VCO. The need for the external components is not amenable to integration of the synthesizer. The major challenge is to find ways to realize low-phase-noise synthesizers with low-Q components.

One approach is to use a wide synthesizer control bandwidth to couple a noisy on-chip oscillator to a very-low-phase-noise crystal more closely than a conventional narrow-band PLL so that the output is more dependent on the clean reference. The phase noise contribution from the on-chip oscillator to the output close to the carrier within the synthesizer control bandwidth is thus suppressed. Because a wide PLL bandwidth requires a high comparison frequency, this type of synthesizer is most amenable to the synthesis of a few widely spaced frequencies, and is thus most compatible with block down-convert receiver architectures such as the wideband IF double conversion architecture .

The IF frequency synthesizer in the wideband IF architecture is used to tune the individual channels. Because this second synthesizer is at a much lower frequency, minimization of its phase noise contributions is much easier. But the spurious tone specifications is much harder because the reference frequency to the PLL is now at the channel spacing. One approach is to use a narrowband PLL which suppresses the tones outside the PLL bandwidth. By doing the channel selection at IF, the divider ratio required is RF/IF times smaller than doing it at RF. The smaller divider ratio not only reduces the tones generated by the PLL assuming a fixed PLL bandwidth, but also reduces the phase noise contribution to the output from the frequency reference, the phase detector and the divider.

For many applications transceiver integration levels will be such that the receiver path, transmit path, the complete synthesizer, and perhaps the RF power amplifier will coexist on a single integrated circuit, along with a significant amount of A/D conversion and baseband processing. This in turn requires the synthesizer maintain its phase noise and spurious tone performance in the presence of components which deliver significant current and voltage perturbations to both the substrate GND and supply. Fully differential implementation of the complete PLL path is important for this reason.

1.2 Aims and Goals

The main aim of the report is to design and analyze the frequency synthesizer circuit for wireless communication systems. Basically the designed frequency synthesizer of phased lock loop consists of five components

1. Phase frequency detector
2. Charge pump
3. Loop filter
4. Voltage control oscillator
5. Frequency divider

The above mentioned components of the Phase locked loop has to be designed in order to maintain its precise characteristics of its functionality.

1. The PFD should be designed without dead zone and should operate at relatively slow speed

2. As the charge pump is responsible for adding or removing charge from the loop filter, which in turn will increase or decrease the control voltage on the VCO.

3. Loop filter which acts as low pass filter is designed inorder to remove non-linearities of the signal which is the output of the charge pump.

4. The VCO is designed which has the linear characteristics for frequency to the control voltage, should have wide tuning range .

5. The simple frequency divider is to be designed which operates in the high frequency range.

1.3 Thesis Organization

The complete thesis is organized in four chapters.

The chapter1 described the motivation and introduction to the frequency synthesizer used in phased lock loop systems.

The chapter2 explain the fundamental principles and basics of the synthesizer design. It also explains the traditional architectures of the components of the phased lock loop like phase frequency detector, charge pump, loop filter, voltage control oscillator and frequency divider.

The chapter3 explain the detailed description and design procedure of the each individual components of the phase locked loop. The simulation results of each component in presented along with schematic and symbolic representation.

The chapter 4 explain the conclusion and future work of the concept of the frequency synthesizer.

CHAPTER 2

Phase Locked Loop Fundamentals

2.1 Basic introduction to PLL

Well-timed on-chip clocks for various applications such as clock-and-data recovery, microprocessor clock generation and frequency synthesizer Phase locked loops (PLLs) generate. The basic concept of phase locking has remained the same since its invention in the 1930s. However, design and implementation of PLLs continue to be challenging as design requirements of a PLL such as settling and low phase noise become more stringent. A large part of this thesis focuses on the design of a PLL for high frequency and high performance digital systems. In order to understand the challenges and trade-off behind the design of such a PLL, this chapter provides a brief study of Phase locked loops.

Introduction to PLL

The basic block diagram of a PLL is shown in Figure.2.1.1 A PLL is a closed-loop feedback system that sets fixed phase relationship between its output clock phase and the phase of a reference clock. A PLL tracks the phase changes that are within the bandwidth of the PLL. A PLL also multiplies a low-frequency reference clock, fout , to produce a high frequency signal, fref . The basic operation of a PLL is as follows. The phase frequency detector produces an error output signal based on the phase difference or frequency difference between the feedback signal from divider output and the reference signal. Over time, small frequency differences accumulate as an increasing phase error. The difference or error signal is low pass filtered and drives the oscillator

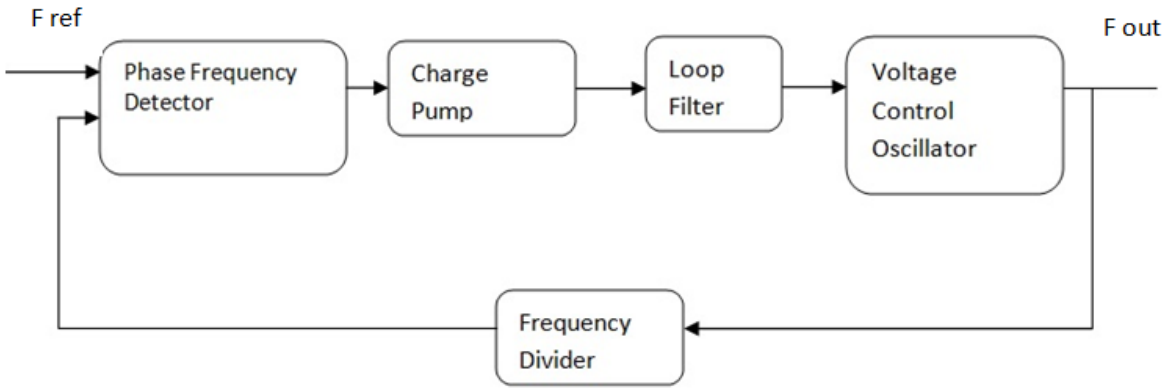


Figure 2.1.1: Basic block diagram of PLL

The filtered error signal acts as a control signal (voltage or current) of the oscillator and adjusts the frequency of oscillation to align Φdiv with Φref. The frequency of oscillation is divided down to the feedback signal by a frequency divider. The phase is locked when the feedback signal has a constant phase error and the same frequency as the reference

clock. Because the feedback signal is a divided version of the oscillator's signal frequency, the frequency of oscillation is N times the reference signal.

Components of the Phased lock loop

The below figure2.1.2 represents the block diagram of a charge-pump PLL. A PLL comprises of several components:

(1) Phase frequency detector,
(2) Charge-pump,
(3) Loop filter,
(4) Voltage-controlled oscillator
(5) Frequency divider.

The chapter 2 describes the detailed fundamentals and concept of each individual block of the Phase locked loop.

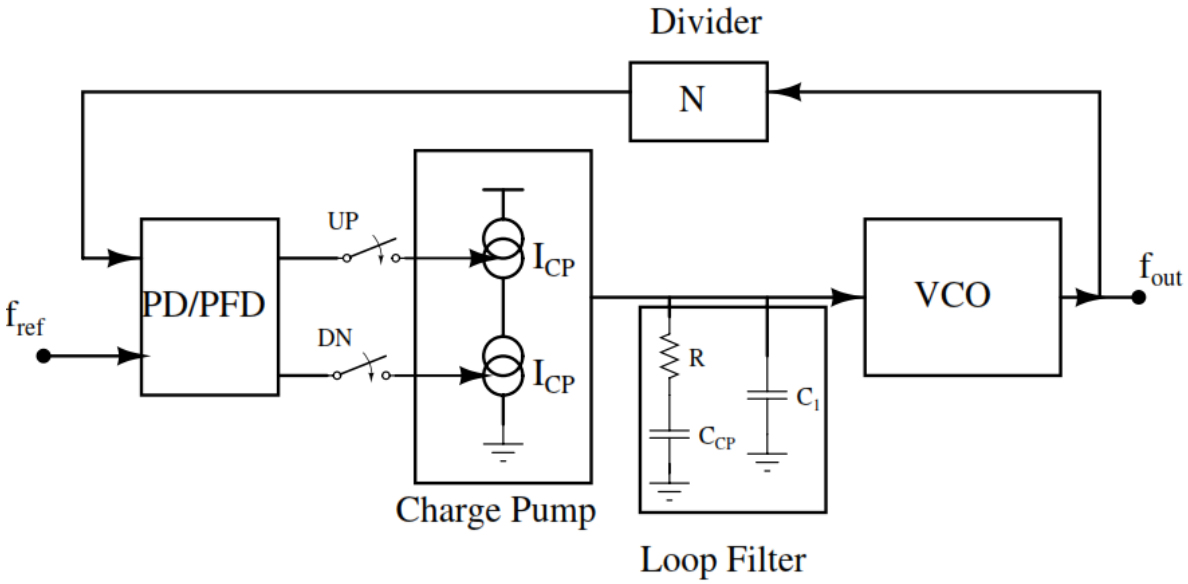


Figure 2.1.2 Representation of individual block of Phase locked loop

2.2. Phase frequency detector

2.2.1 Phase detectors

In a phase locked loop circuit, the emphasis on the first block is phase detector which plays a role of comparator, results a signal which is function of input signal to the system and output signal of the voltage control oscillator. Let us assume Θdiff represents the phase difference of the resultant when comparing the input signal phase and vco signal phase. The phase difference and produced by the resultant comparator produces a proportional voltage Vd.

The relation characteristics of Θdiff & vd is shown in the figure2.2.1

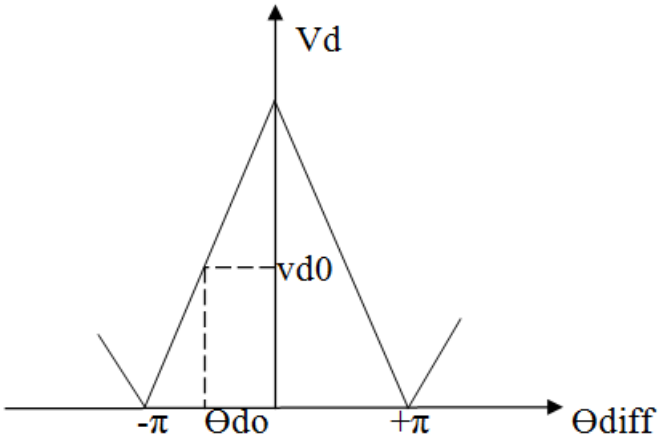


Figure 2.2.1: Phase detector characteristics

Observations from phase detector characteristics determine the curve is linear and periodic with period 2π radians.

When the phase difference is zero between the two inputs of the phase detector generates a free running voltage vd0. The obtained free running voltage vd0 is associated with phase Θdo which is π/2 as shown in the figure2.2.2. Basic ideology is that the phase difference of zero should be obtained for free running voltage vd0 of the phase detector. By this statement we conclude the expression for thee phase error.

$$\Theta e = \Theta d - \Theta do$$

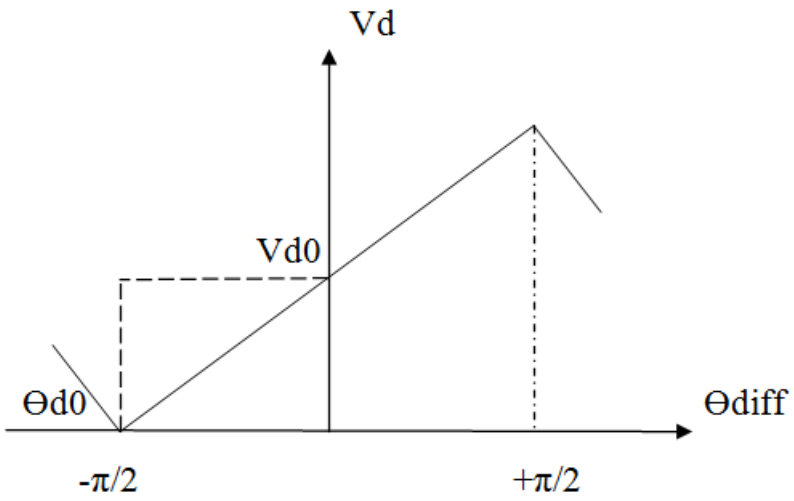


Figure 2.2.2: Shifted characteristics of phase detector

We can observe the linear characteristics of phase detector in the range of (-π/2, +π/2)

We can conclude the expression for slope of the curve from the shifted characteristics of phase detector

$$K_d = \frac{dv_d}{d\theta_e}$$

The following equation represents the general model of the phase detector.

$$v_d = K_d\theta_e + V_{do}$$

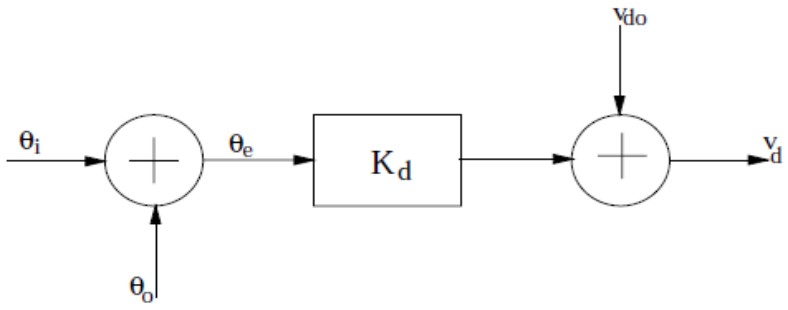


Figure 2.2.3: General model of phase detector

There are numerous ways to implement a phase detector circuit but the most common approach is multiplication phase detectors. The most important multiplying digital phase detectors are the following

I. The ex-or gate
II. J_K flip-flop
III. Phase frequency detector

The basic principle operation of the mentioned phase detectors are multiplying the input signal to voltage control oscillator signal which results in a error signal which is function of phase error of the resultant.

The detector XOR circuit produces error pulses on both rising and falling edges, other types of phase detectors may respond only to positive or negative transitions.

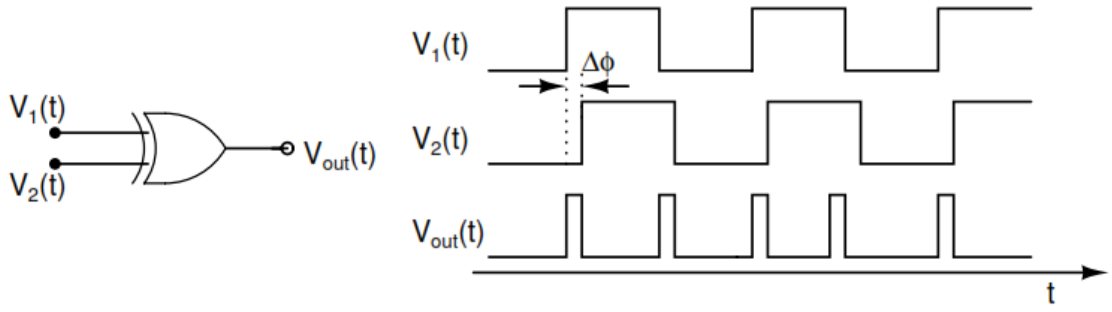


Figure 2.2.4: Exclusive OR gate as phase detector

There are different types of the phase detectors used in phase lock loop design. analog type multipliers accepts the sinusoidal inputs where as the digtal type multipliers used the digital pulse signals as the inputs. there are both advantages and disadvantages on both types of phase detectors for accurating in both phase and frequency measurements.

2.2.2 Phase frequency distortion

The basic understanding of Frequency distortion and phase distortion are as follows:

1. Frequency distortion

Practically the signal is not a simple sinusoidal voltage but it is a complex shaped wave. such a signal is equivalent to a signal obtained by adding a number of sinusoidal voltages of different frequencies. These sinusoidal voltages are called the frequency components of the signal. if all the frequency components of the signal are not amplified equally well by the amplifier frequency distortion is non-constant gain for different frequencies. This occurs due to the inter electrode capacitance of the active device and other relative components of the circuit.

2. Phase distortion

This type of distortion occurs if the relationship between the various frequency components making up the signal waveform is not the same as in the output.the main cause of the phase distortion is the reactive components of the circuit.this distortion is not important in audio amplifiers because our ears are not capable of distinguishing the relative phase of different frequency components but this distortion is considerable in audio amplifiers used in television.

In the frequency synthesizing operation in phase lock loop the input signal applied is digital hence we require digital phase detector in the design. among the present available phase detectors the phase frequency detector turns out to be the best with its accuracy in the operation performance.PFD provides unlimited pull inrange which guarantees digital phase lock loop acquisition under the critical operating condition.

When a PLL circuit is turned on,its output of VCO operates at a frequency far from the input frequency , i.e., the loop is not locked. The non-linear Phenomenon is observed in transition of loop from unlocked state to locked condition because phase detector senses unequal frequencies . the acquisition range is in the order of Wlpf that is loop locks only if the difference between win and wout is less than roughly wlpf. In the typeI PLL, if thw Wlpf is reduced to suppress the ripple on the control voltage, the acquisition range decreases . this drawback of decrease in acquisition range decreases. This drawback of decrease in acquisition range is rectified in modern PLL incorporate frequency detection in addition to phase detection.

The basic principle is to compare win and wout by means of a frequency detector, generating a dc component Vlpf2 which is proportional to win-wout and applying the obtained result to voltage control oscillator in negative feedback loop. At intial stage, FD drives wout towards win while PD remains unfunctional. When difference value is relatively small the phase lock loop takes over acquiring lock.

The schematic overview increases the acquisition range to the tuning range of voltage control oscillator.

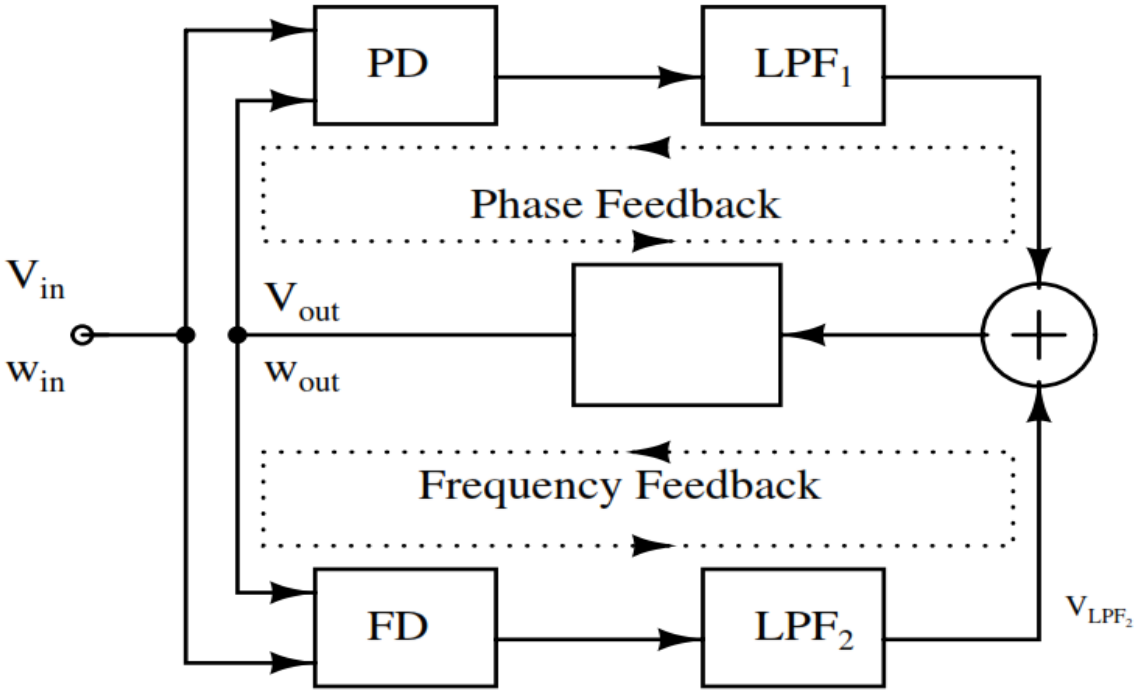


Figure 2.2.5: Addition of frequency detection to increase the acquisition range

For periodic signals it is possible to merge the two loops by devising to merge the two loops by devising a circuit that can detect both phase and frequency differences called a phase frequency detector shown in figure 2.2.5.

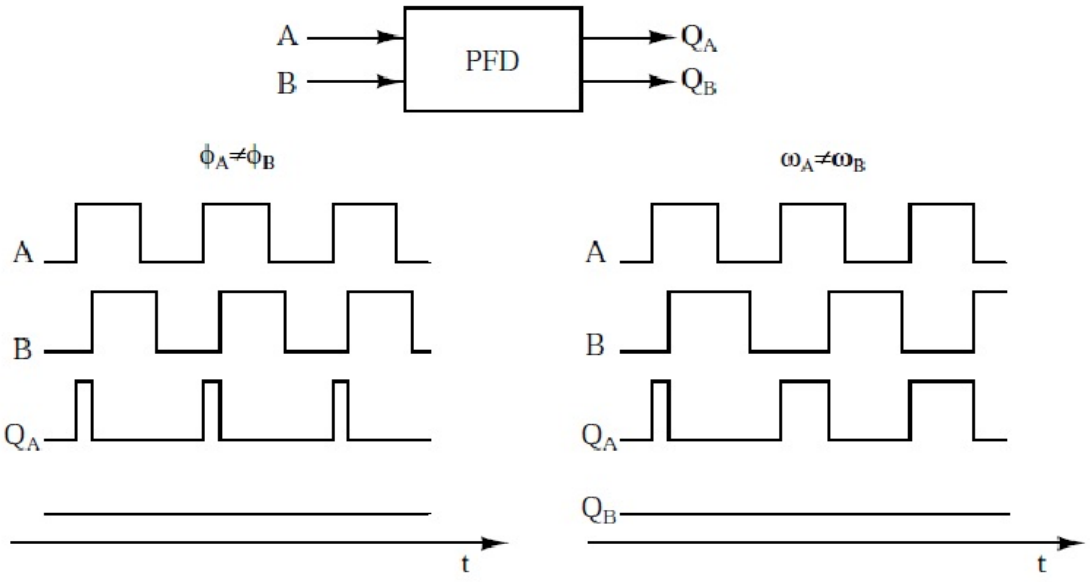


Figure 2.2.6: Conceptual operation of PFD

The circuit employs sequential logic to create three states and respond to the rising (or falling) edges of the two inputs explained in the figure2.2.6.

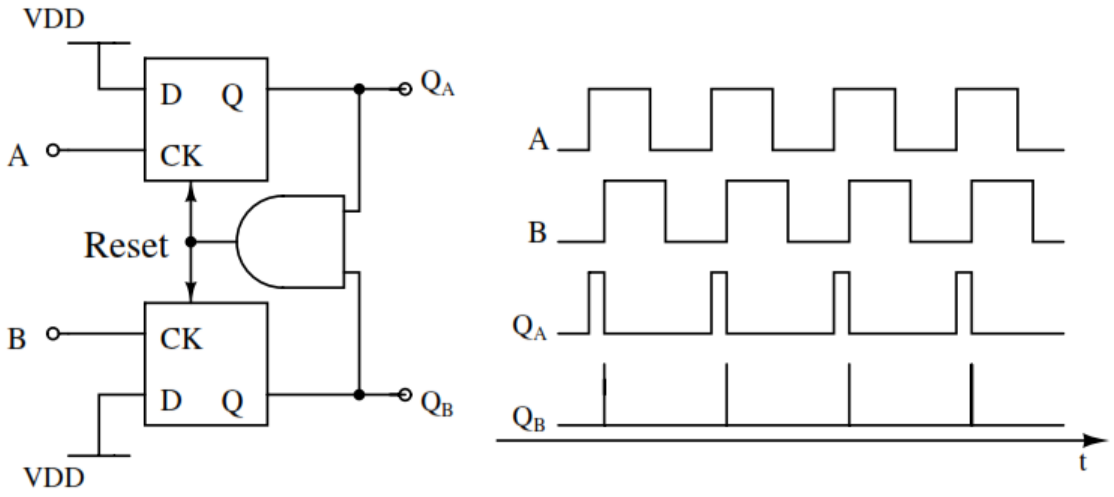


Figure 2.2.7: Traditional PFD design

If initially QA= QB= 0, then a rising transition on A leads to Q = 0.The circuit remains in this state until B goes high, at which point Q returns to zero. The behaviour is similar for the B input. The outputs QA=1 and QB=0 are called the "UP" and "DOWN" pulses, respectively. The circuit of can be realized in various forms.Figure 2.1.7 shows a simple implementation consisting of two edge-triggered, resettable D flipflops with their D inputs tied to a logic ONE. The inputs of interest, A and B, serve as the clocks of the flipflops. If QA=QB=0, and A goes high, QA rises. If this event is followed by a rising transition on B, QB goes high and the AND gate resets both flipflops. In other words, QA and QB are simultaneously high for a short time but the difference between their average values still represents the input phase or frequency difference correctly. The input-output characteristics of the above PFD can be plotted.

Defining the output as the difference between the average values of QA and QB when A = B and neglecting the effect of the narrow reset pulses, it can be noted that the output varies symmetrically as begins from zero. For ΔΦ=360 degrees Vout reaches its maximum or minimum and subsequently change sign. The primary advantages of the phase detector architectures shown in Figure2.2.7 are its size and simplicity. Unlike the classic architecture and the four RS latch architecture which require 9 and 10 standard cells, respectively, to construct, this architecture requires only 5 cells, two for each flip-flop and one the AND gate. In addition, the behavior of this phase detector is conceptually simpler.

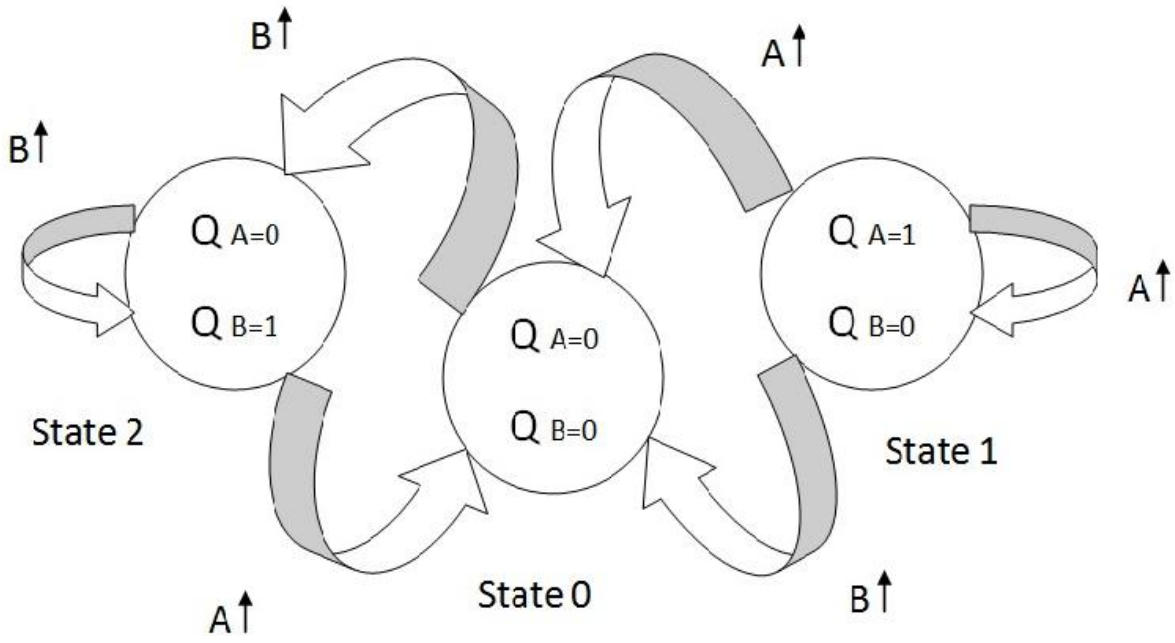


Figure 2.2.8: State diagram of phase frequency detector

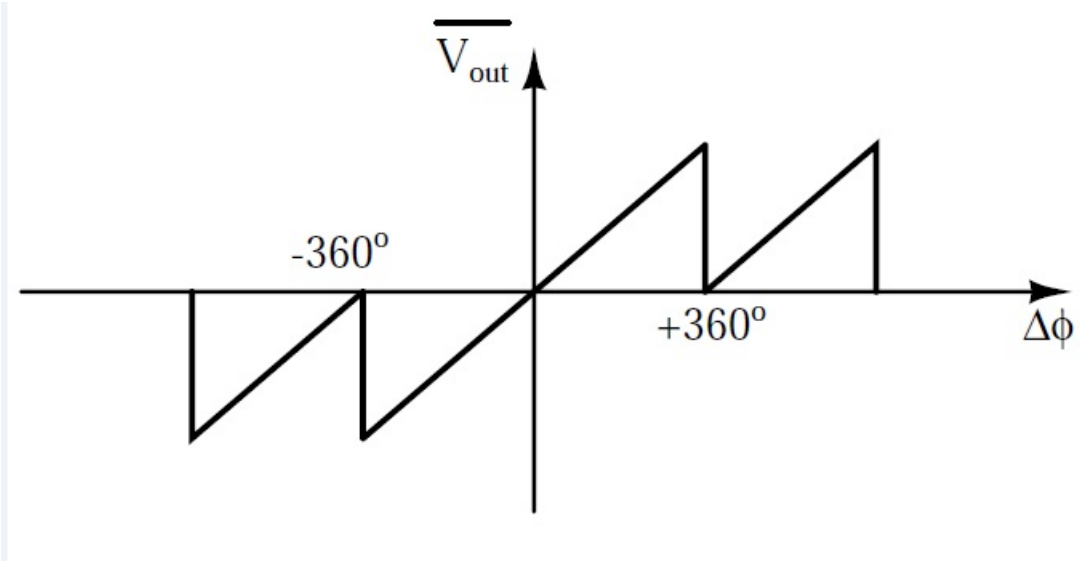


Figure 2.2.9: Input-output characteristic of the three-state PFD.

Consider the case where the reference signal is leading the feedback signal. When the reference signal transitions high, the associated flip-flop is clocked, causing the high signal on its data input to be passed through to its output. This corresponds with the UP output signal being asserted. The delay before the output transitions is equal to the flip-flop clock-to-Q delay. This signal will now stay high regardless of what the reference signal does until the phase detector's state is reset. Next, the feedback signal clocks the second flip-flop, causing the DN output to be asserted. When the DN output asserts, the AND gate will cause both flip-flops to be reset, thus resetting the state of the whole phase detector. The length of time for which both outputs will be asserted is equal to one gate delay plus the flip-flop reset-to-Q delay. Assuming the same limiting case as for the previous architectures, the maximum operating frequency for this phase detector will be

$$F_{max} = \frac{1}{2(T_{clk-q} + T_d + T_{rz-q})}$$

The flip-flops used with this design must accept an asynchronous reset signal. Also, the type of flip-flop used will generally have an all-overriding reset, meaning that its output can not be asserted as long as the reset signal is high.

2.2.3 Dead zone

Dead zone is minor difference in the phase of the inputs that a phase frequency detector will not able to detect. The other main reasons is due to the delay time of the logic components and reset of feedback path of flipflops. Figure 2.2.10 explains the dead zone problem.

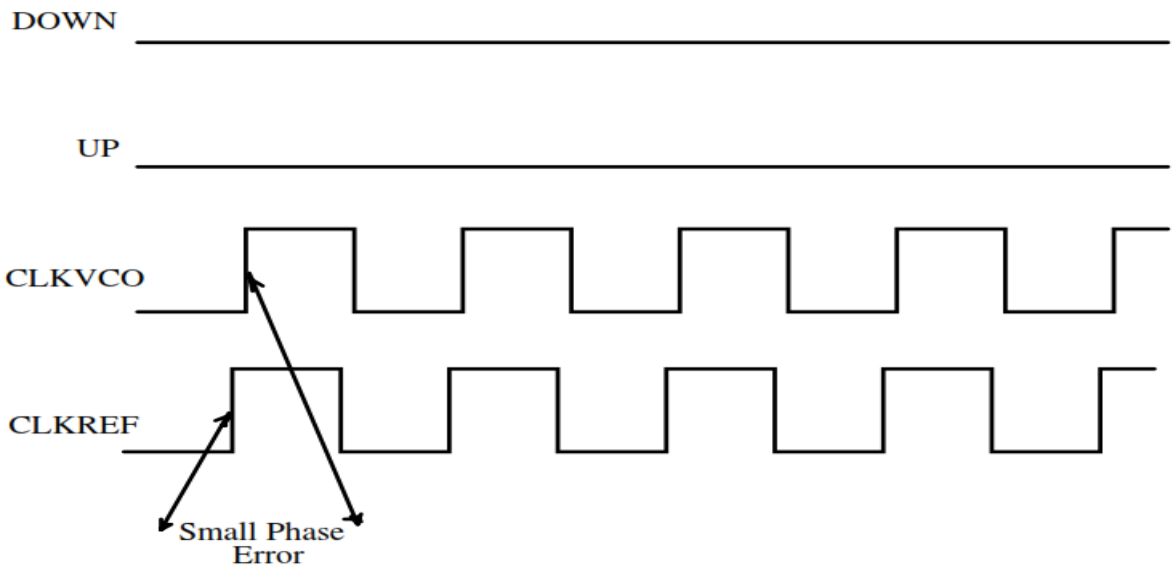
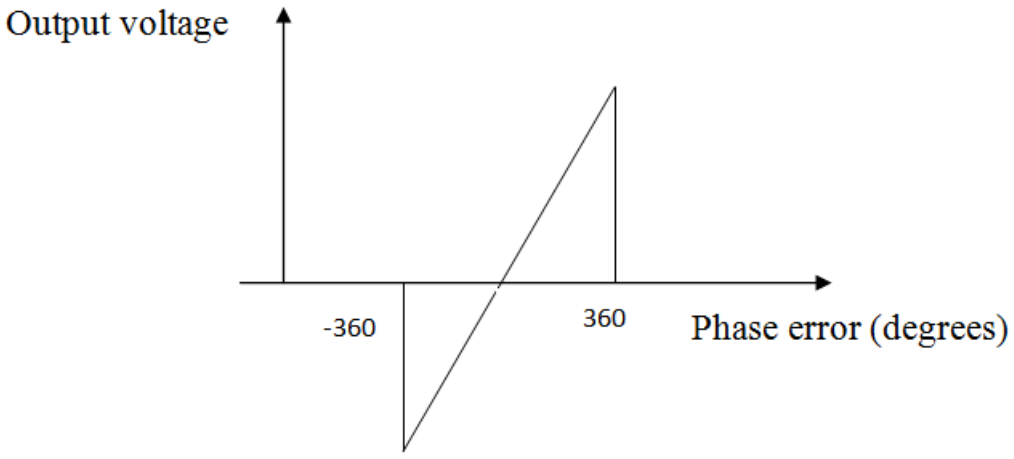
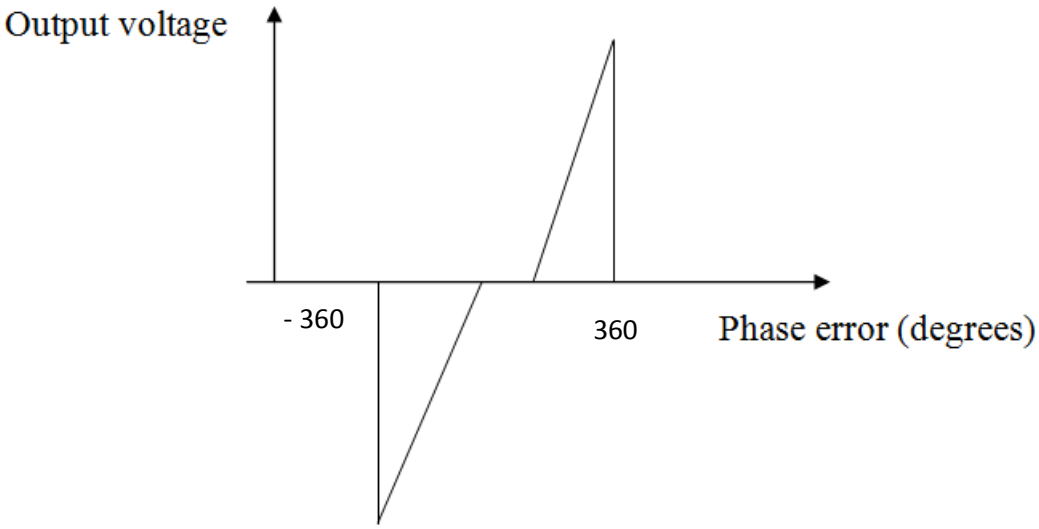


Figure 2.210: Dead zone representation by waveforms



a. No dead zone



b. Presence of dead zone

Figure 2.2.11: Phase error Vs output voltage a) No dead zone

b) Presence of dead zone

The dead zone of phase frequency detector relations becomes non-linear around zero. A large number of solutions are made in order to eliminate this undesirable effect by reducing the delay time in internal components of the PFD and also by creating new reset techniques that eliminate the delay constraints.

2.3 Charge pump

The output of a PFD can be converted to DC (voltage/current) in many different ways. Since the difference between the average values of QA and QB is of interest, the two outputs can be low-pass filtered and sensed differentially, as shown in Figure. A more common approach is to interpose a “charge pump”(CP) between the PFD and the loop filter. A charge pump consists of two switched current sources that pump charge into or out of the loop according to two logical inputs. Figure 2.3.1 illustrates a charge pump driven by a PFD and driving a capacitor.

The circuit has three states. If QA=QB=0 then S1 and S2 are off and Vout remains constant. If QA is high and QB is low, then I1 charges CP. Conversely if QB is high and QA is low, then I2 discharges CP Thus if, for example, A leads B, then QA continues to produce pulses and Vout rises steadily called UP and DOWN currents, respectively,I1 and I2 nominally equal.

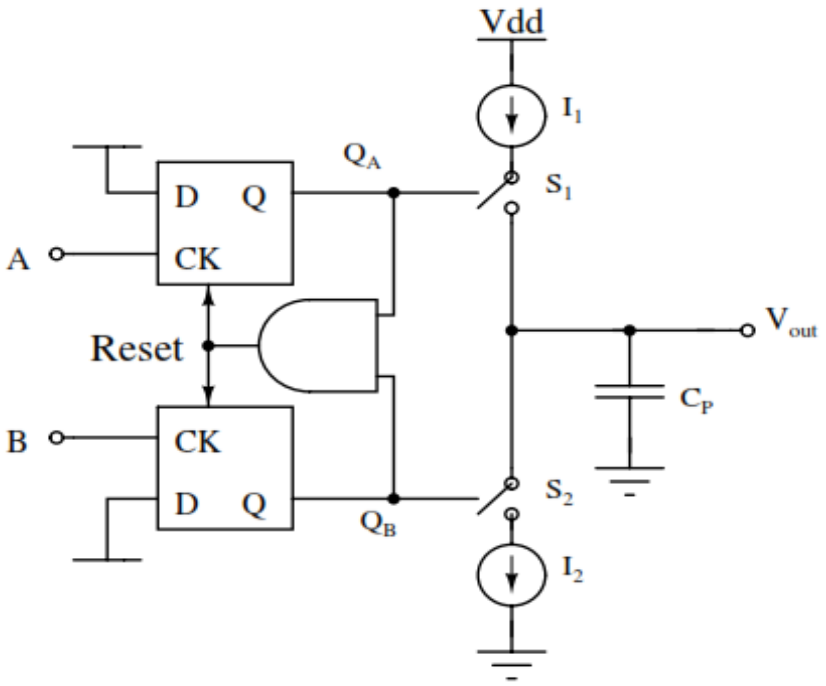


Figure 2.3.1: Phase Frequency detector with charge pump

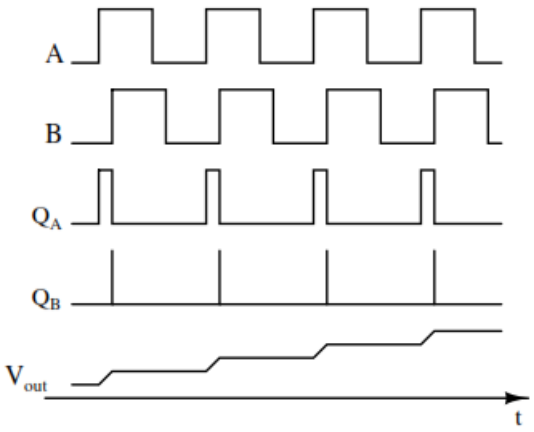
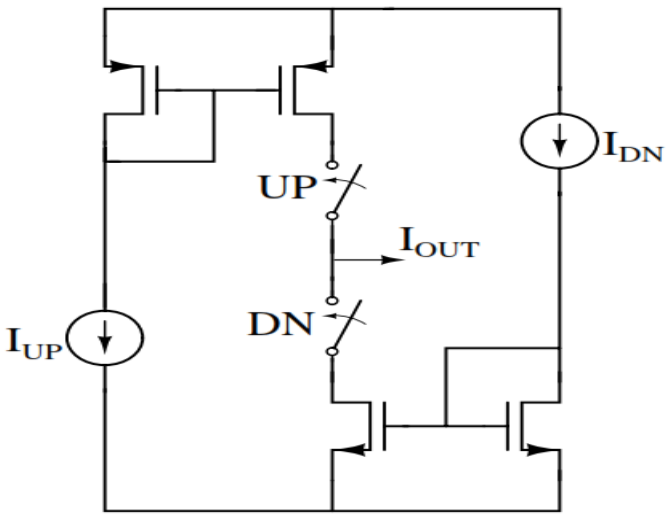


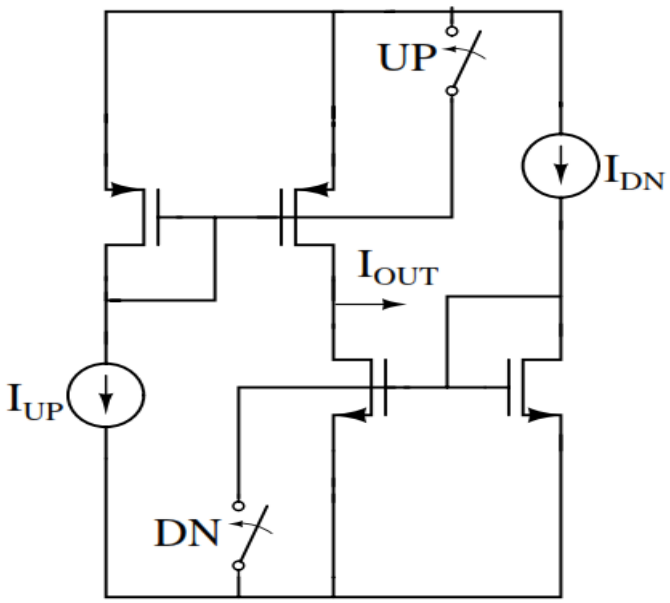
Figure 2.3.2: Output waveform of combination of PFD and Charge pump

2.3.1Charge pump architectures

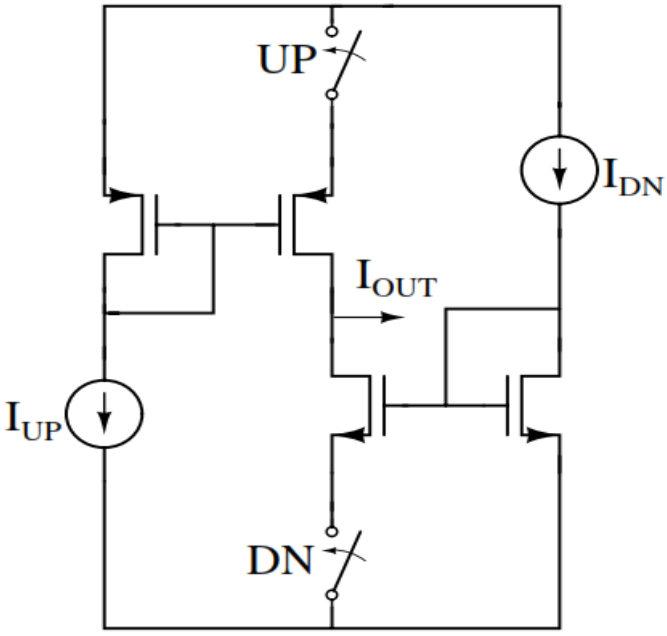
Three generic topologies of charge-pumps are shown in Figure.2.3.3.The switch is put at the drain, gate and source of the current source (or sink) transistor in Figure. (a), (b) and (c), respectively. The one with switch at drain has the shortest switch time, but its peak current matching is a problem. The one with switch at gate has the longest switch time and it is less used in practice. Charge-pumps using the current steering



a. Switch in drain



b. Switch in gate



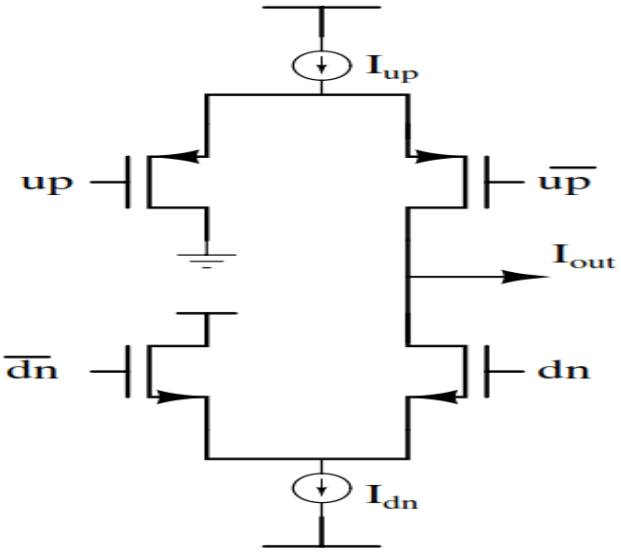
a. switch in source

Figure 2.3.3: Simplified schematic of generic charge-pumps

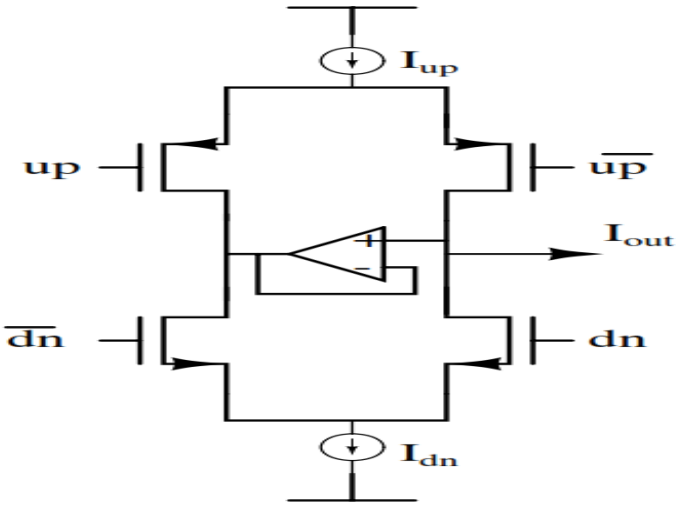
a) switch in drain b)switch in gate c)switch in source

technique shown in Figure.2.3.4 feature faster transient response and no supply current glitches. A buffer is used in Figure.2.3.4.b (b) to better match the charge and discharge currents, and to minimize charge sharing at the output. The charge pump in Figure.2.3.4 (c) uses symmetric switches, but the two switch-to-output paths are asymmetric.

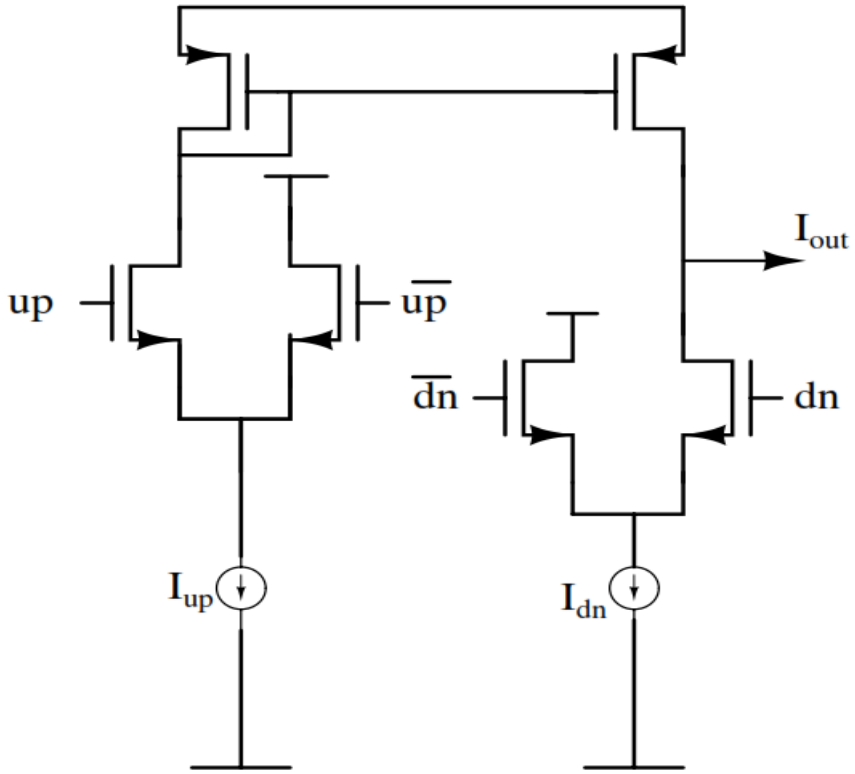
Many efforts have been made to improve current matching and/or reduce charge injection and charge-sharing due to switching operation in the literature. However, we also need to pay attention to the transient characteristic of charge pump because the PFD pulse width is very small (typically around 1ns) in the locked state.



a. basic block



b. with buffer



c. nmos switch only

Figure 2.3.4: Current steering charge-pumps

Fast and symmetrical transient response is critical for good matching in the charge pump. Fortunately, the reference frequency is very high in the fractional-N synthesis and the reference spur is much less concerned. The Simplified schematic of the charge pump in the prototype PLL is the same as the one illustrated in Figure.2.3.4 (a). It has the properties of fast transient response and good timing delay matching from switching controls, and DN , to output current Iout.

2.3.2 Non Ideal Effects in Charge Pump

1. As shown in above figures switches are constructed using PMOS and NMOS. The inherent mismatches between these two switches results in mismatch in charging and discharging current in addition to timing mismatch. Hence there is variation in control voltage at the output. In fact the ratios W/L are adjusted so as to have equal UP and DOWN currents. Even though, mismatching is observed between these currents in simulation. That means, since two current sources are themselves mismatched, the control voltage experiences the random changes in it.

2. There is also problem of charge sharing between output node of CP (in fact between filter capacitor) and the parasitic capacitances between drain and source of switch transistors. This results in sudden change in control voltage which may disturb the VCO.

3. Another effect is clock feed through. The high frequency signal provided at the gate of switch transistor passes to the output node via gate to drain parasitic capacitor Cgd. This also results in jumps in control voltage. Since the VCO sensitivity is high, even a small jump in control voltage results a large jump in output frequency.

4. Another effect is limited output voltage. If we want higher output voltage the current source value must be increased. This is not possible in every condition, since that increases power consumption also.

Apart from this reference spur in PLL is also one of the critical problem which arises due to current mismatches in charge pump. To remove the non ideal effects in CP, so many different architectures are proposed. In practice charge pumps are roughly classified into two categories. “Single ended charge pump” and “Differential charge pump”.

2.3.3 Single Ended and Differential Charge Pumps

In single ended charge pump only two inputs UP and DOWN are given to the respective switches, while in differential charge pump two outputs of PFD are given to the two differential switches with each input inverted and given to the second input of the respective switch. Figure2.3.5 shows one of the examples of differential charge pump. Without going into the details of differential charge pump, the advantages and limitations of differential charge pump are listed below.

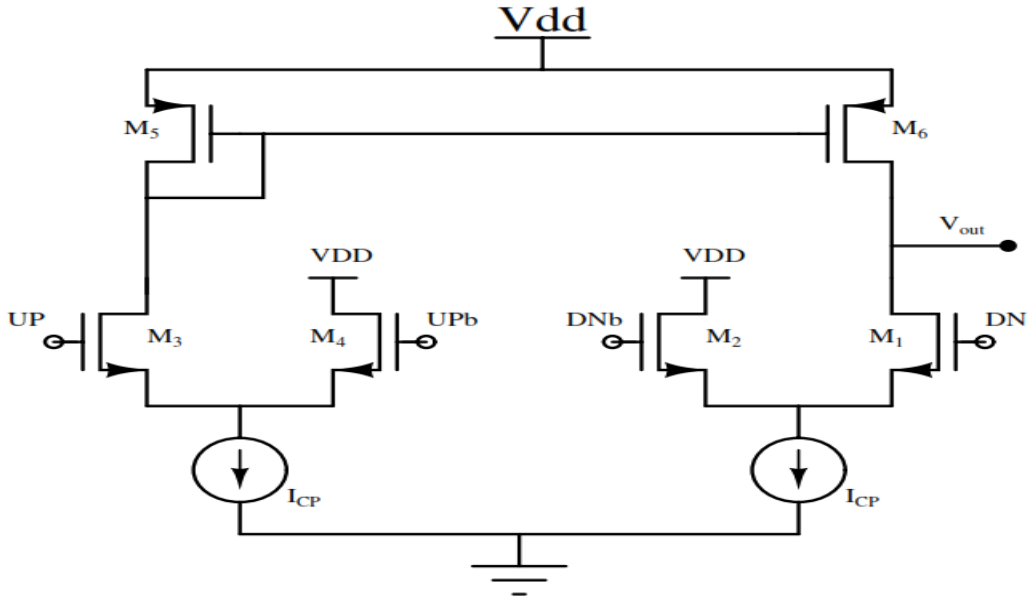


Figure 2.3.5: Current steering differential charge-pumps

Advantages of Differential Charge Pumps

1. The switching mismatch between NMOS and PMOS does not affect the overall performance substantially. The matching requirement between NMOS and PMOS transistors are relaxed to the matching between NMOS or between PMOS transistors respectively.

2. The differential CP uses switches using NMOS and the inverter delays for UPb and DNb signals do not generate any offset due to its fully symmetric operation.

3. This configuration doubles the range of output voltage compliance compared to single ended charge pump.

4. Differential stage is less sensitive to the leakage current since leakage current behaves as common mode offset with the dual output stages.

Limitations of Differential Charge Pumps

Though differential CP has many advantages listed above, they suffer from critical drawbacks. They require two loop filters and common mode feedback circuitry. Since more number of transistors are required, with two or more current sources, they occupy large silicon area. This also leads to higher power consumption.

Limitations of Single Ended Charge Pumps

1. Switch mismatch, clock feed through, charge sharing problems are still not eliminated fully.

2. Limited output voltage compliance range. For source CP shown above if we want higher output voltage we have to increase the charging and discharging current values.

3. Switch mismatch also results in timing mismatch as well as dead zone.

4. Parasitic capacitances are dominant in single ended CP. Using of OPAmp may solve above mentioned problems; but designing of OPAmp it itself tedious process and also increases unnecessary hardware.

Even though single ended charge pump has these disadvantages, they are more popular than differential design, because they do don't require two loop filter and offer tri-state operation with lower power consumption. Also the problems listed above are not those much difficult to handle. With proper modification into the architecture, these problems can be eliminated or minimized easily. Also, single ended charge pumps require fewer

components than differential charge pumps; hence they occupy less area in a chip. In the next session we will discuss the different architectures of single ended charge pumps with their simulation and comparison.

2.4 Loop filter

The output of the combination of phase frequency detector and charge pump leads to a signal which is composed of dc component with a superimposed undesirable ac component. The loop filter is basically a low pass filter which eradicates the undesirable ac component of the resultant signal. Loop filter is considered to be the important block in design of PLL system because it determines the overall performance of the system.

There are two different type of loop filters, active and passive type loop filters. Present technology applications utilize an active filter based on operational amplifier concepts. the most simpler in design and easily monitored is passive type loop filters.

The design of the loop filter is basic idea of selecting the bandwidth of the Phaselock loop. The PLL system with absence of loop filter in the design is considered as the first order loop filter which offers little noise suppression. Hence we prefer the higher order passive type loop filter in the design for better noise cancellation and better performance.

As already mentioned that the out signal of combination of PFD and CP consists dc component which is proportional to the phase error, the remaining terms are of ac components having frequencies of 2w1,4w2,……etc. These higher frequencies are undesirable which are filtered out by the low pass filter. The basic principle of loop filter is to suppress the higher frequency signals and pass the lower frequency components.

Consider the first order low pass filter as shown in the figure2.4.1.a The closed loop filter transfer function of the above typeI PLL is given by

$$H(s) = \frac{\frac{I_p K_{VCO}}{2\pi C_p}}{s^2 + \frac{I_p K_{VCO}}{2\pi C_p}}$$

The closed loop system contains two imaginary poles at

$$S_{1\,2} = \pm j \sqrt{\frac{I_p K_{VCO}}{2\pi C_p}}$$

and is therefore unstable.The instability arises because the loop gain has only two poles at origin.(two integartors).as shown in the figure 2.4.1.b each integrator contributes a constant phase of 90 degress allowing the system to oscillate at the gain crossover frequency.

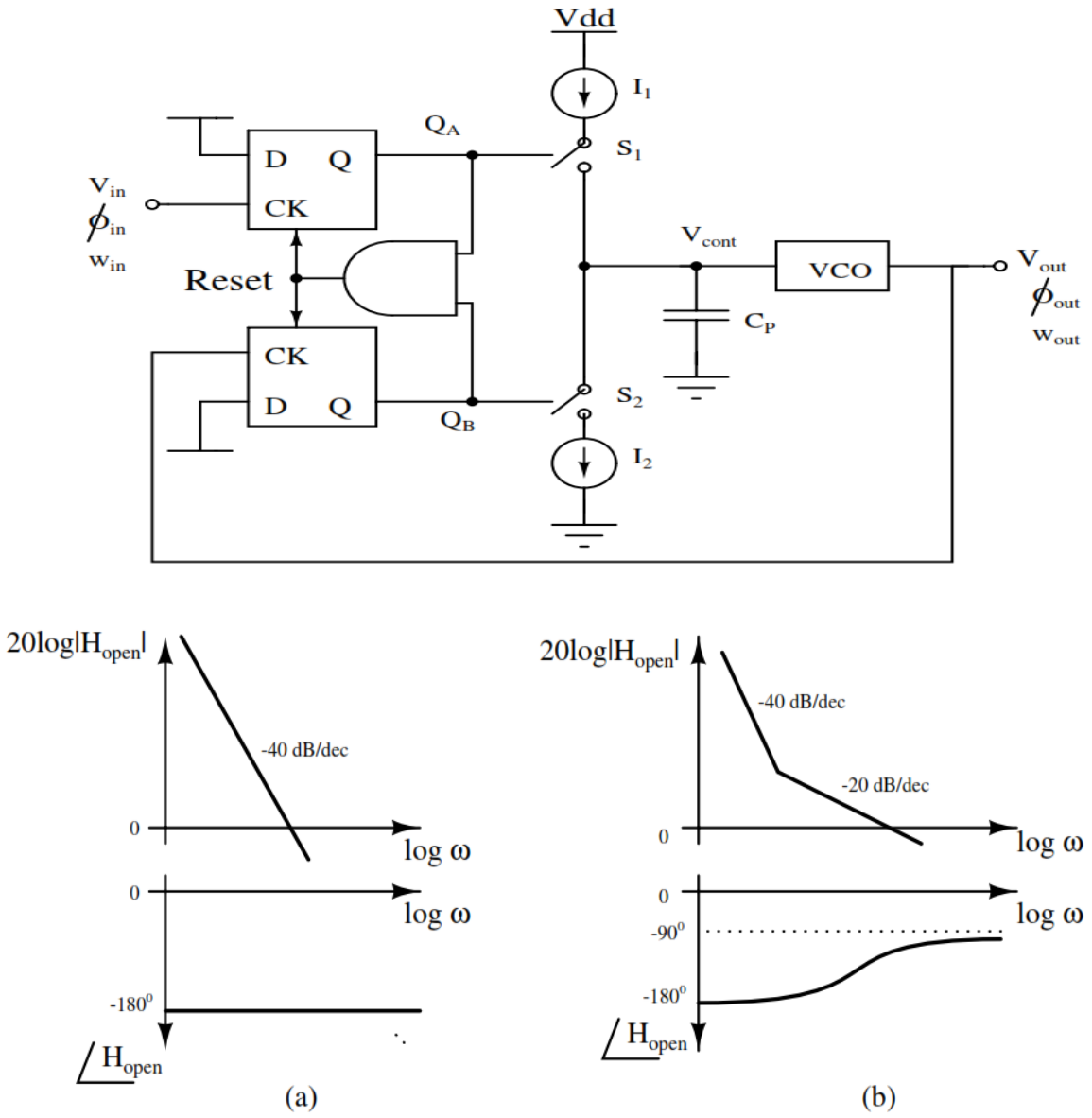


Figure 2.4.1(a) First order low pass filter (b) Loop gain characteristic of simple charge-pump PLL (c) addition of zero

In order to stabilize the system we must modify the phase characteristics such that the phase shift is less than 180 degress at gain crossover frequency. This task is accomplished by introducing a zero in the loop gain, i.e., by adding a resistor in series with the loop filter capacitor as shown in figure 2.4.1.c

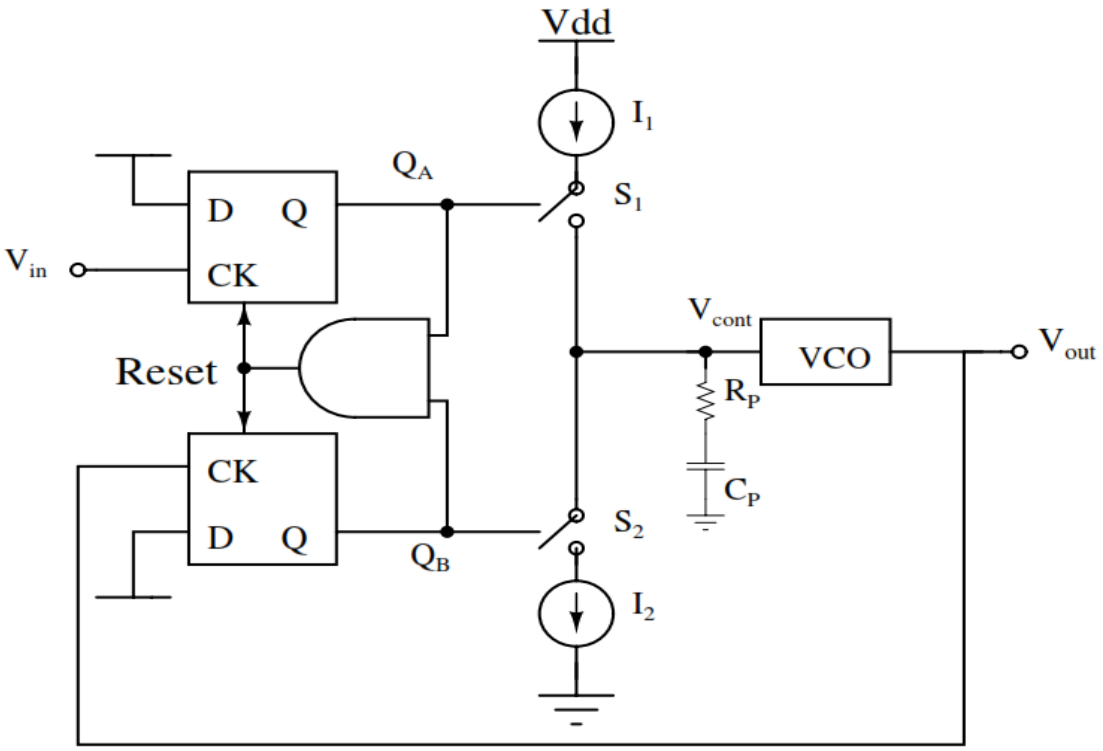


Figure 2.4.2: Addition of zero to charge-pump PLL.

The compensated type II Phase lock loop of figure2.4.2 suffers from a major drawback, because the charge pump drives the combinational circuit of resistor Rp and capacitor Cp, every time current is injected in the loop filter the control voltage experiences a large drift. Even though the in the locked condition the mismatch between I1 and I2 and the charge injection and clock feed through S1 and S2 introduce voltage drift in Vcont. This leads to adverse effect of ripples which disturbs the performance of VCO, resulting in error of output phase. Inorder to compensate the mentioned undesirable effects the second capacitor is added in parallel wih Rp and Cp suppressing the ripples.

The loop filter which is of second order filter now yielding to third order PLL by introducing the capacitor in parallel with Rp and Cp combination, creating difficulties in stability issues. If C2 is adjusted to about one fifth of CP the closed loop time and frequency responses remain unaffected. In further if we desire further to reduce the reference spur levels we go on appending the resistor and capacitor combinations accordingly.

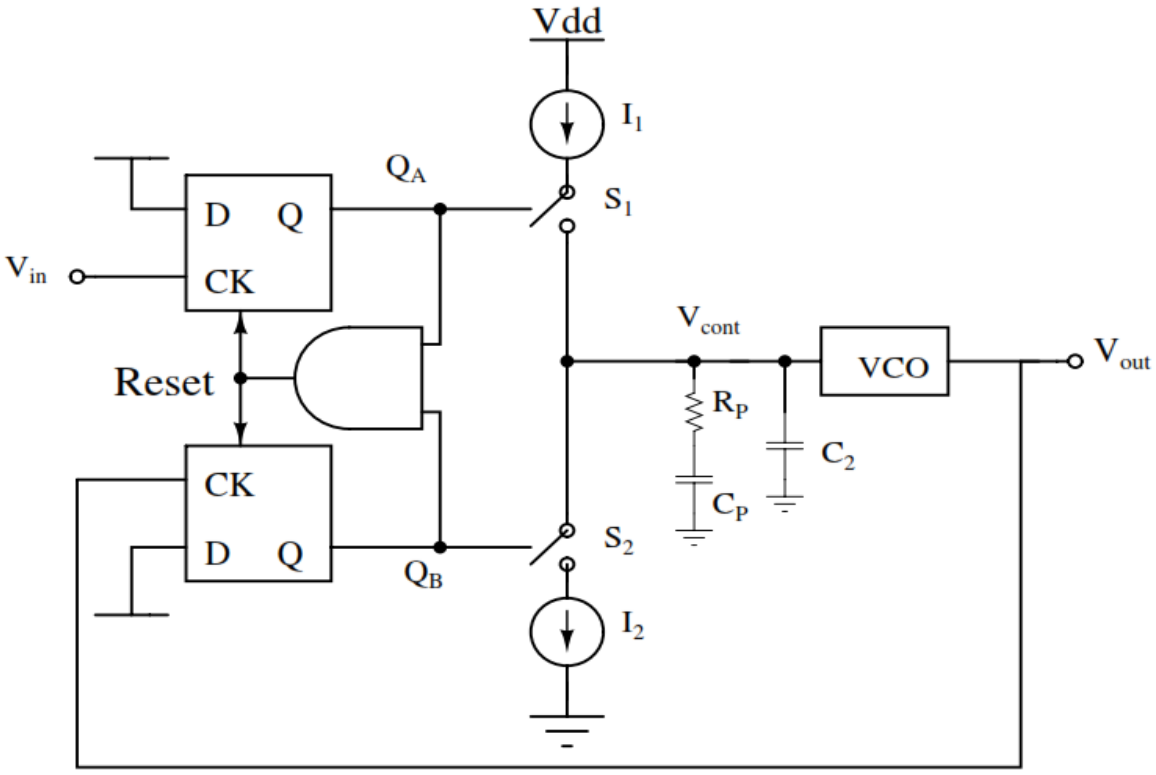
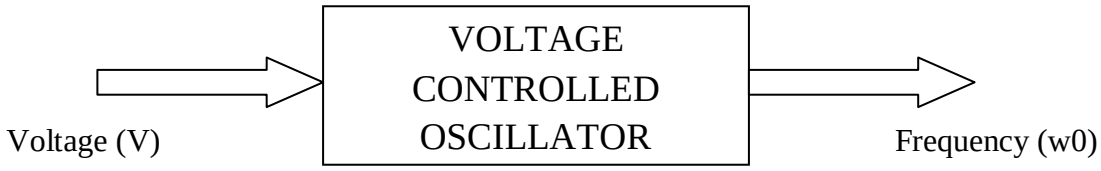


Figure 2.4.3: Addition of C2 to reduce ripple on the control voltage

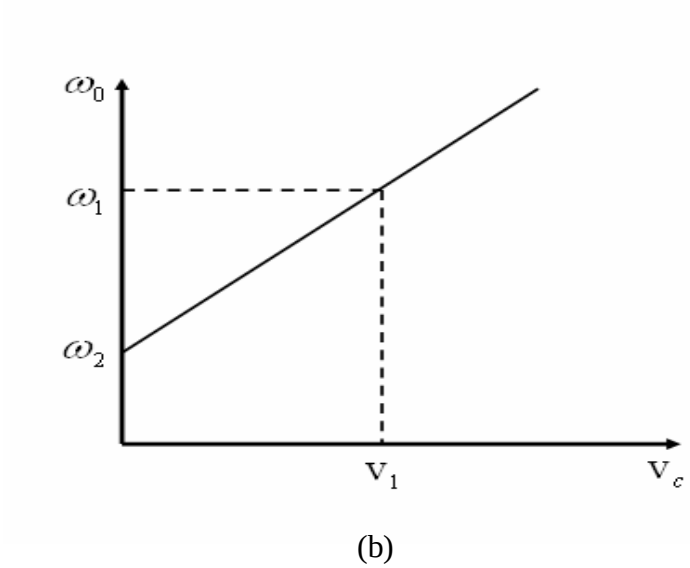
2.5 Voltage Control Oscillator

The VCO is a key block of a PLL frequency synthesizer. Most applications require that oscillators be "tunable", i.e., their output frequency be a function of a control input, usually a voltage.

A voltage controlled oscillator (VCO), results in an output frequency wo is linearly Proportional to the control voltage Vc generated by the Phase detector. This linearity relation between the control voltage and the output frequency simplifies the Phase lock loop design. A typical characteristic of a voltage-controlled oscillator is shown in the figure2.5.1



(a)



(b)

Figure 2.5.1 a)Representation of VCO b)Transfer characteristics of voltage control oscillator

The linearity characteristics are observed in the limited range of the curve beyond this particular range the voltage control oscillator performance becomes degraded and non-linear. Depending on the desirable requirements of the design, range can be selected such that the circuit always remain in its linear range, so the non-linear range is excluded in the consideration. The general model of the VCO is thus given as

$$\Delta w = Ko(vc - Vco)$$

where Vco is the control voltage, when PLL is in lock.

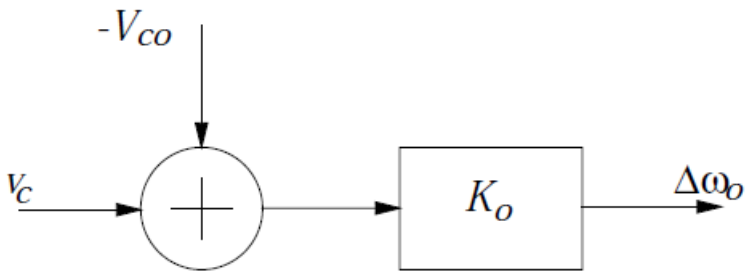


Figure 2.5.2: General model of VCO

2.5.1Barkhausen criteria

As a basic Requirement for producing self sustained near sinusoidal oscillation an oscillator must have a pair of complex-conjugate poles in the right half of the s-plane. As shown in Figure 2.5.3 an oscillator can be modelled as a feedback system with a loop gain T(s)=G(s)H(s). Where 1-T(s) is the characteristic equation of the system from which poles are found. According to barkausen criteria for any feedback system the fulfillment of the following conditions is often used as an indication of instability.

Negative feedback model:

Angle [T(jw)] = 180 degrees
Magnitude [T(jw)] > 1

Positive feedback model:

Angle [T(jw)] = 0 or 360 degrees
Magnitude [T(jw)] > 1

The above conditions are necessary but not sufficient. The system may fail to oscillate even after satisfying the above conditions.

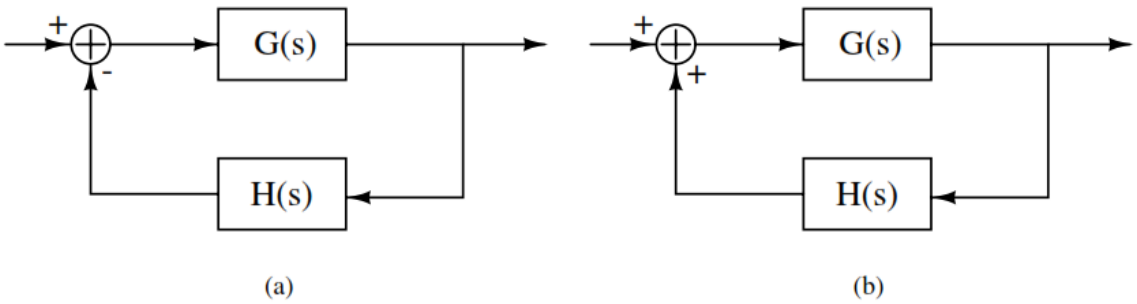


Figure 2.5.3: Oscillator feedback model (a) Negative feedback model (b) Positive feedback model

2.5.2 parameters of VCOs performance

Some of the important performance parameters of VCO are given below

Centre frequency: The centre frequency is determined by the environment in which the VCO is used.

Tuning range: The required tuning range dictated by the two parameters

1. The variation of the VCO centre frequency with process and temperature and

2. The frequency range necessary for the application.

The center frequency of some CMOS oscillators may vary by a factor of two at the extremes of process and temperature, thus mandating sufficiently wide (≥2x)tuning range to guarantee that the VCO output frequency can be driven to the desired value. Also some applications incorporate clock frequencies that must vary by one desired value. Also, some applications incorporate clock frequencies that must vary by one to two orders of magnitude depending on the mode of operation, demanding a proportionally wide tuning range. An important concern in the design of VCOs is the variation of the output phase and frequency as a result of noise on the control line. For a given noise amplitude, the noise on the output frequency is proportional to K vco because

$$Wout=wo+KvcoVcont.$$

Thus, to minimize the effect of noise in V cont, the VCO gain must be minimized a constraint in direct conflict with the required tuning range. The allowable range of Vcont is from V1 to V2 and the tuning range must span atleast w1 to w2, then kvco must satisfy the following requirement

$$Kvco >= (w2-w1) / (v2-v1)$$

Note that for a given tuning range Kvco increases as supply voltage decreases, making the oscillator more sensitive to noise on the control line.

Tuning Linearity:

The tuning characteristic of VCOs exhibit non-linearity, i.e., their gain K is not constant. This non-linearity degrades the settling behaviour of phase locked loops. For this reason, it is desirable to minimize the variation of Kvco across the tuning range. Actual oscillator characteristics typically exhibit a high gain region in the middle of the range and a low gain at the two extremes. Compared to a linear characteristic, the actual behaviour displays a maximum gain greater than that predicted by, implying that for a given tuning range, non-linearity inevitably leads to higher sensitivity for some region of the characteristic.

Output Amplitude:

It is desirable to achieve large output oscillation amplitude, thus making the waveform less sensitive to noise. The amplitude trades with power dissipation, supply voltage, and the tuning range. Also, the amplitude may vary across the tuning range, an undesirable effect.

Power dissipation:

As with other analog circuits, oscillators suffer from trade-offs between speed, power dissipation, and noise. Typical oscillators drain 1 to 10mW of power.

Supply and common-mode rejection:

Oscillators are quite sensitive to noise, especially if they are realized in single-ended form. But the differential oscillators exhibit supply sensitivity. The design of oscillators for high noise immunity is a difficult challenge. Note that noise may be coupled to control line of VCO as well. For these reasons, it is preferable to employ differential paths for both the oscillation signal and the control line.

Output signal purity:

Even with constant control voltage, the output waveform of a VCO is not perfectly periodic. The electronic noise the devices in the oscillator and supply noise lead to noise in output phase and frequency. These effects are quantified by “jitter” and “phase noise” determined by the requirements of application.

Types of Integrated Oscillators

Integrated VCOs for high-frequency communication applications can be implemented using ring architecture, relaxation circuits, or LC based networks. Among these, LC oscillators have the phase noise and frequency performance because of their use of passive resonant elements with high Q factors. LC oscillators have been constructed using bonding wires, integrated inductors. Using external parts, however rises the cost of the system and introduces other problems such as increased parasitic levels and increased power dissipation; therefore fully monolithic designs are highly desirable. There are other problems related with the utilization of bonding wires as the high Q inductor of the LC oscillator such as the lack of accurate control of the inductance value. In state of the art CMOS processing it is possible to

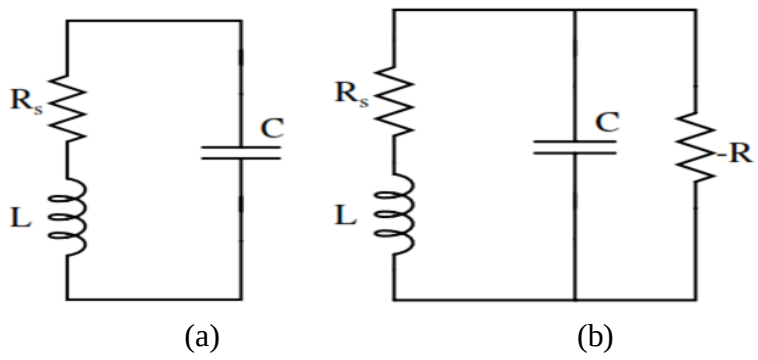
fabricate integrated inductors with high quality factors.They can be implemented monolithically at the expense of adding processing steps that significantly increases the cost and the expense of adding processing steps that significantly increase the cost and complexity of the system. Micro-Electro-Mechanical Systems (MEMS) designers, for example use various etching techniques to obtain high performance monolithic inductors. Addition of inductors to a CMOS process also introduces problems such as the control of eddy currents in the substrate and magnetic coupling.

Ring oscillators, on other hand , are suitable for monolithic system design using any digital CMOS fabrication process. Ring designs may require less die area when compared to the LC counterparts because of the lack of area consuming passive elements (inductors and varactors). In addition, the design of ring oscillators is straightforward using integrated circuit design techniques. Other properties of ring oscillators such as the availability of multiple phases at the output and wide tuning range can be useful for some specific applications including frequency synthesizers and over sampling circuits. These characteristics of ring oscillators lead to conclusion that they are still important in modern integrated communication systems. As implied above the noise performance of ring oscillators is generally worse than LC oscillators because of the low quality factor Q of the ring structure .However by using different ring architectures and circuit techniques, it is possible to achieve frequencies and noise levels comparable to LC designs. The final candidate for the high frequency integrated VCO design is relaxation oscillator.

A relaxation oscillator employs the same elements as a ring oscillator without the need for high-quality inductors. The only difference is the use of an additional capacitive element. This is in contrast to high-speed ring oscillator designs ,which utilize the capacitive parasitic s of the Metal oxide semiconductor transistors(MOS).Only a few CMOS relaxation oscillators have been published ,with the fastest running at 900 MHz .They also do not match the noise performance of LC and ring oscillators because of their relatively low effective quality Q factor.

2.5.3 LC-Oscillators

The core of an LC oscillator is a resonator tank that is constructed from on chip inductors and varactors. This tank performs as the frequency selective network that was shown in the oscillator model of Figure.2.5.4(b). As shown in Figure.2.5.4(a), the resonator tank can be simply modelled as a parallel connected LC network along with the series parasitic resistance of the Rs of the inductor. The tank might have a very good quality factor ,



(a) (b)

Figure 2.5.4: a) Resonator tank circuit b) LC oscillator model

however the tank alone is not sufficient for steady oscillations because of the energy loss on the 34arasitic. After excitation, the resonator will only oscillate for approximately Q many cycles until all the stored energy is dissipated on the Rs unless the energy loss is accompanied before. Therefore every LC oscillator employs an active circuitry that cancels the parasitic resistance with its negative effective resistance by providing the required energy at every cycle. This active circuitry is shown as the LC oscillator is strictly determined only by the characteristics of the resonator, that is $Wr=1/\sqrt{LC}$ and ideally is not effected by the active circuitry if the capacitive loading of the –R element is ignored.

Ring oscillator usually takes less area and has a large tuning range. The LC oscillator often takes more chip area due to spiral inductors and has a smaller tuning range.

2.5.4 Ring Oscillators

As discussed in the previous sections, the Barkhausen criterion for oscillation can be satisfied with a positive feedback loop that does not contain any frequency selective elements. A ring oscillator can be constructed by closing the feedback loop around an amplifier block while an LC oscillator needs both the amplifier block and the frequency selective network to operate properly. A ring oscillator is realized by connecting a number of amplification stages in series as shown in below Figure.2.5.5.Then the loop is closed by connecting the output of the last element to the input of the first element forming the positive feedback. The most basic ring oscillator employs single-ended inverters in place of the amplification stages. In this case, an odd number N of inverter stages is needed for steady oscillations. Otherwise the oscillator latches up at a DC level which corresponds to the satisfaction of the Barkhausen criterion at zero frequency. From another perspective, an odd number of stages will oscillate because if one modes is excited, the pulse will propagate through all the stages and will reverse the polarity of the initial node. It was already implied that the frequency of oscillation will be 1/(2*N*Td) where Td is the propagation delay of a single stage for this case.

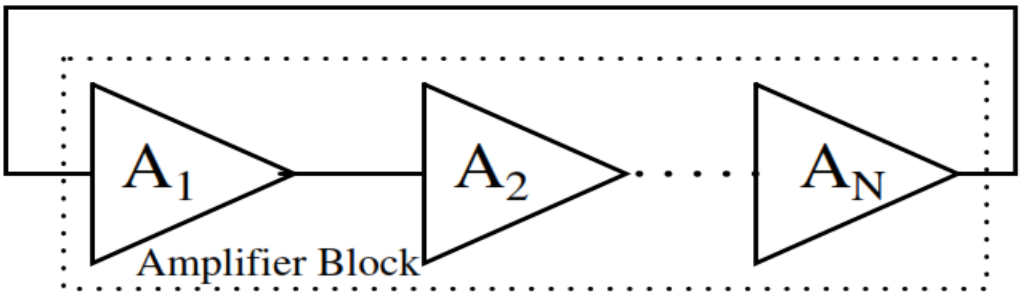


Figure 2.5.5: Ring oscillators

2.5.5 Differential Ring Oscillator

A ring oscillator consists of a number of gain stages in a loop. While single ended rings are well understood, easy to size and convenient to port over processes they are limited to an odd number of delay stages making them incapable of providing quadrature outputs. As a result differential ring oscillators are the only choice for the systems which require quadrature signals, on the other hand the differential implementations can utilize even number of stages by simply configuring one stage such that it does not invert. With four

stage differential ring oscillator we can produce quadrature signals very easily, a three stage ring oscillator is used for VCO. The differential structure of the VCO reduces the common mode noise effect, which improves the system's overall jitter performance. Jitter(Phase noise)increases as the number of stages of the VCO increases. The lower the number of steps, the higher the free running frequency of the VCO. The number of stages is typically chosen to be three or four. By dissipating the total power of the large number of stages in a small number of stages, one can achieve a better phase noise. Hence, three stages are chosen for this design. This VCO has a single control voltage that is used to set the desired output frequency.

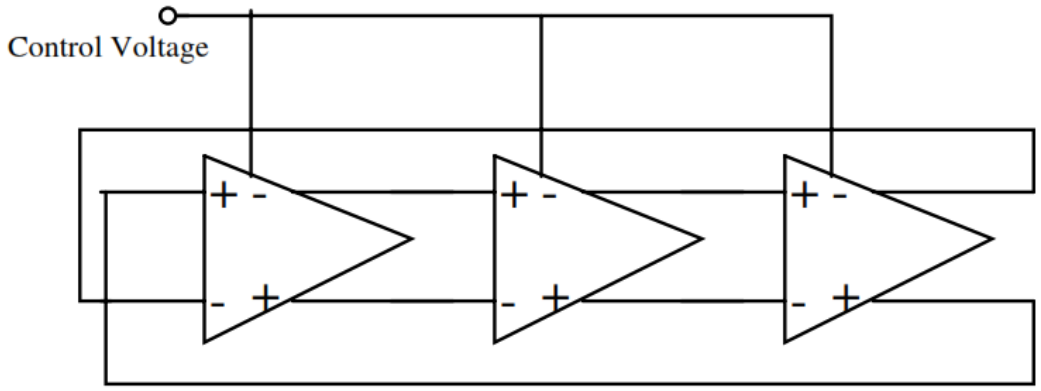


Figure 2.5.6: Differential Ring oscillators

2.6 Frequency synthesizers

PLL consists of the three blocks Phase detectors, loop filters and VCO (voltage-controlled oscillator).When the PLL is used as a frequency synthesizer, another block is added which is divide-by-N counter. The counter divides by a factor *N*, the frequency of the VCO output signal is then forced to be *N* times the reference frequency. In most cases, the divider ratio *N* is made programmable. There are two main PLL frequency synthesizers.

2.6.1 Integer-N PLL Frequency Synthesizers

A basic PLL-based integer-N frequency synthesizer consists of four basic components: a phase detector (PD), a loop filter, a voltage controlled oscillator (VCO), and a programmable frequency divider. The phase detector compares the phase of the input signal against the divided phase of the VCO. The output of the phase detector is a measure of the phase difference between the two inputs. The difference voltage is then filtered by the loop filter and applied to the VCO. The control voltage on the VCO changes the frequency in the direction that reduces the phase difference between the input signal and the frequency divider output. For an integer-N synthesizer, the output frequency is a multiple of the reference frequency

$$f_{out} = N f_{ref}$$

Where N is the loop frequency division ratio, is an integer. From above equation, the frequency resolution is equal to the reference frequency. Due to this limitation of the reference frequency, for narrow-band applications, the reference frequency of the synthesizer is very small. So the small reference frequency results in a very small loop bandwidth, Moreover, a very large frequency division ratio.

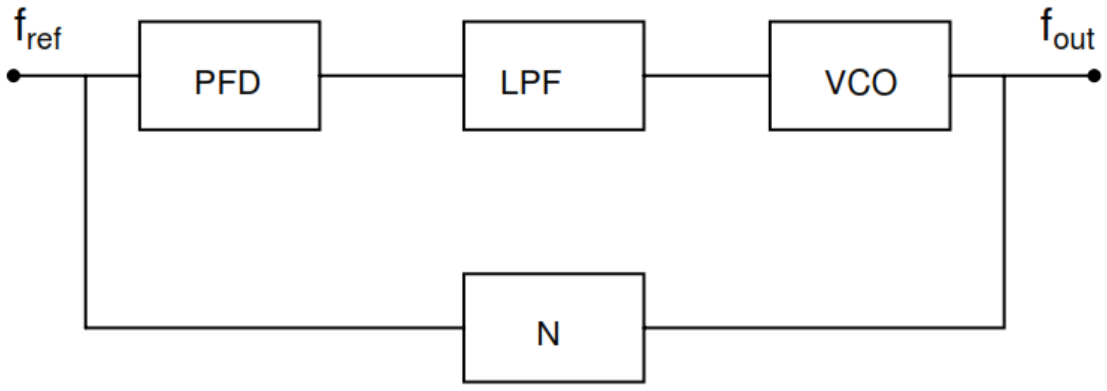


Figure 2.6.1: Integer synthesizer architecture

The conventional integer-N PLL with low reference frequency has several disadvantages. First, the lock time is long due to its narrow loop-bandwidth. Second, the reference spur and its harmonics are located at low offset frequencies. Third, the large division ratio (N) increases the in-band phase noise associated with the reference signal, phase detector, and frequency divider. Finally, with a small loop bandwidth, the phase noise of the VCO will not be sufficiently suppressed at low offset frequencies. So, fractional-N

frequency synthesizers are introduced to improve the phase noise and settling time performance of integer-N PLL synthesizers.

2.6.2 Fractional-N PLL Frequency Synthesizers

Fractional-N frequency synthesizers are used to overcome the disadvantages of integer-N synthesizers. In fractional-N synthesizers, fractional multiples of the reference frequency can be synthesized, allowing a higher reference frequency for a given frequency resolution. In Figure2.6.2. the division modulus of the frequency divider is steered by the carry bit of a simple digital accumulator of x-bit width. The symbol N/N + 1 of the divider means that the division ratio is N +1 when the carry bit is 1, otherwise the division ratio is N. To realize a fractional division ratio i.e. N + F, with F -> [0, 1], a digital input K = F/ 2n is applied to the accumulator. A carry output is produced every K cycles of the reference frequency which is also the sampling frequency of the accumulator. This means that in 2x clocks of reference frequency the division ration is N for (2n-K) clocks, and the division ratio is N + 1 for K clocks. This results in an average division

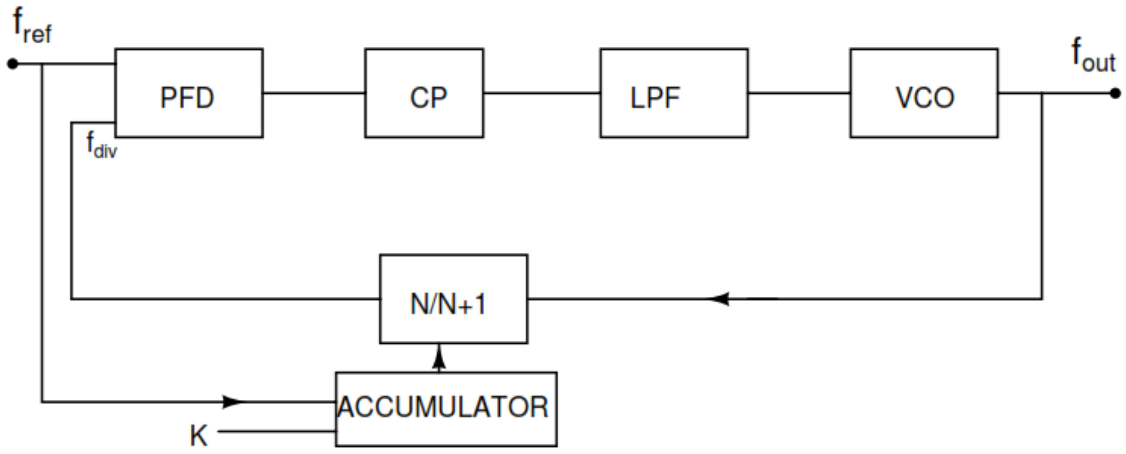


Figure 2.6.2: Fractional-N frequency synthesizer architecture

The ratio N(average) is given by

$$N_{avg} = \frac{(2^x - K)N + K(N+1)}{2^n} N_{avg} = N + \frac{K}{2^n}$$

This means that a non-integer division ratio can be realized. The most important disadvantage of fractional synthesizer architecture is the generation of spurs in the output spectrum due to the noise on the modulus control called pattern noise in the overflow signal. The pattern noise can be better understood if the accumulator is regarded as a $\sum \Delta$modulator.

2.6.3 Divider Architecture and Hierarchy

A crucial aspect of the present-day consumer electronics industry is the short time available for the introduction of new products in the market. Short time-to-market demands architectures providing fast design time, simple layout work, and easy optimization. Furthermore, from a high re-usability point of view, architecture with easy adoption of the input frequency range, maximum and minimum division ratios is more desirable. For these reasons, we prefer a generic and fully programmable architecture.

Generic Chain Architecture:

The multi-modulus divider system architecture is depicted in Figure.2.6.3. It consists of a chain of divide-by-2/3 dual-modulus prescalers in cascade, connected like a ripple counter. The multi-modulus divider operates as follows. In every division period, the last cell of dual-modulus prescaler in the chain generates signal mod (n-1). This signal then propagates up the chain. An active mod signal would enable the cell to divide by three once in a division cycle, as long as the programmable input bit p is set to 1.

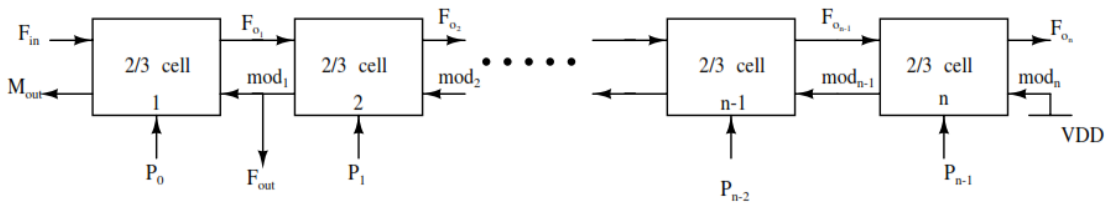


Figure 2.6.3: Multi-modulus Divider architecture

In other word, the dual-modulus divide-by-2/3 cell would divide by three only ONCE in a whole division cycle, if it ever gets enabled to do so by having both the programmability p and the signal mod enabled. For the rest of the division cycle, the cell divides the input by two. Thus, division-by-three action only adds one extra period of each cell's input signal to the period of output signal. For example, each divide-by-three action in a cell with a 2.5 GHz (0.4ns period) input would introduce an extra 0.4 ns to the output period. The output period then becomes 1.2ns instead of 0.8 ns. Applying the principle to the whole chain, the output period can be

$$T_{out} = 2^n T_{in} + 2^{n-1} T_{in} p_{n-1} + 2^{n-2} T_{in} p_{n-2} + 2 T_{in} p_1 + T_{in} p_0$$

$$= \left(2^n + 2^{n-1} p_{n-1} + 2^{n-2} p_{n-2} + 2 p_1 + p_0\right) T_{in}$$

CHAPTER: 3

METHODOLOGY AND TOOLS USED

3.1 Introduction:

Cadence Design tools is an EDA software that is used extensively in designing and manufacturing semiconductor devices and circuits for various fields. They are used in different design and verification process like Custom IC design, logic design, design and verification of system, verification at functional level, digital implementation, design of RF circuits and PCB, IC packaging and Sip Design. For a designer the Custom IC Design Tools is an essential tool of the Cadence design Systems as it includes the whole process flow starting from schematic entry up to post layout simulation.

These tools are completely general, supporting different fabrication technologies. When a particular technology is selected, a set of configuration and technology-related files are employed for customizing the Cadence environment. This set of files is commonly referred as a Design kit.

Analog IC Design Flow and required tools:

Fig.3.1 shows the basic design flow of an analog IC design, together with the Cadence tools required in each step.

First, a schematic view of the circuit is created using the Cadence Composer schematic editor. Alternatively, a text netlist input can be employed.cThe circuit is simulated using the Cadence Affirma analog simulation environment. Different simulators can be employed, some with the Cadence software (e.g., Spectre) some from other vendors (e.g., HSPICE) .Once circuit specifications are fulfilled in simulation; the circuit layout is created using the Virtuoso Layout Editor. The resulting layout must verify some geometric rules dependent on the technology (design rules). For enforcing it, a Design Rule Check (DRC) is performed. Optionally, some electrical errors (e.g. shorts) can also be detected using an Electrical Rule Check (ERC). Then, the layout should be compared to the circuit schematic to ensure that the intended functionality is implemented. This can be done with a Layout Versus Schematic (LVS) check.

All these verification tools are included in the Diva software in Cadence (more powerful Cadence tools can also be available, like Dracula, or Assura in deep submicron technologies). Finally, a netlist including all layouts parasitic should be extracted, and a final simulation of this netlist should be made. This is called a Post-Layout simulation, and is performed with the same Cadence simulation tools.

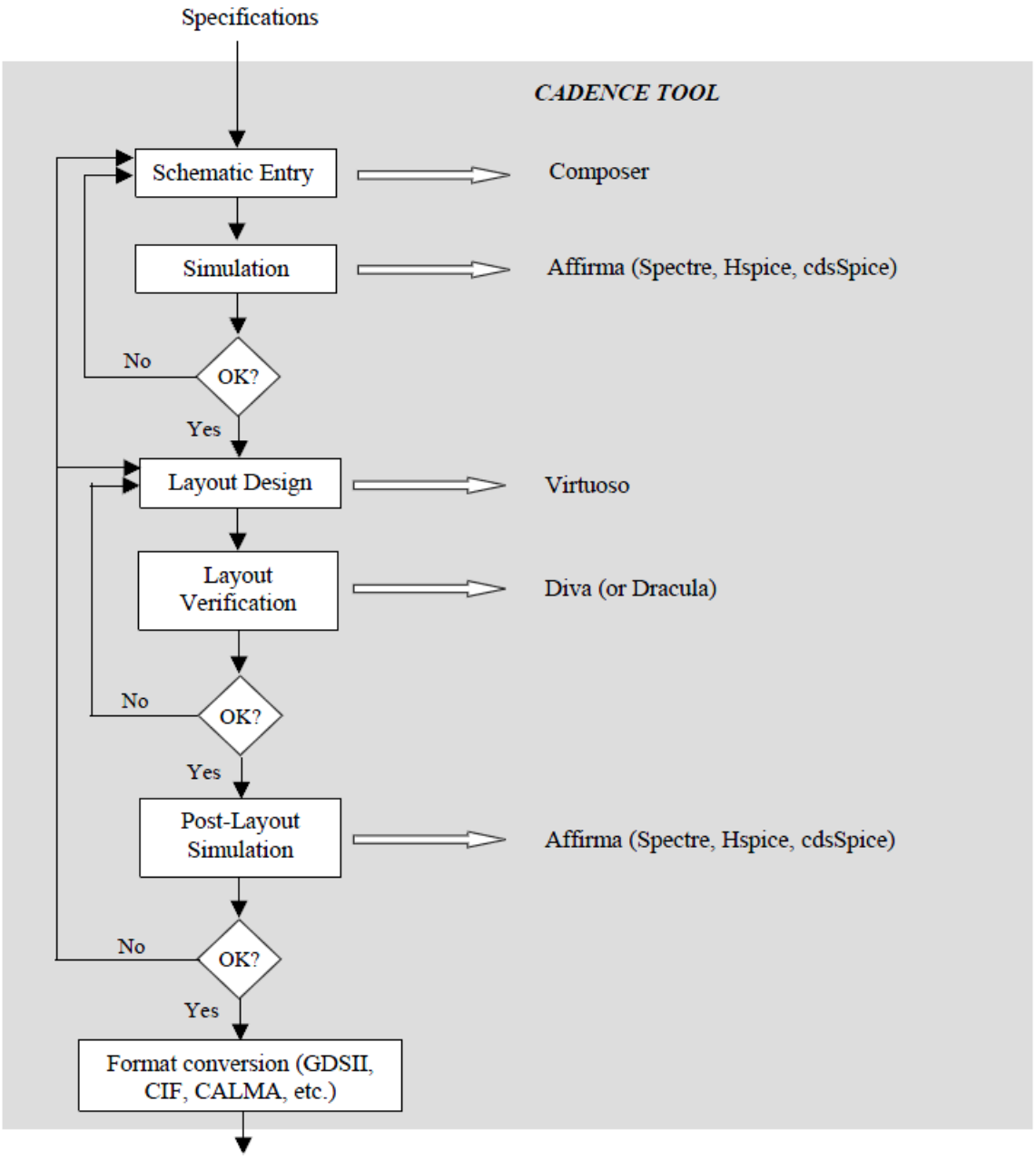


Figure 3.1: Analog IC design flow and Cadence tools involved

CHAPTER: 4

Design and Implementation

This chapter discusses the design schematic and simulation implementation of Phase locked loop sub blocks. The problem characterization and specifications of these blocks have already been described in previous chapters. It discusses circuit topologies and sub blocks identification for implementation of PLL. All the sub blocks have been tried independently before anal implementation. This chapter starts with the design of Phase frequency detector, followed by the design of charge pump and loop filter, voltage control oscillator and divider. The PLL based frequency synthesizer is shown in Figure.4.1

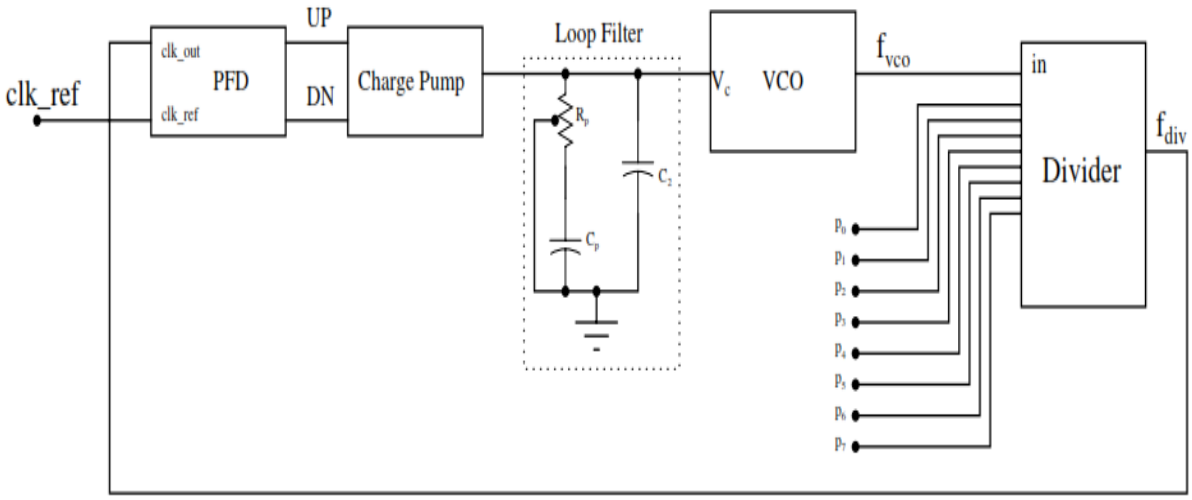


Figure 4.1: PLL based frequency synthesizer

The standard tri-state PFD, was implemented using two resettable flip-flops. To eliminate dead-zone a delay element was added to the reset path. Because most gates used in the design of the PFD are operating at a relatively slow speed, it was possible to minimize power consumption without affecting signal performance.

The charge pump is responsible for adding or removing charge from the loop filter, which in turn will increase or decrease the control voltage on the VCO. Careful design of charge pump is necessary such that flicker and thermal noise contributors to in-band phase noise are mitigated. A differential CMOS charge pump with a single ended output is used in this dissertation. The divider was formed by cascading in order to provide maximum divide ratio as desired.

4.1 Design of Phase frequency Detector

Phase frequency detector is one of the important parts in PLL circuits. A simple implementation of PFD consisting of two edge-triggered, resettable D flipflops with their D inputs tied to a logic ONE. The first design is the traditional PFD architecture.

PFD Design and Simulation

The traditional PFD consists of two flip-flops and a NOR gate to provide a reset path when both outputs go high at the same time as shown in Figure.4.1.1. Due to the reset path this design suffers from large dead zone. As we can see from the figure4.1.1, this design has two D flip-flops and NOR gate.

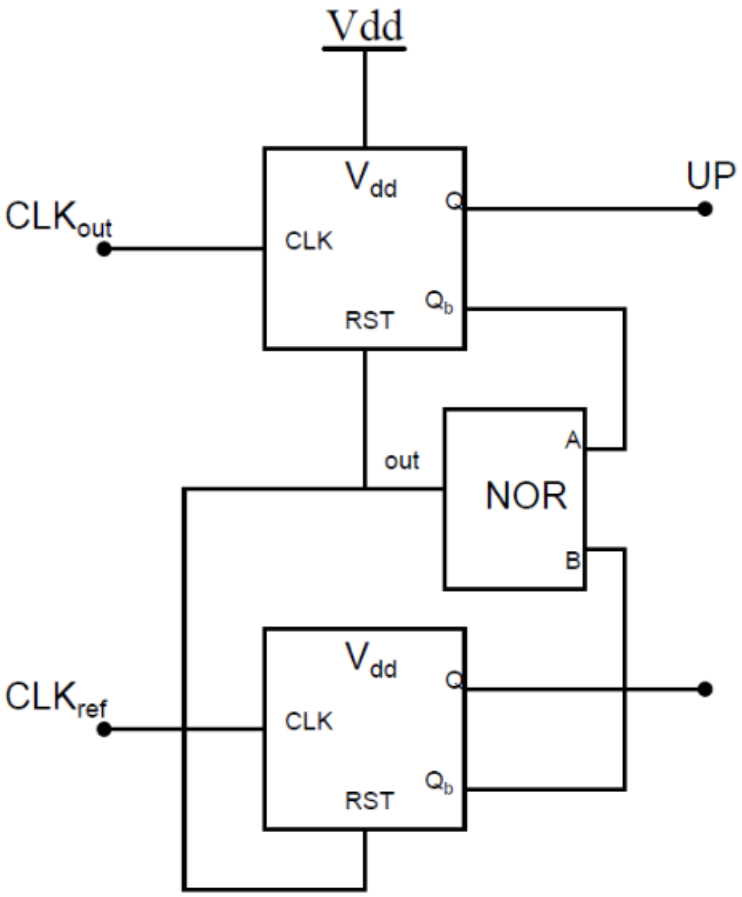


Figure4.1.1: Traditional Phase frequency detector

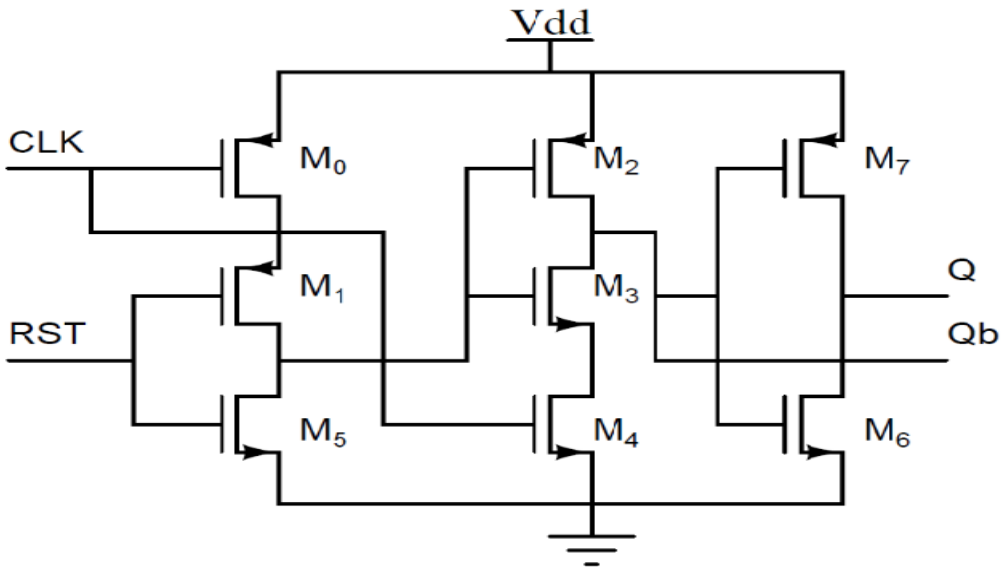


Figure 4.1.2 The schematic design of the D flip-flop

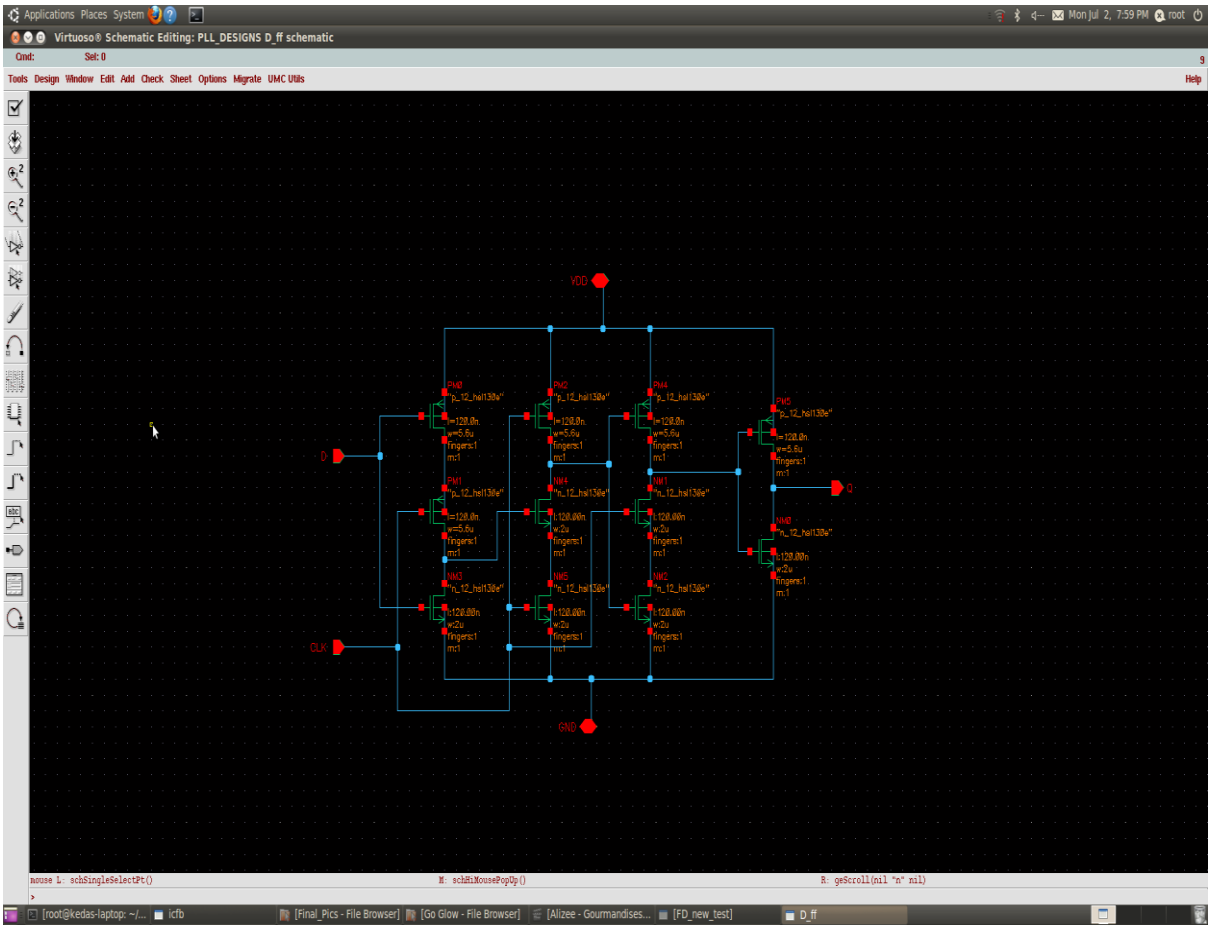


Figure 4.1.3: Virtuoso schematic design of D-flipflop

The D flip-flop circuit operates as follow. When both CLK and RST are low,node 1 will be connected to VDD through M1, M6. At the raising edge CLK, the node 2 will be connected to ground through M3,M4. Since node 1 is connected to VDD that will turn off M2 keeping node 2 from charging high. as RST signal charges up, node 1 will be connected to the ground through M5, which will lead to pull up node 2 and it will become high due to switching M2 on. Transistor M1 job is to prevent a short circuit in the M0,M1,M5 path. When CLK is low and RST is high a large current will flow this path so M1 is placed there to prevent this current and lower the power consumption of the D flip flop.

Since we are getting flipped value of Q, an inverter has been added at the end of the circuit to flip the value and get a correct value of Q. Both flip-flops have the same design, one of them will control the UP output of the PFD and the other will control the DOWN output. The direct output from node 2 of both flip-flop are connected to a NOR gate, and the output go this NOR gate will be connected to the RST input of the flip-flops to enable reset when both output go high at the same time.

Due to the NOR reset path, the time needed to charge the NOR gate and reset both flip-flops will be added to the reset delay time in the internal components of the flipflops and produce a large dead zone. We can see that the NOR gate needs around 80 Pico seconds to charge up and be able to reset both flip-flops, and because of this delay both outputs will be high at the same time, therefore they will switch on both transistors in the charge pump preventing it from charging the output up or down according to this phase error.

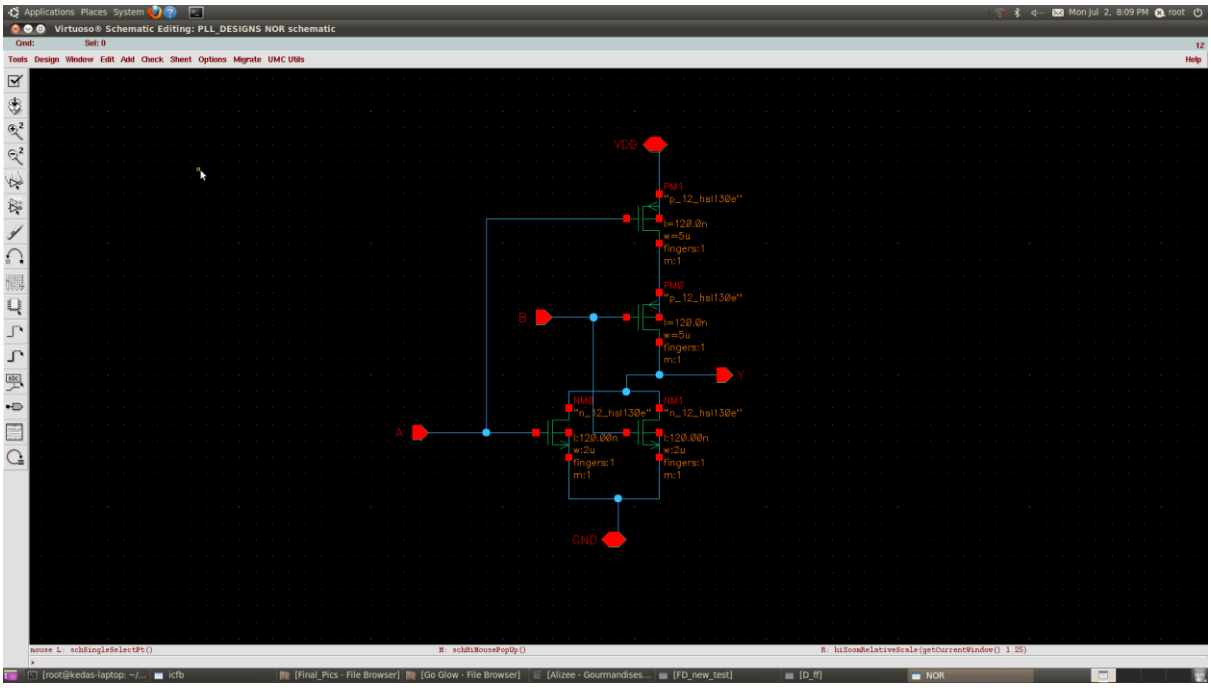


Figure 4.1.4: Schematic of NOR gate

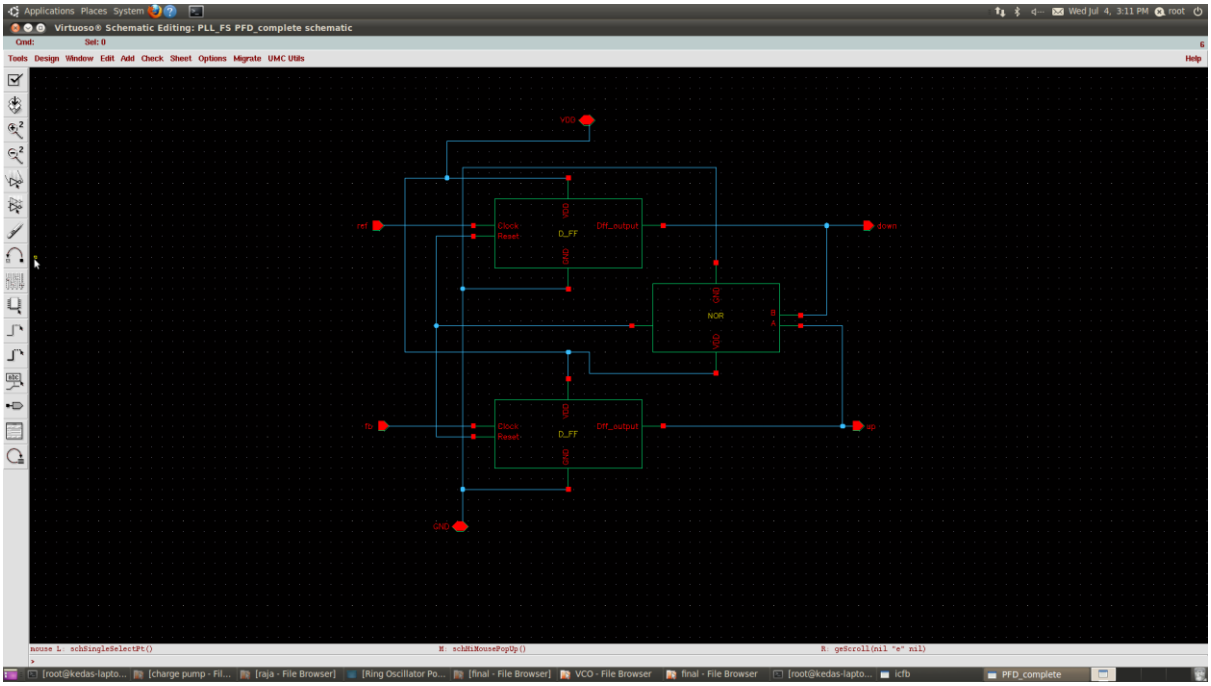


Figure 4.1.5: Virtuoso schematic of the Traditional PFD

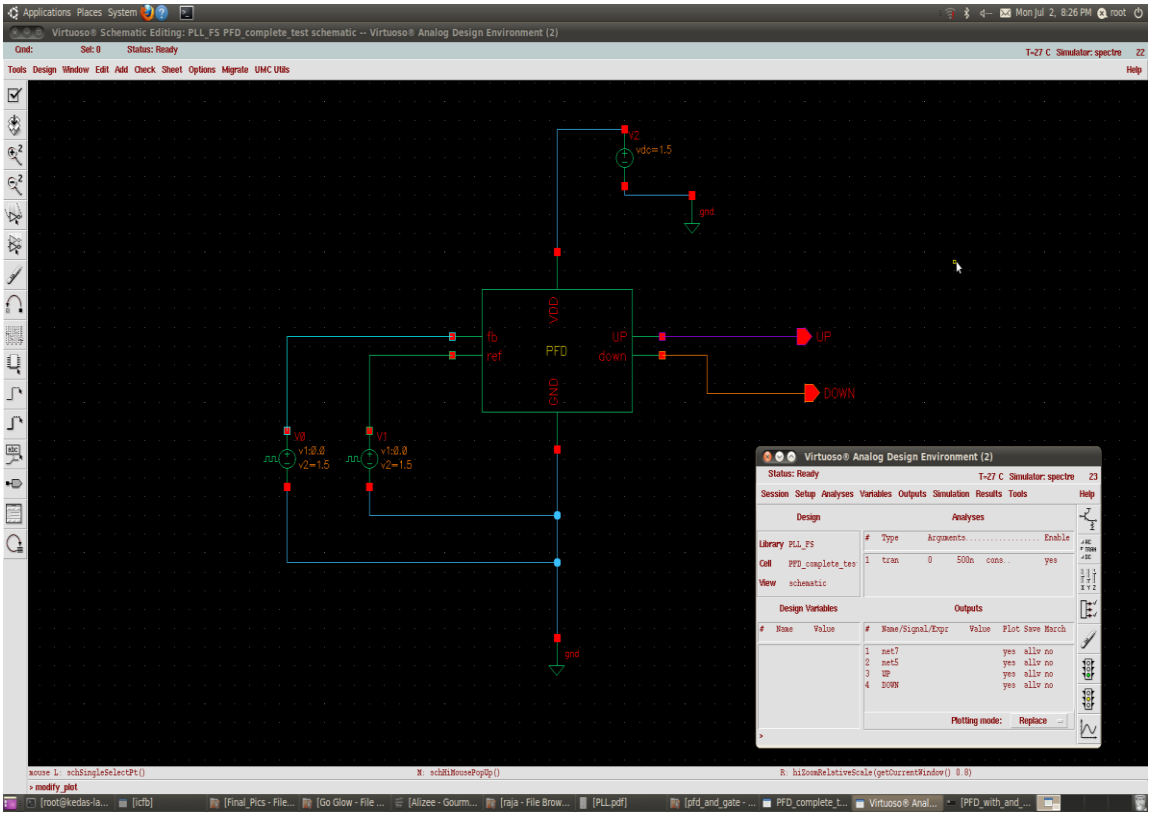


Figure 4.1.6: Traditional PFD test

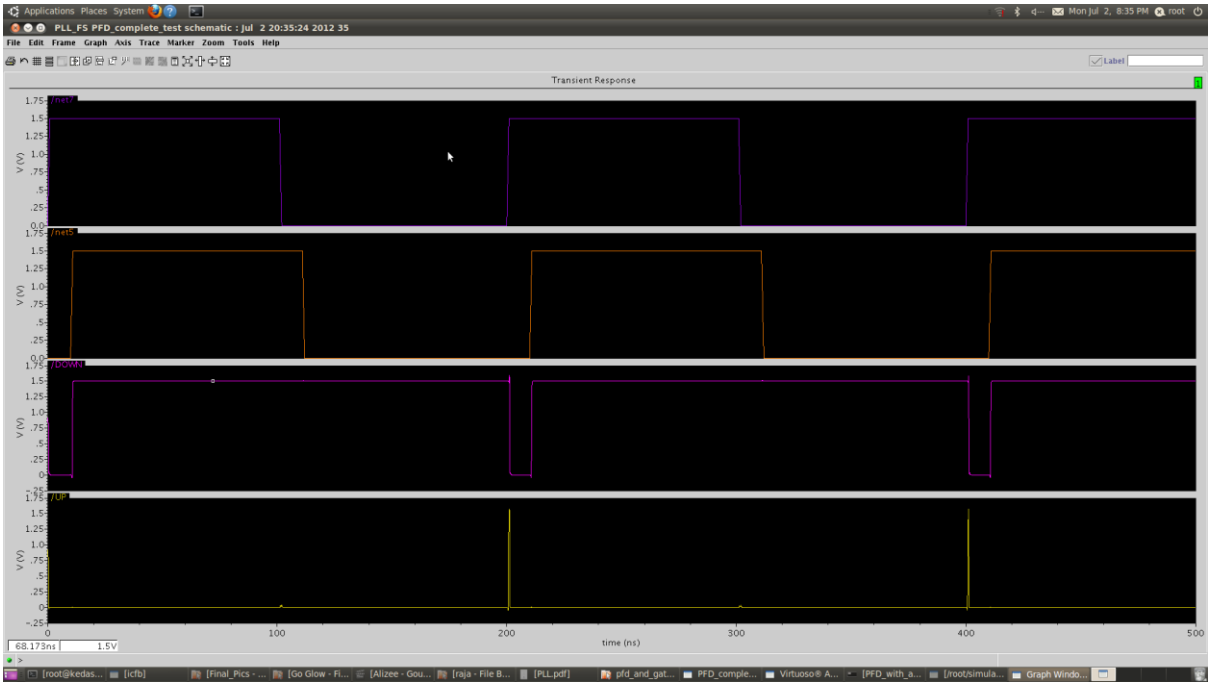


Figure 4.1.7: Waveform when reference signal is in lead with feedback signal

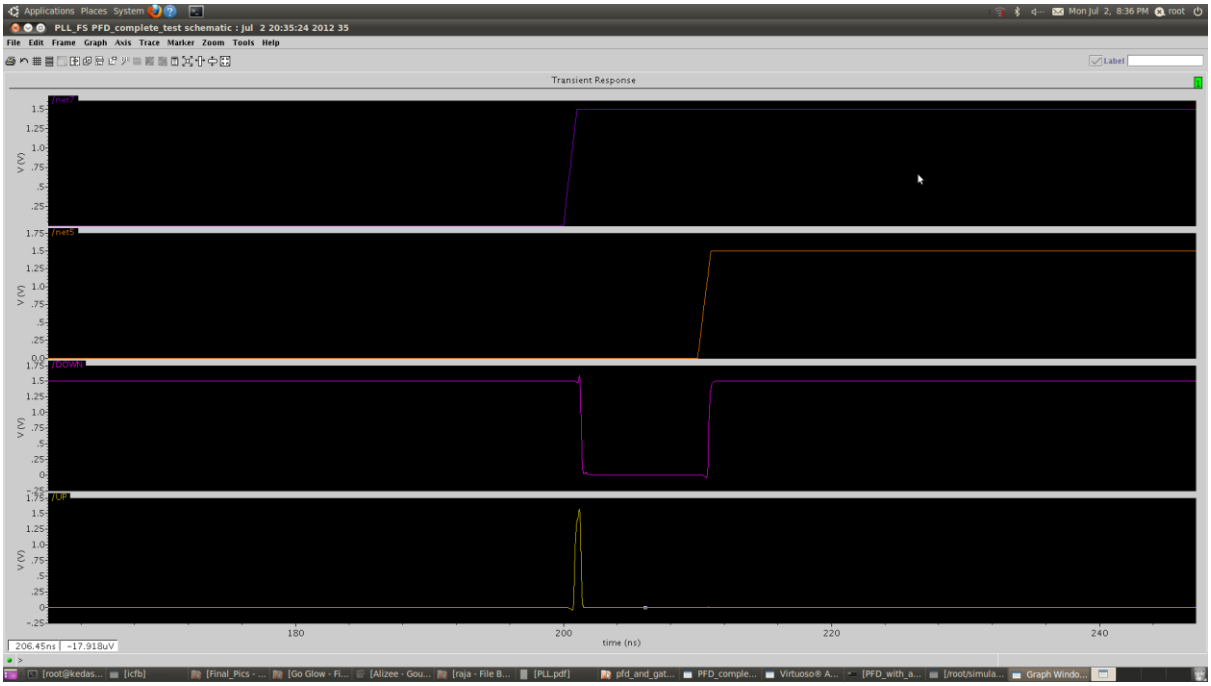


Figure 4.1.8: Observation of delay from the wave form which is of order 2ns

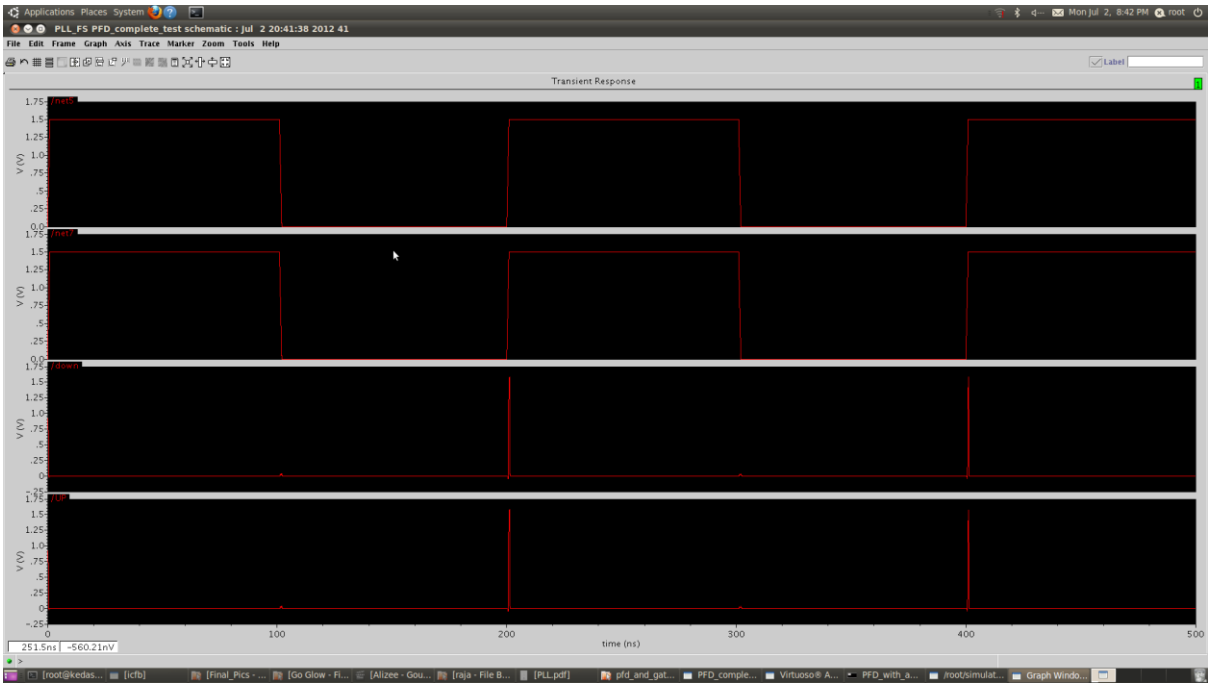


Figure 4.1.9: Waveform when reference signal is in same phase with feedback signal

Modified PFD structure

The simulation of the modified type 1 PFD shows that the dead zone of this circuit is reduced as compared to the previous one, which make it a better candidate for our system than the traditional type1 PFD, beside the lower power consumption make the design more suitable for cell phones that use a limited power supply.

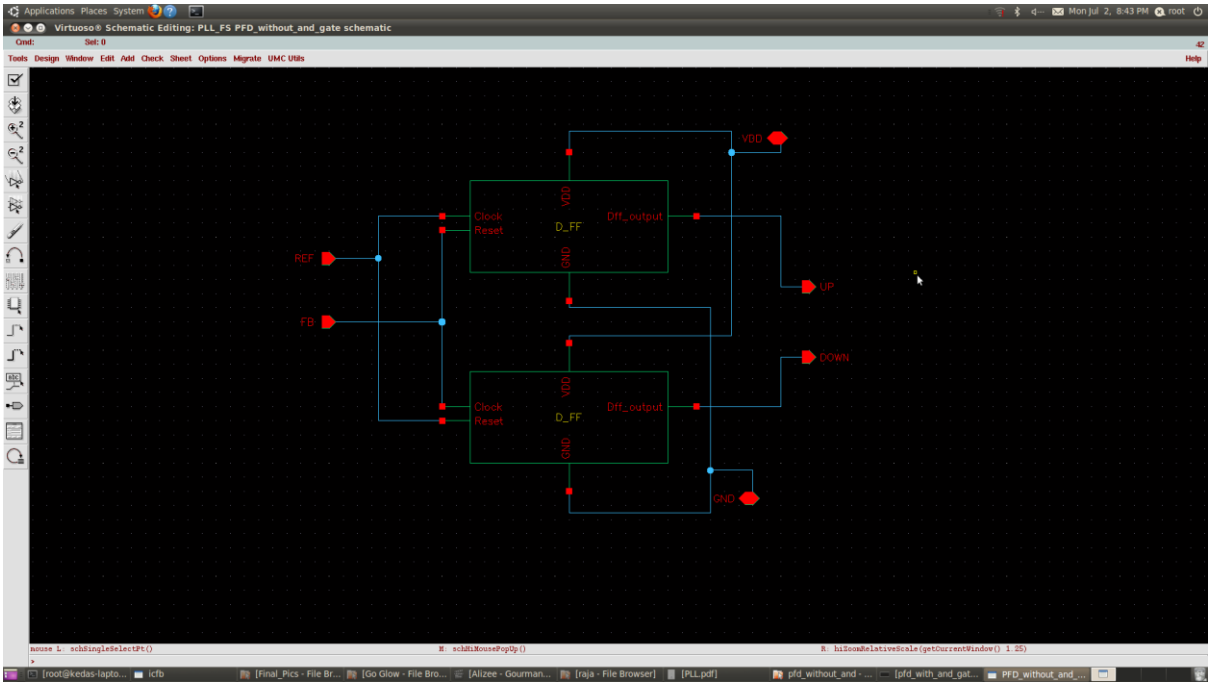


Figure 4.1.10: Schematic of the modified PFD structure

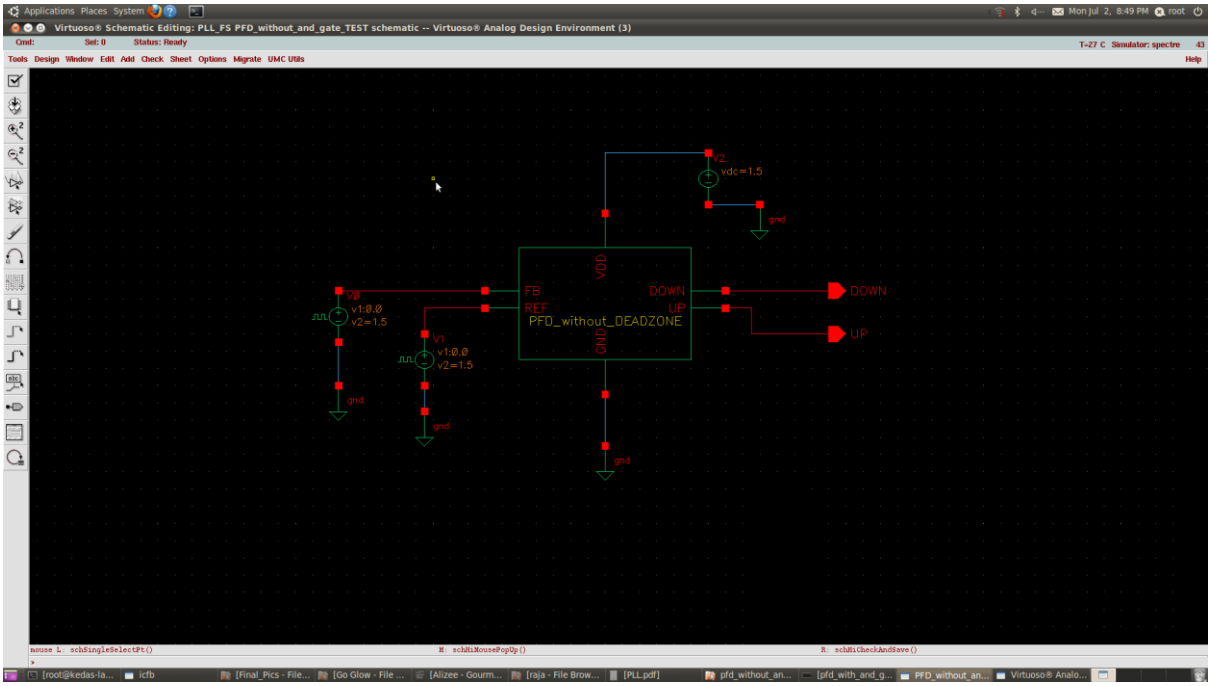


Figure 4.1.11: Testing the modified PFD structure

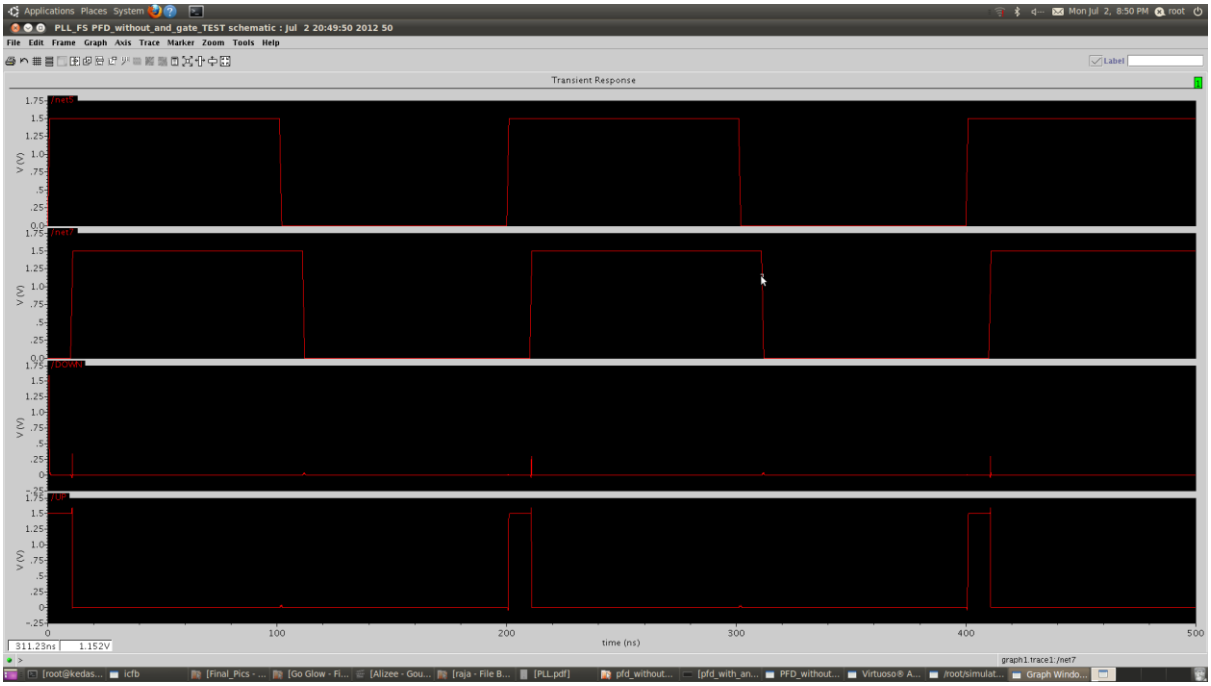


Figure 4.1.12: Waveform when reference signal is in lead with feedback signal under the modified PFD structure

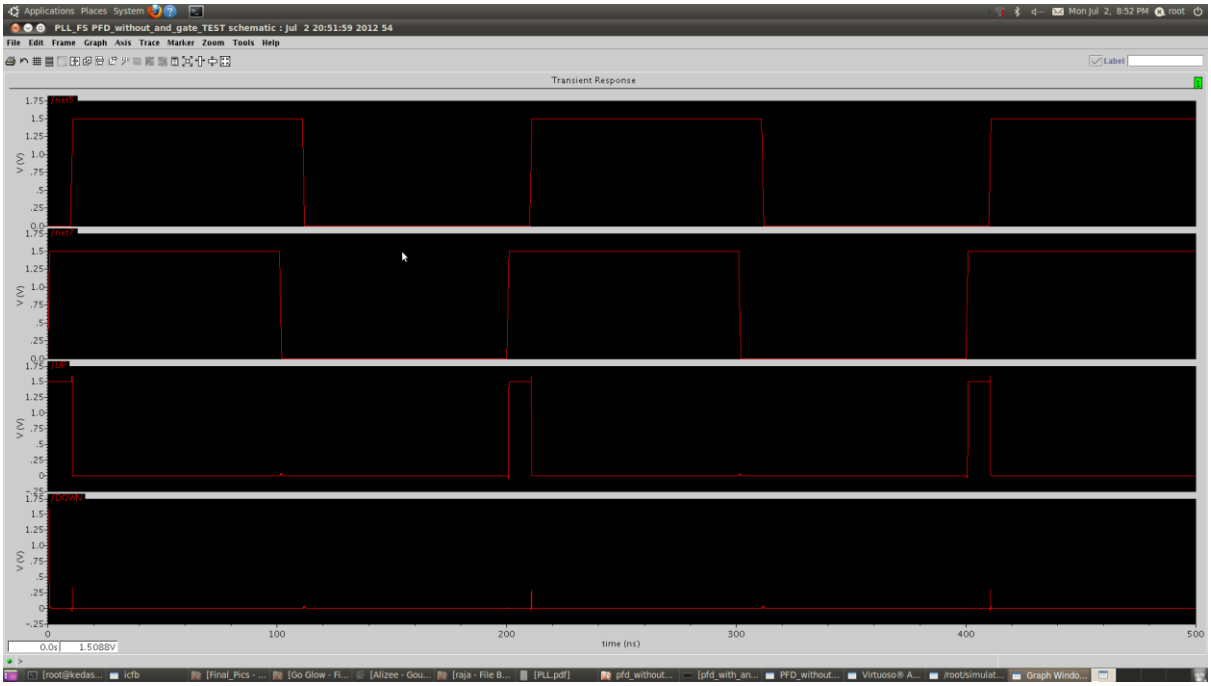


Figure 4.1.13: Waveform when reference signal is in lag with feedback signal under the modified PFD structure

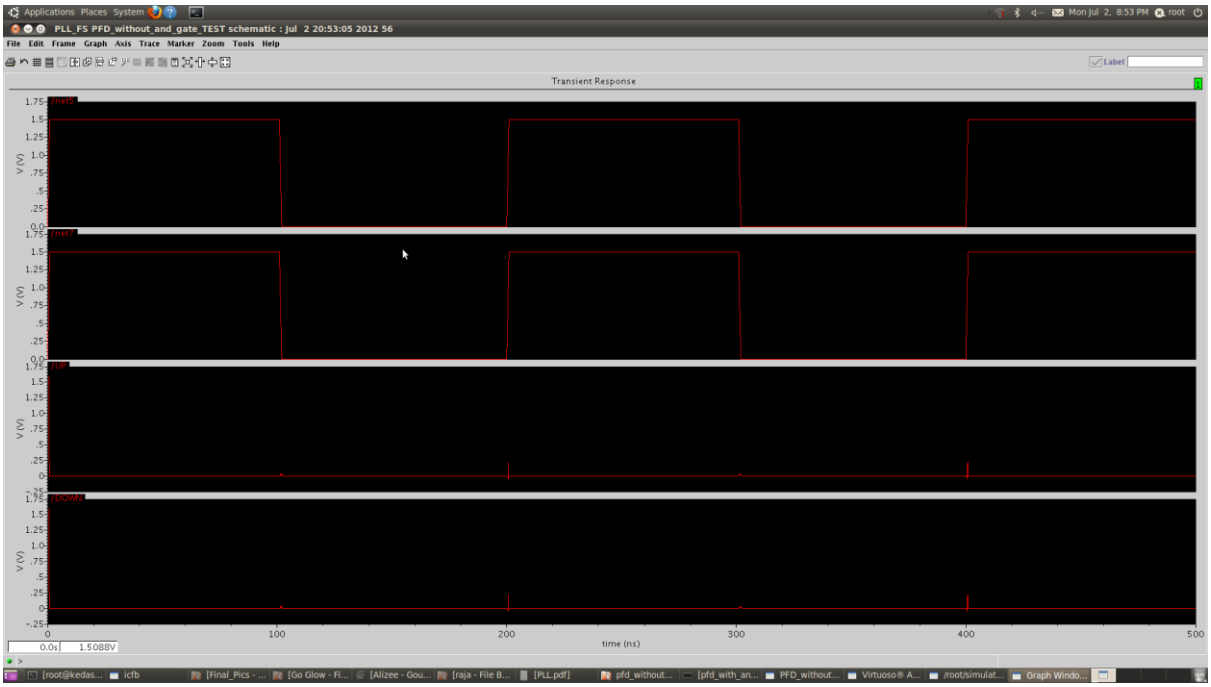


Figure 4.1.14: Waveform when reference signal is in same phase with feedback signal under modified feedback signal

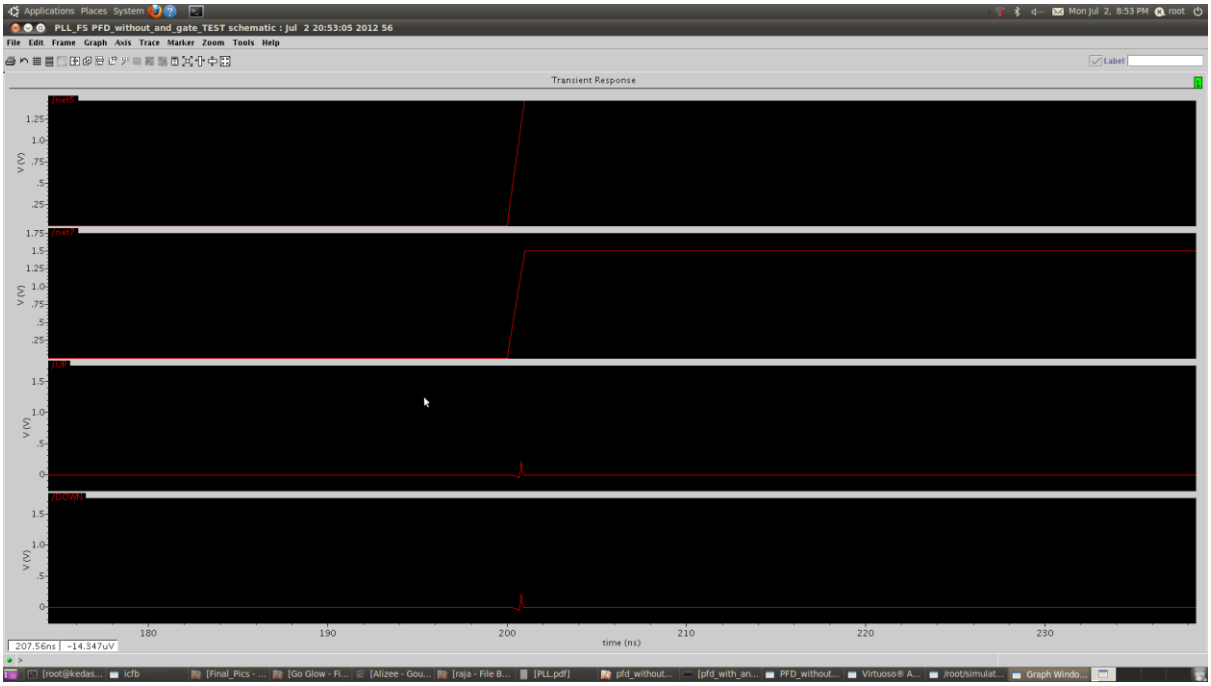


Figure 4.1.15: Reduction in the delay of the signal under the modified PFD structure

4.2 Design of charge pump

The charge pump is responsible for adding or removing charge pump from the loop filter, which inturn will increase or decrease the control voltage on the VCO. A differential CMOS charge pump with a single ended output was shown

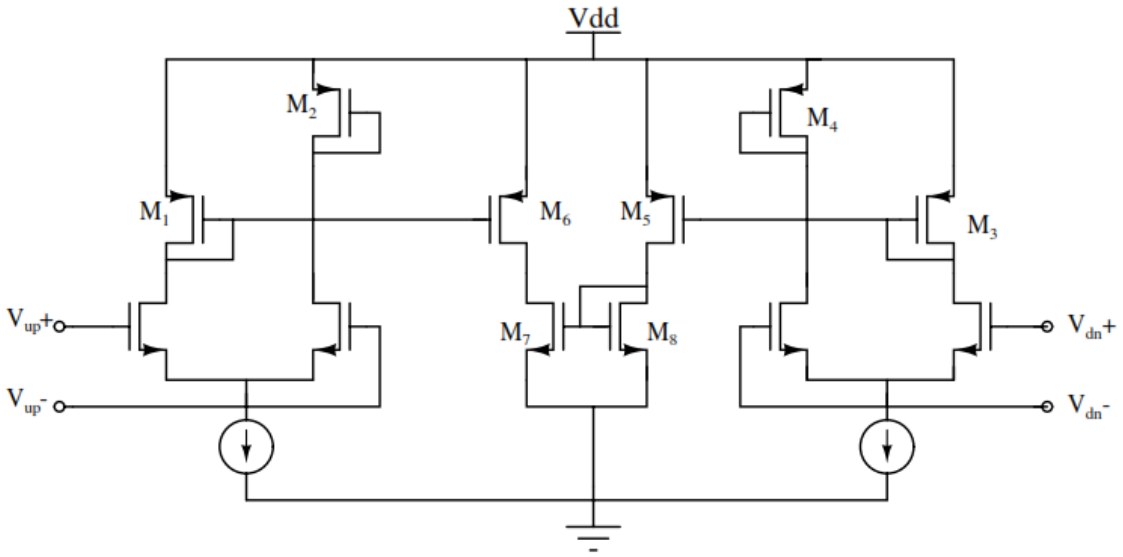


Figure 4.2.1: Schematic of charge pump

When the up signal is high, the drain potential of M1 ((gate potential of M6) decreases, which in turn increases the current through the M6. The loop filter is connected across drain potential of M6. so, the current (charge) is pushed in to the loop filter which increases the control voltage of VCO.

Similarly when down signal is high the the drain potential of M3 gate potential of M6 decreases ,which in turn increases the current through the M5. The current through M5 is mirrored onto the M7 which pulls the charge from the loop filter, which decreases the control voltage of VCO.

Circuit Design:

Current consumption considered in the circuit as 100µA. When the up signal is high the entire current is steered in M1. M1 is operating in the saturation mode. The current through the MOSFET in saturation region is

$$I_d = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_{th})^2(1 + \lambda V_{ds})$$

The current through the MOSFET in linear region is given by

$$I_d = \mu_n C_{ox} \frac{W}{L}((V_{gs} - V_{th})V_{ds} - \frac{V_{ds}^2}{2})$$

In the above circuit current source is implemented by using current mirror bias circuit. So assume the drain source potential of current source as 0.8Vwhich is required to drive that transistor into saturation. And assume the overdrive voltage of M1 is 0.6Vand drain source potential of UP signal transistor is 0.6V.So the drain current and overdrive voltage are known from that we will get the (W/L) values of M1, M2 and input transistors. The proposed circuit is differential circuit.

CMOS design can be more advantageous in decreasing current mismatching issues normally associated with charge-pump design. The purpose of using differential design is improved phase-noise performance as all common mode noise will be removed. This means that there will be improved supply and ground noise rejection.

The power consumption was reduced by designing the charge pump to operate with modest current of 100µA.The total power dissipated by the charge pump is 334µW. In general, as the charge pump current Ids decreases, the charge pump's total average output noise also decreases.

The charge pump's output transistors M6 and M7 should have high output impedance. This will minimize current mismatch between up and down currents as the output voltage is varied. Furthermore, M6 and M7 must also be gm, matched to better equalize charge and discharge times respectively.

The output of the Phase frequency detector is connected to the Up and Down circuitry by which the signal is connected to the charge pump. The Up and Down circuitry provides the rectification for the delay by acting as the buffer stage and to provide the phase shift of 180 degrees respectively.

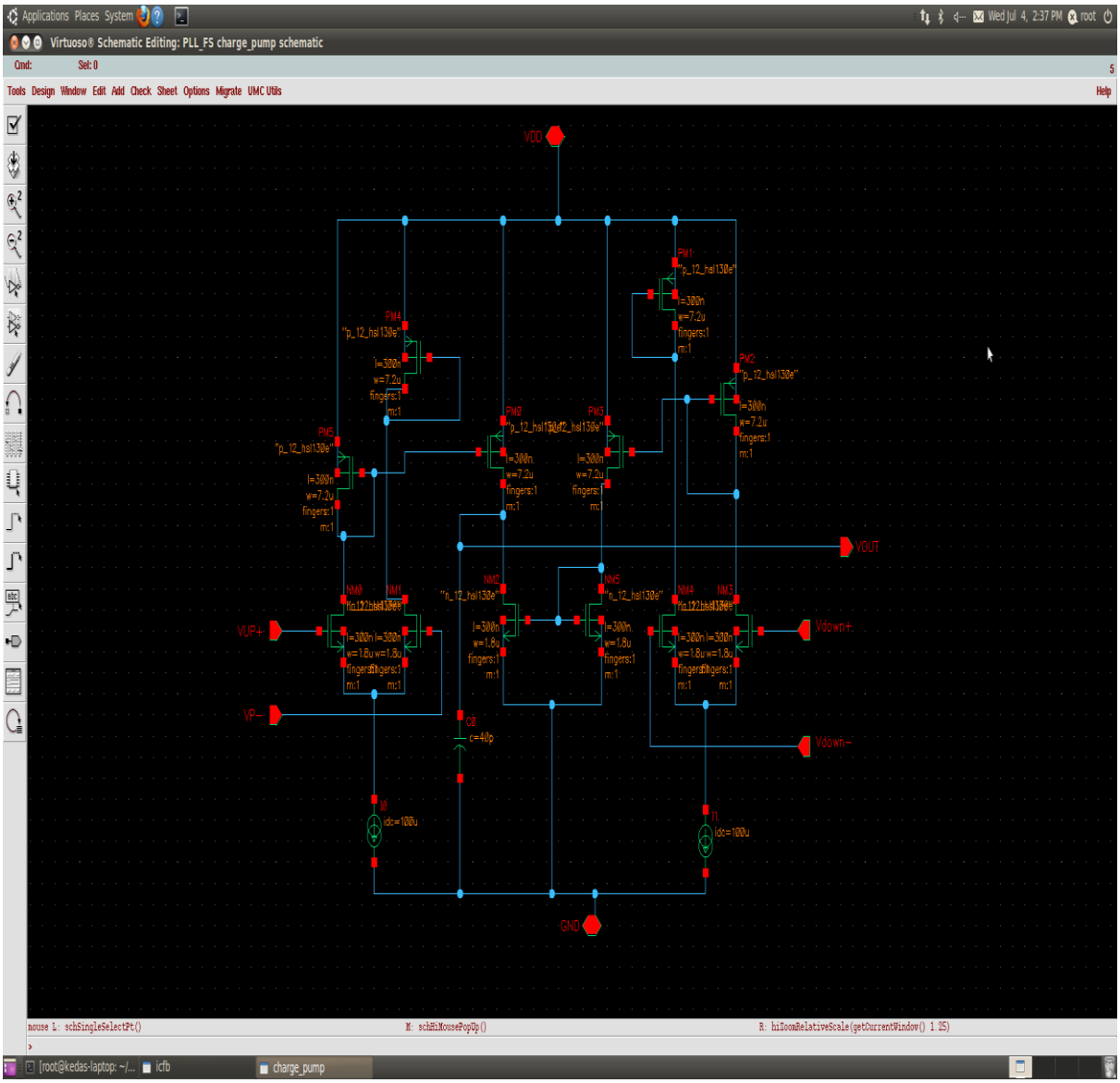
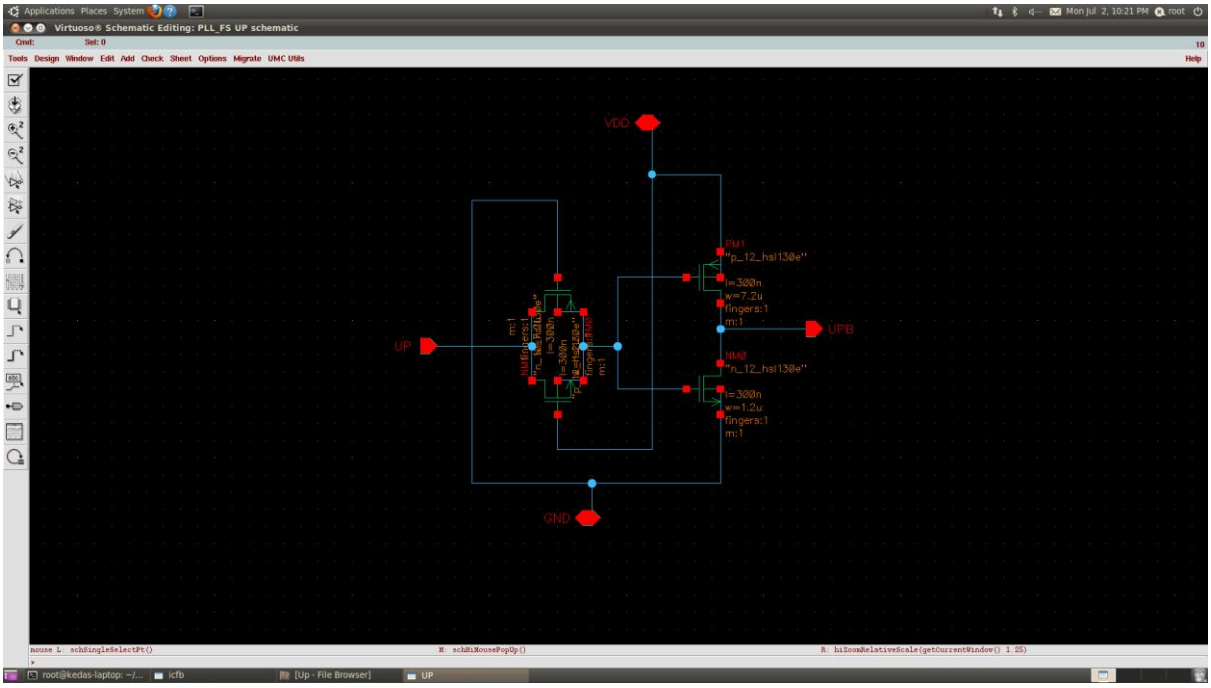


Figure 4.2.2: Virtuoso Schematic view of the charge pump

Figure 4.2.3: Schematic and symbolic representation of UP circuit



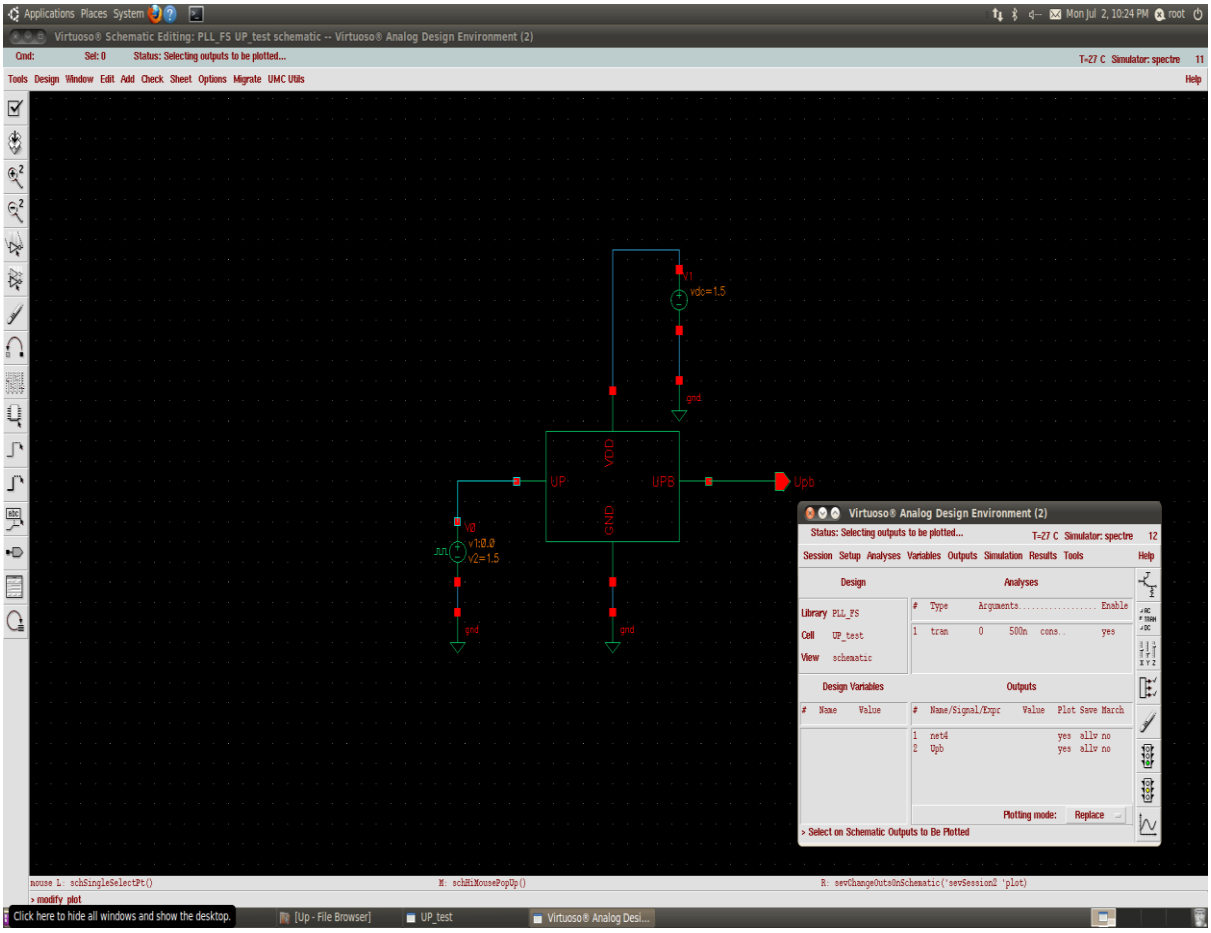


Figure 4.2.4: Transient response of the Up circuitry

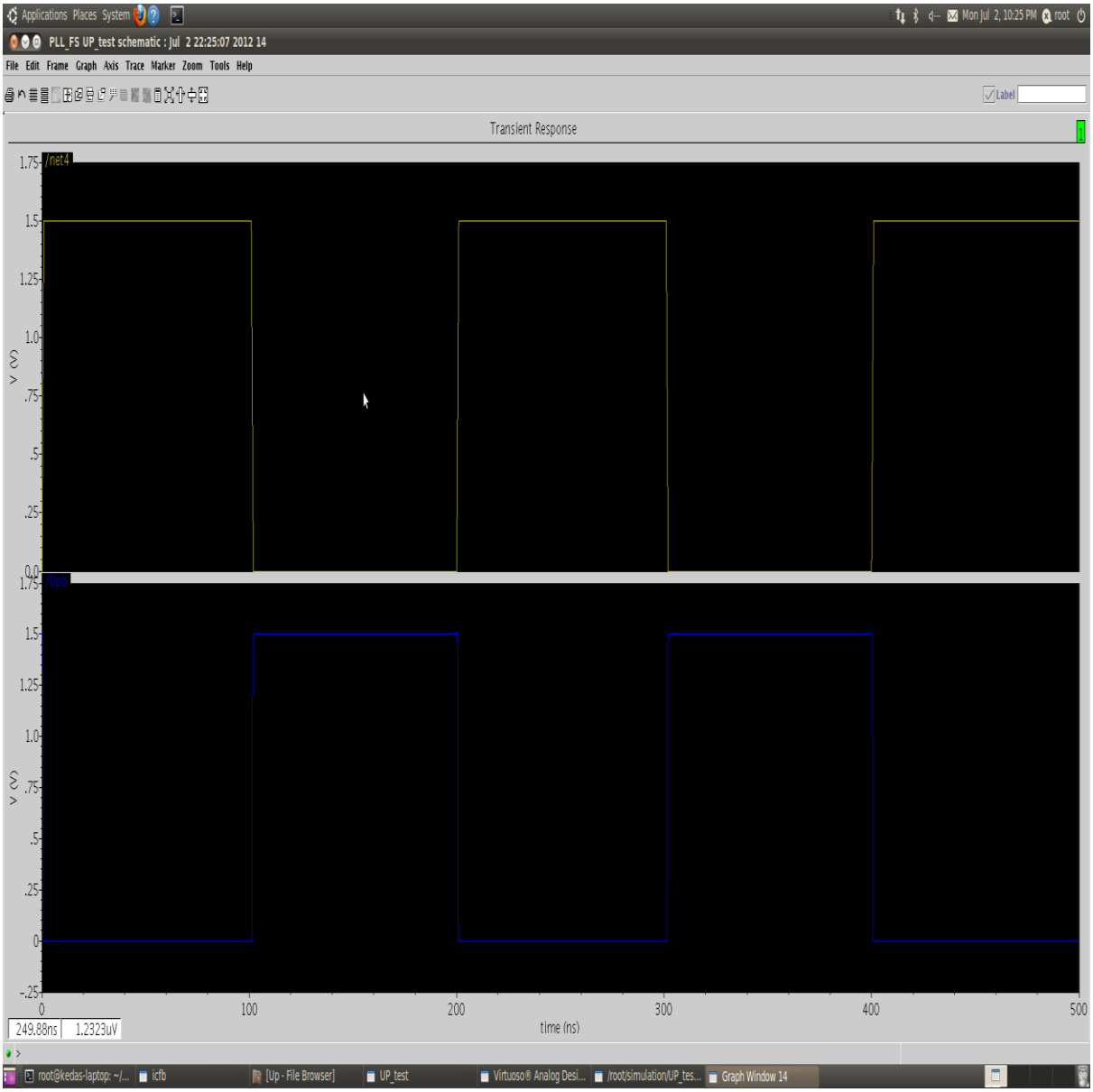
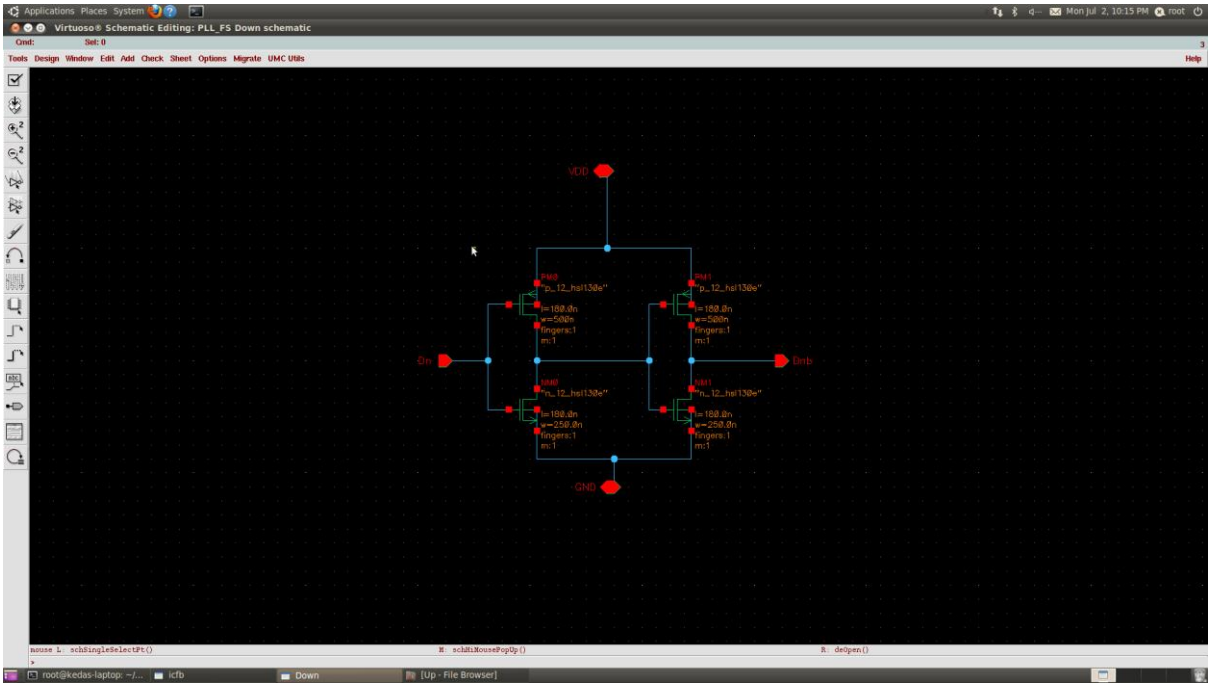


Figure 4.2.5: Schematic and symbolic representation of the down circuit



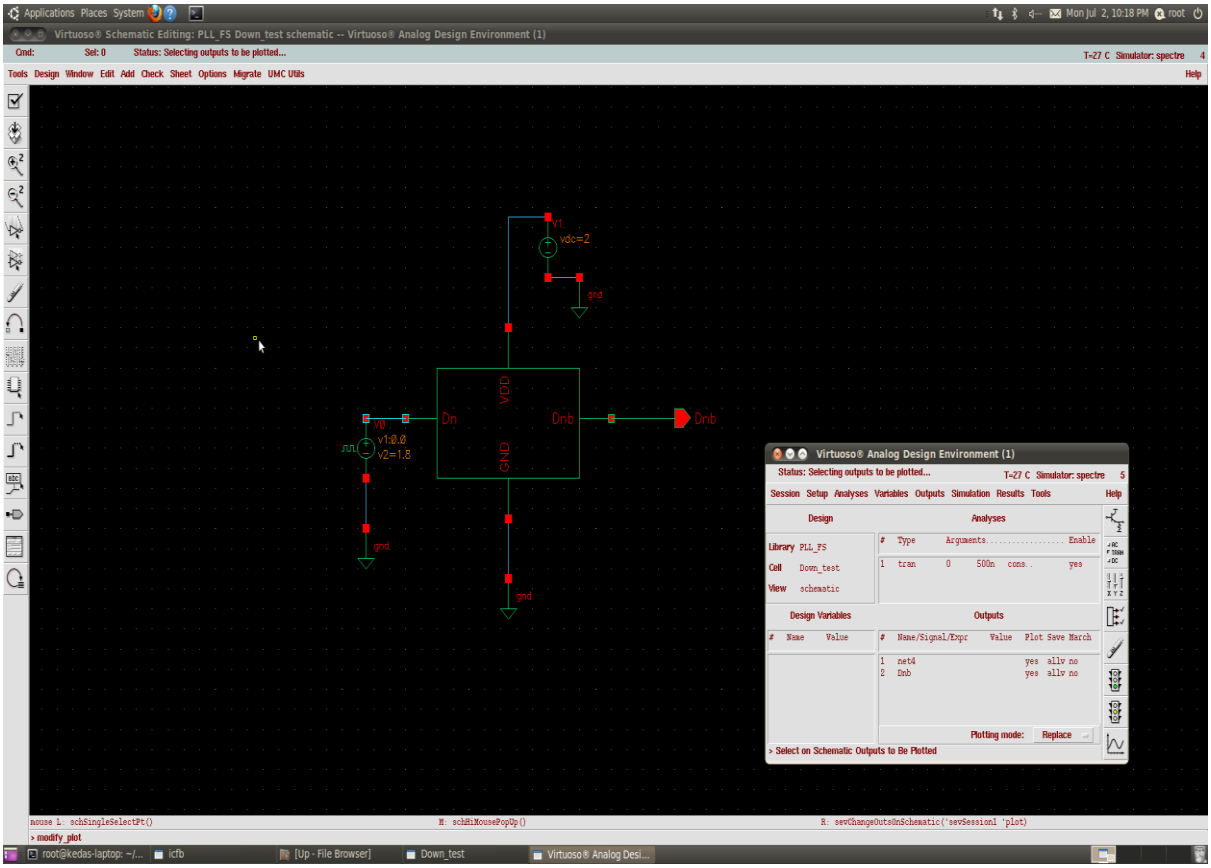


Figure 4.2.6: Transient response of the Down circuitry

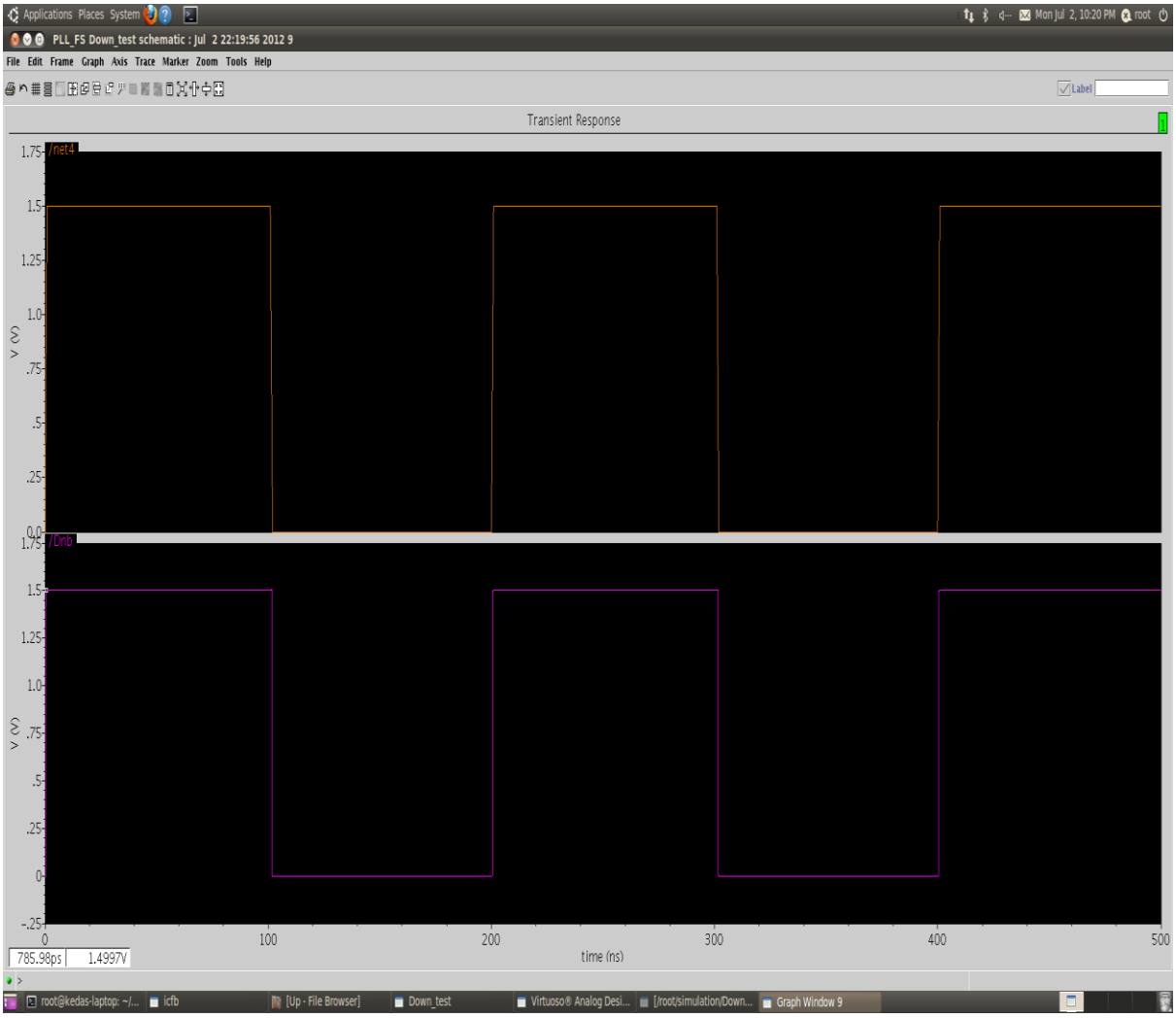


Figure 4.2.7: Appending the up and down circuits to the charge pump inorder to provide the positive and negative pulse for the circuitry

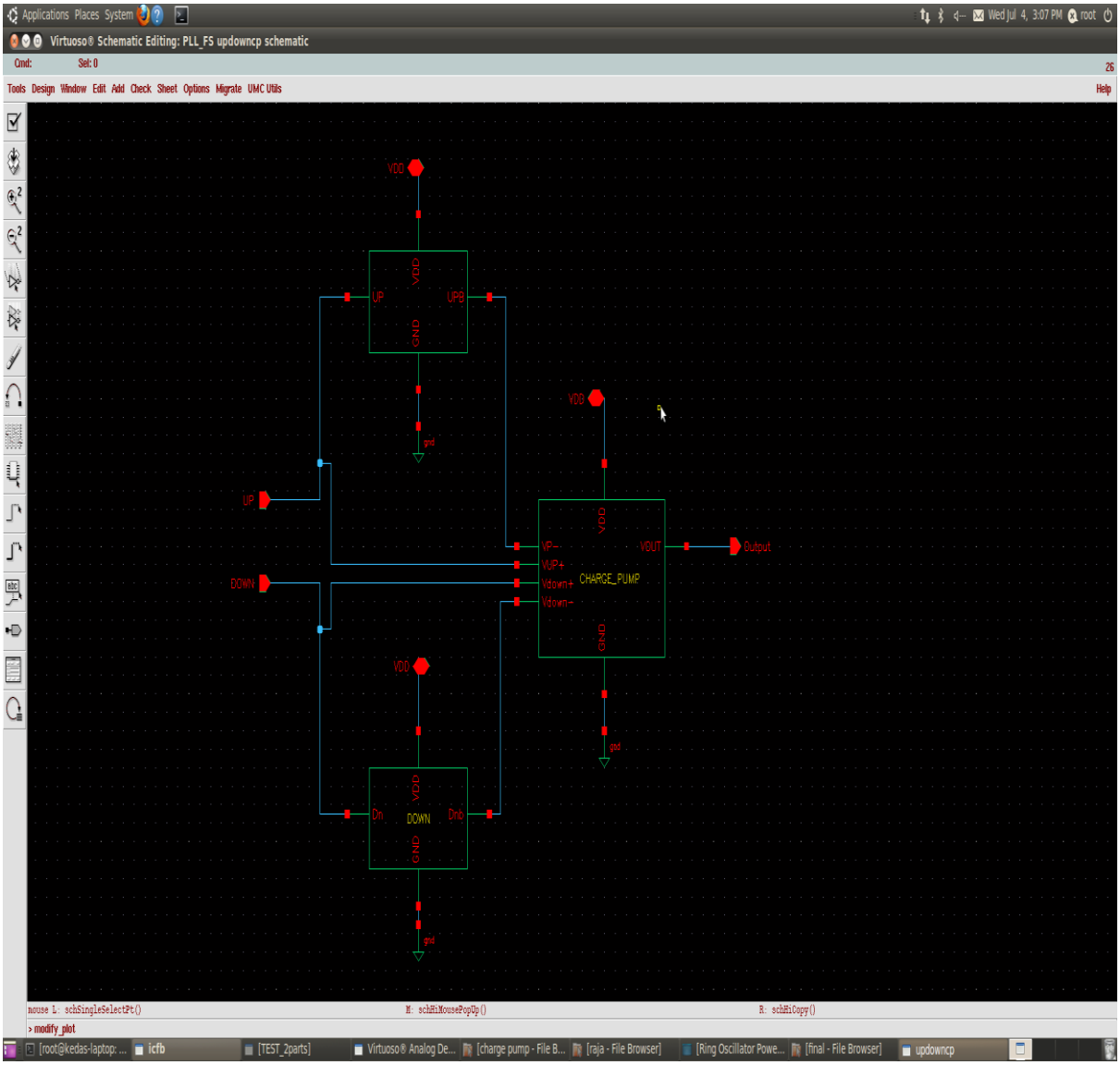
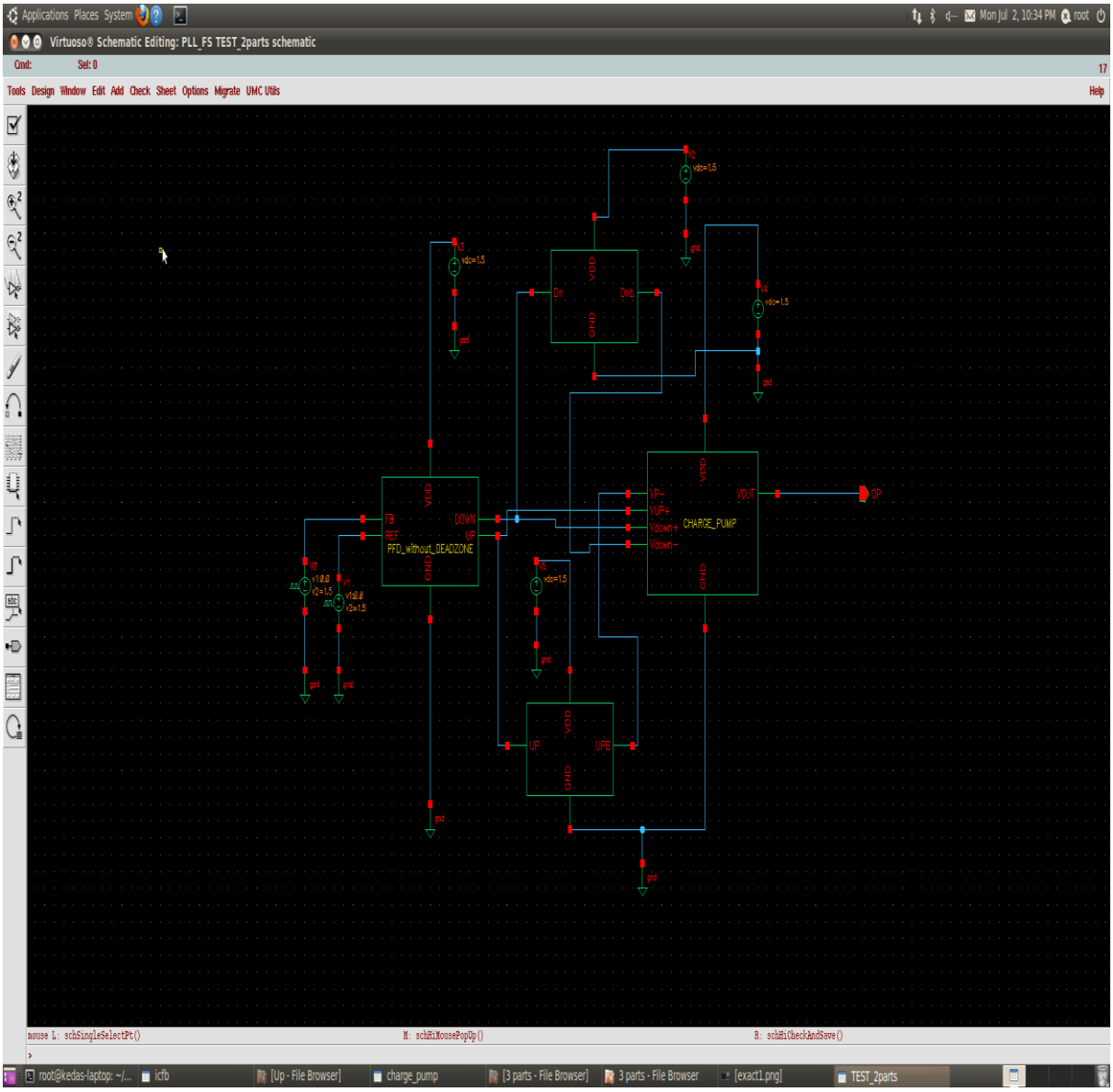


Figure 4.2.8: Appending the above functionality block to the Phase frequency detector



Simulation waveform of the combinational block (Phase frequency detector with Charge pump)

Figure 4.2.9: Output of Charge Pump for reference frequency leading frequency divider output

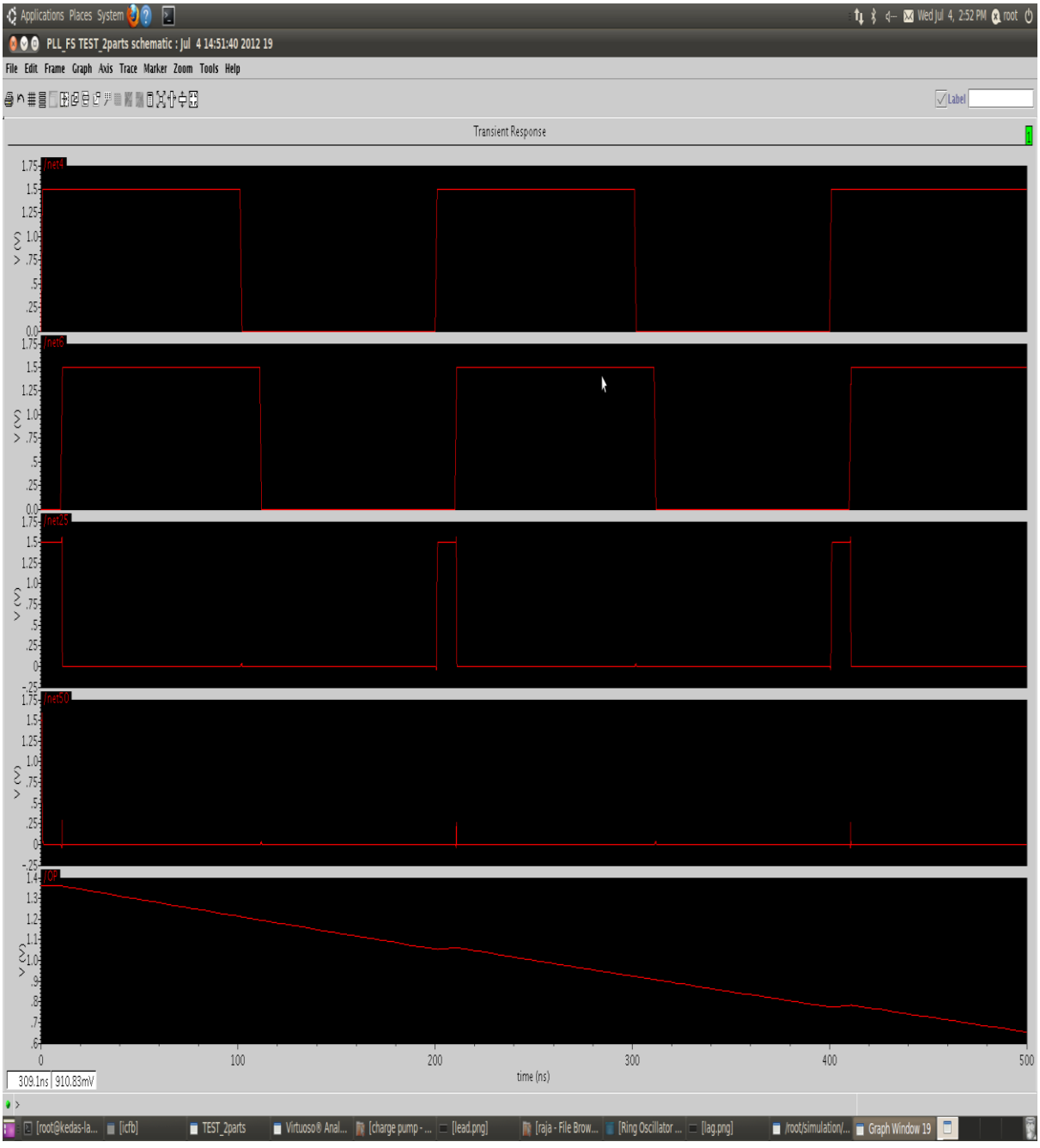
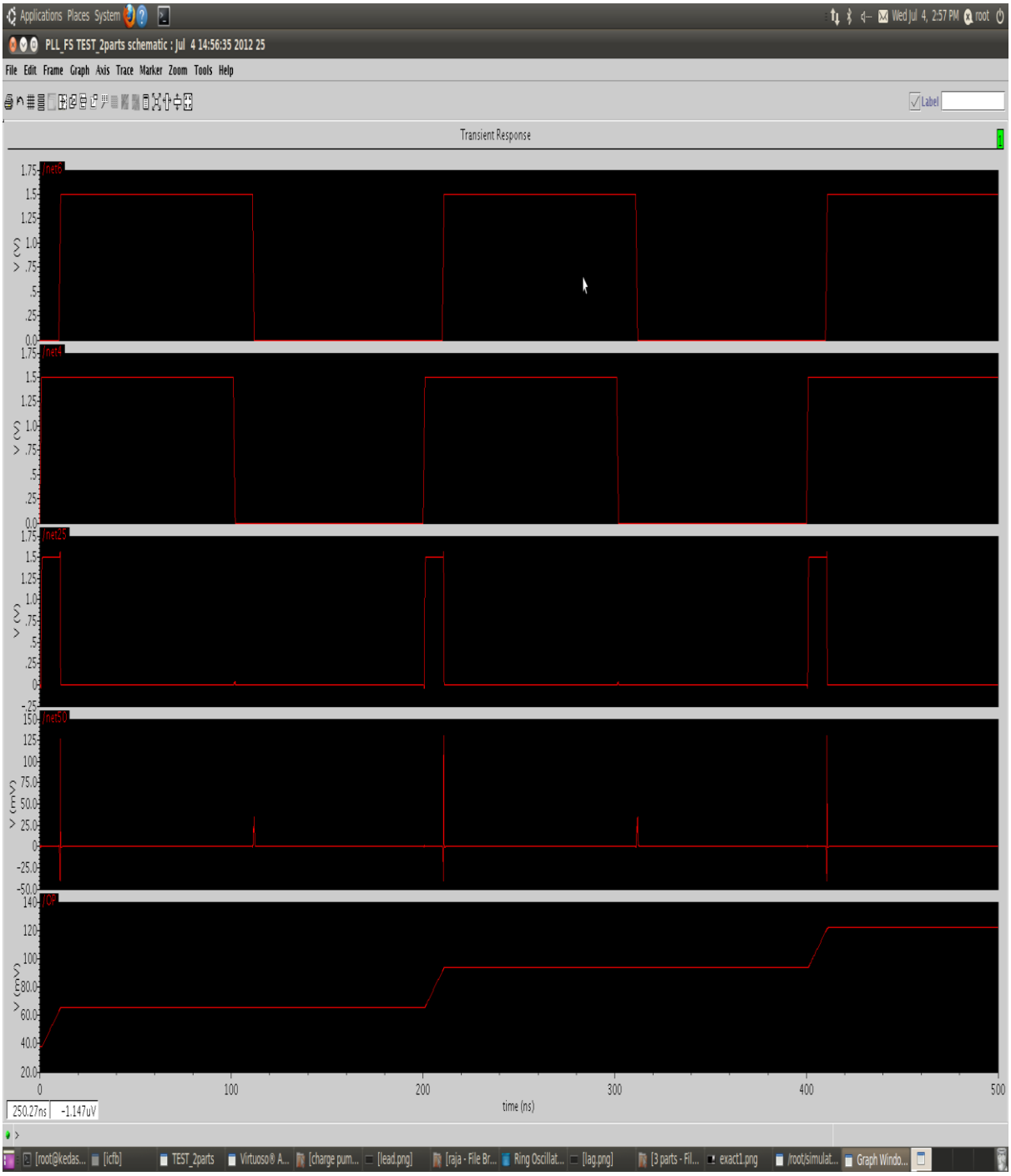


Figure 4.2.10: Output of Charge Pump for reference frequency lagging frequency divider output



4.3 Loop Filter Design

Loop filter design is considered as an important block of the frequency synthesizer design since most performance parameters (phase noise, stability, lock time, reference spurs) of the synthesizer depend on the loop filter parameters. A major design consideration in the design of Passive type loop filter is the PLL is to minimize the integrated phase noise to meet the specifications by changing charge pump current and loop bandwidth while meeting the lock time specifications and reference spur levels. The loop filter parameters Rz ,Cz and Cp are designed for given PLL parameters; Icp, Kvco and N and for specified loop bandwidth(Wc) and phase margin(Φm).

The PLL parameters; VCO gain and feedback divide ratio can be considered as design constants; however we have freedom to chose charge pump current value. Each charge pump current value will result in a set of loop filter parameters for given phase margin and loop bandwidth values. Smaller charge pump current results in smaller loop filter capacitance values and hence ease the loop filter integration.

The loop filter is designed to satisfy three requirements:

1. Loop stability (phase margin and peaking)
2. Phase noise matching between PLL and VCO
3. Acceptable spur suppression.

Loop filter resistor thermal noise: The thermal noise of the resistor appears as a noise on the control voltage of the VCO and hence gets gained up by the VCO gain. The noise contributed gets band-pass filtered by the PLL transfer function. To minimize this noise contribution, the loop filter resistor value and the gain of the VCO needs to be minimized. From the settling time, calculate the minimum loop bandwidth. To achieve a settling time of 50μs, the minimum loop bandwidth calculated from is 80KHz.

$$T_L = \frac{4}{f_c}$$

Here a loop bandwidth of fc = (wc/2π) = 120kHz which is 50% more than the minimum value, is chosen. Note that there are also other limitations on the loop bandwidth.

For example, the loop bandwidth should be less than 1=10 of the reference frequency for stability concerns. Moreover, the loop bandwidth affects the noise transfer characteristic of the PLL. To minimize the phase noise, the optimal loop bandwidth is where the high-pass VCO noise contribution is equal to the total low-pass noise contribution from the reference, PFD and charge-pump, etc.

Since the reference spur level requirement is not very stringent, a second order passive loop filter is adopted. Choose Wz=(Wc/3) and Wp2=(3Wc) that is Fz=(Wz/2π) and Fp2=(Wp2/2 π).

Therefore, the phase margin calculated from

$$\phi_m = \phi_z - \phi_{p_2} = \tan^{-1}(\frac{W_c}{W_z}) - \tan^{-1}(\frac{W_c}{W_{P_2}})$$

is Φm = 53 degrees. A large phase margin helps cover variations of the VCO conversion gain and loop filter values to guarantee the loop stability. Now, with a charge-pump current of Icp= 100 µA. the loop filter values of R1, R2 and C2 can be calculated from

$$W_z c = \frac{1}{R_1 C_1}$$

$$W_{p_2} = \frac{1}{R_1 \frac{C_1 C_2}{C_1 + C_2}} \approx \frac{1}{R_1 C_2}$$

$$W_c = \frac{I_{cp} R_1 K_{vco}}{2\pi N} \frac{C_1}{C_1 + C_2} = 2\pi * 1\ 2 * 10^6 rad\ \ s$$

From the above equation, calculated R1=2.4 K ohms.

Therefore the two capacitors are C1= (1/WzR1) =200pico farad
C2= (1/Wp2R1) =20pico farad

R1	2.4 kilo ohms
C1	200 pico farad
C2	20 pico farad

Table 4.3.1: Representing the values of resistor and capacitances of loop filter

Figure 4.3.1: Schematic and symbolic representation of loop filter

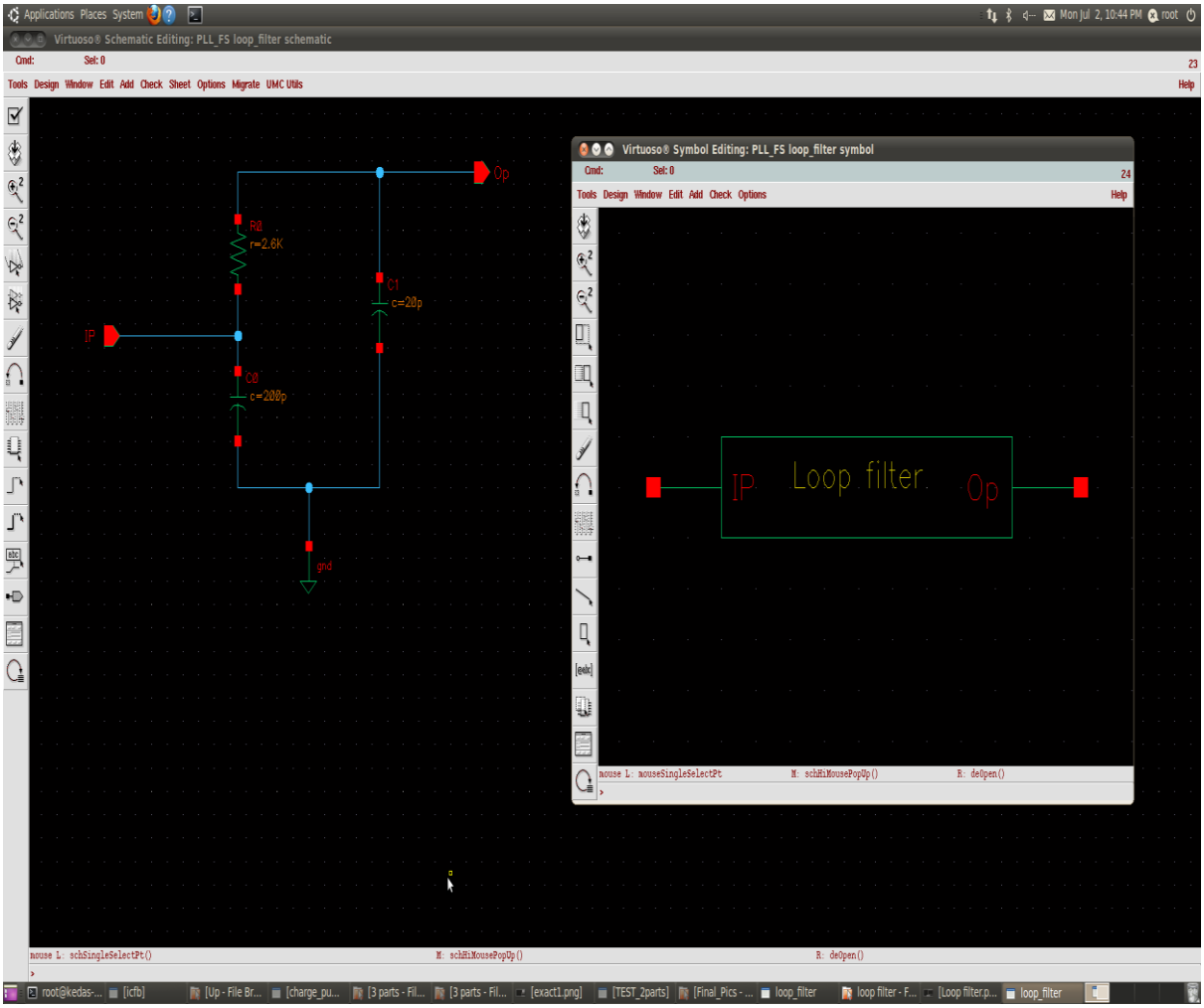


Figure 4.3.2: Appending loop filter Block to main circuitry

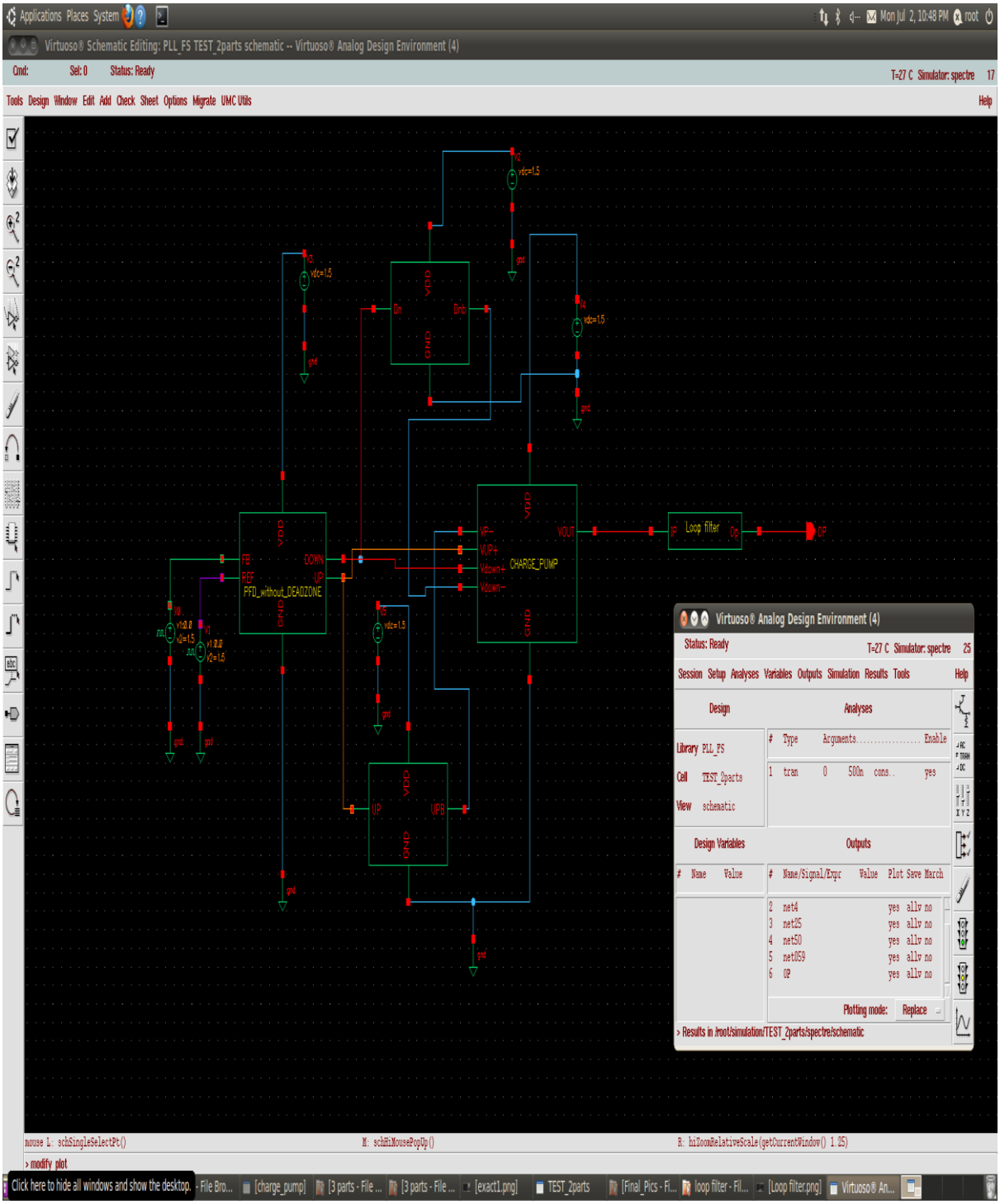


Figure 4.3.3: Resultant waveform after appending the loop filter with Phase lead

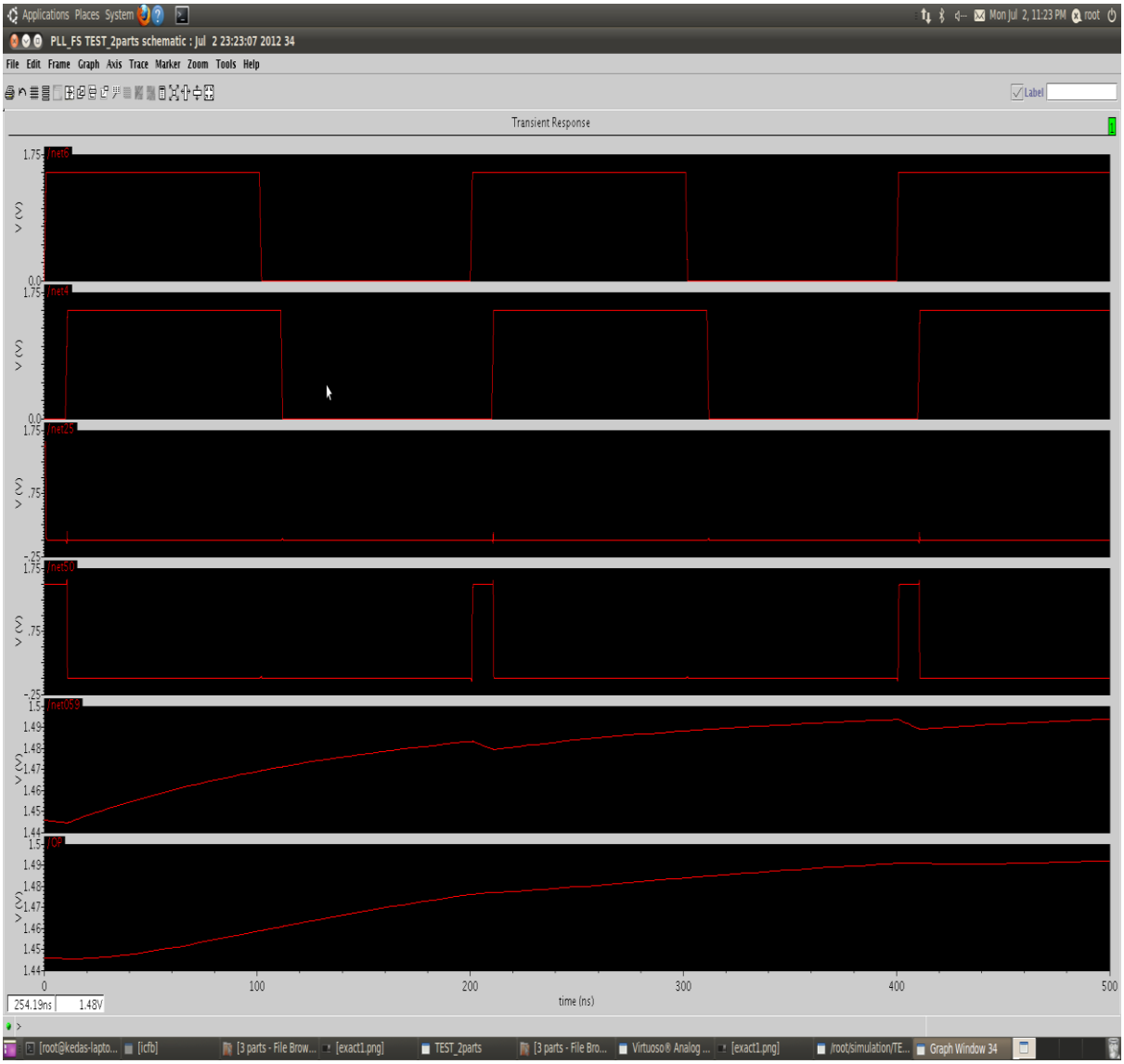
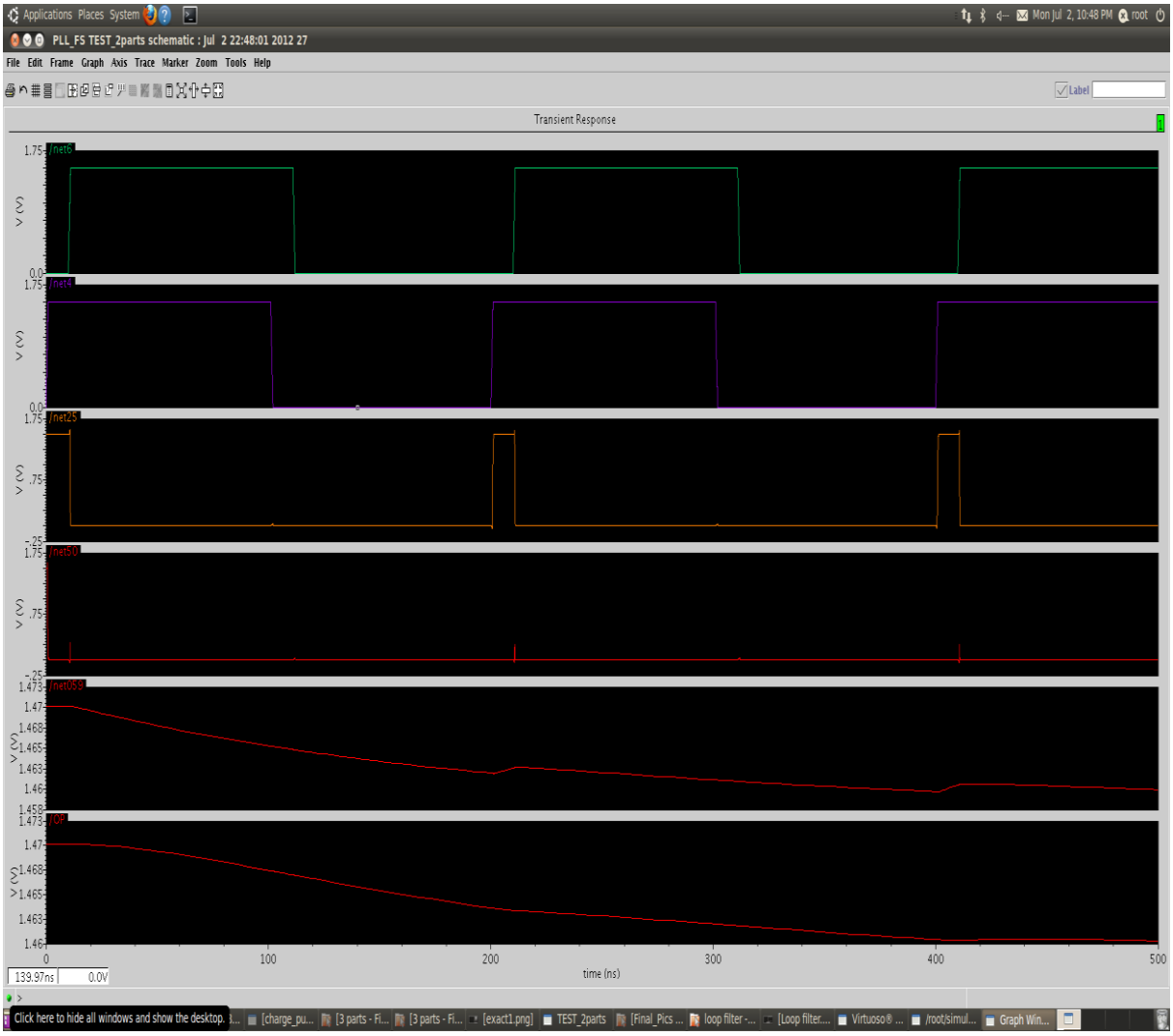


Figure: 4.3.4: Resultant waveform after appending the loop filter with Phase lags



4.4 DESIGN OF VOLTAGE CONTROL OSCILLATOR

Voltage Controlled Oscillators are main component which are widely used in communication systems. Chip minimization and simplicity of the circuitry are the main purpose for implementing this type controlled oscillator into this PLL system. It can be seen from the configuration of the VCO that there are only 18 transistors involved.

The operation principle of the Voltage control oscillator is similar to that of a ring oscillator functionality; ring oscillator may operate in a non-saturating mode at a very high frequency.

Basically, in the Voltage control oscillator configuration, the ring of inverters consists of an odd number of inverting stages to ensure that the oscillation in the circuitry. In the case of this design, an even number of stages (4 stages) is used instead, but a SET pin is implemented for the desirable functionality of starting the circuit operation.

The first stage of the VCO; the input voltage is applied at the input pin on the NMOS. As it can be seen, the current at the drain of both the NMOS and PMOS are the same and is controlled by the input voltage at input of the NMOS. The current from the first stage is then mirrored onto each inverter/current source stage. This inverter/current source stage is repeated four times in the design. The middle PMOS and NMOS operates as inverters and the top PMOS and bottom NMOS acts as current sources which limit the amount of current available to the inverter in the middle.

The complete VCO configuration is designed with the SET pin. The SET pin is implemented with a NAND gate placed between the feedback loop of the first and last stage of the inverter/current source stage. As stated earlier, the SET pin is needed to start the oscillation within the VCO. In this particular design, since the SET pin is being implemented with a NAND gate, the SET input must always stay high to ensure oscillation. The two inverters at the end are needed to buffer out the output of the VCO.

The design of the complete block diagram of the voltage control oscillator has been made in step by step procedure. Each block the Voltage control oscillator has 3 individual blocks. The three individual blocks are as follows

1. Current source stage
2. NAND gate
3. Inverter gate

These three stages has been designed schematically and verified. The following represents of the schematics of the NAND gate, Inverter and the Current source stage.

Figure 4.4.1: Schematic of current source stage

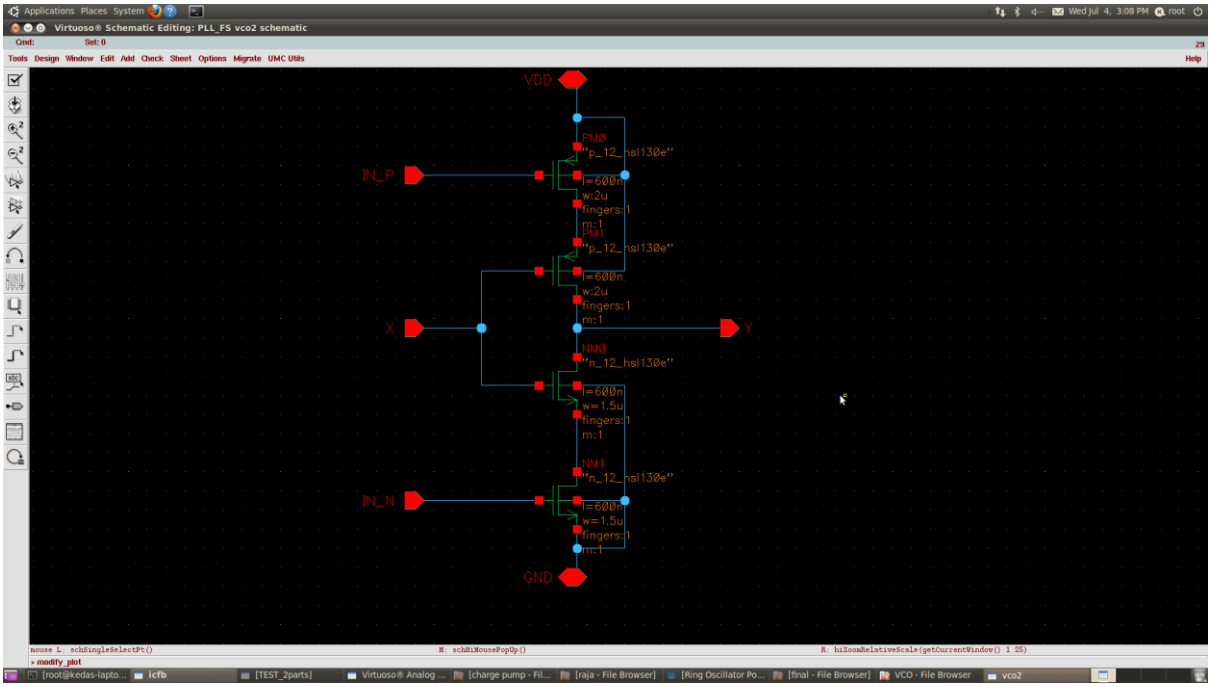


Figure 4.4.2: Schematic of NAND gate

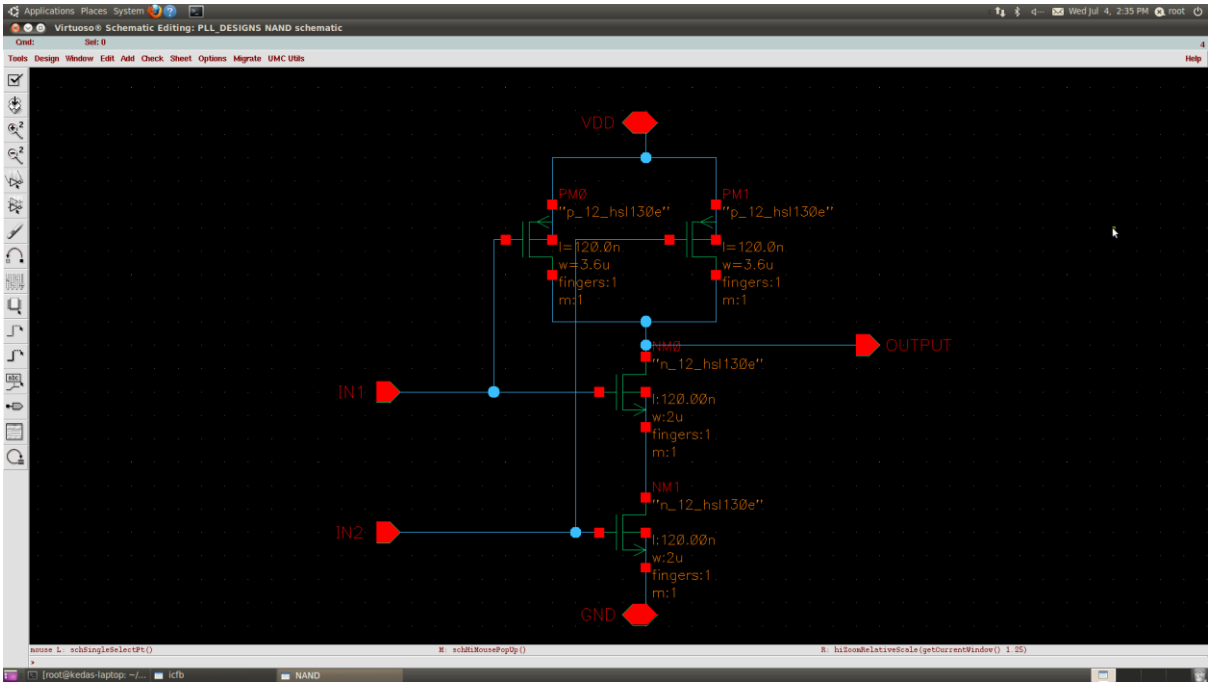
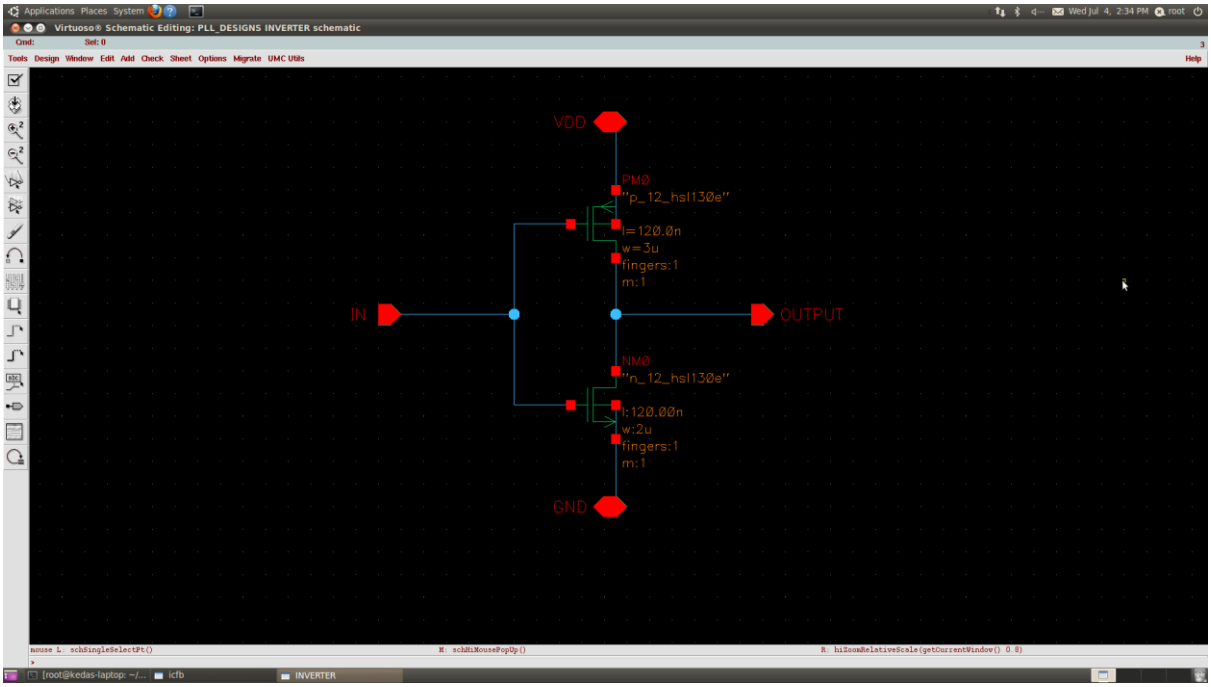


Figure 4.4.3: Schematic of inverter gate



The schematics of the current source stage, inverter and nand gate are verified for its accurate functionality before combining them in the complete block diagram represented in Figure 4.4.4.

Figure 4.4.4: Complete Block implementation of the VCO

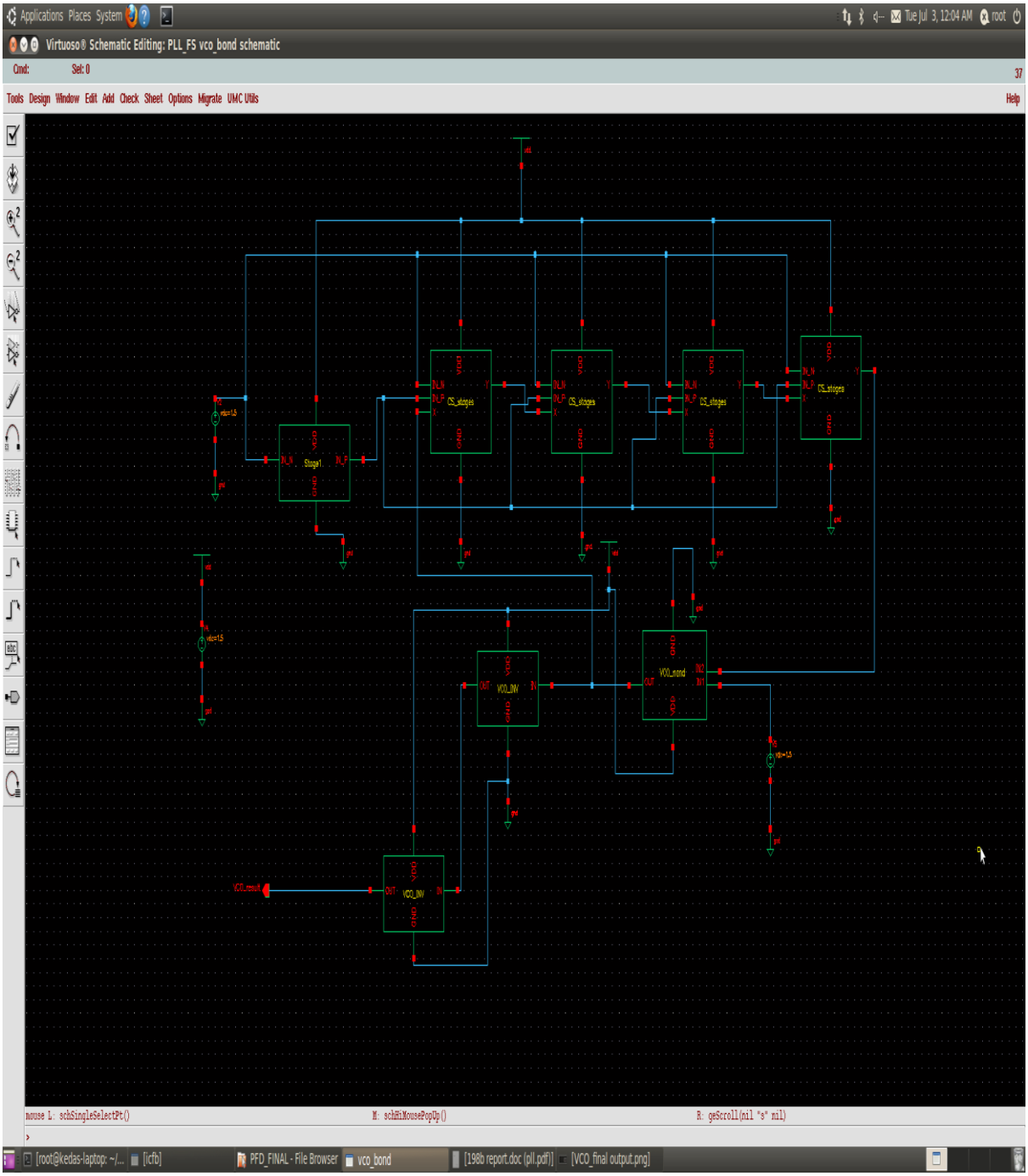
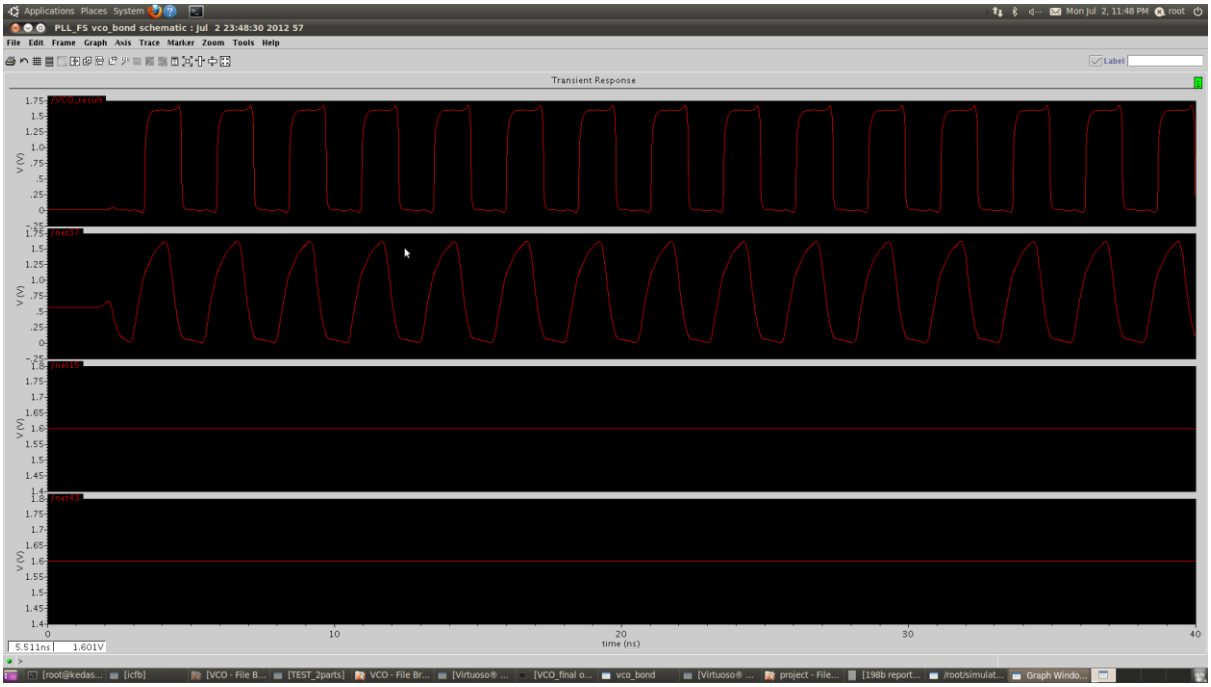
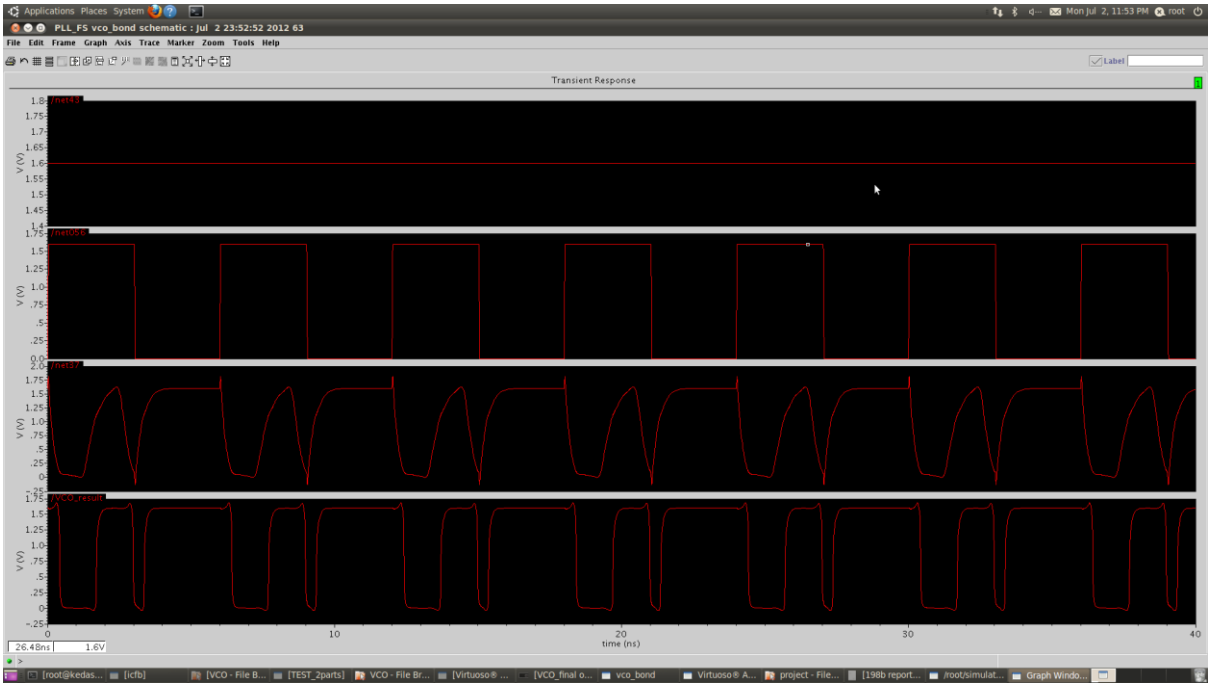


Figure 4.4.5: Transient response of the VCO with setup signal



From the transient response waveform in figure 18, the INPUT pin is always set to high to bias the circuit to be on. The SET pin of the NAND gate is also always on high to insure that the VCO would constantly oscillate. The VCO is definitely oscillating with clean and strong output.

Figure 4.4.6: Transient response of the VCO by varying the setup signal



The SET pin of the NAND gate is crucial to the design of this Voltage control oscillator because without it, the VCO would not function correctly. For Observation without its functionality if the SET pin is not "high" all the time, the VCO will not produce oscillations, it will only change state at the output when the SET pin change state. This complete observation can be seen in the above transient response waveform of the VCO.

Control voltage	Oscillating frequency
1.6 volts	190 Mega hertz
1.9 volts	230 Mega hertz
2.3 volts	255 Mega hertz

Table 4.4.1: VCO characteristics for Control voltage and oscillating frequency

4.5 Design of frequency divider

The divider circuit performs the operation of reducing the frequency of the VCO output by a factor before feeding it back to the input of the PFD. This single component (if ideal) gives the entire system the capability to operate in an infinite range of frequency. With a non-programmable divider, the input frequency is limited to a single input. A non-programmable divider is adequate since the input frequency is specified to be limited to a single constant value.

There are various types of non-programmable dividers, but the most commonly implementation is based on flip-flops such as the D, T, and JK. All these types provide similar performance capabilities and are suitable for this application. While many divider structures exist, a digital approach was used for this project consisting of two D Flip Flops. The circuit was designed to use as little power as possible while maintaining functionality. The frequency divider is designed for the following specifications shows in Table.4.6.1:

Design parameters	Specified Values
Supply voltage	1.5 volts
Input frequency	500Mhz to 1.7Ghz
Division ration	Up to 8

Table.4.5.1: Frequency divider design specifications

Before configuring positive-edge triggered D-FF to divide by four, the first step is the flip- flop needs to first divide by two. A D-FF consists of two inputs (D and CLK) and two outputs (Q and Q not). To convert the D-FF into a frequency divider, the D-input is first tied to Q not. The input signal is given into the CLK and the output is taken at Q. this is basic operation of toggling the signal which performs the frequency division operation. Since the flip-flop is positive-edge triggered, the D-FF will output the value of D when the clock is on the rising edge.

Assuming the initial state of Q is zero, then Q not and D are set to one. On the first rising edge of the input signal, the FF will sample D (D=1) and the output one (Q=1). This will convert Q not and D to zero and the flip-flop will wait until the next rising edge of the CLK. On the next rising edge of the signal, the D-ff will again sample the input D (D=0) and output zero. Q not will go back to one and the cycle will repeat. For every two periods of the input signal, the flip-flop will output a signal twice the original period. This effectively divides the signal's frequency by a fact of two (f = 1/T). To divide by a factor of four, another D-FF is implemented in the same configuration. The Q of the first flipflop is connected to the CLK of the second D-FF and the output will have a period of 4 times larger than the original input.

The process of dividing the signal by desired factor is performed by cascading the stages of the primarily performed Divider-by-4. Thus by cascading the two blocks of Divider-by-4 results in the Divider-by-8.

The aspect ratios (W/L) of the transistors employed in DY-FFs determine its operation speed. As far as the power efficiency is concerned, the DY-FFs may be used for high speed operation, Low power dissipation is also one of our major concerns for selecting the size of FFs. Therefore, to develop a divider which achieves lower power consumption, the transistors in the first stage required larger aspect ratios. The transistor sizes in the second stage are smaller. Since the later stages have smaller Fin, max, their transistor sizes can be reduced accordingly.

Transistors	Width	Length
M1	500nm	180nm
M2	500nm	180nm
M3	125nm	180nm
M4	250nm	180nm
M5	250nm	180nm
M6	250nm	180nm
M7	250nm	180nm
M8	250nm	180nm
M9	250nm	180nm
M10	500nm	180nm
M11	500nm	180nm
M12	125nm	180nm
M13	250nm	180nm
M14	250nm	180nm
M15	250nm	180nm
M16	250nm	180nm
M17	250nm	180nm
M18	250nm	180nm
M19	500nm	180nm
M20	250nm	180nm

Table 4.5.2: Transistor sizing for the divider

Figure 4.5.1: Schematic design of the frequency Divider-by-4

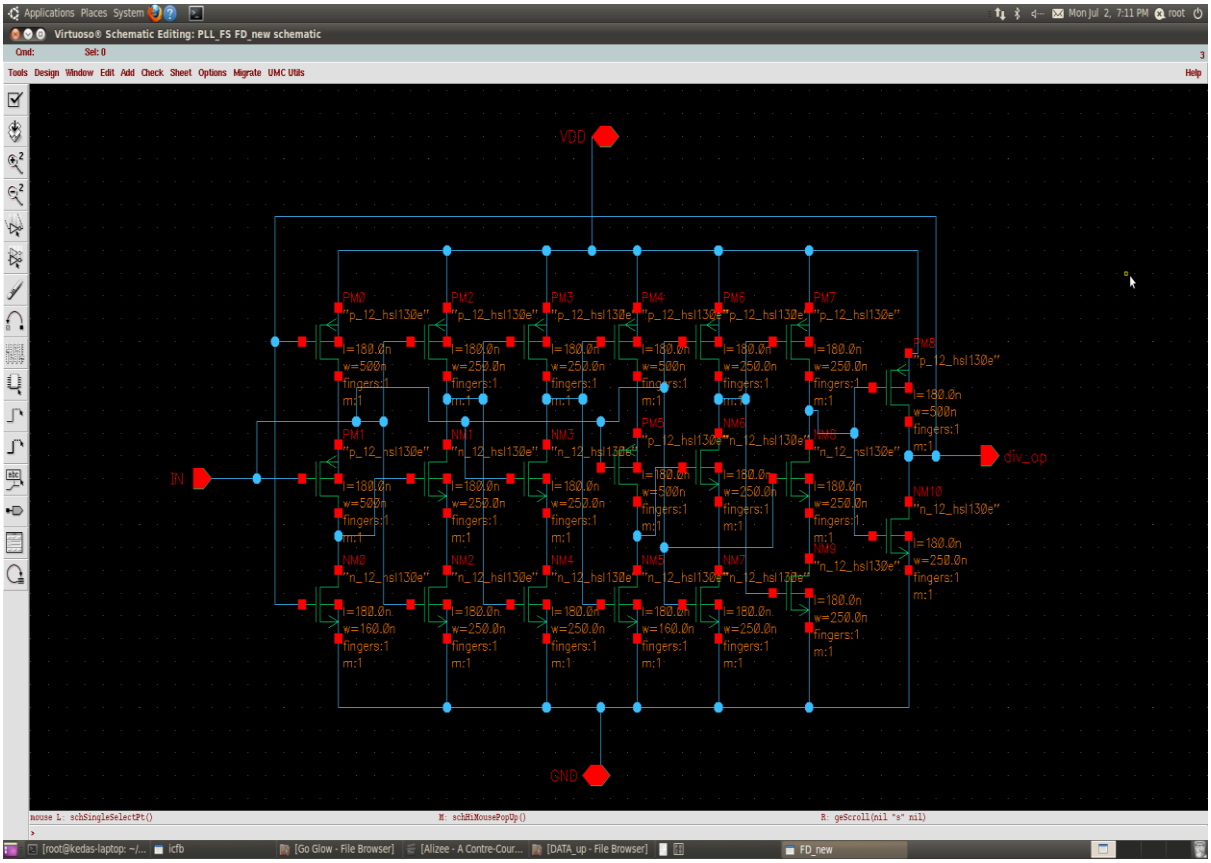


Figure 4.5.2: Symbolic representation of the Divider-by-4

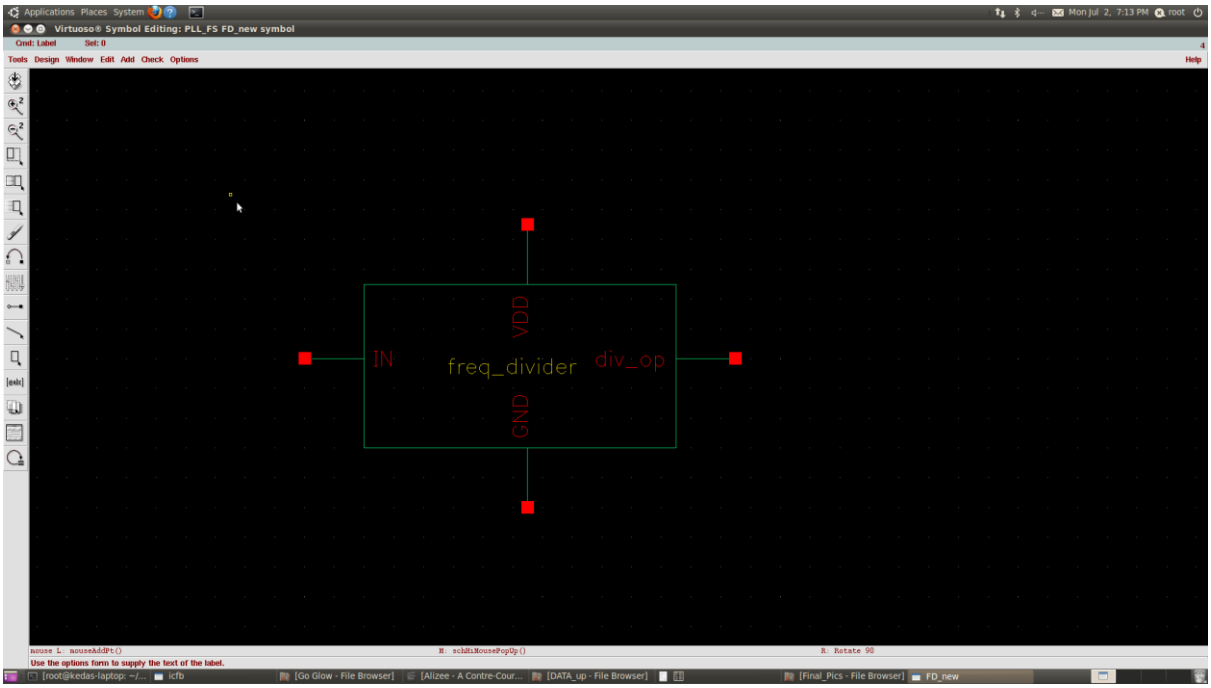


Figure 4.5.3: Testing the frequency divider-by-4

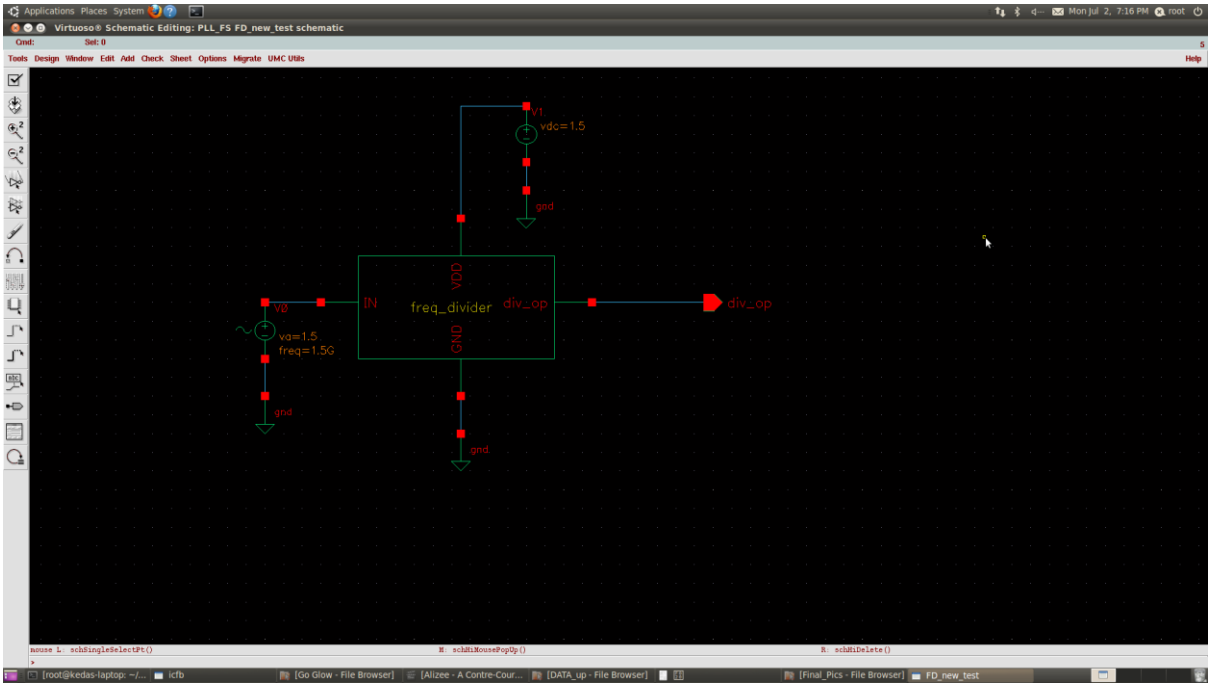


Figure 4.5.4: Transient response Output waveform of the divider

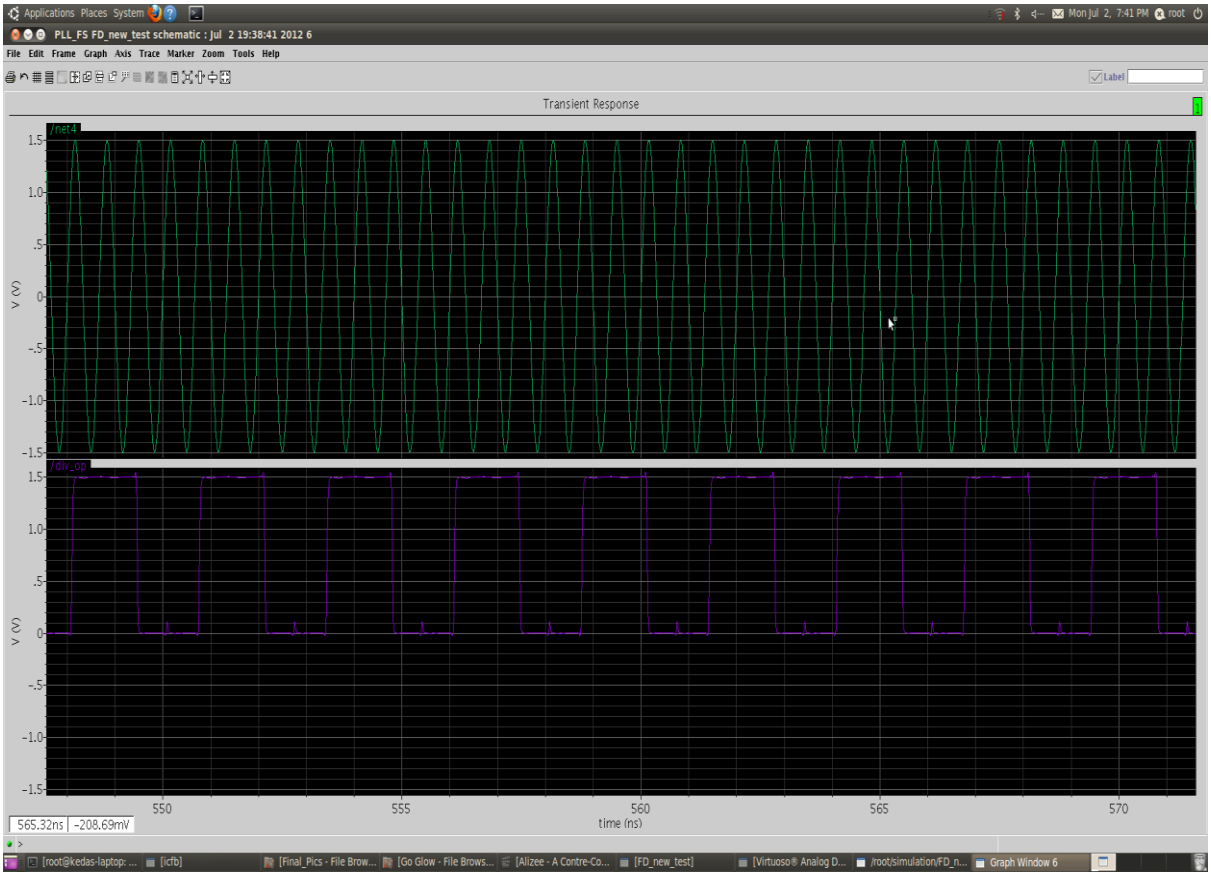


Figure 4.5.5: Cascaded symbolic representation of the divider-by-8

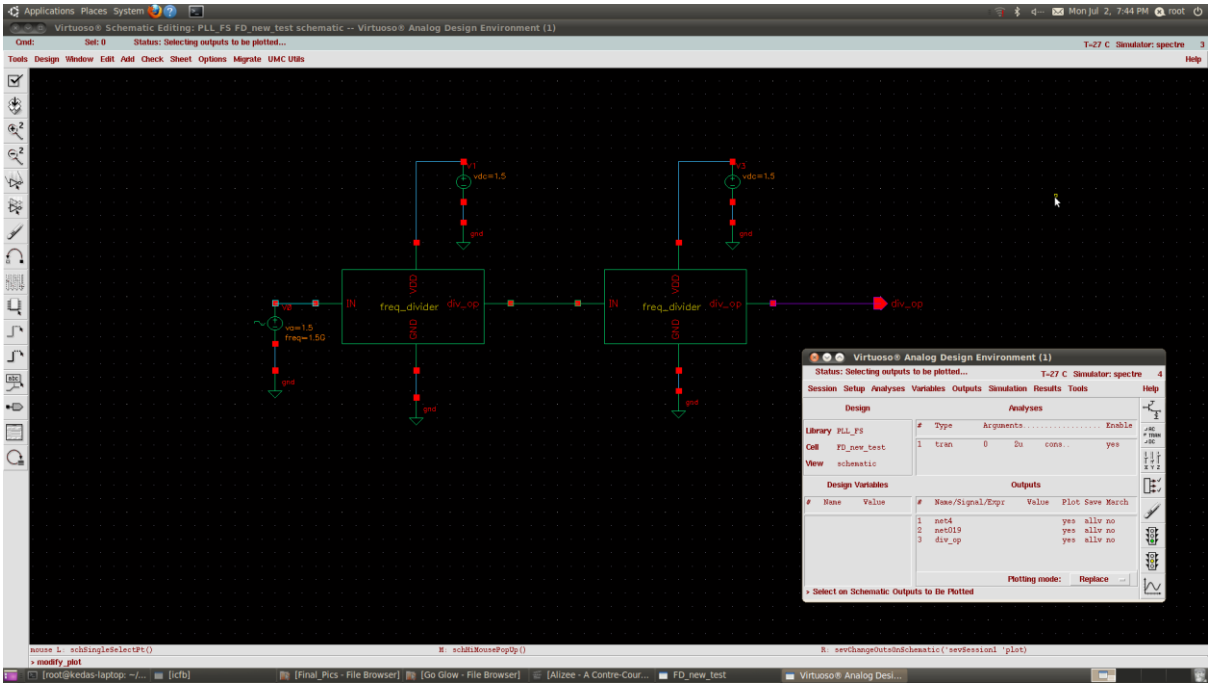
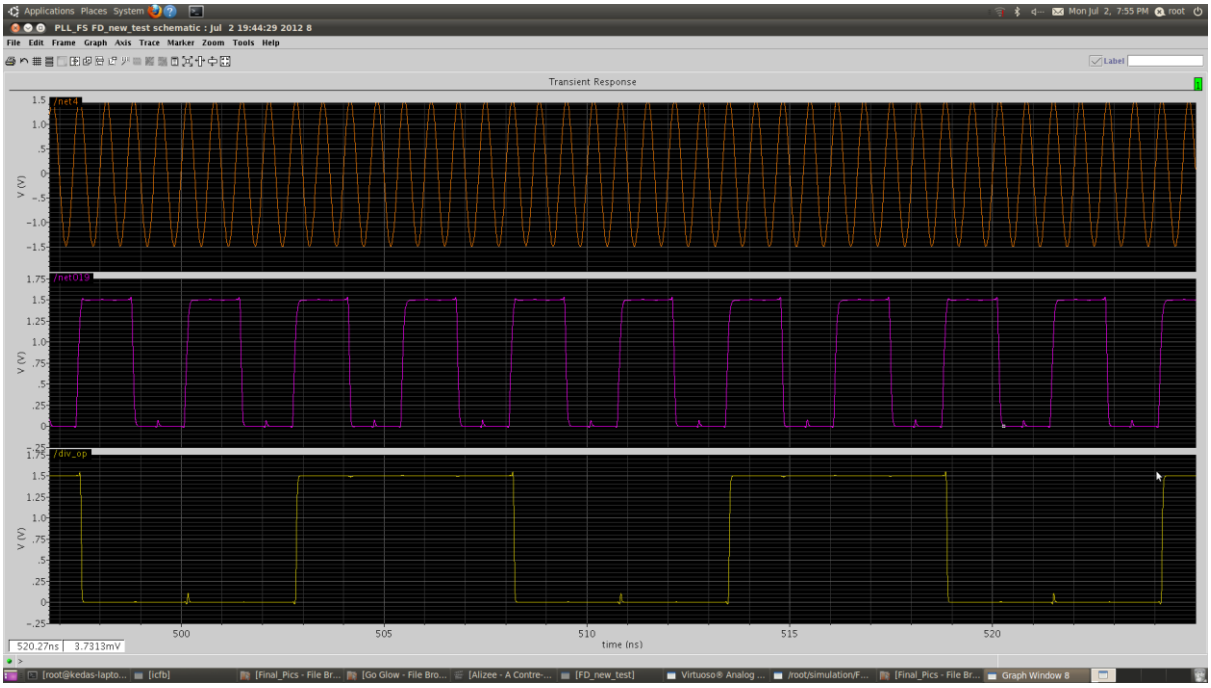


Figure 4.5.6: Transient response Output waveform of the resultant cascaded representation of Divide-by-8



CHAPTER: 5

Conclusion and Future Work

The entire design was carried out in proprietary UMC 130 nm CMOS technology. The design phase locked loop (PLL) was carried out which operates in the frequency range upto 1.8 Giga hertz. The design has been very precise in each individual component to maintain in its functionality. The modified Phase frequency detector which rectifies the reset path control over the dead zone is performed. The differential charge pump along with the passive loop filter is designed according. The voltage controlled oscillator is designed by the concept of the ring oscillator which is controlled by setup signal operates in high frequency range obeying the property of linearity with control voltage. The simple basic divider is considered in the design to obtain frequency division by 8.

The main component which contributes to the power consumption and operates in very high frequency range has to be chosen with accurate results. In future work the Active loop filter designed with operational amplifiers leads to reduce the non-linearity has to be designed. The Voltage control oscillator has to be designed which covers a wide range. The Divider has to be designed with recent technologies of programmable high frequency and low power consumption characteristics.

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2. http://www.minicircuits.com/pages/app_notes.html

3. www.circuitsagebeta.com

4. http://www.complextoreal.com/chapters/pll.pdf

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