A

Major Project Report

On

FREQUENCY SYNTHESIZING USING PHASE LOCK LOOP FOR HIGH FREQUENCY APPLICATIONS

Submitted in Partial fulfilment of the requirement

For the award of the degree of

MASTER OF TECHNOLOGY

In

(VLSI & Embedded Systems)

Submitted by

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DTU/M.Tech/160

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July 2012

DECLARATION BY THE CANDIDATE

July 2012

Date: _____

I hereby declare that the work presented in this dissertation entitled **"FREQUENCY SYNTHESIZING USING PHASE LOCK LOOP FOR HIGH FREQUENCY APPLICATIONS"** has been carried out by me under the guidance of **Mr. Rajesh Rohilla**, Associate Professor, Department of Electronics & Communication Engineering, Delhi Technological University, Delhi and hereby submitted for the partial fulfillment for the award of degree of Master of Technology in VLSI & Embedded Systems at Electronics & Communication Department, Delhi Technological University, Delhi.

I further undertake that the work embodied in this major project has not been submitted for the award of any other degree elsewhere.

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CERTIFICATE

It is to certify that the above statement made by the candidate is true to the best of my knowledge and belief.

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ABSTRACT

Increase in demand for affordable high performance communication devices, particularly in mobile systems, is the driving force behind the development of high speed, low cost and low-power circuits in CMOS technology. This is mainly due to the fact that CMOS process facilitates the integration of analog and digital circuits on the same chip. A major technique to reduce the power consumption in a CMOS chip is the use of low swing signalling. Integrated phase locked loops(PLL's) are the versatile components in many communication and control applications.

PLL's are the integral part of many communication and computing applications.. The designed PLL operates from a single 1.5 Volts supply and its frequency range of operation is upto 1.8 giga hertz. The phase locked loop each individual components such as Phase frequency detector, charge pump, loop filter, Voltage control oscillator and divider is designed for frequency synthesizing. The PLL is designed and simulated in a 130 nano metres standard CMOS technology

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