CHAPTER -1

INTRODUCTION

1.1 Background

Operational amplifier is undoubtedly one of the most versatile and an integral part of many analog and mixed-signal systems. With variety of different levels of complexity operational amplifier (op-amp) to be used so as to realize functions ranging from a basic simple dc bias generation to high speed amplifications or filtering. By using only few of external components, operational amplifier can perform a number of analog signal processing tasks. General purpose operational amplifier (op-amp) can be used as buffers, summers, integrators, differentiators, comparators, negative impedance converters, and many other various applications. Today Op-amps are among the most widely used electronic devices, being used in a vast array of consumer, industrial, and scientific devices.

Operational Amplifiers are commonly known as Op-amps. In spite of being most common analog circuit Operational Amplifier are among the most widely used building blocks in Analog Electronic Circuits. Op-amps are used equally in both analog and digital circuits. The efficient performance of operational amplifier makes significant impact on the analog systems. With the improved computer aided design (CAD) tools, advancements of semiconductor modeling, steady miniaturization of transistor scaling, and the advanced fabrication processes, the integrated circuit market is growing rapidly and continuously. Recently, significant efforts have been made in reducing the power consumption of the operational amplifiers and in developing and designing circuits that can operate with extremely small voltage supplies. The increasing trend toward implementing systems with low supply voltages has created challenging task in the designing of modern analog circuits. The realization of high-speed, high gain, large gain-bandwidth product, and low power amplifier [1, 2] demands innovative circuit design techniques and advances in integrated circuits process technology.

CMOS technology has become more attractive that were traditionally built with bipolar transistors. As MOS channel length decreases, the transistor cut-off frequency increases and the realization of CMOS wideband amplifiers becomes more feasible. For

these, many techniques are presented to design CMOS wideband amplifiers. These are then later optimized for minimum power consumption [2, 3]. CMOS technology can offer a higher level of integration and has the ability of operating at relatively low supply voltages. With transistor length being scaled down to a few tens of nanometers, analog circuits are becoming increasingly more difficult to improve upon. So, as the transistor is scaled, the higher is its packing density, the higher its circuit speed, and the power dissipation gets lower [4].

To increase the intrinsic gain of CMOS devices, there is the need in the MOSFET design industry to shrink the gate oxide thickness, t_{ox}, which results in reduction of the tolerance at the gate for high voltage levels. So, for reliability purposes, it is advantageous to reduce the maximum voltage supply $V_{DD.}$ But by reducing supply voltage, forces analog designers to face challenges such as reduced input common mode range, output swing and linearity. Designing of high-performance analog circuits is becoming more challenging with the persistent trend toward reduced supply voltages as V_{T0} does not scale in a linear fashion with the reduction in minimum device length at the same rate as V_{DD}. Some fabrication processes offer low V_{T0} which suites for analog blocks.

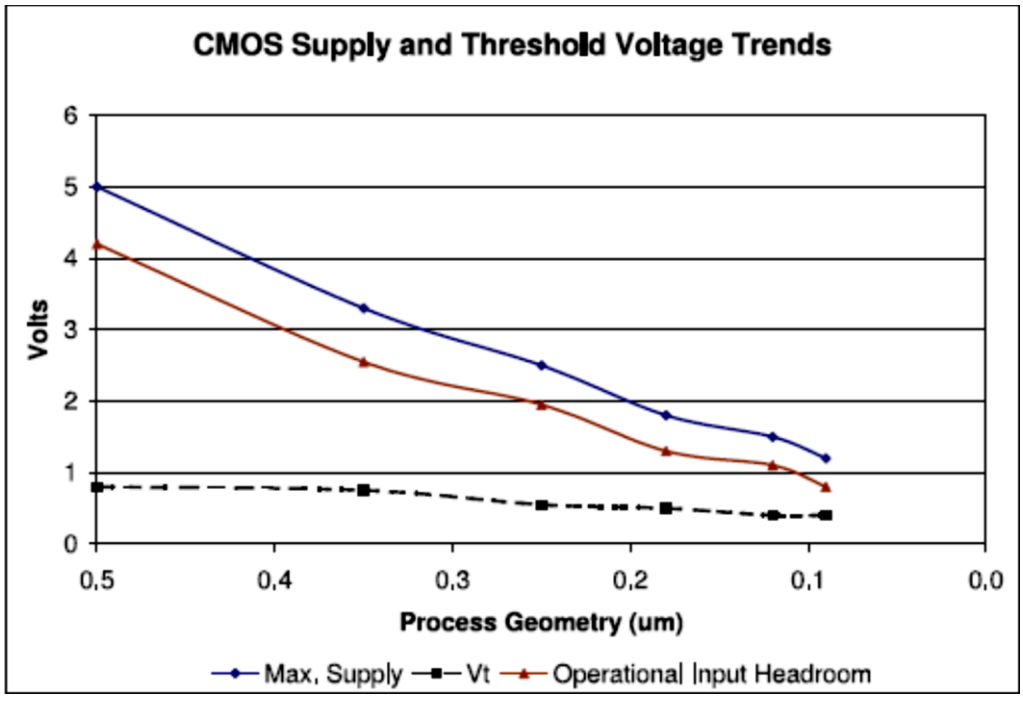


Fig 1.1: Operating voltage trend in CMOS technology [4]

Operational amplifiers with moderate DC gains, high output swings and reasonable open loop gain bandwidth product (*GBW*) are usually implemented with two-stage structures. In CMOS technology the open loop gain of op amps is lower compared to bipolar counterpart due to the inherently lower transconductance of CMOS devices as well as the gain reduction due to short channel effects that come into play for submicron CMOS processes. As a result gain enhancing methods often required to improve the gain. These methods however require more complicated circuit structures and higher power supply voltage, and may produce a limited output voltage swing [5]. To achieve high gain, a conventional cascode amplifier, which increases the gain by stacking up transistors but it is not suitable in low voltage design as the cascode structure results in small voltage swings.

Instead of this a multistage amplifier is widely used to boost the gain by increasing the number of gain stages horizontally. However, all multistage amplifiers suffer from the closed-loop stability problem due to the presence of multiple poles. Different frequency-compensation topologies for multistage amplifiers have been used in different circuits. There is a basic well-known technique for compensating multistage amplifiers known as Nested-Miller Compensation. But this technique suffers from reduced bandwidth when there is increase in gain stages. Some other techniques also have been used recently with some modification to the NMC (Nested-Miller Compensation). However, as all published compensation topologies uses passive capacitive-feedback networks, the bandwidth of the amplifier is still limited for high-speed applications in low-power condition. In the recent time however, some more techniques has been proposed which offers reduction of the compensation capacitor value effectively which results in greatly reduced physical dimension and finally both the bandwidth and transient responses are highly improved.

1.2 Motivation

The design of complex systems with analog, digital, and switched-capacitor building blocks integrated on one chip greatly suffers from large signal variations on the power supply lines. The use and development of high performance amplifiers are necessary especially in those cases where low-level signals have to be measured. For this

reason the performance of such amplifiers must be studied carefully and analyzed accordingly.

There are numerous electrical characteristics on which performance of Operational Amplifier depends, e.g., gain-bandwidth, slew rate, common-mode range, output swing, offset, power consumption etc. We often used two stage operational amplifiers to achieve both high dc gain and large output voltage swing. These op amps require frequency compensation. Our aim is to create the physical design and simulate a high gain -low power Op-amp. There are various methods to achieve trade-offs between gain, power, speed, output swing, slew rate, area etc.

The evolution of low power microelectronics began with the invention of transistor in the late 1940's and next came the invention of the integrated circuit in the late 1950's. Historically, the most demanding applications of low power microelectronics have been battery operated products. However, in early 1990's low power microelectronics rapidly evolved as a mainstream of microelectronics. The increasing packaging density of the transistor and increasing clock frequencies of CMOS microchips were considered as the principal reasons for this transformation. The motivation for the low power electronics has stemmed from three reasonably distinct classes of need:

(1) Among these earliest and the most demanding is the portable battery operated equipment that is sufficiently small in size and weight and long in operating life to satisfy user.
(2) The most recent need is for ever increasing packing density in order to further enhance the speed of high performance systems which imposes severe restrictions on power dissipation density.
(3) The broadest need is for conservation of power.

An ideal op-amp having a single ended output is characterized by a differential input, infinite voltage gain, infinite input resistance and zero output resistance. In a real op-amp however these characters cannot be generated but their performance has to be sufficiently good for the circuit behavior to closely approximate the characters of an ideal op-amp in most applications. With the introduction of each new generation of CMOS

technologies design of op-amps continues to pose further challenges as the supply voltages and transistor channel lengths scale down.

1.3 System Overview

This section briefly discusses the basic concept of op-amp. An amplifier with the general characteristics of very high voltage gain, very high input resistance, and very low output resistance generally is referred to as an op-amp. Most analog applications use an Op-Amp that has some amount of negative feedback. The Negative feedback is used to tell the Op-Amp how much to amplify a signal. And since op-amps are so extensively used to implement a feedback system, the required precision of the closed loop circuit determines the open loop gain of the system.[6]

A basic op-amp consists of 4 main blocks:
(a) Current Mirror.
(b) Differential Amplifier.
(c) Level shift, differential to single ended gain stage.
(d) Output buffer.

The general structure of op-amp is as shown in figure 1.2 below:

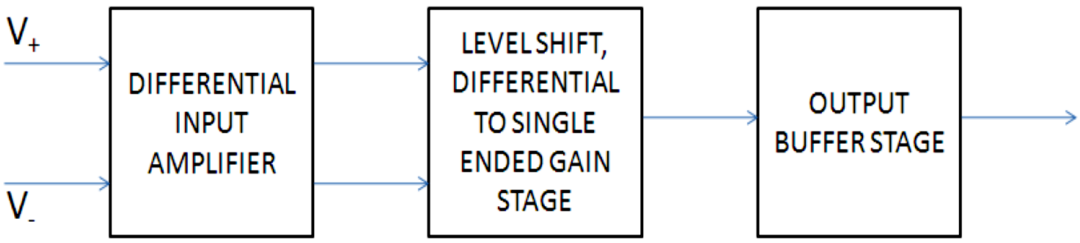


Fig 1.2: General Structure of op-amp

The first block is input differential amplifier, which is designed so that it provides very high input impedance, a large CMRR and PSRR, a low offset voltage, low noise and high gain. The second stage performs Level shifting, added gain and differential to single ended converter. The third block is the output buffer. The output buffer may sometimes

be omitted to form a high output resistance un-buffered op-amp often referred to as Operational transconductance amplifier or an OTA. Those which have the final output buffer stage have a low output resistance (Voltage operational amplifiers).[7-8]

1.4 Applications

There are various applications for which high gain low power op amp with flexible noise performance can be used. Low noise and low power op amp is used in applications like medical field, Active Filters and Signal Processing, sensors applications, battery operated devices, etc. Low power op-amp can be used as bio-potential amplifier. The essential and important role of a bio-potential amplifier is to amplify and filter the extremely weak bio-potential signals. However, the design of this amplifier is not straight forward. Bio-potential amplifiers must be able to cope with various challenges in order to extract the bio-potential signals. Meanwhile, for long-term power autonomy the power dissipation of the amplifier must be minimized. The challenges of designing a bio-potential amplifier for portable bio-potential acquisition systems are Ultra-low power dissipation for long-term power autonomy, high gain and filter characteristics that suit the needs of various applications.

1.5 Thesis Organization

The overall designed thesis is divided into seven chapters and its outline is described as given below:

Chapter 1: Introduction

Brief overview of issues related to modern CMOS technology, necessity of frequency compensation, motivation of the project, applications of op-amp and outline of the thesis is discussed.

Chapter 2: Literature Review

This chapter starts with the description of MOSFET operation thereafter operational amplifier overview and stability consideration for op-amp is stated.

Chapter 3: Operational Amplifier Compensation

This chapter describes the various frequency compensation techniques used in op amp designing along with their advantages and disadvantages.

Chapter 4: Operational Amplifier Design Methodology

This chapter discusses the various methodologies to design the operational amplifier, the equations followed to implement the design, parameters extraction, the comparable study of RC, voltage buffer and current buffer compensation with advantage/disadvantage of current buffer over the others.

Chapter 5: Proposed 2-Stage Operational Amplifier

Under this chapter schematic of final circuit is designed by selecting suitable topology for low power and high gain, composite cascode technique is implemented in each stage, in current mirror and also in current buffer.

Chapter 6: Simulation Results

This chapter contains various simulations results of the final circuit and compares obtained result with results of previously reported op-amp circuits.

Chapter 7: Conclusion and Future Research

This chapter summarizes the major accomplishments of this thesis and presents the scope for future and further research.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

With the growing technology the increasing demand for low power mixed signal integrated circuits for portable or non-portable high performance systems, analog circuit challenges the designers with making analog circuit blocks with lower power consumption with little or no performance degradation. CMOS op amps are ideally suited for low power application. The classic Widlar op amp architecture, mainly developed for bipolar junction transistors (BJT), has required modification for use with CMOS devices. It has proved to be difficult to match the open loop gain of bipolar op amps with CMOS technology [9, 10]. This is basically due to the inherently lower transconductance of CMOS devices.

As a result, multiple stage amplifiers with gain stages of more than three may be used for higher gain analog circuit designs. Nevertheless, multistage amplifiers generally are difficult to compensate. To reduce the power consumption of op-amp circuits one way is by scaling down the power supply voltage which results in a reduced input common mode range and output swing. Since the threshold voltage of MOSFET does not scale down at the same rate as the reduction of the minimum transistor length with the advance of technologies as shown in fig 2.1. V_{GS} is the gate-to-source voltage and V_T is the nominal threshold voltage.

With the decreased threshold voltage the static power dissipation is also increased. Scaling does not benefit analog circuits as much as it does digital circuits since the minimum size transistors are not usually selected in analog circuits because of noise and offset voltage constraints. One important design aspect is the operation region of transistors. When the MOSFET works in strong inversion results in highest power consumption. While power consumption is much lower if the MOSFET works in weak inversion or subthreshold region due to the low quiescent drain current.

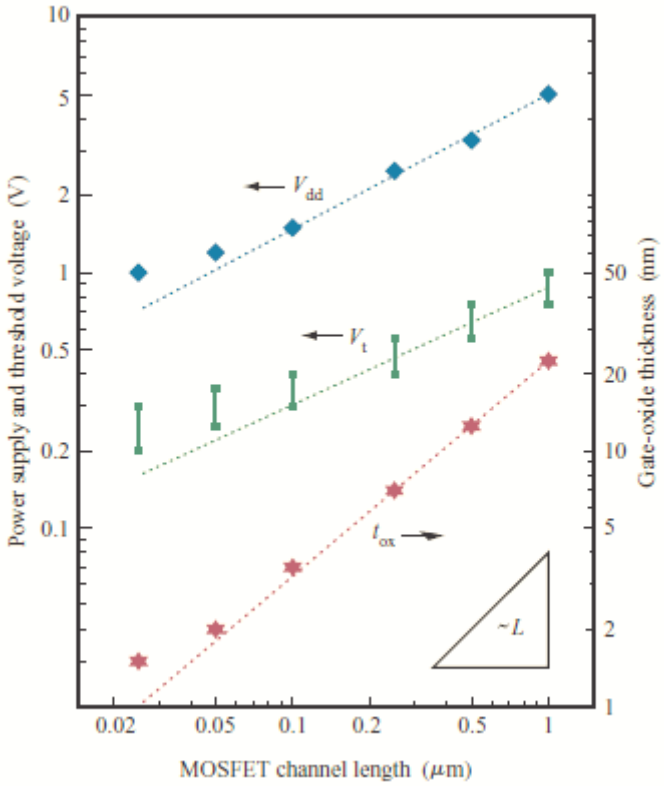


Fig 2.1: Power-supply (V_{dd}), threshold voltage (V_t), and gate-oxide thickness (t_{ox}) vs. channel length for CMOS

2.2 MOSFET Operation

MOSFETs in amplifier stages usually work in their active (saturation) regions. There are basically three main operation regions of an MOS transistor within the active region namely the strong inversion region, the moderate inversion region, and the weak inversion region. When an n-type MOSFET is biased with voltages, three different situations may happen at the semiconductor surface. Assume that the source is tied to the p substrate at the zero voltage ground level, and then a negative voltage V_G applied to the gate will bring excess positive carriers (holes) to the interface and give rise to an accumulation of holes. This phase is called the accumulation. When a small positive voltage V_G is applied to the gate, the majority carriers (holes) near the semiconductor surface are repulsed and leave negative ions behind. This is called the depletion case as there are no free carriers available to cause the current flow. As V_G gets larger, the positive gate voltage starts to attract minority carriers (electrons) in the p substrate to the gate surface area. The gate voltage required for the electron concentration under the gate

to be equal to the majority carrier (hole) concentration in the p substrate is usually called the threshold voltage V_T. V_G gradually increases, when the electron concentration at the surface is larger than the intrinsic carrier concentration while the hole concentration is less than the intrinsic carrier concentration, the minority carrier (electrons) becomes majority at the surface and the channel beneath the gate is inverted to n region. This is called the inversion case. At first, the surface is in a state of weak inversion region due to the small electron concentration. As gate voltage V_G is increased, the moderate inversion region and strong inversion region are reached.

The operation region of a MOS device as a function of $V_{eff} = V_{GS} - V_T$ is shown in fig. 2.2. V_{GS} is the gate-to-source voltage and V_T is the nominal threshold voltage.

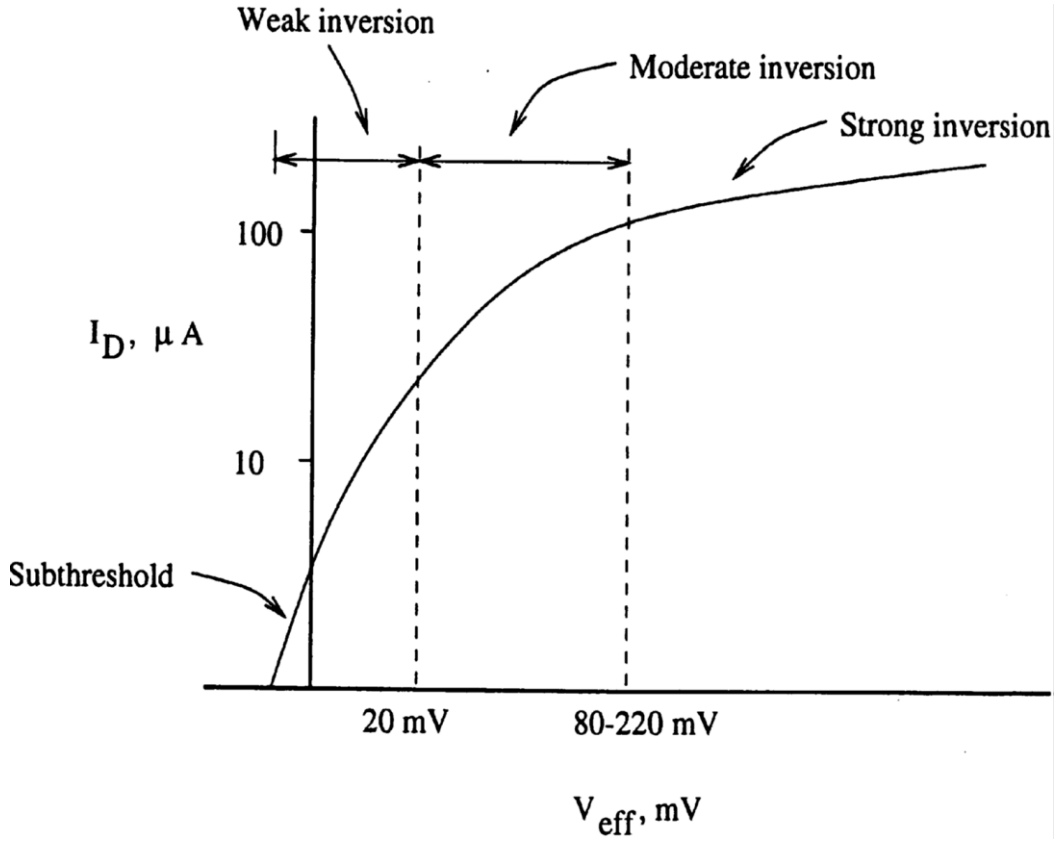


Fig 2.2 Operating regions of a MOS device

2.2.1 Strong Inversion Region

The most frequently used region among the three regions is the strong inversion region. In the strong inversion region, the commonly used drain current I_D with V_{GS} variation is represented by the square law equation

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \quad (2.1)$$

In this expression,

μ - Surface mobility of the channel,

Cox - Capacitance per unit area of the gate oxide,

W - Effective channel width,

L - Effective channel length,

λ is the channel length modulation factor, and V_{DS} is the resulting drain-to-source voltage.

The transconductance in the strong inversion region is

$$g_m = \frac{\partial i_D}{\partial v_{GS}} = \sqrt{2\mu C_{ox}(W/L)I_D}. \quad (2.2)$$

The incremental drain-to-source resistance is

$$r_{ds} = \frac{1}{\lambda I_{DP}}. \quad (2.3)$$

Where I_{DP} is the drain pinch-off current and is often approximated by I_D. The voltage gain A_O of the single stage CMOS amplifier illustrated in Fig. 4.3 is given by

$$A_0 = -g_m r_{ds}. \quad (2.4)$$

In the strong inversion region, the gain varies with I_D as

$$A_0 = \frac{-K_1}{\sqrt{I_D}}. \quad (2.5)$$

This means that the gain is inversely proportional to the square root of the drain current. Lower current actually produces higher gain for strong inversion devices.

2.2.2 Moderate Inversion Region

As shown in fig. 2.2, the MOS device starts operating in the moderate inversion region when V_{eff} varies from a value of about 20 mV to approximately 220 mV [2]. Drift and diffusion currents in this region, are similar. When the drift current dominates the diffusion current increased gate-to-source voltage results in the strong inversion region and on the other hand decreased gate-to-source voltage leads to the weak inversion region when diffusion current starts to dominates the drift current. There is no exact quantitative expression of the relationship between the current and V_{GS} in the moderate inversion region.

2.2.3 Weak inversion region

In the weak inversion region the lower end is the subthreshold region where VGS is less than V_T. As V_{eff} ranges from subthreshold values up to about 20 mV, the device is in the weak inversion region. Weak inversion and subthreshold can be used interchangeably. In the subthreshold region, the drain current decreases but remains finite as V_{GS} drops several tenths of a volt below V_T. The drain current decreases exponentially with V_{GS}. Subthreshold operation of the MOSFET can be used in low-voltage, low-power applications. The subthreshold state is dominated by diffusion current instead of drift current as in the case of strong inversion. The drain current as a function of the gate-to-source voltage is

$$I_D = \frac{W}{L} I_{D0} e^{qV_{GS}/nkT} (1 - e^{-qV_{DS}/kT}) \tag{2.6}$$

where ‘n’ is the subthreshold slope factor, ‘I_{D0}’ is a process-dependent parameter that is dependent also on source-to-bulk voltage and threshold voltage, ‘k’ is Boltzmann’s constant, ‘T’ is the absolute temperature, and ‘q’ is electronic charge. The subthreshold current is independent of the drain-to-source voltage once ‘V_{DS}’ is higher than a few times the thermal voltage kT/q. The transconductance can be found from Eq. (2.6) and Eq. (2.2) as

$$g_m = \frac{W}{L} I_{D0} \frac{q}{nkT} e^{qV_{GS}/nkT} (1 - e^{-qV_{DS}/kT}) = \frac{q}{nkT} I_D. \quad (2.7)$$

It is clear that the transconductance is linear with the drain current in the weak inversion region. The incremental drain-to-source resistance is related to the early voltage V_A by

$$r_{ds} = \frac{V_A}{I_D}. \quad (2.8)$$

While V_A is approximately constant through the weak inversion region for a given channel length, the mid-band gain in the weak inversion region approaches a constant value or

$$A_0 = -g_m r_{ds} = -\frac{q}{nkT} V_A. \quad (2.9)$$

The relatively constant gain in the subthreshold region results in less signal distortion than those in the moderate and strong inversion regions as reported in [10]. The weakly inverted MOSFET is very attractive for low power designs.

2.3 Operational Amplifier Overview

2.3.1 Introduction

An operational amplifier is often called an op-amp. It is a DC-coupled differential input voltage amplifier with a rather high gain. By high we mean a value that is adequate for the application, typically in the range of 10^1 to 10^5. In most general purpose op-amps there is a single ended output. For most general applications of an op-amp a negative feedback is used to control the large voltage gain. The negative feedback also largely determines the magnitude of its output ("closed- loop") voltage gain in numerous amplifier applications, or the transfer function required. The op-amp acts as a comparator when used without negative feedback, and even in certain applications with positive feedback for regeneration. In this chapter ideal op amp and its parameters values, basic op amp structure and its parameters such as gain bandwidth product, common mode rejection ratio, power supply rejection ratio etc are discussed.

2.3.2 Operational Amplifier

The general operational amplifier symbol is as shown in fig 2.3 below:-

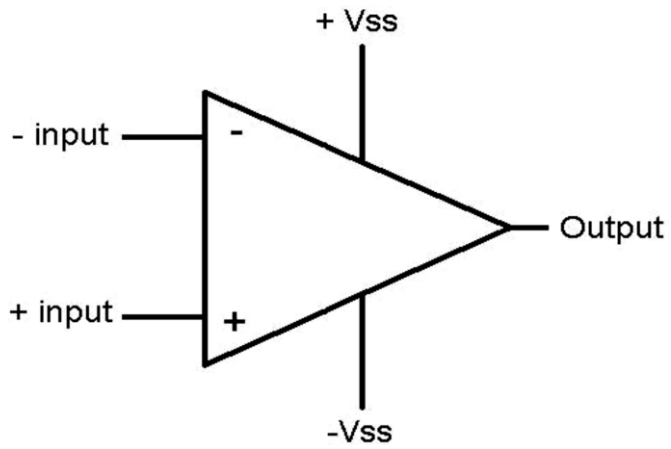


Fig 2.3: General operational amplifier

An ideal Operational Amplifier is a 3-terminal linear device. It consists of two input terminals with very high impedance. The Operational Amplifier output signal is the difference of the two input signals being applied at the high impedance terminals magnified by a constant gain.

Therefore there is almost always a differential signal for an ideal op-amp the input signal and hence a differential amplifier is generally used as the input stage of an Operational Amplifier. The op-amp block diagram shows a common op-amp symbol with two inputs marked by + and – and an output. The terminals for the supply voltages are $+V_{SS}$ and $-V_{SS}$ terminal. In general the op-amp is used with dual power supplies. To drag down the source potential of the NMOS transistors used in the design to a negative potential the V_{SS} terminal is made negative. This ensures the designer that the op-amp can be used for wider range of differential inputs. All transistors of op-amp are supposed to function in saturation for ideal operation of the op-amp circuit. The negative power supply at V_{SS} ensures one of the inputs is grounded even if the differential pair action as the input stage of the op-amp is in saturation. The output voltage, V_{out} of the amplifier is given by the difference between the two input signals applied to the differential amplifier multiplied by some constant gain determined by the specifications of the designed system.

For designing an ideal op-amp many considerations are made. One of those considerations involves the use of perfectly matched transistors for the input differential pair as well as at the load of the differential pair. The use of current mirrors in the op-amp circuit also creates the need for generation of matched transistors.

Ideal Operational Amplifiers have in generally one output (although there are op-amps with differential outputs as well as many applications have need for them) of low impedance which is mostly referenced to a common ground terminal. In an ideal case the output of the op-amp any common mode signals in the input should be ignored, i.e., if signals of identical dimensions are applied to both the inputs the output should be zero ideally. However, in practical amplifiers the output always varies slightly for the common mode input and this change of the output voltage with respect to variations in the common mode input voltage is measured for an op-amp by virtue of its Common Mode Rejection Ratio or CMRR**.**

Most Operational Amplifiers have a characteristic such as high open loop DC gain. We often easily construct an operational amplifier circuit by the application of negative feedback in some form often that has a very accurate gain characteristic which depends solely on the feedback used in the circuit. An operational amplifier output is independent of any common potential applied across both of its high impedance input terminals and the output depends only on the difference between the voltages. If both input terminals of an op-amp are at same potential the resultant output for an ideal op-amp will be zero. The gain of the Operational Amplifiers is commonly referred to as the Open Loop Differential Gain, and is denoted by the symbol (A_O).

Ideal Op-Amp basics & its parameters--

The Thevenin amplifier model is shown in fig. 2.4 below, showing standard op amp notation. It amplifies the voltage difference, $V_d = (V_p - V_n)$, on the input port and produces a voltage, V_O, on the output port that is referenced to ground.

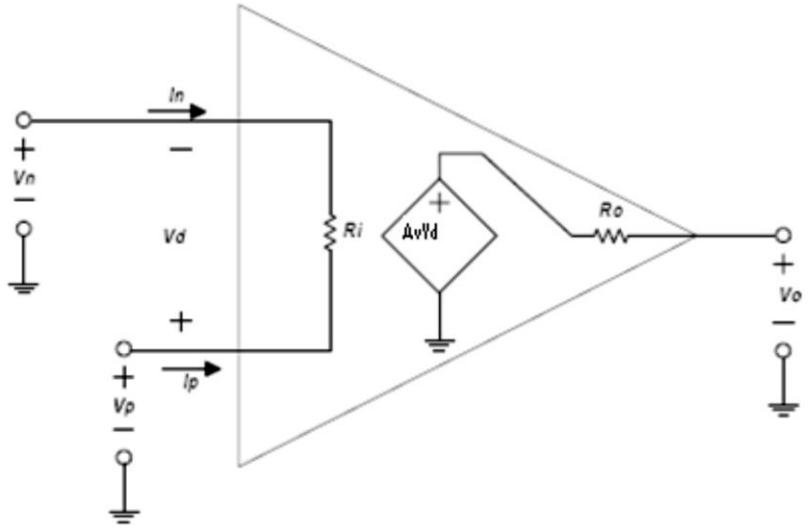


Fig 2.4 Thevenin amplifier model

The ideal op amp model was derived to simplify circuit calculations and is commonly used by engineers in first order approximation calculations. The ideal model makes three simplifying assumptions:

- Gain Av = ∞
- Input Resistance Ri = ∞
- Output Resistance Ro = 0

Applying these assumptions to fig. 2.4 results in the ideal op amp model shown in fig. 2.5

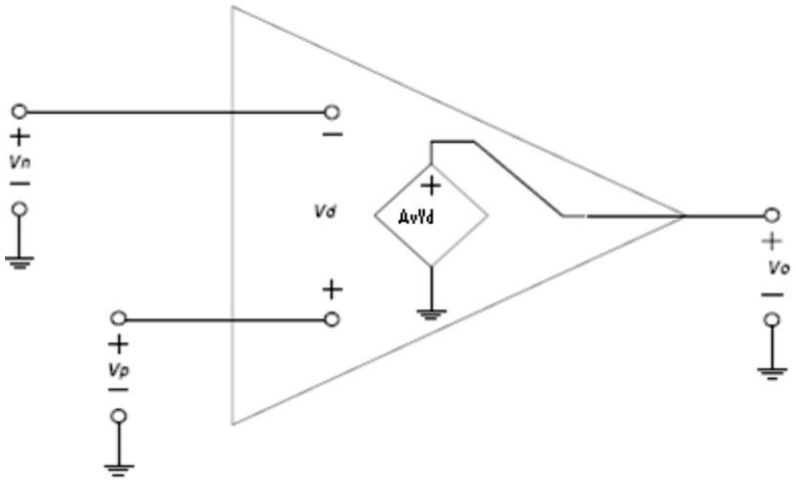


Fig 2.5: Ideal op-amp model

Other simplifications can be derived using the ideal op amp model.

$$I_n = I_p = 0 \quad (2.10)$$

Because $R_i = \infty$ we assume $I_n = I_p = 0$. There is no loading effect at the input.

$$V_O = A_v \times V_d \quad (2.11)$$

Because $R_O = 0$ there is no loading effect at the output.

$$V_d = 0 \quad (2.12)$$

If the op amp is in linear operation, V_O must be a finite voltage. By definition $V_O = A_v \times V_d$. On rearranging, $V_d = V_O/A_v$. Since Av = ∞, $V_d = V_O/\infty$. This is the basis of the virtual ground concept.

- Common mode gain = 0

The ideal voltage source driving the output port depends only on the voltage difference across its input port. It rejects any voltage common to V_n and V_p.

- Bandwidth = ∞
- Offset Voltage = 0
- Slew Rate = ∞

No frequency dependencies are assumed.

- Drift = 0

In performance over time, temperature, humidity, power supply variations, etc there are no changes.

So for an ideal op-amp no current flows in either of the input terminal. This is called the current rule. The differential input offset voltage is also zero. This is the voltage rule. As they predict and help us understand the workings of the amplifier these two properties should be noted carefully and in turn aid the analysis and design of operational amplifier circuits.

However, the infinite gain or bandwidth that characterizes an ideal operational amplifier is seldom found in a real Operational Amplifiers. This output gain is not however frequency independent and is found to gradually decreases at higher frequencies till it reaches "Unity Gain". This is also shown in following fig. 2.6.

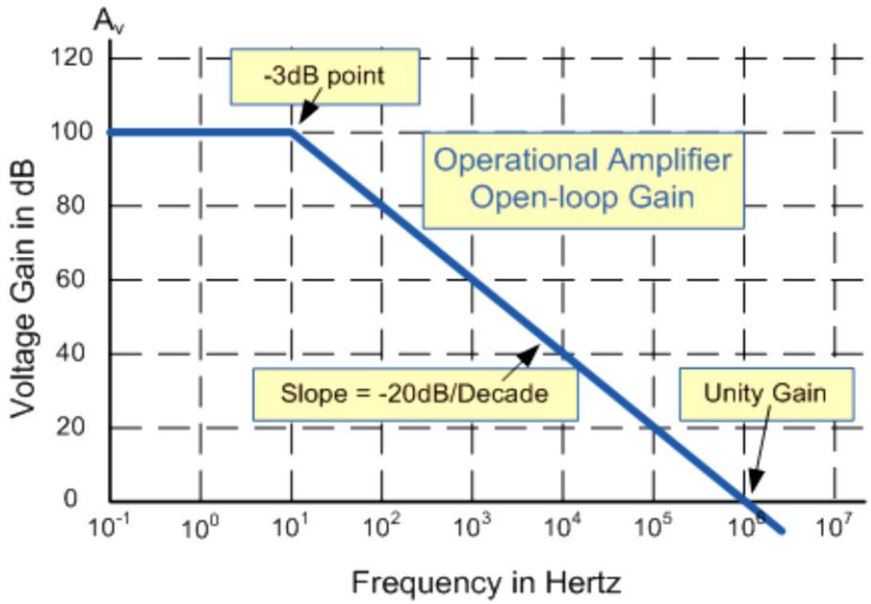


Fig 2.6: Open loop frequency curve

The product of gain against frequency for an op-amp is a constant at any point in the frequency response curve of the op-amp. The open loops frequency response curve shown above shows that. The unity gain frequency, i.e. the frequency at which the curve cuts the frequency axis (gain magnitude = 0 dB) also can be used to predict the amplifier gain at any point along the curve. This constant is referred to as the Gain Bandwidth Product or GBP.

The GBP of an op-amp is given by,

GBP = Gain of Amplifier x Bandwidth

The bandwidth of an operational amplifiers is defined as the frequency range over which the amplifier voltage gain is greater than 70.7% or -3dB (where we consider the maximum gain to be the reference or 0dB) of the maximum output value attained by the gain of the amplifier.

2.3.3 Operational Amplifier Performance Parameters

Open loop gain, Av: Operational amplifiers are mainly used to amplify the input signal and the higher its open loop gain the better it will perform as in many applications they are used with a feedback loop. The required gain can be adjusted according to the

application. Trading with the parameters such as speed and output voltage swings, the minimum required gain must therefore be known. To suppress nonlinearity a high open loop gain is also necessary.

A_V is the ratio of the peak-to-peak output voltage swing to the change in input voltage required to drive the output.

$$A_v = \frac{V_{o(p-p)}}{V_{in}} \tag{2.13}$$

Differential voltage Amplification, A_{VD}: The ratio of the change in the output to the change in differential input voltage producing it with the common-mode input voltage held constant.

$$A_{vd} = \left.\frac{\Delta V_o}{\Delta V_{in}}\right|_{Vincm,const} \tag{2.14}$$

Unity gain bandwidth, UGB: The range of frequencies within which the open-loop voltage amplification is greater that unity. U_{GB} is shown in fig. 2.7.

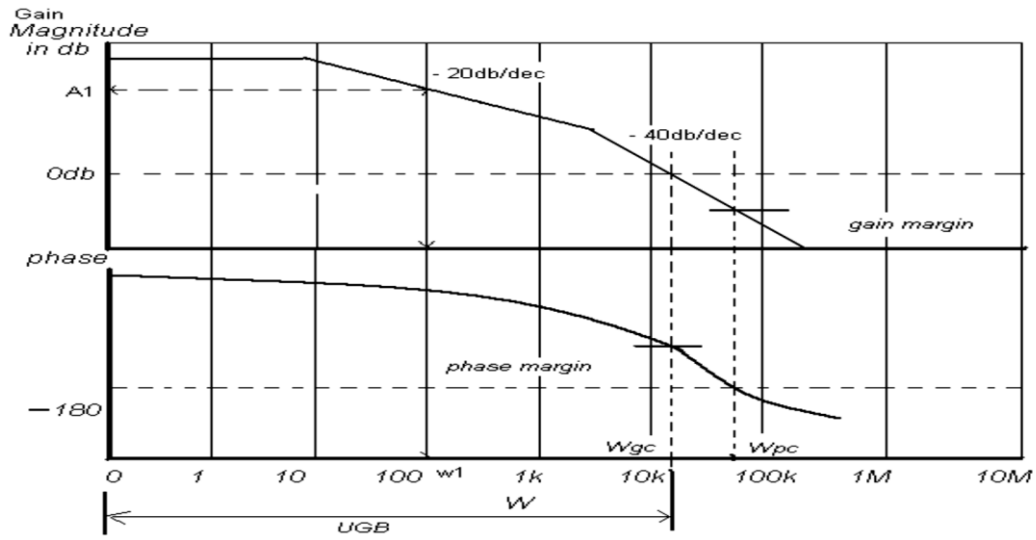


Fig 2.7: Showing unity gain bandwidth (UGB), gain margin (GM), phase margin (PM)

Gain bandwidth product, GBW: The product of the open-loop voltage amplification and the frequency at which it is measured. From fig. 2.7, Gain bandwidth product is

$$GBW = A_1 \times \omega_1 \tag{2.15}$$

Maximum-output swing Bandwidth, BOM: The range of frequencies within which the maximum output voltage swing is above a specified value.

Common-mode rejection ratio, CMRR: The common-mode input voltage is defined by Vin,c = (Va + Vb)/2 as contrasted with the differential-mode input voltage Vin,d = (Va – Vb). The differential gain A_D and also the common-mode gain A_C, where Ac = V_0/ Vin,c.

The CMRR is now defined as the ratio of differential voltage amplification to common-mode voltage amplification.

$$\text{CMRR} = \frac{A_D}{A_C} \tag{2.16}$$

In logarithmic value CMRR = 20 $\log_{10}\frac{A_D}{A_C}$ in dB.

Typical CMRR values for MOS amplifiers are in the 60-80 dB range. As the frequency increases CMRR falls off. Also the measurement of how much the op-amp can suppress common-mode signals at its inputs is done by CMRR. The normal representation of undesirable noise, and hence a large CMRR is an important requirement.

Supply voltage rejection ratio, SVRR*:* The absolute value of the ratio of the change in supply voltages to the change in input offset voltage.

$$SVRR = \Delta V_{Cc} \pm / \Delta V_{os} \tag{2.17}$$

Slew rate, SR: For a large input step voltage, some transistors in the op-amp may be driven out of their saturation regions or completely cut-off. As a result the output will follow the input at a slower finite rate. The maximum rate of change V_0 is called slew rate. It is not directly related to the frequency response. For typical MOS op-amps slew-rates of 1~20 V/μs can be obtained.

$$SR = dv/dt \tag{2.18}$$

In op amps we trade power consumption for noise and speed. The bias currents within the op amp are increased to increase slew rate.

Gain margin, GM: The reciprocal of the open-loop voltage amplification at the lowest frequency at which the open-loop phase shift is such that the output is in phase with the inverting input.

Phase margin, PM: The absolute value of the open-loop phase shift between the output and the inverting input at the frequency at which the modulus of the open-loop amplification is unity. Gain and phase margins are measures of stability for a feedback system, though often times only phase margin is used rather than both. Based on the magnitude response of the loop gain, |Av|, gain margin is the difference between unity and $|A_V (\omega_{180}{}^0)|$ where $\omega_{180}°$ is the frequency at which the loop gain phase, is -180°, called as Phase crossover frequency. Phase margin is the phase difference between phase of Av (ω_{0dB}) and -180° where ω_{0dB} is the frequency at which |Av| is unity, called unity gain frequency. Gain and phase margins are illustrated in fig. 2.7.

Common-mode input voltage range, V_{ICR}: The range of common-mode input voltage that if exceeded may cause the operational amplifier to cease functioning properly.

Maximum peak output voltage swing, V_{OM}: The maximum positive or negative voltage that can be obtained without waveform clipping when quiescent dc output voltage is zero.

Maximum peak-to-peak output voltage swing, V_O(PP): The maximum peak-to-peak voltage that can be obtained without waveform clipping when quiescent dc output voltage is zero.

Equivalent input noise voltage, Vn: The MOS transistor generates noise, which can be described in terms of an equivalent current source in parallel with the channel of the device. The voltage of an ideal voltage source (having internal impedance equal to zero) in series with the input terminals of the device that represents the part of the internally generated noise that can properly be represented by a voltage source.

Equivalent input noise current, In: The current of an ideal current source (having internal impedance equal to infinity) in parallel with the input terminals of the device that represents the part of the internally generated noise that can properly be represented by a current source.

All op amps have associated parasitic noise sources. Noise is measured at the output of an op amp and referenced back to the input; thus, it is called equivalent input

noise. The spectral density of noise in op amps has a 1/f and a white noise component. 1/f noise is inversely proportional to frequency and may dominate the devices noise at frequencies well into the megahertz range [12]. White noise is spectrally flat.

Average noise figure, F: The ratio of the total output noise power within a designated output frequency band when the noise temperature of the input termination(s) is at the reference noise temperature at all frequencies to that part of caused by the noise temperature of the designated signal input termination within a designated signal-input frequency.

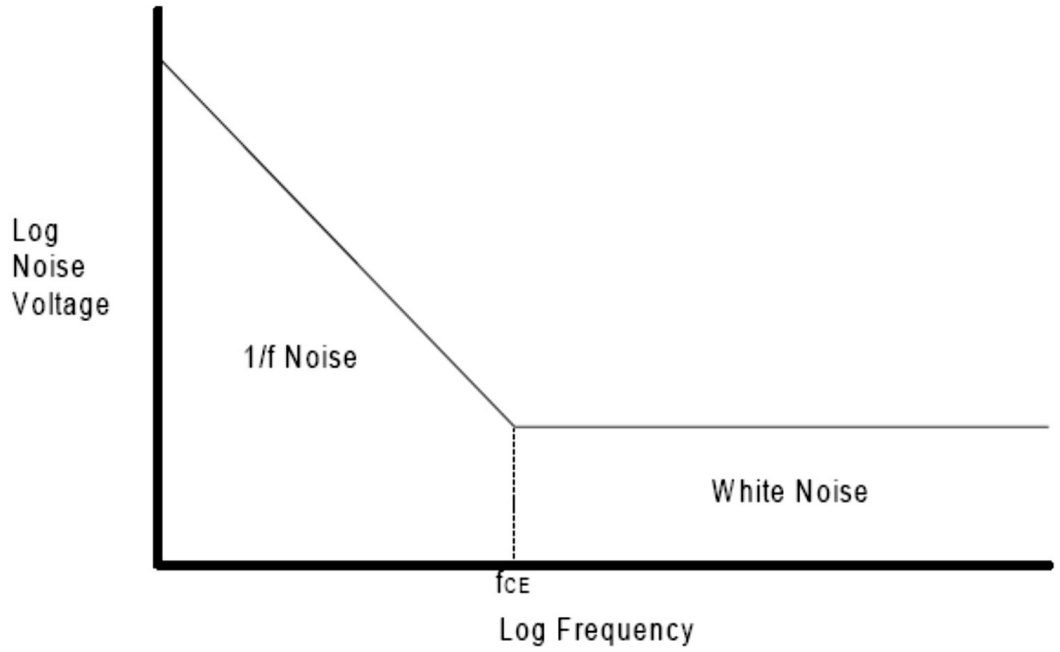


Fig 2.8: Typical op amp input noise spectrum

Input resistance, (Rin): The Input resistance of an op-amp for an ideal device has to be infinite to prevent any current flowing from the source supply into the amplifiers input circuitry. The resistance between the input terminals with either input grounded.

Differential input resistance, Rid: The small-signal resistance between two ungrounded input terminals, fig. 2.9.

Output resistance, Ro: The resistance between an output terminal and ground. For a real MOS op-amp, the open loop output impedance is nonzero. It is usually resistive, and is of the order of 0.1-5KΩ for op-amps with an output buffer, it can be much higher (~1MΩ) for op-amps with un-buffered output. This affects the speed with which the op-amp can charge a capacitor connected to its output and hence the highest signal frequency.

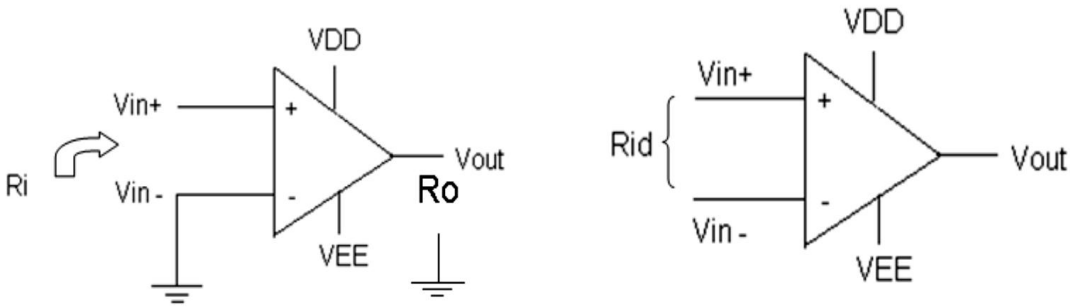


Fig 2.9: Showing Ri, Rid and Ro.

Input offset voltage, Vio: The amplifiers output is supposed to be completely independent of common potentials applied to both inputs. The amplifiers output is supposed to be zero when the voltage difference between the inverting and non-inverting inputs is zero. But in real devices, this is not exactly true, and a voltage $V_{0,off} \neq 0$ will occur at the output for shorted inputs. This is the dc voltage that must be applied between the input terminals to force the quiescent dc output voltage to zero or other level, if specified.

Input offset current, I_{IO}: The difference between the currents into the two input terminals with the output at the specified level.

Input bias current, I_B: The average of the currents into the two input terminals with the output at the specified level.

$$\left.\begin{aligned} I_B &= (I_{b+} + I_{b-})/2 \\ I_{io} &= I_{b+} - I_{b-} \end{aligned}\right\} \qquad (2.19)$$

2.4 Stability Consideration

In general, operational amplifiers are amplifiers with an open loop gain high enough to ensure the closed loop transfer characteristic with negative feedback is approximately independent of the op amp gain. An adequately high gain is the key requirement of an op amp to utilize the negative feedback configuration. As the negative feedback is used widely in application in processing of analog signal, feedback system, however, suffer from potential instability, i.e. they may oscillate.

2.4.1 Feedback Circuit Theory

Fig. 2.10 shows a general negative feedback system, where A is the forward gain network and F is the feedback network from the output back to the input terminal. The feedback signal $V_f(s)$, which is equal to $F(s)V_O(s)$, is subtracted from the source signal $V_i(s)$ to generate the feedback error signal $V_e(s)$, which is the input to A. That is

$$V_e(s) = V_i(s) - F(s)V_O(s) \tag{2.20}$$

Thus,

$$Vo(s) = A(s)(V_i(s) - F(s)V_O(s)) \tag{2.21}$$

And

$$G(s) \equiv \frac{V_o(s)}{V_i(s)} = \frac{A(s)}{1 + A(s)F(s)}. \tag{2.22}$$

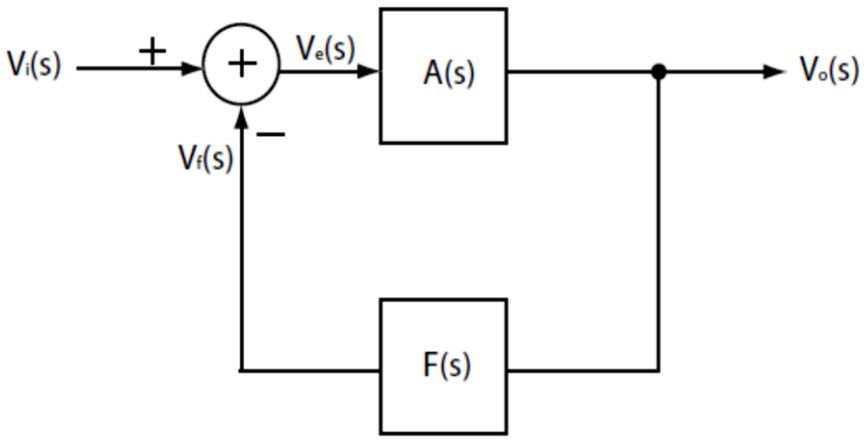


Fig 2.10: General negative feedback system

The quantity A(s)F(s) is called the loop gain and is equivalent to the transmission around the feedback loop. As represented by the configuration of a feedback amplifier in fig. 2.10, A(s) is usually the open loop transfer function and G(s) is the closed loop transfer function. If the loop gain is very high, G(s) is mainly controlled by the feedback network F(s) since $G(s) \approx 1/F(s)$ when $A(s)F(s) >> 1$.

The negative feedback decreases the gain, but it provides a few other benefits such as gain desensitivity, bandwidth extension, impedance modification, and nonlinearity reduction.

Feedback also changes the circuit input and output terminal impedances. With voltage or current quantities as output signals, the feedback networks used to sense the output signal are defined as voltage (shunt) or current (series) connections at the output respectively. With voltage or current quantities provided at the summing terminal, the connections are defined as voltage (series) or current (shunt) types at the input. The voltage (shunt) feedback at the output decreases the output impedance while the current (series) feedback at the output enhances the output impedance. On the other hand, the input impedance to the voltage (series) feedback amplifier is raised while the current (shunt) feedback at the input decreases the input impedance. In conclusion, series feedback increases the impedance while shunt feedback decreases the impedance for both the input and output terminals. Different feedback circuits could be chosen if higher or lower impedance is desired.

Another important effect of a negative feedback system is the reduction of the nonlinearity in analog circuits. There is always nonlinear distortion of the circuits because of the nonlinear amplifying devices. When the nonlinearity is small, the input-output transfer curve is approximately linear. But for large signal swings, the output shows a distorted shape. The change of the small signal gain with the input dc level demonstrates the nonlinear property of the amplifier circuit.

As mentioned, nonlinearity can be regarded as the variation of the small signal gain with the input dc level. Negative feedback keeps the overall closed loop gain nearly constant and almost independent of the amplifier open loop gain. This means that negative feedback reduces distortion resulting from the change in the slope of the amplifier transfer curve. The second order harmonic typically causes more distortion than the other harmonics and it is one of the reasons that the input differential stage is popularly used in order to get rid of the even harmonics.

2.4.2 Stability

By the properties described in the preceding section Negative feedback has become popular and is widely in use. Nonetheless, the negative feedback on the

frequency response of a circuit may cause instability. The feedback circuit may oscillate. Let us consider the negative feedback system shown in fig. 2.11, the closed - loop transfer function as—

$$\frac{Y}{X}(s) = \frac{H(s)}{1 + \beta H(s)} \tag{2.23}$$

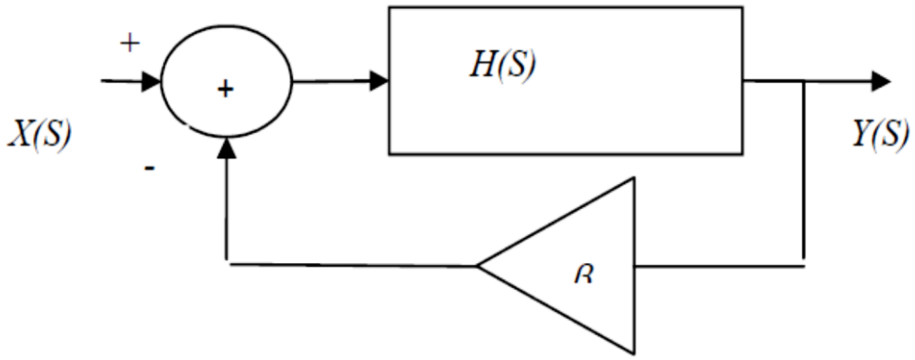


Fig 2.11: negative feedback system

If $\beta H(s = j\omega_1) = -1$, the gain goes to infinity. In this case, the system is not stable since any small noise will be amplified till the circuit starts to oscillate even without the presence of an input signal. This unstable condition called "Barkhausen's Criteria" is expressed as:

$$|\beta H(j\omega_1)| = 1$$

$$\angle \beta H(j\omega_1) = -180°, \tag{2.24}$$

Here β is assumed constant, less than or equal unity and independent of frequency. As negative feedback itself introduces 180° of phase shift, and the capacitance within amplifier's gain stages cause the output signal to lag behind the input signal by 90° for each pole they create. If the sum of these phase lags reaches 360° and gain is sufficient, the feedback signal will be add in phase to the original noise to allow oscillation buildup. The conditions can be summarize as excessive loop gain at frequency for which the phase shift reaches -180° or, excessive phase at frequency for which the loop gain drops to unity. We must have βH more positive than -180° for |βH| = 1 so as to avoid instability.

The most necessary and sufficient requirement to be considered for a feedback system to be stable is that all the poles of the overall closed loop transfer function have negative real parts. This condition that all the poles of the system are in the left half plane is demonstrated by the Laplace plane. It is very difficult to analyze the stability of a complex system from the closed loop poles since finding the zeros of the denominator $1+\beta A(s)$ of the overall transfer function is complicated. Since the poles of the open loop transfer function are usually known, it becomes more direct if we can predict the closed loop stability from the open loop frequency response.

It is a good quantitative way to express the degree of the stability of a feedback circuit by measuring the phase margin (PM) of the open loop gain response. As shown in fig. 2.12, the phase margin is specified as 180^0 plus the actual phase shift at the unity gain frequency ω_t where $|\beta A(j\omega_t)| = 1$. For no oscillation to occur the PM must be greater than 0^0. Gain margin (GM) is defined as the gain difference between the cross over frequency and the phase crossover frequency at which the phase reaches -180^0. The effective way in predicting the stability of a feedback circuit is by using both phase margin and gain margin. In the later sections, it is seen that the phase margin is one of the guidelines for designing and compensating operational amplifiers.

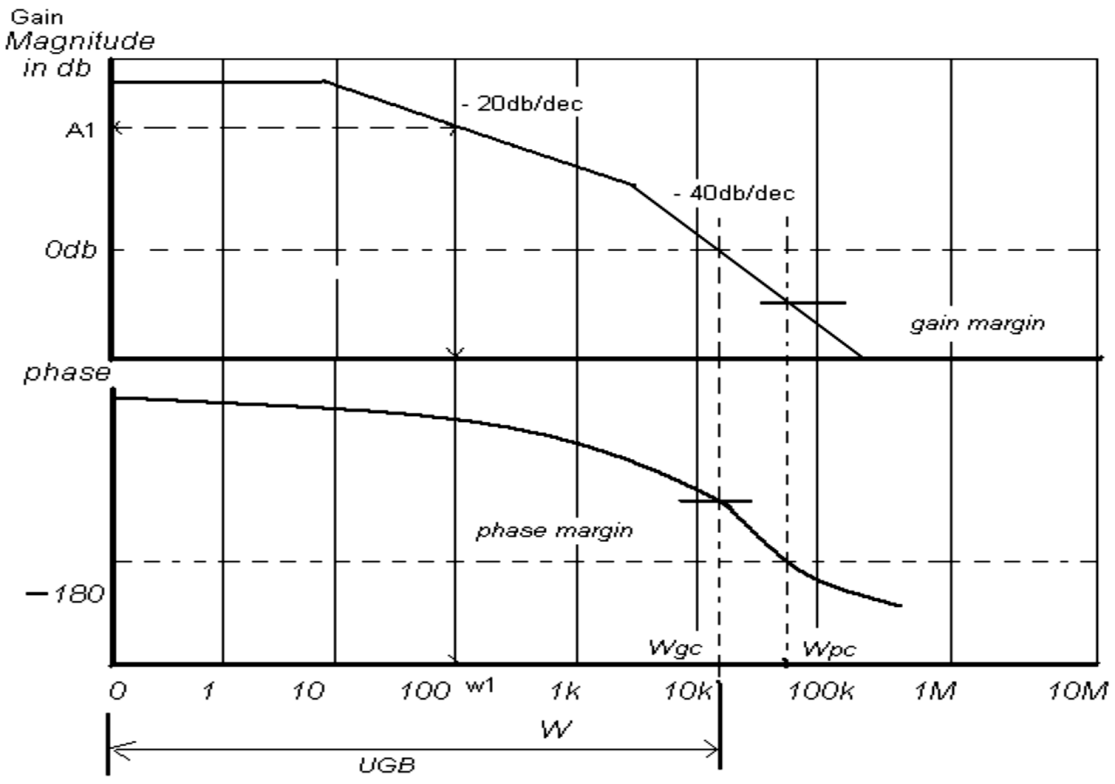


Fig 2.12: General frequency response of op-amp

In a stable system, the gain crossover point must have to occur well before the phase cross over point. If β is reduced (less feedback is applied), then the magnitude plots of fig. 2.12 are shifted down, there by moving the gain cross over closer to the origin and making the feedback system more stable. We often analyze the magnitude and phase plots for βH = H, for the worst case stability (β = 1).

Phase Margin

After designing each op-amp stage and connecting them together, the op amp usually has poor performance and unstable in the unity feedback configuration. The main merit of the stability is the phase margin, the phase shift at unity gain frequency i.e. | βH | must drop to unity before it crosses -180°.

The phase of βH at the gain crossover frequency can serve as a measure of stability, the smaller |βH| at this point, and the more stable the system will be.

Phase margin (PM), defined as:

$$\mathrm{PM} = 180° + \angle \beta H(\omega = \omega_1), \tag{2.25}$$

Where, ω_1 is the gain crossover frequency.

The system is considered to be unstable for a phase margin less than 0°, while for a phase margin between 0° and 45° system is considered marginally stable. Y (jω1)/ X (jω1) = 1/β, suggesting a negligible frequency peaking i.e. the step response of the feedback system shows little ringing and providing a fast settling for PM = 60°. For a greater PM, the system becomes more stable but time response slows down. Thus PM = 60° is typically considered the optimum value [13].

For a two stage op-amp, the open-loop transfer function is given by:

$$A(s) = \frac{A_1 A_2 \omega_1 \omega_2}{(s + \omega_1)(s + \omega_2)} \tag{2.26}$$

which assume that A_3 is close to unity and that ω_3 is very high and negligible. The magnitude and phase function are:

$$|A(j\omega_t)| = \frac{A_1 A_2 \omega_1 \omega_2}{\sqrt{(\omega_1\omega_2 - \omega_t^2)^2 + (\omega_t(\omega_1 + \omega_2))^2}} \tag{2.27}$$

And

$$\angle A(j\omega_t) = -\left(180 + \arctan\left(\frac{\omega_t(\omega_1 + \omega_2)}{\omega_1\omega_2 + \omega_t^2}\right)\right) \tag{2.28}$$

The corresponding unity gain frequency must be derived from the magnitude function, in order to determine the phase margin. The phase can be calculated at the derived unity gain frequency. The necessary compensation steps are to be taken place to stabilize the circuit, after calculating the initial phase margin.

CHAPTER 3

OPERATIONAL AMPLIFIER COMPENSATION

3.1 Introduction

The single stage operational amplifier typically has good frequency response and could achieve a phase margin of 90^0 assuming the gain bandwidth is ten times higher than the single pole. However, the dc gain of the single amplifier is generally not high enough and is even less for submicron CMOS transistors. In general, op amps require at least two gain stages. As a result, op amp circuits have multiple poles. The poles contribute to the negative phase shift and may cause the phase margin become zero before the unity gain frequency. The circuit will then oscillate due to the negative phase margin. This will leads to the necessity of altering the amplifier circuit to increase the phase margin and stabilize the closed loop circuit. This process is called as "compensation".

By intuition, two different approaches may be taken to stabilize the circuit. The most straightforward way is to make the gain drop faster in order for the phase shift to be less than -180^0 at the unity gain frequency. This method achieves stability by reducing the bandwidth of the amplifier. Another compensation method pushes the phase crossover frequency out by decreasing the total phase shift. In this case, the number of the poles of the op amp needs to be minimized while still providing enough gain. Pushing the phase crossover frequency out is the basic idea of approaches like introducing zeros to cancel the poles or using feed-forward paths to improve the phase margin without narrow-banding the bandwidth.

An op-amp commonly is unstable in the unity feedback system, after connecting them together and designing each stage. The methods to compensate the op-amp can be employed by using the measurement technique described in the previous section. In the later sections, various compensation techniques which modify the open loop transfer function or the closed loop transfer function to increase the phase margin have been discussed.

3.2 Basic Frequency Compensation Techniques of Operational Amplifiers

3.2.1 Parallel Compensation

The common way to compensate the op amp is Parallel compensation. A capacitor is connected in parallel to the output resistance of a gain stage of the operational amplifier so that the pole can be modified. Due to the large capacitance value required to compensate the op amp, it is not commonly used in the integrated circuit.

3.2.2 Pole Splitting – Single Capacitor Miller Compensation (SCMC)

This method was first used in bipolar architecture and then widely imitated in CMOS operational amplifier designs. By putting a compensation capacitor between the input and output nodes of the second inverting stage of the op amp, the dominant pole is created due to Miller [14, 15] feedback. This method maintains a high mid-band gain for the op amp since the capacitor does not affect the dc response of the amplifier. As the transistor gain of the second stage increases, the dominant pole decreases and the non-dominant pole increases.

For a two-stage op amp Single Capacitor Miller Compensation (SCMC), significantly reduces the frequency of dominant pole and moves the output pole away from the origin. This effect is called “pole splitting”, is a common technique in op-amp design. In this method, a capacitor, C_C, is connected in parallel with the second stage, as shown in fig. 3.1.

Miller’s theorem states that the impedance seen in parallel with a gain stage can be modeled as impedance connected from the input of that gain stage to the ground, and impedance connecting from the output of that gain stage to the ground.

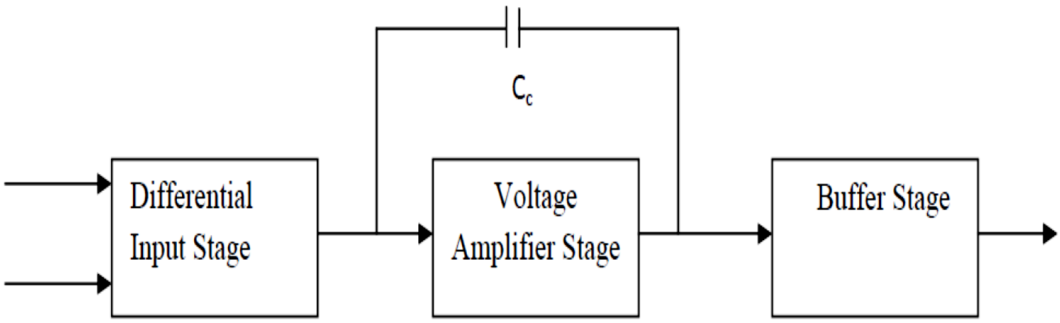


Fig 3.1: Implementation of pole-splitting (Miller Compensation)

In this case because the impedance is purely capacitive and the second stage has inverting gain, the first capacitor has a reflected capacitance of C_C (1 + A), where A is denoted as the gain of the second stage. When a large capacitor is needed to reduce the pole of the first stage, it can be generated by a smaller capacitor and the described Miller multiplication. The second capacitor has a value much closer to the compensation capacitor C_C, especially for large gains [16].

Before the implementation of pole-splitting, the first and the second stage have pole frequencies

$$\omega_1 = \frac{1}{R_1 C_1} \tag{3.1}$$

And

$$\omega_2 = \frac{1}{R_2 C_2} \tag{3.2}$$

respectively, where R_1,C_1 and R_2,C_2 are the output resistance and capacitance of each stage.

After compensation, these frequencies becomes

$$\omega_1 = \frac{1}{R_1\left(C_1 + C_c(1+A)\right)} \tag{3.3}$$

and

$$\omega_2 = \frac{1}{R_2\left(C_2 + C_c\left(1+\frac{1}{A}\right)\right)} \tag{3.4}$$

due to the Miller capacitance seen in parallel.

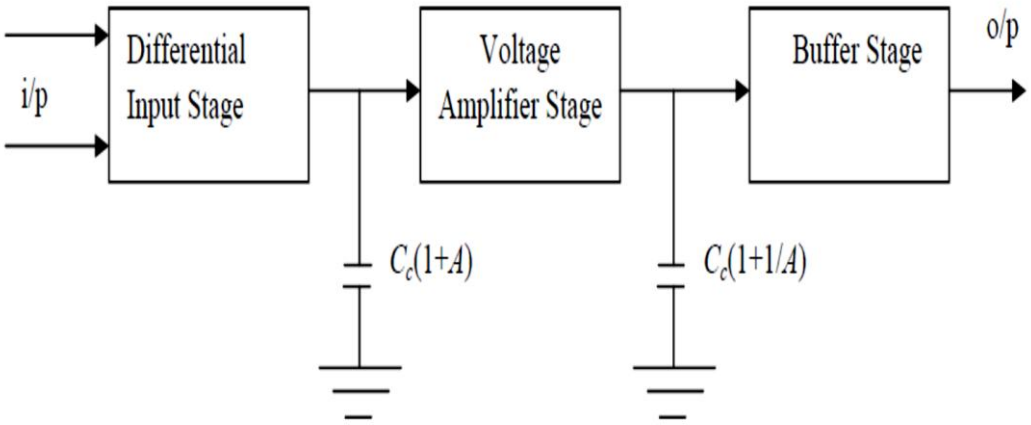


Fig. 3.2: Miller equivalent of circuit in Fig. 2.12

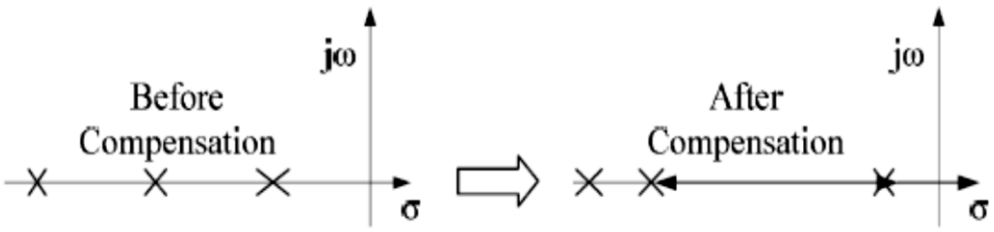


Fig. 3.3: Pole splitting

Operational amplifier's phase improves that makes op amp more stable than that was before compensation, due to reduced frequency of first stage. In the making the op-amp stable, bandwidth is considered one of the significant tradeoff. The first stage bandwidth reduction results in the reduction of overall bandwidth. Due to changing demands of technology, the factors that are considered to be optimized other than bandwidth and phase margin are voltage swing, slew rate, common mode rejection, power consumption. Some of the compensation techniques developed focus on optimizing these different factors based on their specific application.

While designing the op-amp with cascade topology, the zeros are quite far from the origin, in two-stage op amps incorporating Miller compensation, a nearby zero appears in the circuit. As with poles in left half plane, a zero in the right half plane contributes more phase shift, thus moving the phase crossover toward the origin. From Bode approximations, the zero slows down the drop of the magnitude, thereby pushing the gain crossover away from the origin which results in stability degradation.

Two effective means have evolved for eliminating the effect of the right half-plane zero. One approach has been to insert a source follower in the path from the output back through the compensation capacitor to prevent the propagation of signals forward through the capacitor. An even simpler approach is to insert a nulling resistor in series with the compensation capacitor [17].

3.2.3 Single Capacitor Miller Compensation with a Nulling Resistor

In practice so as to cancel the first nondominant pole we can move the zero. This occurs if the value of nulling resistor (R_Z) is chosen such that the frequency of zero is same as that of the first nondominant pole.

The possibility of canceling the nondominant pole makes this technique quite attractive and advanced, but it also has some drawbacks.

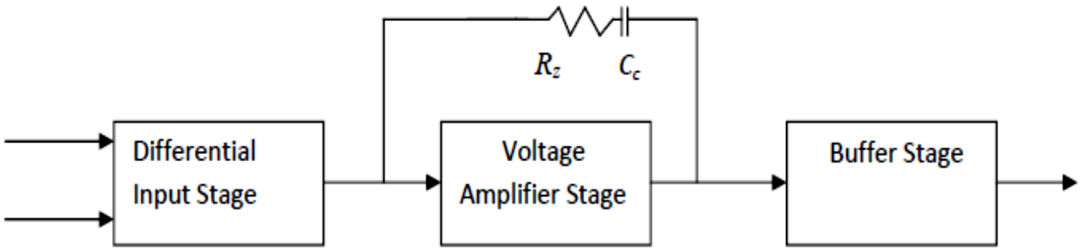


Fig. 3.4: Addition of Rz in series with compensation capacitor

Drawbacks can be stated as:-

1. The load capacitance seen by an op amp may vary in switched-capacitor circuit during the period which requires a corresponding change in *Rz* and which complicates the design.

2. The actual implementation of *Rz* in integrated circuit. As the nulling resistor realized by a MOS transistor in the triode region, *Rz* changes substantially as

output voltage excursions are coupled through *Cc* to node *X* of MOS transistor, which degrade the large-signal settling response [18].

3. The effect of the nulling resistor to the positions of the poles as well as that of the zero and pointed out the pole splitting would break down if the resistor becomes too big. When the resistor gets very large, there is no pole splitting since the compensation capacitor is actually open circuit.

3.3 Other Multistage Operational Amplifier Compensation Techniques

Many gain boosting schemes have been reported to improve the gain. In general, these gain enhancing designs require more complicated circuit structure and a larger power supply voltage, but generate smaller output swing. As a result, multiple stage amplifiers might be more suitable for low power, low voltage, and high density analog circuit designs. The frequency response of the multistage amplifier is not as good as that of the single stage and this amplifier has a higher probability of oscillation in feedback circuits.

Although SCMC and SMCNR are quite simple to implement into a design, several other techniques are popular for compensation in op amps consists of multiple gain stages. Some frequency-compensation topologies are as below:

1. **Nested Miller Compensation (NMC)**
2. **Reversed nested Miller compensation (RNMC)**
3. **Multipath NMC (MNMC)**
4. **Nested Gm-C compensation (NGCC)**
5. **Single Miller Feed-Forward Compensation (SMFFC)**
6. **Nonstandard NMC Schemes**
7. **No Capacitor Feed-Forward (NCFF)**
8. **Negative Miller Capacitance Compensation (NMCC)**

3.3.1 Nested Miller Compensation (NMC) and the Variants

Unlike in single stage amplifier multistage amplifiers have more poles and zeros. The frequency response and time response are far more complicated than those of the single stage op amps. As a result, all multistage amplifiers suffer closed loop stability problems. Single Miller compensation is used for the simple two-stage amplifier; while the extended version of the SMC compensation, nested Miller compensation (NMC) [19] is applied to amplifiers with three or more stages. Because of the rapid bandwidth reduction, op amps with more than four stages are rarely investigated. NMC exploits the nested structure of feedback capacitors to cause the pole splitting compensation. There are some drawbacks related to the NMC approach. The total of N-1 nested compensation capacitors must be placed between the dominant node and the other nodes to split the individual poles from the dominant output pole to stabilize an N stage op amp. fig. 3.5 shows the structure of a three stage NMC op amp.

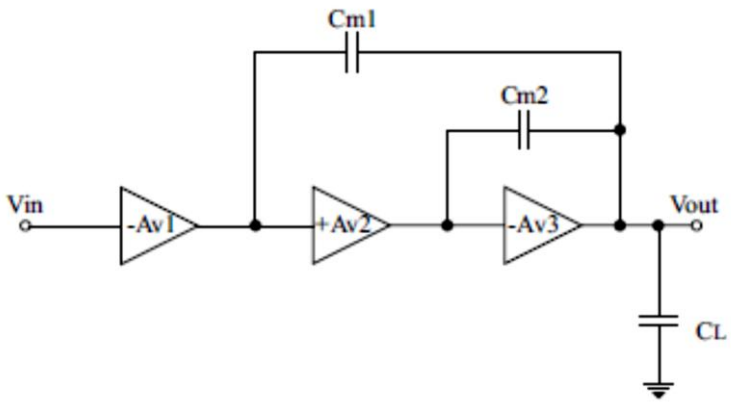


Fig. 3.5: Structure of a three-stage NMC amplifier.

The nesting topology of the compensation capacitor reduces the bandwidth substantially [20]. The specific configuration requires the compound non-inverting gain stages to connect to the inverting output stage in order to secure negative feedback for the nested compensation loops. The necessity to drive the compensation capacitors along with the capacitive load requires the output stage to have a high transconductance to attain wide bandwidth and high slew rate. Consequently, elevated power consumption is unavoidable especially for large load capacitor.

To address the bandwidth degradation problem, the variations of the NMC are developed. NMC using nulling resistor (NMCNR) [21], reversed nested Miller

compensation (RNMC), multipath NMC (MNMC) [22], nested Gm-C compensation (NGCC) [23] have been presented.

3.3.2 Reversed nested Miller compensation (RNMC)

By using the reversed compensation topology RNMC improves the bandwidth over NMC compared to NMC as shown in fig. 3.6.

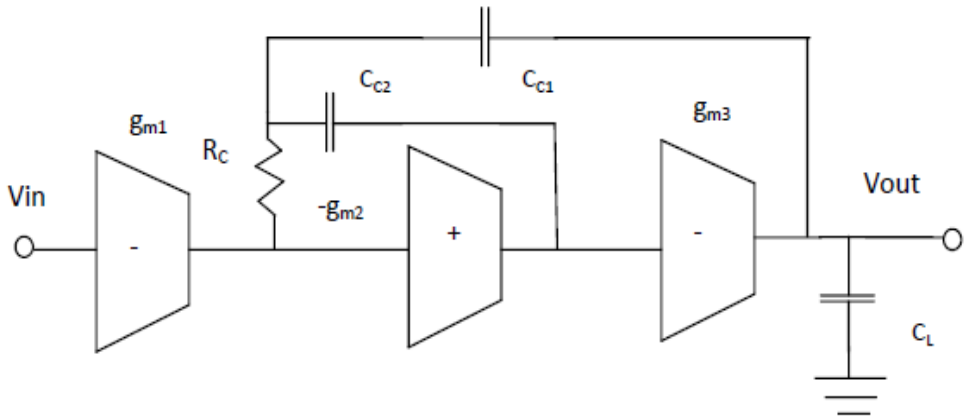


Fig. 3.6**:** Block diagram of the basic RNMC.

The RNMC technique sets the second gain stage as negative while the output stage positive. The Miller capacitor loop is around the second stage without connection to the considerable output capacitive load. HNMC combines the NMC and the RNMC topological properties in a multistage (above three) op amp. In this circumstance, the circuit could consist of only inverting amplifier except for the input stage.

3.3.3 Multipath NMC (MNMC)

The difference between NMC and MNMC is the added feed-forward amplifier stage -Af1 connected between the input of the first stage and the input of the last stage of the multistage op amp as shown in fig. 3.7.

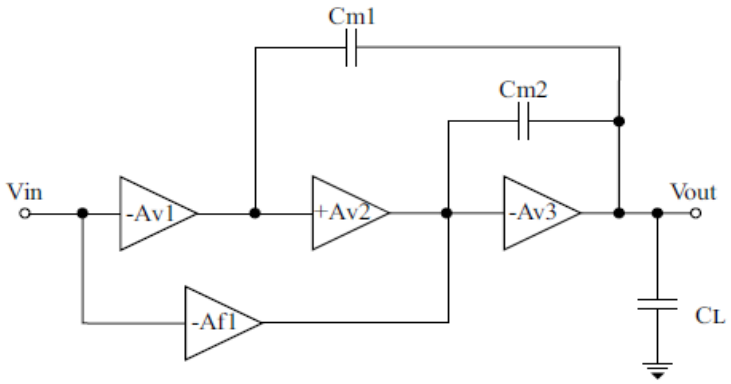


Fig 3.7: Multipath NMC (MNMC)

The feed-forward stage added can produce a LHP zero to counteract the second nondominant pole to broaden the bandwidth. For both NMC and MNMC methods, it is required that the load transconductance be much larger than the first and second stage transconductance. It is difficult to meet this condition for low-power designs. In this topology circuit complexity and power consumption increased. The increased circuit complexity and power consumption should be considered. Moreover, the pole zero doublets may seriously degrade the settling time of the amplifier.

3.3.4 Nested Gm-C compensation (NGCC)

Another method was proposed, called NGCC. The difference between NGCC and MNMC is that NGCC replicates the feed-forward Gm N-1 times for an N stage op amp recursively as shown in fig. 3.8. Compared to MNC, NGCC has simpler stability conditions due to the much simpler transfer function which makes the op amp design more facile.

The basic idea of most of these variations of the NMC schemes is not to drop the overall bandwidth of the multistage amplifiers by the pole zero cancellation in the pass-band caused by the feed-forward path of the multipath topology. All of those compensation techniques mentioned above use Miller capacitors whose sizes are related to the load capacitor value. The required sizes of the compensation capacitors would shoot up with larger capacitive loads which does not make these techniques preferable one for low area need. The experimental results of the varied versions of NMC showed that the bandwidth does not get improved significantly for considerable capacitive loads.

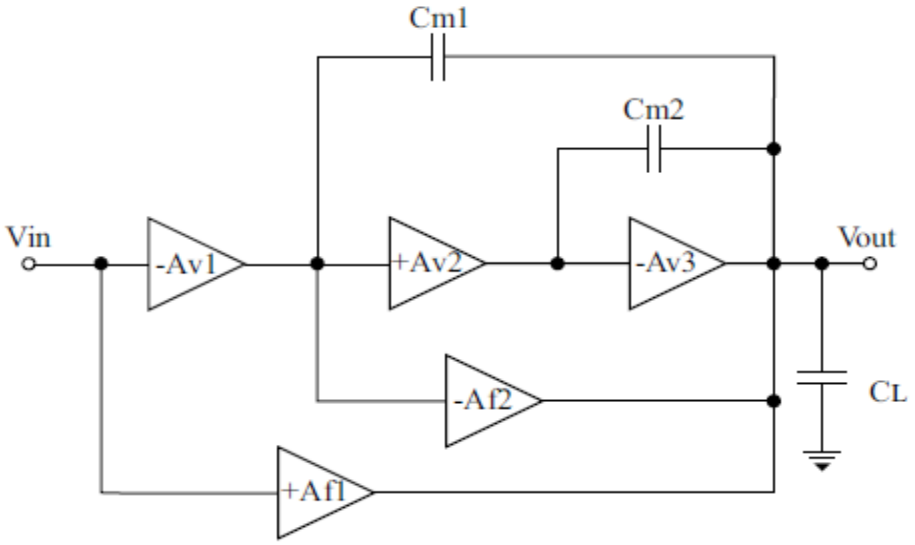


Fig 3.8: Nested Gm-C compensation (NGCC)

3.3.5 Single Miller Feed-Forward Compensation (SMFFC)

Many compensation techniques mentioned above are not suitable for large load capacitors. The demand for lower power consumption, lower chip integration area, capability for driving large capacitive loads and stable high gain bandwidth of amplifiers calls for improved frequency compensation patterns. The topologies using a single Miller capacitor in three stage amplifiers could greatly reduce the needed sizes of the compensation capacitors compared to NMC related schemes and results in amplifiers with smaller chip area. The topology of the SMFFC op amp is represented in fig. 2.9.

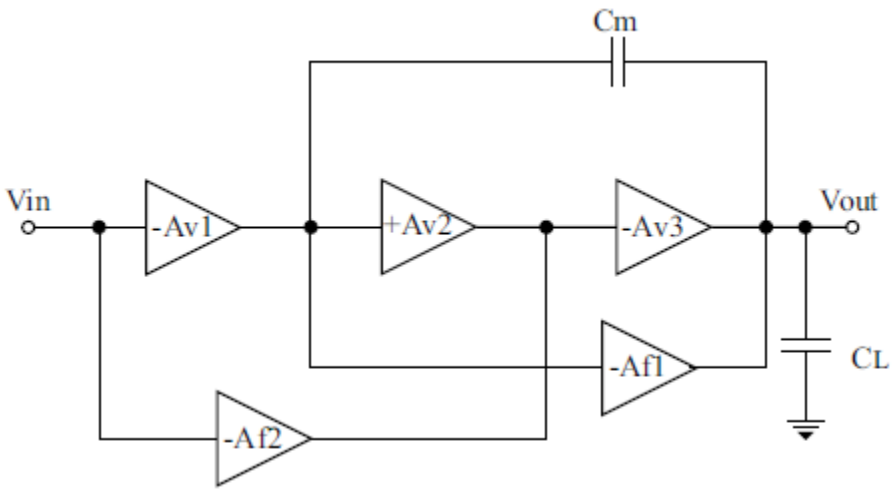


Fig 3.9: Single Miller Feed-Forward Compensation (SMFFC)

Instead of using pole zero cancellation, SMC with one forward path adopts the separate pole approach for compensation in the situation of large capacitive loads. SMFFC employs two forward paths and provide a LHP zero to compensate the first nondominant pole to alleviate the bandwidth reduction and improve the phase margin.

The strictly rational selection of gains among the three stages is the key point for this SMFFC scheme. For the gain distribution like Av1 > Av2 > Av3, the second and third poles of the amplifier would be placed at higher frequencies that lead to a coarse single pole system for an easier frequency compensation strategy. The appropriate selection of the moderate gain of the second stage will then decrease the compensation capacitor size. Unfortunately, this method does not truly resolve the compressed gain bandwidth issue due to the super high gain of the first stage and the nature of the pole separation.

Gain enhanced feed-forward path compensation (GFPC) is much like the modified SMC version with one feed-forward path, but for two stage amplifiers.

3.3.6 Nonstandard NMC Schemes

The nonstandard NMC topologies have been investigated to deal with the drawbacks with the NMC and MNMC in order to be able to drive large capacitive loads. The reported strategies include damping factor control frequency compensation (DFCFC), embedded RC compensation (ERC), active feedback frequency compensation (AFFC), and dual loop parallel compensation (DLPC).

The ERC duplicates the RC compensation process N-2 times for an N stage op amp. ERC compensation circuits do not load the output stage as NGCC circuits do. The non-inverting gain stages are not necessary in ERC as in NMC or the standard variations of NMC. ERC topology extends the bandwidth via the zero pole cancellation through the embedded compensation network without connection to the output load. Usually ERC uses a low gain, high conductance output stage to have the similar loading isolation benefit as the buffer output stage of the Widlar architecture.

DFCFC can substantially improve the bandwidth of a three stage amplifier with good frequency and transient responses when driving large capacitive loads. But it is not

so effective for small capacitive load applications. Some other compensation methods turn out to be more suitable than DFCFC when driving a small capacitive load.

3.3.7 No Capacitor Feed Forward (NCFF)

One feed-forward compensation scheme for multistage operational transconductance amplifiers with no Miller capacitors is proposed by Thandri and Silva-Martinez. By using the positive phase shift of LHP zeros to cancel the negative phase shift of the poles, a high gain, high bandwidth amplifier with a good phase margin is developed.

During the design there are some design consideration has to be consider: the feed-forward and second stage must place the nondominant poles after the overall unity gain frequency of the amplifier to alleviate phase deduction; the pole zero cancellation should happen at high frequencies to achieve better time domain response. This NCFF method applies the feed-forward path as shown in fig. 3.10 to create LHP zeros.

The transient response might be degraded severely by the pole-zero doublets. The complexity of the presence of extra poles and zeros can cause the design of the NCFF scheme to be very difficult. To achieve better time domain response some other constraints of the NCFF scheme should also be recognized. The NCFF is not suitable for big capacitive loads.

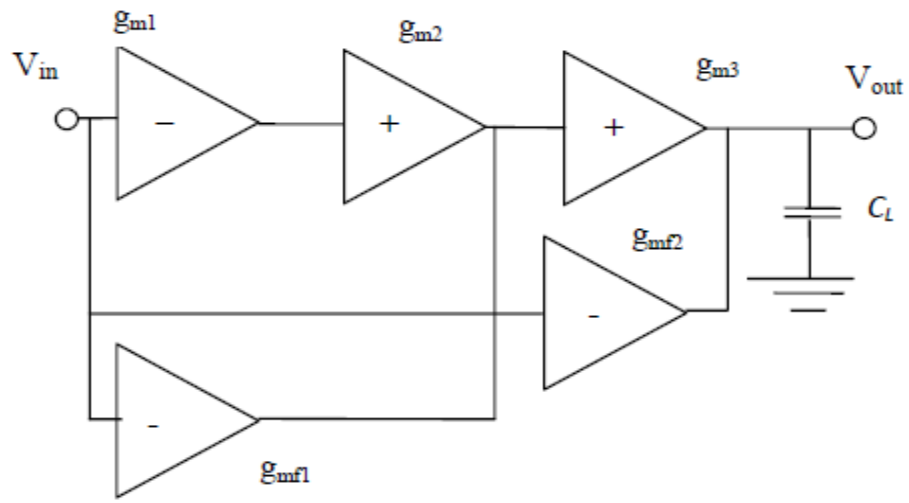


Fig. 3.10: No capacitor feed forward (NCFF)

A good performing amplifier should have both good frequency response and transient response. The undesired low frequency pole-zero doublets may lengthen the settling time of the amplifier or even make the closed loop unstable.

3.3.8 Negative Miller Capacitance Compensation (NMCC)

The negative Miller capacitance compensates high speed CMOS op amps that consist of an operational transconductance amplifier (OTA) and a buffer. The buffer with a dc gain of A is used to detach the OTA from the load. The OTA is compensated with a capacitor Cc connected between the input and output of the buffer as in fig. 3.11.

The OTA is compensated with a capacitor Cc connected between the input and output of the buffer. Assuming the op amp drives a load with a parallel combination of a resistor R_L and a capacitor C_L,

The effective capacitance seen at the input of the buffer is—

$$C_{eff,in} = C_c(1 - A) \tag{3.5}$$

And

$$C_{eff,out} = C_L + C_c\left(1 - \frac{1}{A}\right) \tag{3.6}$$

where, ‘A’ represent the gain of buffer.

Since the gain of the buffer is positive and smaller than one, the reflected Miller capacitor Since the gain of the buffer is positive and smaller than one, the reflected Miller capacitor $C_C(1- 1/A)$ at the output will be negative. The total effective output capacitance is reduced to be smaller than the original load capacitance due to the negative Miller capacitance.

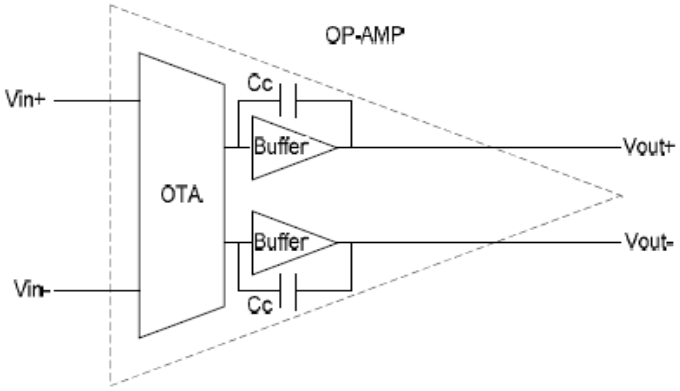


Fig. 3.11: Op-amp bandwidth extension method [23].

This effect pushes the first non-dominant pole (i.e., the pole closest to the origin after the dominant pole) to a higher frequency. Implementation of this scheme into a circuit design has three distinct advantages:

- Undesired capacitance is removed.
- It can be applied to drive a large capacitive load.
- When node capacitance is removed, the associated bandwidth and phase margin of that circuit improved.

This chapter introduced us about the background of feedback systems and the frequency compensation techniques for feedback operational amplifiers. To stabilize op amps, the common techniques are pole splitting and pole zero cancellation using a capacitor and resistor [3]. This section discusses and compares the existing methods of achieving compensation for multistage amplifiers. It points out the advantages and disadvantages of the different compensation topologies in order to help the op amp designers better understand and choose the appropriate structure for different circumstances.

CHAPTER 4

OPERATIONAL AMPLIFIER DESIGN METHODOLOGY

4.1 Introduction

The practical structure of op-amp consists of 3 main blocks. As shown in fig. 4.1.

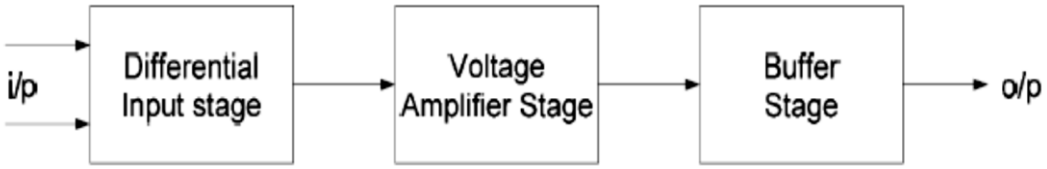


Fig. 4.1: Typical two stage op-amp

Classic op amp architecture is made up of three stages as shown in fig. 4.1, even though it is referred to as a "two-stage" op amp, ignoring the buffer stage (third stage). The first stage usually consists of a high-gain differential amplifier. This stage has the most dominant pole of the system. A common source amplifier usually meets the specification of second stage, having a moderate gain. The third stage is most commonly implemented as a unity gain source follower with a high frequency and negligible pole.

With the two stage classic op-amp architecture, high gain stages are difficult to achieve with Complementary Metal Oxide Semiconductor (CMOS) technology and basic amplifier topologies. A typical CMOS differential amplifier stage is shown in fig. 2.4

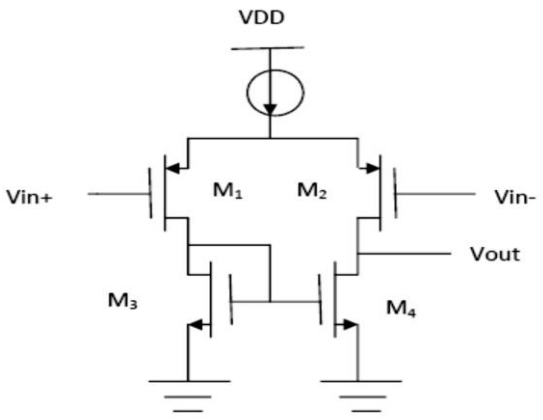


Fig. 4.2: CMOS differential input stage

Differential amplifiers are often desired as the first stage in an op amp due to their differential input to single ended output conversation and high gain. The input devices in fig. 4.2 are p-channel MOSFETs (PMOS).

For the CMOS differential input stage, the gain and bandwidth are calculated as—

$$A_1 = g_{m1}(r_{ds2} \parallel r_{ds4}) \tag{4.1}$$

And

$$\omega_1 = \frac{1}{Cout(r_{ds2} \parallel r_{ds4})} \tag{4.2}$$

Implementation of cascode scheme can increase the moderate gain of this stage to a high value. The stage's dominant pole has an output capacitance, C_{out}, consisting of mainly, the drain-to-bulk capacitance of M2 and M4. Although often negligible, another pole and zero are generated by M1 and M3. The second stage implementation of a common source amplifier shown in fig. 4.3. Similar to the first stage, additional cascade devices can increase gain of this stage. Higher gains are often desirable for this stage when using Miller compensation techniques, although higher gains leads to lower bandwidth and the designer has to decide between these tradeoffs based on the specifications of the system.

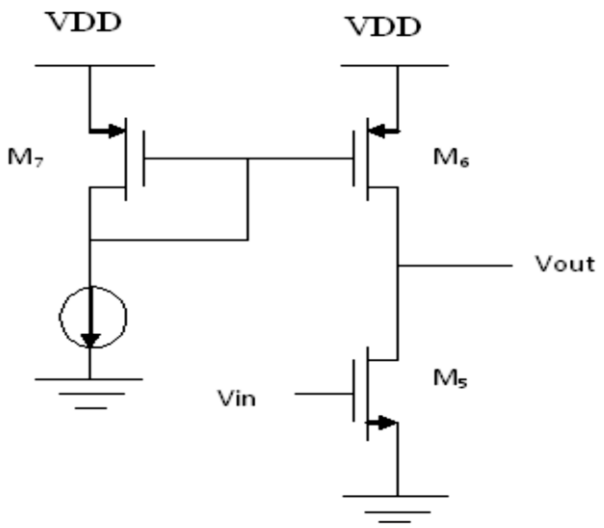


Fig. 4.3: Common source amplifier stage

For the circuit in fig. 4.3, the gain and bandwidth are calculated as—

$$A_2 = -g_{m5}(r_{ds5} \parallel r_{ds6}) \tag{4.3}$$

And

$$\omega_2 = \frac{1}{C_{out}(r_{ds5} \parallel r_{ds6})} \tag{4.4}$$

The output capacitance is dominated by the drain-to-bulk capacitance of M5 and M6.

The final output stage is normally realized with a simple source follower as shown in fig. 4.4. With gain less than, but closer to unity, the source follower acts as a buffer for the previous two stages, reducing the overall gain negligibly and barely affecting the overall bandwidth with its high frequency pole. The gain for the source follower is defined as

$$A_3 = \frac{g_{m8}}{G_L + g_{m8} + g_{ds8} + g_{ds9}} \tag{4.5}$$

Where, G_L is the load conductance that the stage will drive.

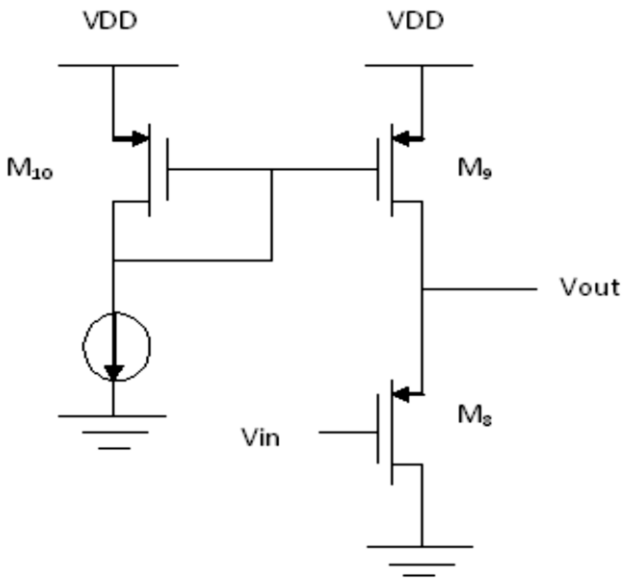


Fig. 4.4: Source follower

4.2 Weak Inversion Technique for Low Power Design

A simple model for weak inversion is given as—

$$i_D = \frac{W}{L} I_{Do} \exp\left(\frac{v_{GS}}{n(KT/q)}\right) \tag{4.6}$$

Where 'n' is the subthreshold slope factor and its value of n is greater than 1 and less than 3 and I_{Do} is process dependent parameter. It depends on V_{SB} and V_T.

The point at which transistor enters the weak inversion region can be approximated as—

$$v_{gs} < V_T + n\frac{KT}{q} \tag{4.7}$$

Operation of the MOS device in subthreshold region is very important when low power circuits are desired.

From above equation, the transconductance can be derived as—

$$g_m = \frac{I_D}{nKT/q} \tag{4.8}$$

There is linear relationship between transconductance and current. Also transconductance is independent of device geometry. But in strong inversion relationship between transconductance and current is square law and also function of device geometry.

4.3 Parameter Extractions of MOS in Subthreshold Region

Procedure for extracting parameters of MOS in subthreshold regions is mentioned here. I_D for weak inversion is given as—

$$I_D = I_o \frac{W}{L} e^{\frac{V_{GS}-V_{TH}}{nU_T}} \left(1 - e^{\frac{V_{DS}}{nU_T}}\right) \tag{4.9}$$

Where,

$$I_o = 2.n.\mu.C_{ox}U_T^2 e^{\frac{V_{THo}}{nU_T}} e^{\frac{(n-1)V_{BS}}{nU_T}} \tag{4.10}$$

U_T is thermal voltage which is 25.9mV, V_{TH} is threshold voltage and 'n' is subthreshold parameter.

Subthreshold parameters of MOS in weak inversion can be calculated experimentally using I_D and V_{GS} curve in weak inversion region. Subthreshold parameter 'n' is normally measured from the slope of linear region $\ln(I_D)$ and V_{GS} curve in weak inversion region. Parameter extraction (I_O and n) for n-MOS in subthreshold region is given here.

4.3.1 Subthreshold Slope Factor 'n' Extraction

Subthreshold parameter 'n' is normally measured from the slope of linear region $\ln(I_D)$ and V_{GS} curve in weak inversion region. From this curve we can measure the slope of the $\ln(I_{DS})$ vs V_{GS} curve shown in fig 4.5. This slope is also derived by differentiating the drain current in subthreshold region with respect to V_{GS} i.e. slope is obtained by differentiating equation (4.6) and is given as

$$slope = \frac{1}{nU_T} \tag{4.11}$$

Where U_T is the thermal voltage and its value is 25.9mV. From equation (3.3), Subthreshold parameter 'n' can be calculated as n= 1.172.

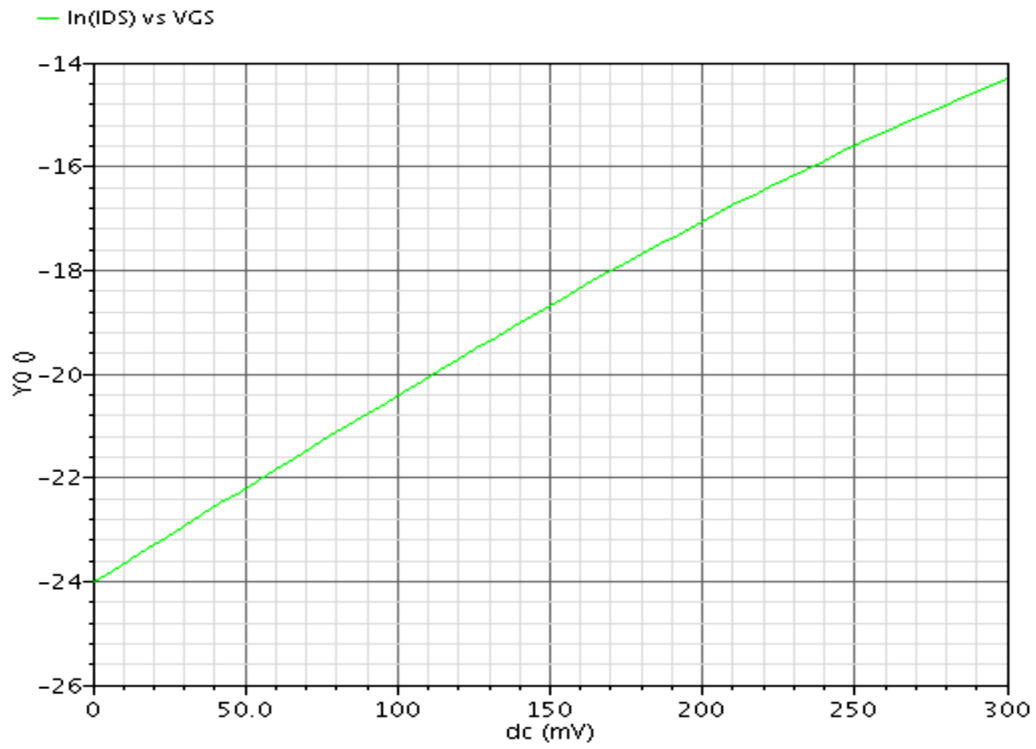


Fig. 4.5**:** ln(I_D) and V_{GS} curve in weak inversion region

4.3.2 I_O EXTRACTION

Io is calculated from I_D and V_{GS} curve in weak inversion region. I_D and V_{GS} curve in weak inversion region is given below in fig 4.6.

Procedure for Calculating I_o:

Select four to five set of values of V_{GS} and corresponding values of I_D. And then calculate value of Io using equation (4.9) for each set of values. And then by taking average of all values to get final value of Io. I_D and V_{GS} curve in weak inversion region is given below in fig. 4.6.

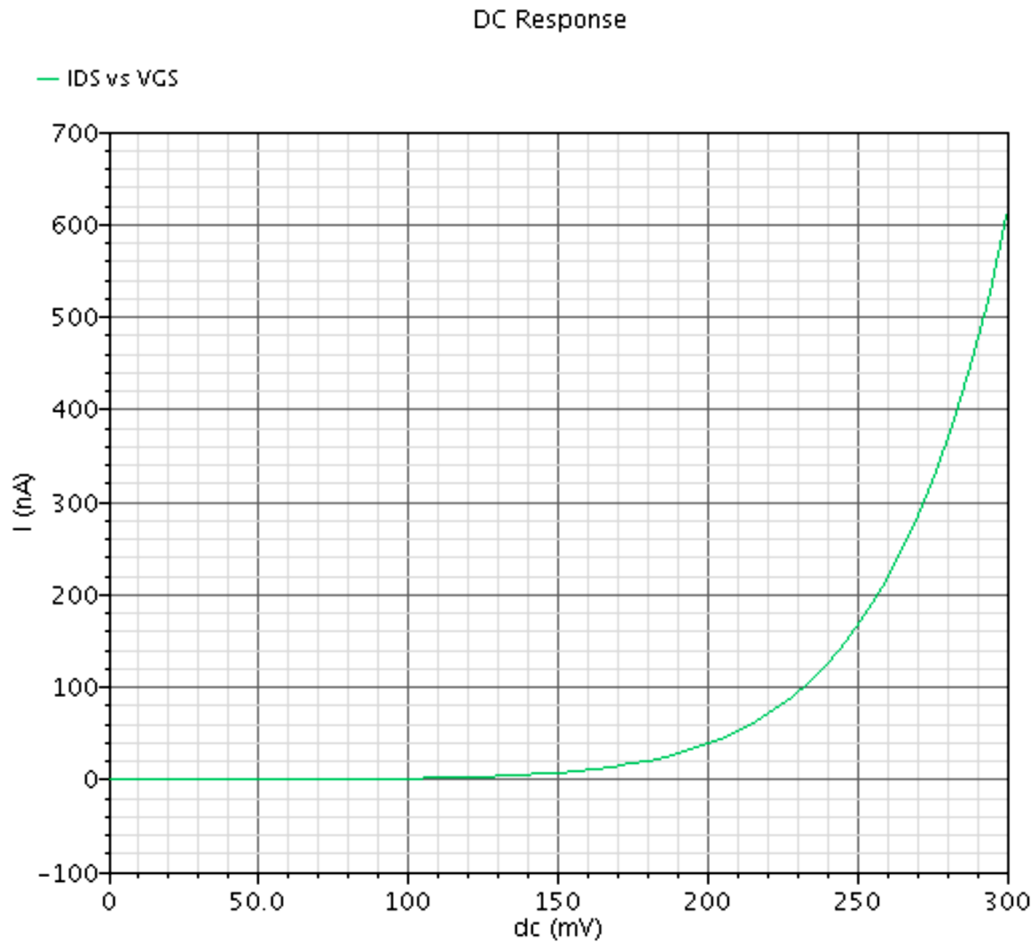


Figure 4.6 ID and VGS curve in weak inversion region

Average value of Io = 263.5 nA.

4.3.3 Calculation Channel Length Modulation Coefficient (Lambda, λ)

Channel length modulation coefficient can be calculated from curve IDS vs VDS given in fig. 4.7. Channel length modulation coefficient can be calculated experimentally by using following formula:

$$\frac{I_{DS1}}{I_{DS2}} = \frac{1+\lambda V_{DS1}}{1+\lambda V_{DS2}} \tag{4.12}$$

For 1µm length

$\lambda_{n,sub}$ = 0.28, for NMOS transistor in subthreshold region , λ_n = 0.13 for strong inversion and λ_p = 0.0215, for PMOS transistor.

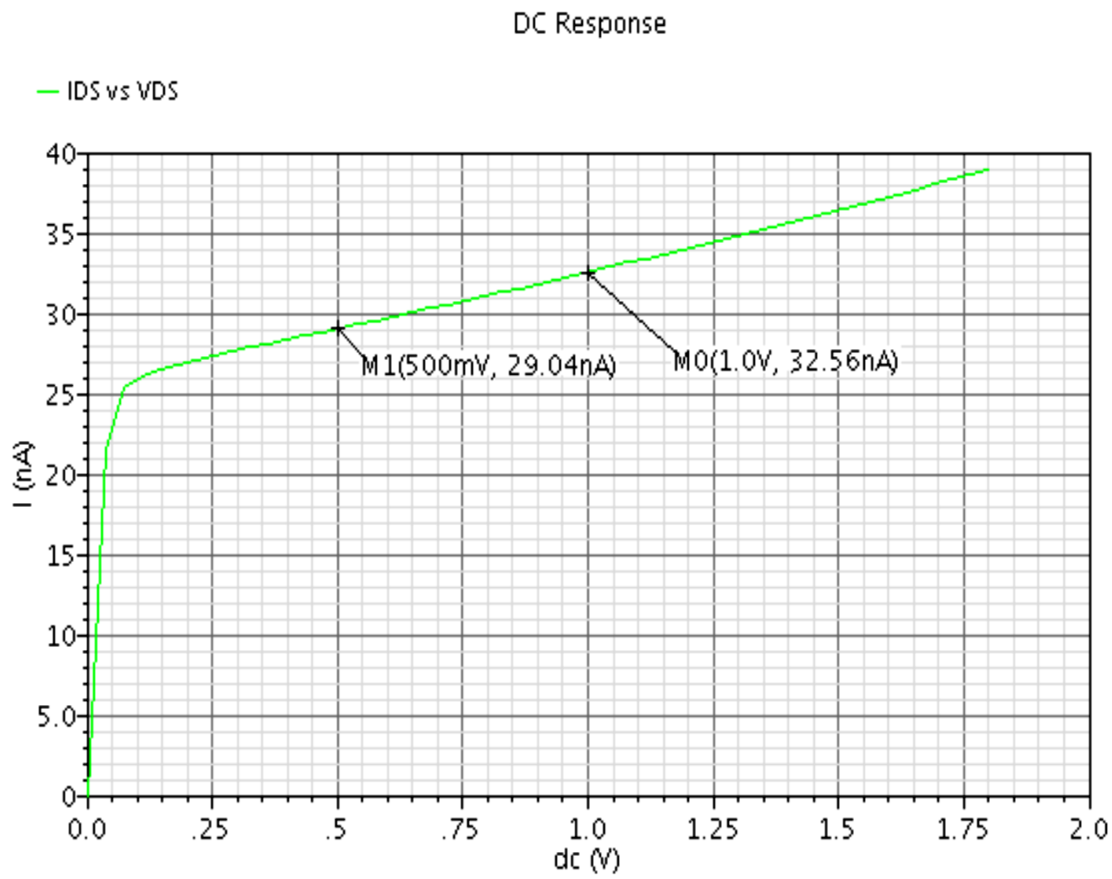


Figure 4.7: Plot between ID vs VDS for NMOS in subthreshold

4.4 Optimized Design Approaches

The two-stage operational amplifier is a widely used analog building block as shown in fig.4.1. Indeed, it identifies a very simple and robust topology which provides good values for most of its electrical parameters such as dc gain, output swing, linearity, CMRR, etc. To avoid closed-loop instability, frequency compensation is necessary in op amp design. For two-stage CMOS op amp, the simplest compensation technique is to connect a capacitor across the high gain stage. This results in the pole splitting phenomena which improves the closed-loop stability significantly.

However, due to the feed-forward path through the Miller capacitor, a right half-plane (RHP) zero is also created. An uncompensated right half-plane zero drastically reduces the maximum achievable gain-bandwidth product, since it makes a negative phase contribution to the open-loop gain at a relatively high frequency. In order to compensate the right-half plane zero, an appropriate design approach is essential. Such a zero can be nullified if the compensation capacitor is connected in conjunction with either

a nullifying resistor or a common-gate current buffer. After compensation of right half-plane zero, the maximum gain-bandwidth product is limited by second pole.

Various techniques for the compensation of the right half-plane zero in two stage CMOS op amp have been proposed and as well adopted. A compensation technique was proposed which uses a nulling resistor in series with the compensation capacitor. In an another solution a voltage buffer is introduced in compensation branch which breaks the forward path through the compensation capacitor while the other one uses a current buffer to break the forward path. Both current and voltage buffers can be adopted for compensation of the right half-plane zero due to their advantages over nulling resistor as it is more sensitive to process and temperature variation.

To achieve a high gain-bandwidth product a very high g_{m5} value is required. However, it has been shown that it is possible to take advantage of techniques for compensation of the right half-plane zero to obtain a better frequency response. The original of these techniques was applied to NMOS op amps and then to CMOS op amps. Three different solutions for compensation are:

1. **Nulling Resistor Approach**
2. **Voltage Buffer Approach**
3. **Current Buffer Approach**

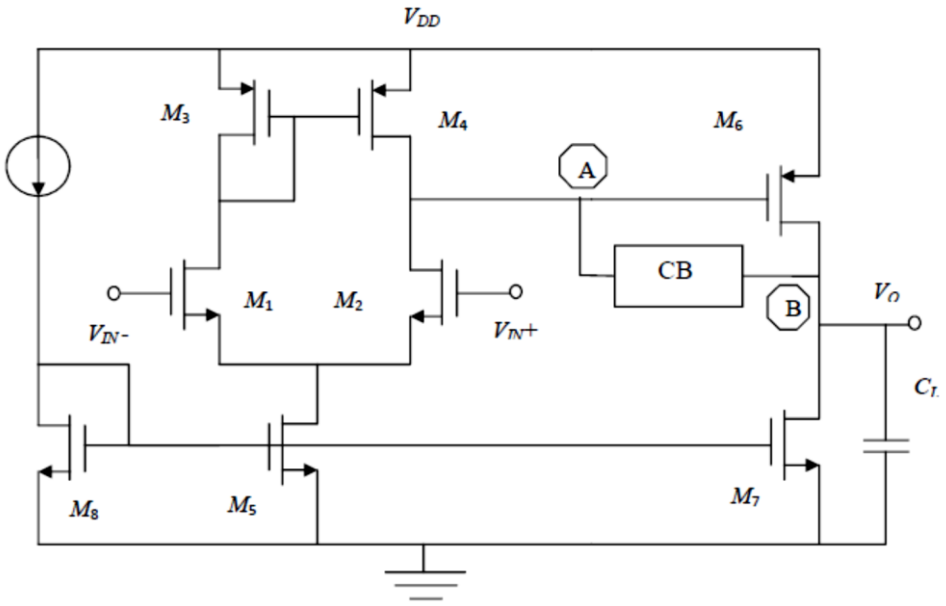


Fig. 4.8: Two-stage op amp

4.4.1 Nulling Resistor Approach

The most popular compensation technique is that based on the nulling resistor, since it can be implemented using only an MOS transistor biased in the triode region. In this approach the left half-plane zero introduced by the nulling resistor R_C.

$$f_z = \frac{1}{2\pi} \frac{g_{m5}}{(g_{m5}R_C - 1)C_C} \tag{4.13}$$

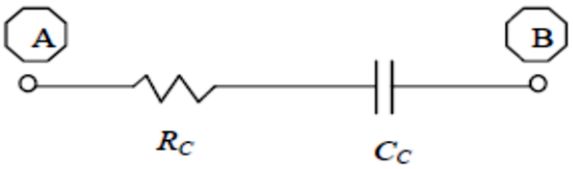


Fig. 4.9: RC compensation block

is exploited to compensate for the second pole. Therefore, the compensation sets the following condition,

$$\frac{g_{m5}}{C_L} = \frac{g_{m5}}{(g_{m5}R_{CR} - 1)C_{CR}} \tag{4.14}$$

where C_{CR} and R_{CR} are the new compensation capacitor and resistor, respectively. Once this compensation is achieved, the new second pole is

$$f_{SP} = \frac{1}{2\pi R_{CR} C_{o1}} \tag{4.15}$$

where C_{o1} is the equivalent capacitance at the output of the first stage and is equal to $C_{db2} + C_{db4} + C_{gs5}$. This second pole does not depend on the load capacitance; hence a higher gain-bandwidth product can be achieved by nulling resistor approach. In order to achieve the desired phase margin the dominant pole can be choose accordingly.

4.4.2 Voltage Buffer Approach

The adoption of an ideal voltage buffer (i.e., with zero output resistance) to compensate the right half-plane zero gives the same second pole. and hence, the same

W_{GBW}. Usually, the simple common drain is employed and connected between nodes A and B in fig.4.8.

Taking into account for the finite output resistance of the buffer which is about equal to $1/g_{m9V}$, the compensation branch introduces a left half-plane zero at $fz = g_{m9V} /2\pi C_{CV}$. Therefore, a pole-zero compensation with the original second pole is achieved by setting

$$\frac{g_{m5}}{C_L} = \frac{g_{m9V}}{C_{CV}} \tag{4.16}$$

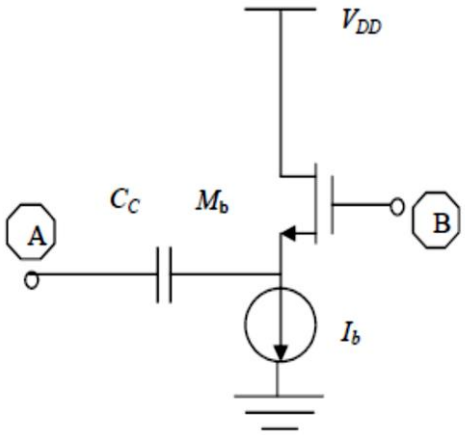


Fig. 4.10: Voltage buffer compensation block.

This compensation shows high accuracy since it only depends on matching tolerances between transconductance and capacitors.

The approaches based on nulling resistor and voltage buffer give the same compensation capacitor and hence the same gain-bandwidth product. However, a voltage buffer in the compensation branch greatly reduces the output swing preventing its use in many practical cases [24].

4.4.3 Current Buffer Approach

The compensation based on current buffer (i.e., block CB in Fig. 4.8 is replaced by the circuit in fig. 4.11).This approach is very efficient both for the gain-bandwidth and the PSRR performance. It also does not have the drawback of the voltage buffer which reduces the amplifier output swing.

In this design approach the minimum allowable value of C_C is much smaller. The ability to use smaller provides a higher degree-of-freedom in trading noise performance with power consumption. For this purpose, the common gate in fig. 4.11 can be used which is connected between nodes A and B in Fig. 4.8.

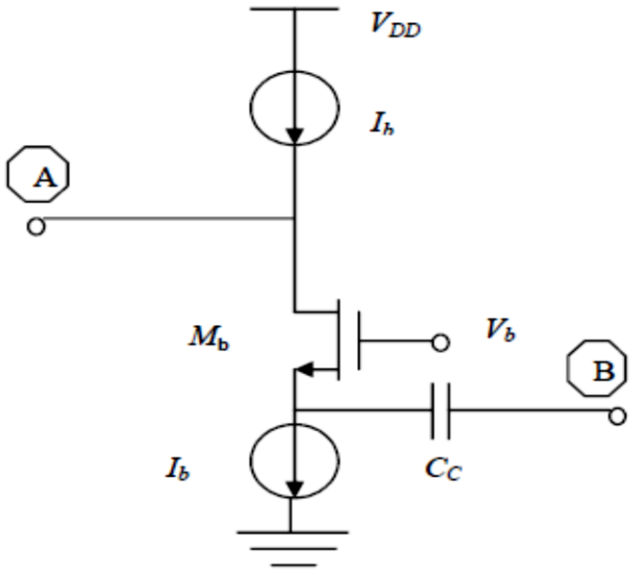


Fig. 4.11: Current buffer compensation block.

4.4.4 Comparison of Design Approaches Based on Performance Parameter

The table given below which are based on simulation results [25].

Table I: Comparison of Design Approaches.

Design Approach	**Compensation capacitor, C_C** (pF)	**UGB** (MHz)	**Power** (μW)
Nulling Resistor	2.5	5	590
Voltage Buffer	0.8	20	630
Current Buffer	0.75	28	790

Results show that the compensation with current buffer reduces the gain, but produces the best gain-bandwidth product. The small value requirement of C_C makes it suitable for circuit design where high capacitive load had to drive.

A better and commonly used implementation is achieved by placing the current buffer in the differential stage, in series with the source coupled pair. Circuit design in this way reduces the complexity of the circuit, improve the both low frequency PSRR and gain, and the power dissipation remains less, compare to the nulling resistor approach.

4.4.5 Advantage /Disadvantage with Current Buffer Approach

- ADVANTAGES
- ✓ Good GBW
- ✓ High PSRR
- ✓ Improved slew rate (low CC value)
- ✓ Area efficient (low CC value)
- ✓ Power and area tradeoff
- ✓ Does not reduce output swing (unlike voltage buffer)
- DISADVANTAGE
- ✓ Gain reduces
- ✓ Low noise performance
- ✓ Increased offset

4.5 Designing of Operational Amplifier Using g_m/I_D Method

The two stage operational amplifier is widely used analog building block. Schematic for two stage op-amp with compensation block is shown in figure 4.12. Where CB is the compensation block. The design procedure is based on the following main parameters: phase margin, gain bandwidth product, load capacitance, slew rate, and input common mode range.

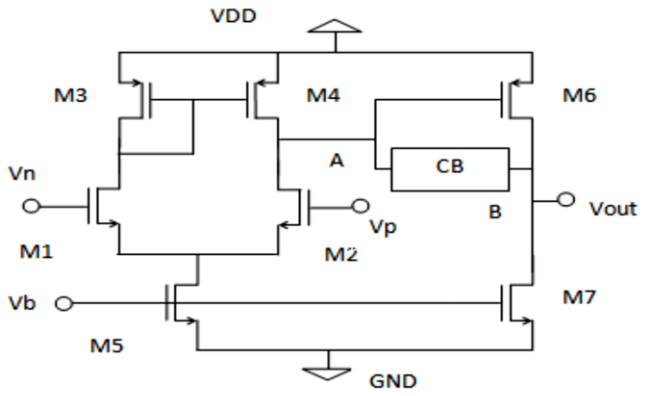


Figure 4.12**:** Circuit diagram of two stage op-amp

The g_m/I_D characteristic curve of MOSFET tells about the region of the transistor operation and helps in calculating the dimensions of transistor. The main advantage of this method is that this curve is unique for given technology. This curve is called as current density plot. This curve gives the knowledge of inversion level i.e. whether the transistor is operating in weak inversion or in moderated inversion or in strong inversion. Knowledge of inversion level allows proper evaluation of design tradeoffs among gain, bandwidth etc. basically weak inversion favours gain and strong inversion favours bandwidth. This method minimizes the time spent on design stage and achieves major accuracy in results. The value of g_m/I_D is maximum in weak inversion and its value is equal to $1/nU_T$. The g_m/I_D ratio decreases as the operating point moves toward the strong inversion when I_D or V_G are increased. The normalized current is independent of the transistor size. So, this current density plot is independent of size of transistor.

The design flow for g_m/I_D methodology is as follows:

1. Determine the g_m from the given specification such as gain and bandwidth.

2. Determine the current from the given specifications such as power dissipation.

3. Decide L for the design depending on the specification requirement.

4. Get g_m/I_D ratio.

5. Determine Bias voltage for current source bias for desired g_m/I_D.

The relationship between g_m/I_D and the normalized current is a unique characteristic for all transistor of the same type (NMOS or PMOS).

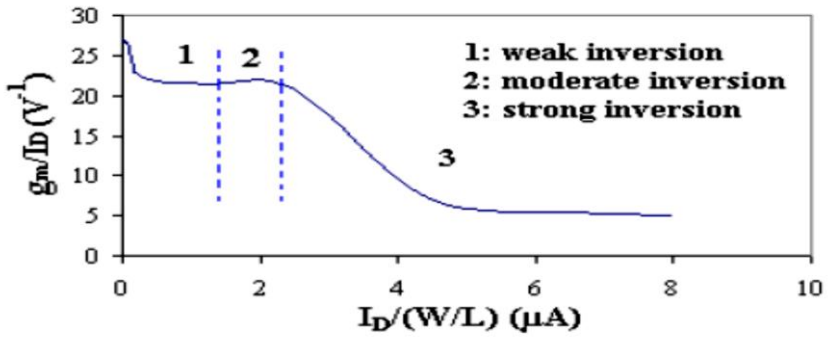


Fig. 4.13: g_m/I_D Vs $I_D/(W/L)$ curve for NMOS

This technique is used to calculate sizes of transistors using values of g_m/I_D and I_D/W. these values are calculated from specifications. For example, first we fix the length L. Current is calculated from power dissipation. Power dissipation is given as:

$$P_D = V_{DD}I \tag{4.17}$$

From power dissipation we calculate current, from gain and bandwidth we calculate g_m/I_D for NMOS and PMOS transistors and from this corresponding normalized current we calculate W of each transistor.

Gain and bandwidth for two stage op-amp is given as:

$$A = \frac{g_{m1}}{I_{D1}}\frac{g_{m6}}{I_{D6}}\frac{1}{(\lambda_n + \lambda_p)^2} \tag{4.18}$$

$$UGB = \frac{g_{m1}}{2\Pi C_C} \tag{4.19}$$

And from,

$$g_{m1} = \frac{I_{D1}}{nU_T} \tag{4.20}$$

$$\frac{g_{m1}}{I_{D1}} = \frac{1}{nU_T} \tag{4.21}$$

And from eq. 4.2 we can calculate $\frac{g_{m6}}{I_{D6}}$ (4.22)

For 60^0 phase margin,

$$C_C = 0.22C_L \tag{4.23}$$

In RC compensated operational amplifier, resistor R allows independent control over the placement of the zero. In order to remove the right hand plane zero, R = $\frac{1}{g_{m6}}$. Another way is to move RHP zero to the LHP and place it on the top of p_2 (2nd pole), for this value of R is given as:

$$R = \frac{1}{g_{m6}}\left(\frac{C_C + C_L}{C_C}\right) \tag{4.24}$$

Using relation between $I_{D1,}$ I_{D5} and I_{D7}, aspect ratios for M_3, M_4, M_5, M_6 and M_7 can be calculated.

Op-amp design equations are as follows—

$$g_{m1} = g_{m2} = g_{mI},\ g_{m6} = g_{mII},\ g_{ds2} + g_{ds4} = G_I, \text{ and } g_{ds6} + g_{ds7} = G_{II} \tag{4.25}$$

$$Id = \frac{\mu_{n,p}\, Cox\left(\frac{W}{L}\right)Veff2}{2} \tag{4.26}$$

$$g_m = \sqrt{2\mu_{n,p}Cox\frac{W}{L}Id} \tag{4.27}$$

$$g_m = 2\frac{Id}{V_{eff}} \tag{4.28}$$

$$\text{Slew rate} \quad SR = \frac{I_5}{C_C} \tag{4.29}$$

$$\text{First stage gain } A_{v1} = \frac{-gm_1}{gds_2 + gds_4} = \frac{-2gm_1}{I_5\,(\lambda_2 + \lambda_4)} \tag{4.30}$$

$$\text{Second stage gain } A_{v2} = \frac{-gm_6}{gds_6 + gds_7} = \frac{-gm_6}{I_6\,(\lambda_6 + \lambda_7)} \tag{4.31}$$

$$\text{Gain Bandwidth} \quad GB = \frac{gm_1}{C_C} \tag{4.32}$$

$$\text{Positive CMR} \quad V_{in}(\max) = V_{DD} - \sqrt{\frac{I_5}{\beta_3}} - |V_{TO3}|(\max) + V_{T1}(\min) \tag{4.33}$$

$$\textit{Negative CMR} \quad V_{in}(\min) = V_{SS} + \sqrt{\frac{I_5}{\beta_1}} + V_{T1}(\max) + V_{DS5}(\text{sat}) \tag{4.34}$$

$$\textit{Saturation voltage}\ V_{DS}(\text{sat}) = \sqrt{\frac{2I_{DS}}{\beta}} \tag{4.35}$$

It is assumed that all transistors are in active region for the above relationships.

CHAPTER 5

PROPOSED 2-STAGE OPERATIONAL AMPLIFIER

5.1 Introduction

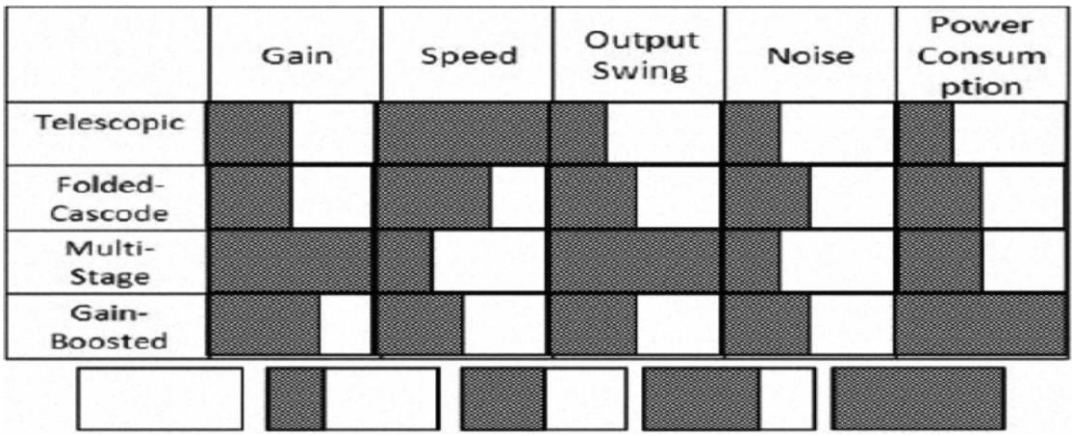
Nowadays, research in analog-circuit design is focused on low-voltage, low-power battery operated equipment. A reduced supply voltage is necessary to decrease power consumption and for the same reason, low-power circuits are also expected to reduce thermal dissipation. Advancements required by International Technology Roadmap for Semiconductors (lTRS), means that with current CMOS standard fabrication processes, circuits must work at supply voltages as low as 1.5 V. Working at lower voltages poses new constraints, especially important for the specific case of analog design. However, a reduction in performance is not desirable. For various recently developed high-performance integrated electronic systems or subsystems, e.g. A/D converter, switched-capacitor filter, RF modulator and audio system, CMOS operational amplifiers with high unity-gain bandwidth and large dynamic range are necessitated.

For high-accuracy circuits, op amps with very high open loop gain and high unity gain frequency are required in order to meet both accuracy and fast settling requirements. Satisfying both of these requirements is difficult with short-channel CMOS processes, since the intrinsic gain of the devices is limited. Thus, going to lower voltages and higher efficiencies require innovative circuits to solve current design needs of faster circuits and better performance. So from previous argument, it is deduced that the designing of op-amps puts new challenges in low power applications with reduced channel length devices.

5.2 Selection of Circuit Topology

In Table II a comparison of performance of various op-amp topologies is represented.

TABLE II: Comparison of Performance of Various Op-Amp Topologies.



As seen from table II, multi-stage op-amps are suitable for high gain, high swing and low noise applications. While as for the multistage topology, especially more than two stages, the stability problem will become severe for us. Large common mode input range is another benefit of two stage op-amps. Considering design specifications a two stage amplifier seems to be good. In a two stage op-amp, the first stage and second stage provides high gain and large swing respectively. In contrast to cascode op-amps, a two stage configuration isolates the gain and swing requirements.

Two stage amplifiers may be used for higher gain analog circuit designs. In general, high gain architectures need complex compensation to stabilize the op amp and generally require more than one compensation capacitor. In papers, various aspects and applications using the cascode connection which consists of the series association of two MOS transistors have been reported. However, most variations are focused on one of the devices working in the active (saturation) region and the other device operating in the triode region.

This chapter discusses the design of a high gain, low power, and general purpose op-amp with the structural simplicity of the classical Widlar architecture. The proposed op amp structure applies composite cascode connections in both the input stage and the second stage to achieve high gain with low power consumption. The op amp employs the traditional two gain stages and buffer stage of nearly unity gain. A larger output voltage swing is then available using composite cascode amplifier stages than with conventional

cascode. As discussed in the former chapter, low power op amp can be designed by operating the MOS transistors in the subthreshold or weak inversion region. While the composite cascode provides high output impedance at a low bias current while setting some devices in the subthreshold region along with the other active region transistors, low power dissipation and high gain can be achieved at the same time.

5.3 The Composite Cascode Connection

The composite cascode connection reduces the bias headroom voltage required for a conventional cascode. The structure of the composite cascode connection is shown in fig. 5.1. Both of the gates of M1 and M2 are driven by the input signal and share a single bias source V_{GG}.

If M2 and M1 have similar W/L aspect ratios, M1 will operate in the triode region while M2 will operate in the active region. In this case the composite cascode works like a common-source stage, but with higher voltage gain. If M2 is chosen with a much higher aspect ratio than M1, with appropriate bias of V_{GG} and I_{bias}, M1 is placed in the strong inversion region while M2 is operating in the weak inversion region. The gain in this case can be further increased. Although the bandwidth is lower than that of the conventional cascode due to the larger capacitance of the weak inversion device M2, this capacitance may be advantageous in the dominant pole compensation of the conventional op amp.

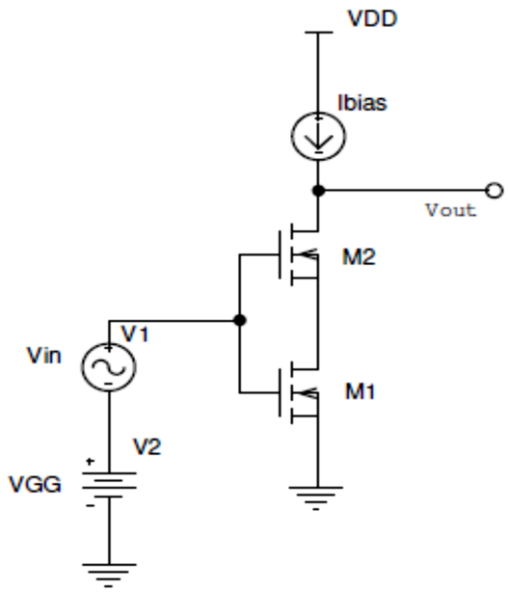


Fig. 5.1: Composite cascode amplifier

Assuming the current source has infinite output impedance, the output resistance is—

$$r_{out} = r_{ds1} + r_{ds2} + (g_{m2} + g_{mb2})r_{ds1}r_{ds2}. \tag{5.1}$$

The voltage gain for the circuit of fig. 5.1 is—

$$A_0 = -[g_{m1}r_{ds1} + g_{m2}r_{ds2} + g_{m1}r_{ds1}(g_{m2} + g_{mb2})r_{ds2}]. \tag{5.2}$$

If the current source load has a finite resistance R instead of the assumed infinite output impedance, the voltage gain then becomes

$$A_0 = -\frac{[g_{m1}r_{ds1} + g_{m2}r_{ds2} + g_{m1}r_{ds1}(g_{m2} + g_{mb2})r_{ds2}]}{1 + \frac{1}{R}[r_{ds1} + r_{ds2} + (g_{m2} + g_{mb2})r_{ds1}r_{ds2}]}. \tag{5.3}$$

5.4 Practical Composite Cascode Circuit

Fig. 5.2 shows a practical composite cascode amplifier stage in which the ideal current source load has been replaced by PMOS devices M3 and M4.

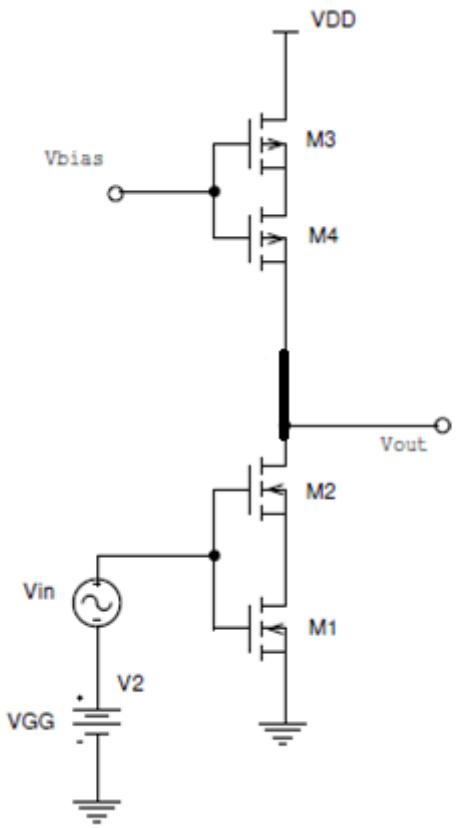


Fig. 5.2: Practical composite cascode stage

Here M4 is chosen to have a larger W/L aspect ratio than M3 similar to the ratio of M2 compared to M1. M4 is operated in the subthreshold region while M3 is in the active region. The output impedance looking into the drain of M4 is given by Eq. (5.1). If the impedance looking into the drain of M4 is equal to the impedance looking into the drain of M2,

$$R = [r_{ds1} + r_{ds2} + (g_{m2} + g_{mb2})r_{ds1}r_{ds2}] \tag{5.4}$$

According to Eq. (5.3), the voltage gain of the composite cascode stage is then

$$A_0 = -\frac{1}{2}[g_{m1}r_{ds1} + g_{m2}r_{ds2} + g_{m1}r_{ds1}(g_{m2} + g_{mb2})r_{ds2}]. \tag{5.5}$$

If M3/M4 are biased in the triode region, the gain would be lower but still greatly above that of the single stage amplifier.

5.5 Circuit Realization

The general purpose BJT op amp has traditionally been designed to have the classical Widlar architecture which consists of a high gain differential input stage, a moderately high gain second stage, and a low gain stage that acts as a buffer. The first two stages are used to provide overall voltage gain high enough for the op amps. MOS op amps are ideally suited for low power application. The classic Widlar op amp architecture, originally developed and widely used for bipolar devices, has been mimicked in CMOS devices. But it requires modification for use with CMOS devices. This is due to the inherently lower transconductance of CMOS devices as well as the gain reduction due to short channel effects that come into play for submicron CMOS processes.

The benefit of higher cutoff frequency due to smaller channel length is not needed for the first stage in pole splitting compensation methods. Relatively longer channel length devices can be used there. The use of longer channel devices also leads to higher voltage gains because of reduced channel length modulation effects and higher output resistance. Additionally, The larger gate areas of the input devices will also reduce the threshold voltage and transconductance mismatch.

5.5.1 Input Differential Composite Cascode Stage

As shown in fig. 5.3, the first stage is the differential-to-single ended practical composite cascode stage biased with tail current.

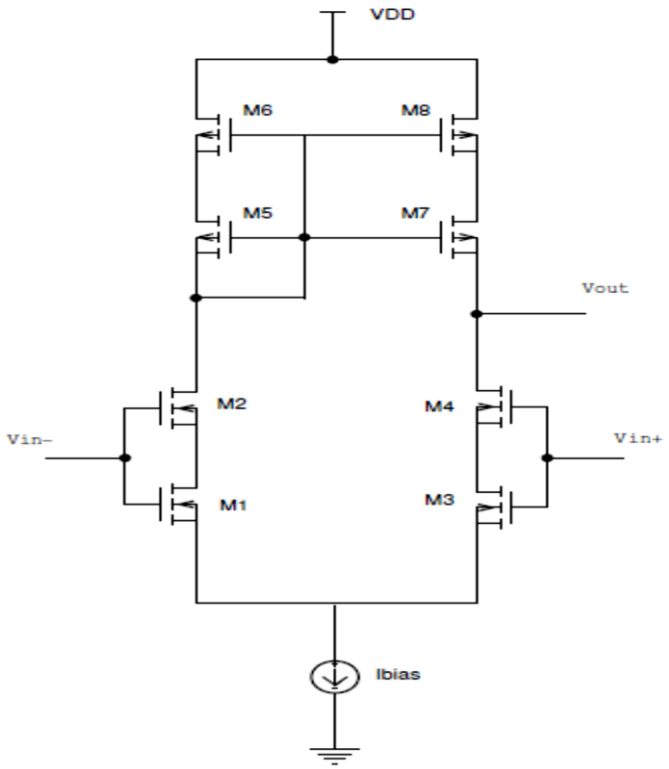


Fig. 5.3: Op amp input differential composite cascode stage

The composite cascode connection in both N-channel and P-channel allows the input to swing from the positive power supply to the negative power supply. The gain in the weak inversion region is relatively independent of drain current. In the composite cascode configuration, the output transistor is selected to have a much higher W/L aspect ratio than that of the lower transistor. This allows a simple adjustment of the tail current to place the drain connected device M2 in the weak inversion region while the source connected device M1 operates in the strong inversion region.

5.5.2 Composite Cascode Current Mirror

The current mirror used to provide the bias current to the input stage and the bias voltage to the second stage is shown in fig. 5.4.

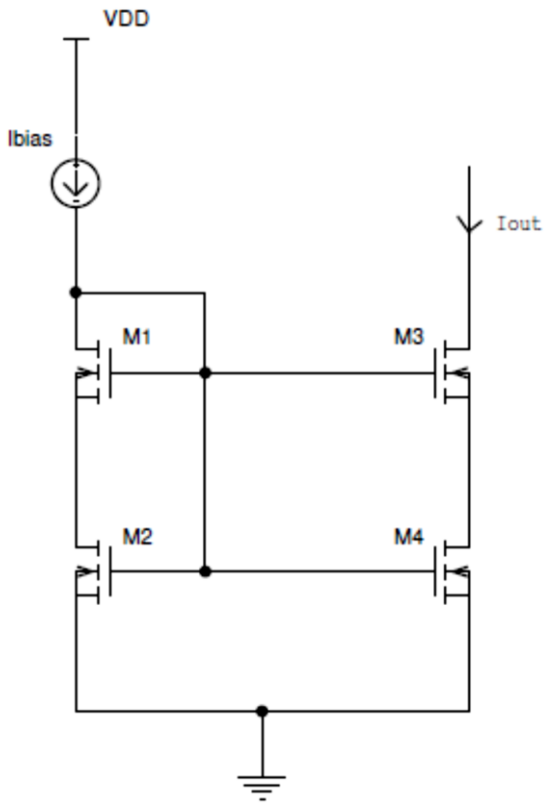


Fig. 5.4: Op amp composite cascode current mirror

The bias current for the input differential stage is only 3 μA. This N type current mirror is also connected in the composite cascode structure in order to provide the robust bias current and voltage which can self adjust by tracking of the corresponding variation of the other composite cascode stages.

5.5.3 Second Composite Cascode Stage

The second stage is a common source stage implemented as a composite cascode shown in fig. 5.5.

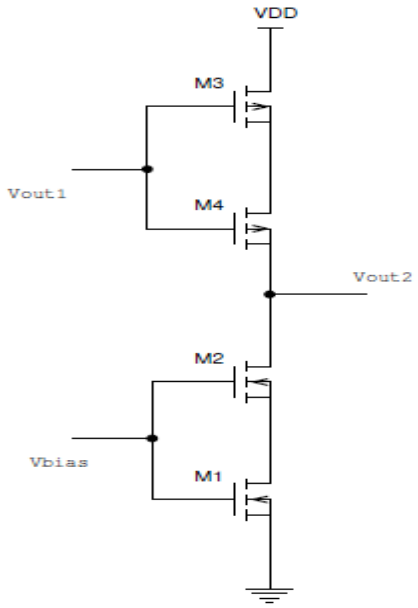


Fig. 5.5: Op amp second composite cascode stage

5.5.4 Current Buffer

This current buffer compensation technique [17] is based on removing the feed forward path from the output of first stage to the output of operational amplifier. Schematic for two stage operational amplifier with compensation block is shown in figure 4.8. Where, CB is compensation block. In this technique Compensation block is current buffer as shown in fig. 5.6.

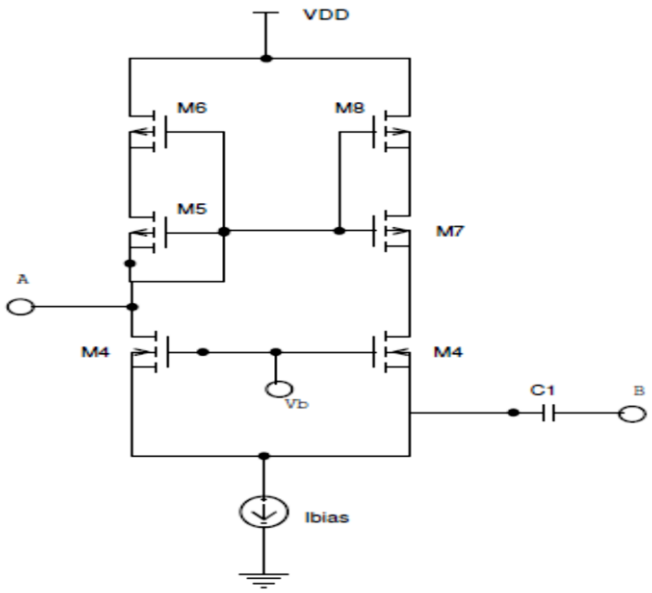


Fig. 5.6: Current buffer

5.5.5 Schematic of CMOS Operational Amplifier

Fig. 5.7 shows the overall schematic of a CMOS operational amplifier using composite cascode stages, with two gain stages followed by a buffer output stage as presented earlier, which implements the classical Widlar op amp structure. In entire operational amplifier design there is no use of any extra bias voltage or current supplies. The only bias circuit is built inside the op amp chip which is used to allow self adjustment.

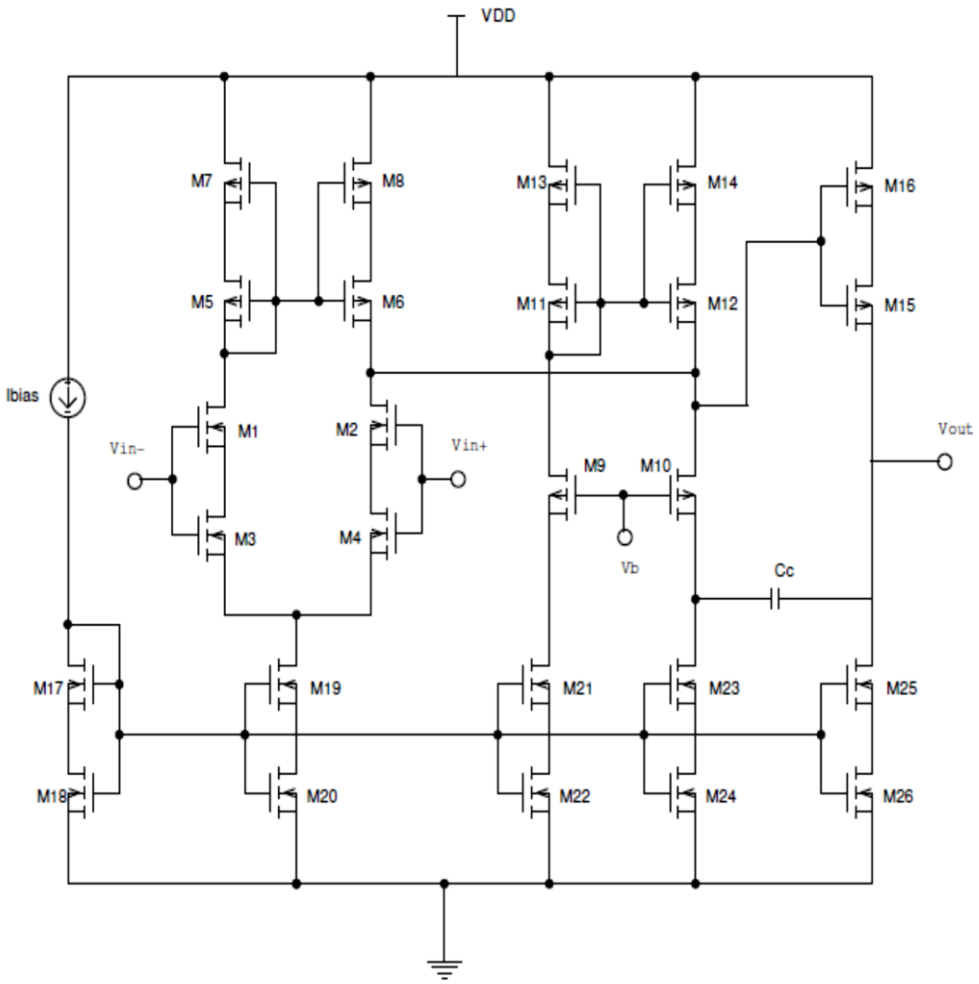


Fig.5.7: Schematic of two stage operational amplifier

Table III: Operational Amplifier Devices Sizes

Devices	Width (μm)/Length (μm)
M1,M2	50/1
M3,M4	2/2
M5,M6	120/1
M7,M8	5/1
M9,M10	21/1
M11,M12	44/1.2
M13,M14	2/1
M15	100/1
M16	5/1
M17,M19	80/1
M18,M20	5/1.5
M21,M23	48/1
M22,M24	6/1.5
M25	43/1
M26	2/2
C_C	0.5pF
C_L	1pF
I_{Bias}	3μA

CHAPTER 6

SIMULATION RESULTS

The amplifier is powered from a 1.8 volts power supply. The different bias voltages which are required by op amp circuit are produced by bias circuit. Based on the proposed compensation technique a CMOS op amp has been designed and simulated in a standard 0.18 μm CMOS technology. The power consumption is 54.2 microwatt.

6.1 AC Response

In fig. 6.1, one method of measuring the AC performance is presented.

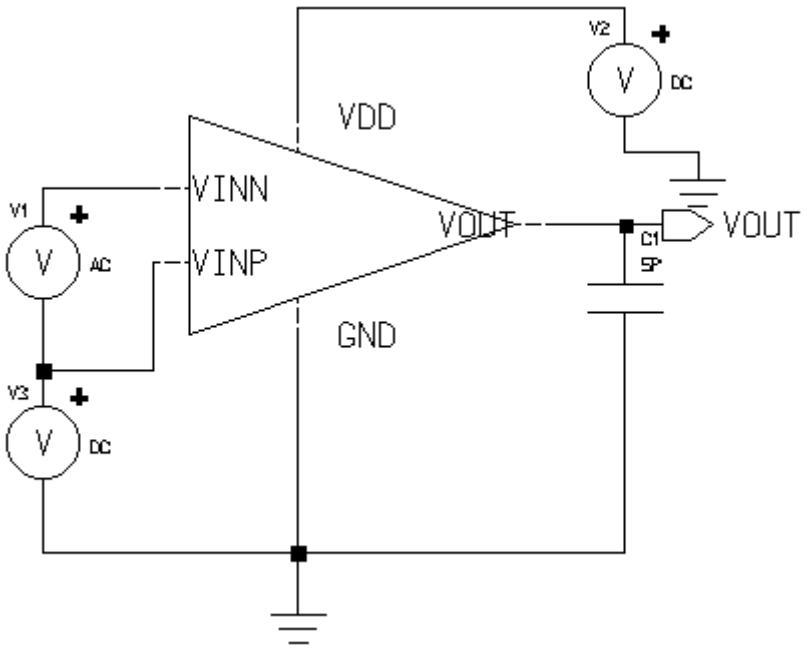


Fig. 6.1: Configuration for simulating the open loop frequency response of op amp.

In this configuration, the amplifier is open loop, and the small AC signal is applied at the input. DC input is used to bias the transistors.

In fig 6.2, a Bode and phase plot for 1.8V, 27°C is shown. As can be seen, the open loop gain is 95.2 dB, and a phase margin is 64.6 degree.

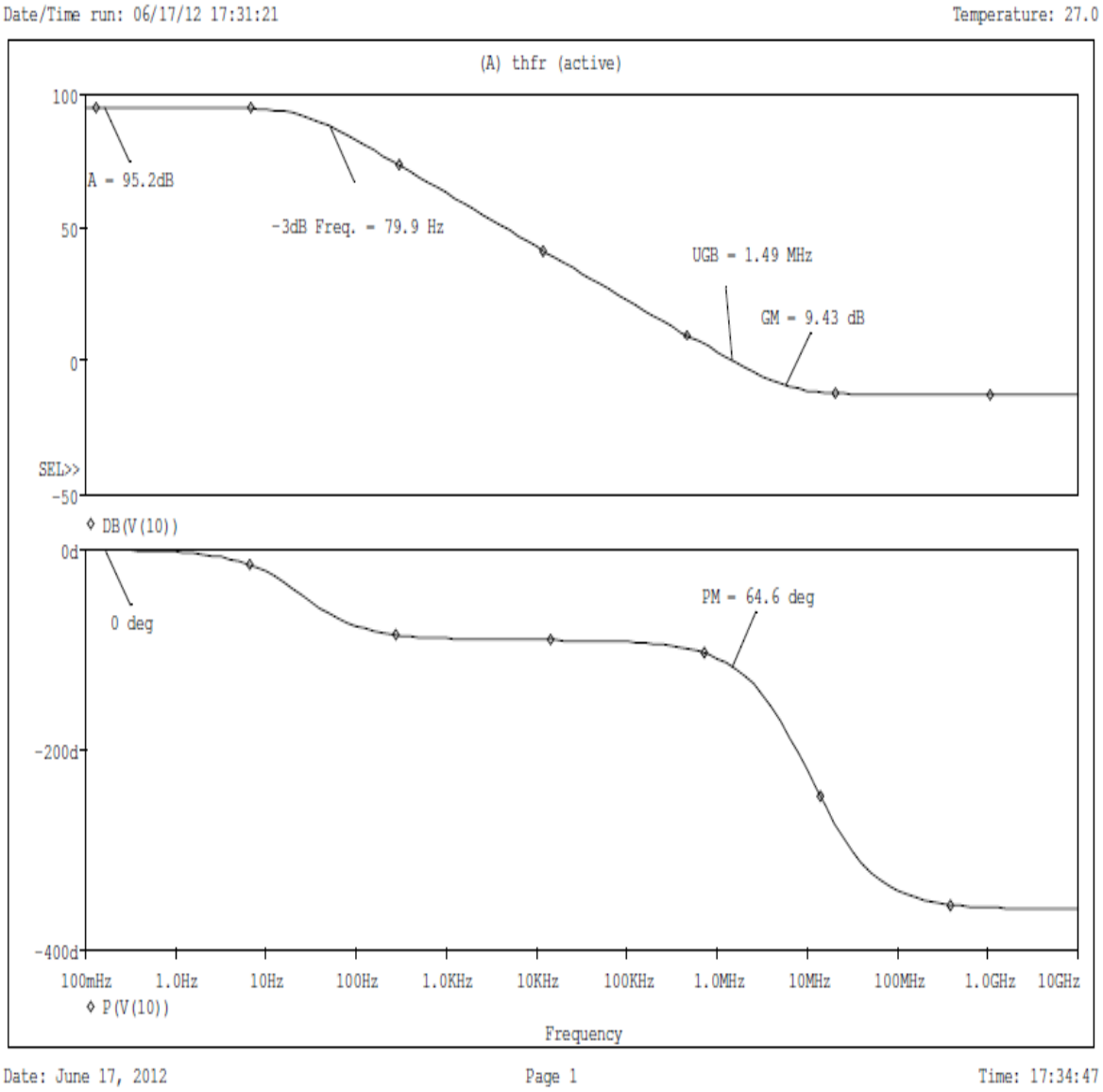


Fig. 6.2: Frequency response of op amp.

6.2 Transient Results

A transient simulation of the amplifier in open loop gain configuration with the sinusoidal signal at the input with a 1 volt dc bias.

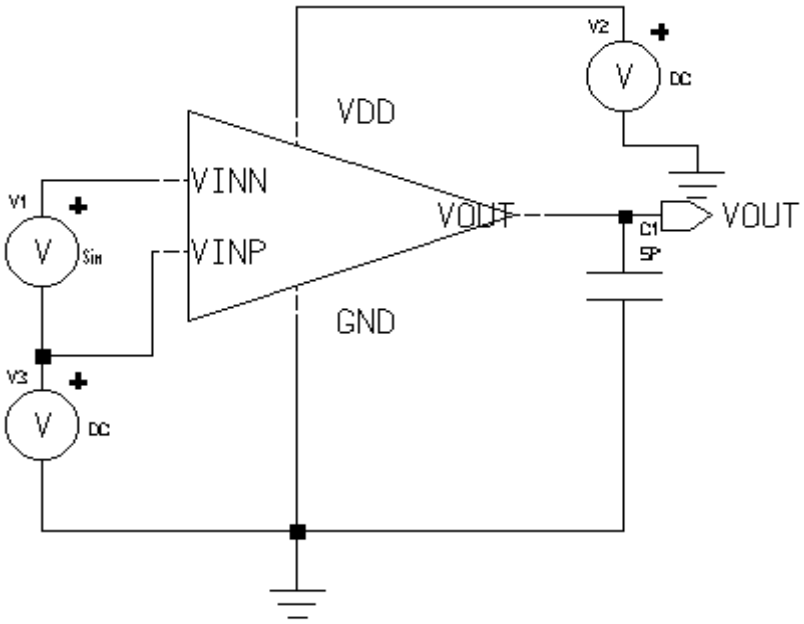


Fig. 6.3: Schematic for the simulation of the transient response.

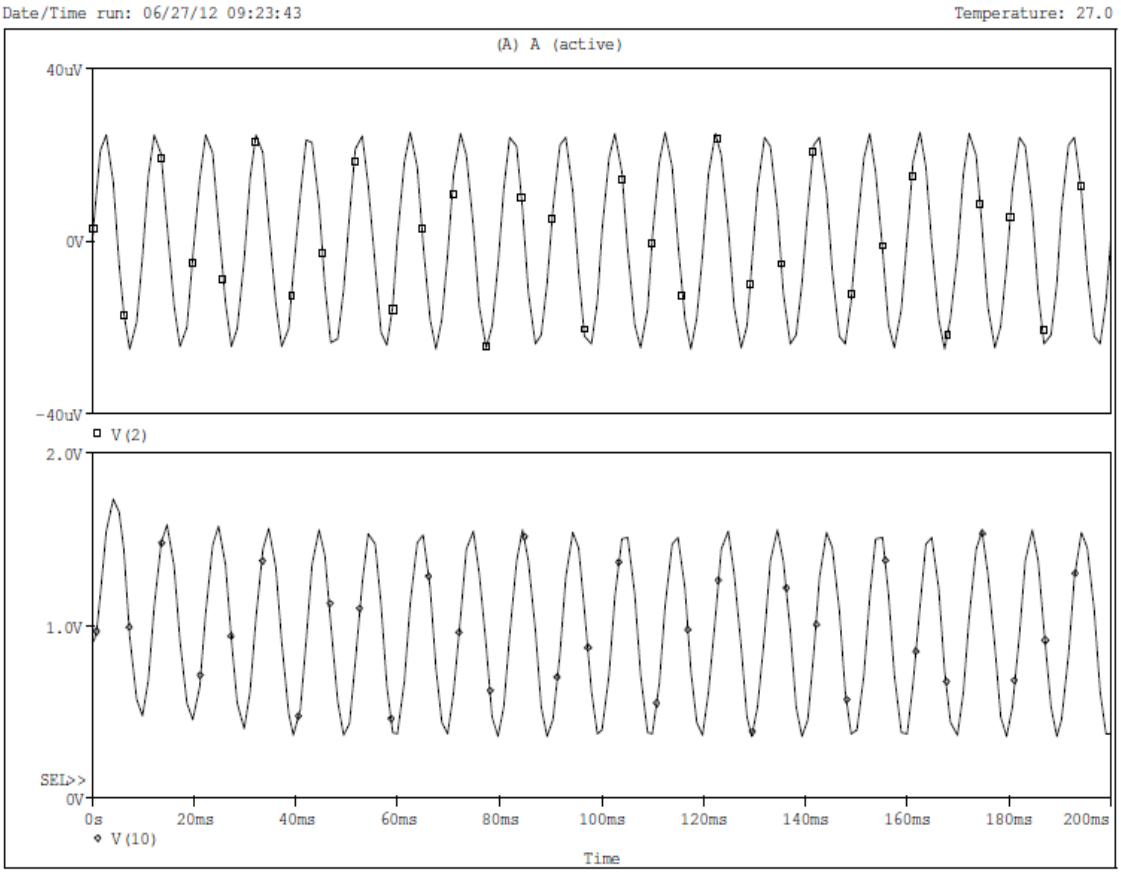


Fig. 6.4: Output and input signals for transient analysis without unity feedback

6.3 Step Response

In fig. 6.5, a step from ground to VDD is applied at the input with unity feedback configuration. As was measured, the amplifier's slew rate is 11.9 V/µs for the rising edge and 8.3 V/µs for the falling edge as shown in fig. 6.6.

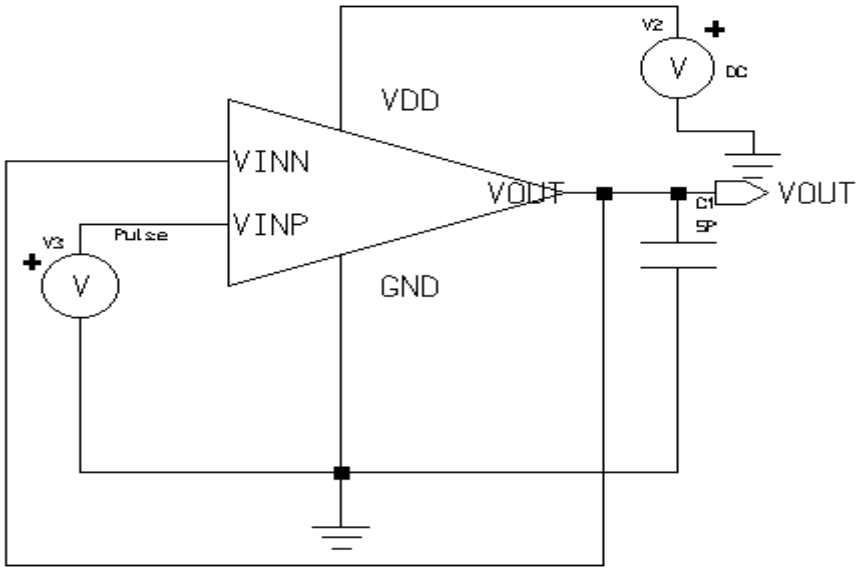


Fig. 6.5: Schematic for the simulation and measurement of the slew rate.

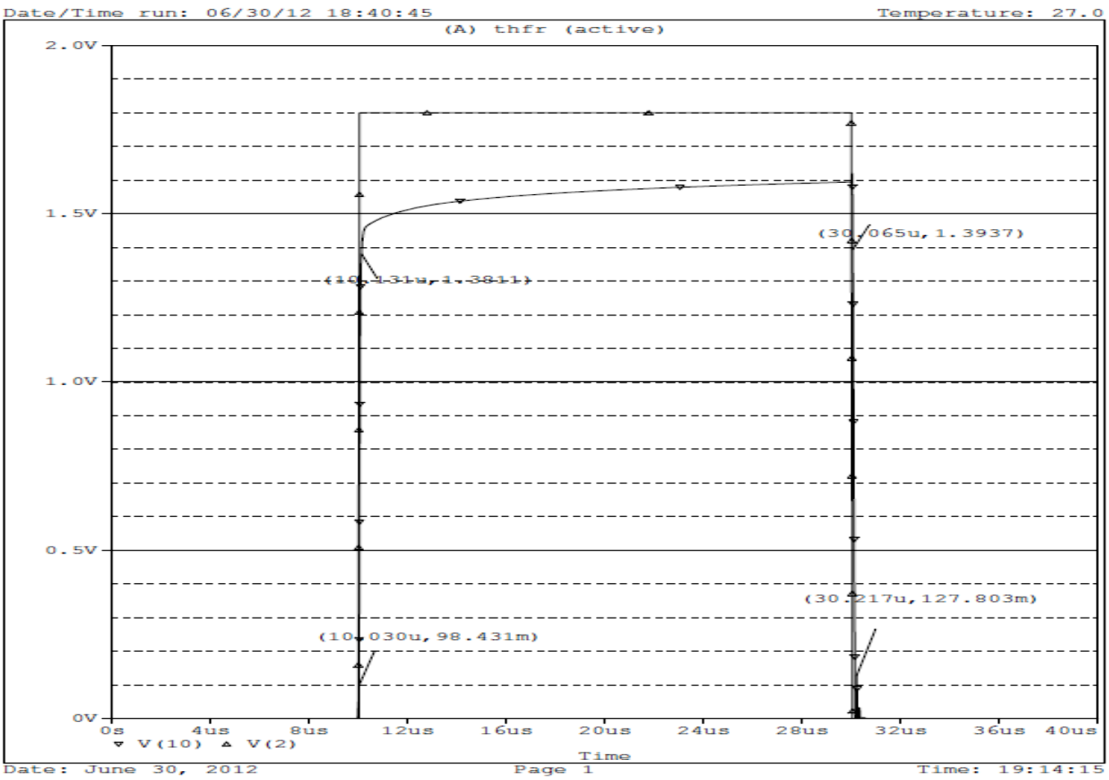


Fig. 6.6: Slew Rate for the rising and falling edge with unity gain configuration

The positive slew rate is the slope of the rising edge of the output. This is computed from the two points on the rising edge. That is,

$$SR^{+} = \frac{1.301V - .0984V}{10.131\mu s - 10.030\mu s}$$

$$SR^{+} = 11.9\ V/\mu s$$

Similarly, the new slew rate is computed as follows:

$$SR^{-} = \frac{0.127V - 1.393V}{30.217\mu s - 30.065\mu s}$$

$$SR^{-} = 8.3\ V/\mu s$$

6.4 Common Mode Rejection Ratio

In order to simulate common mode rejection, first we find the common mode gain .For common mode gain the same ac signal is applied with 1V dc bias at both the terminal. The magnitude of ac source is 1 volt. When the simulator sweeps the frequency, there will be a 1V AC source on both the positive and negative inputs and hence the AC signal at the output will be the common mode gain. The previously calculated gain (from fig. 6.2) can be divided by this gain to give the CMRR. The common mode rejection ratio was found to be 99.1 dB at low frequency.

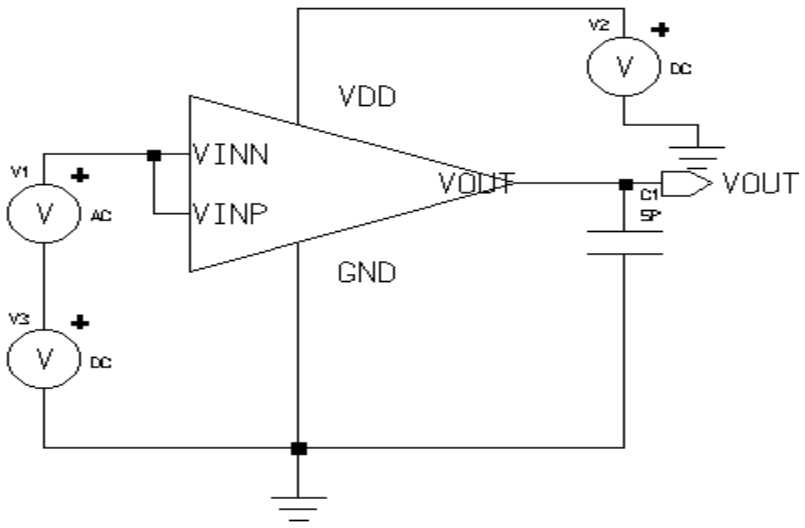


Fig. 6.7: Schematic for the simulation of common mode gain and CMRR

The common-mode input range is determined when the output cease to follow the input linearly. At the low end, it determines V_{G1}(min) = -1.23V, and at the high end, it determines V_{G1}(max) = 0.86V. These are much closed to the corresponding design specifications.

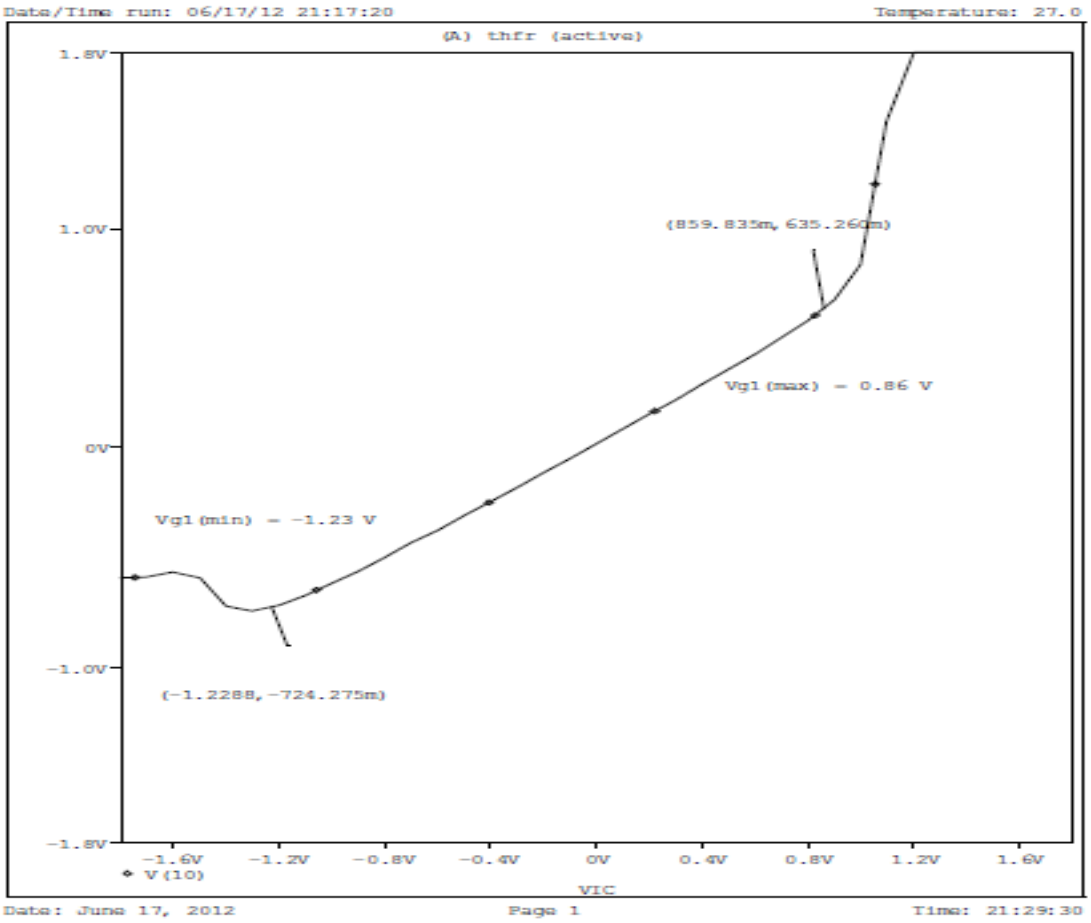


Fig.6.8 Common mode rejection ratio CMRR

The common-mode gain is obtained by locating two points as far apart in the linear range about the operating point. This is shown in the graph above, and computed as follows:

$$A_{CM} = \frac{0.635 - (-0.724)}{0.859 - (-1.23)}$$

$$A_{CM} = 0.651$$

$$\text{CMRR} = \frac{A_{VD}}{A_{CM}} = \frac{57544}{0.651} = 88393.2$$

$$\text{CMRR} = 99.1 \text{ dB}$$

6.5 Power Supply Rejection Ratio

PSRR was measured by placing a 1V AC signal on the power supply where the amplifier is in unity gain feedback configuration. PSRR is equal to the ratio of the AC signal at the output node to the AC signal on V_{DD}. The PSSR obtained is 148.2db, from fig. 6.10.

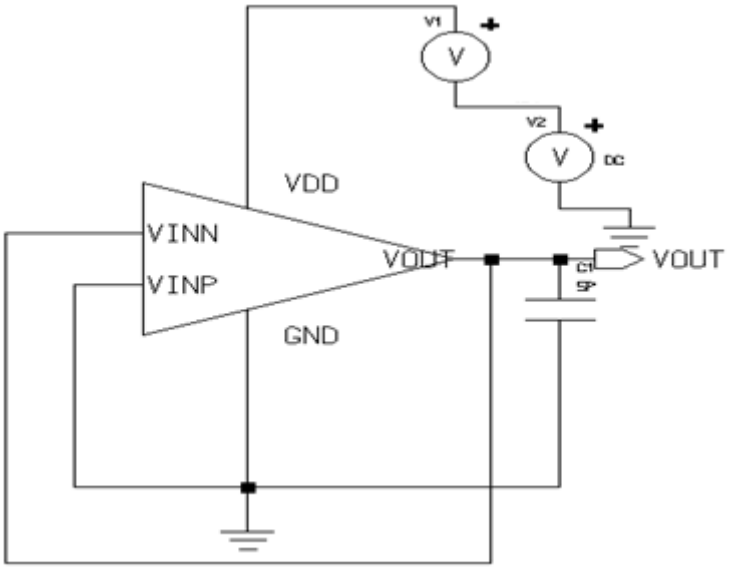


Fig. 6.9: Schematic for the simulation of PSRR

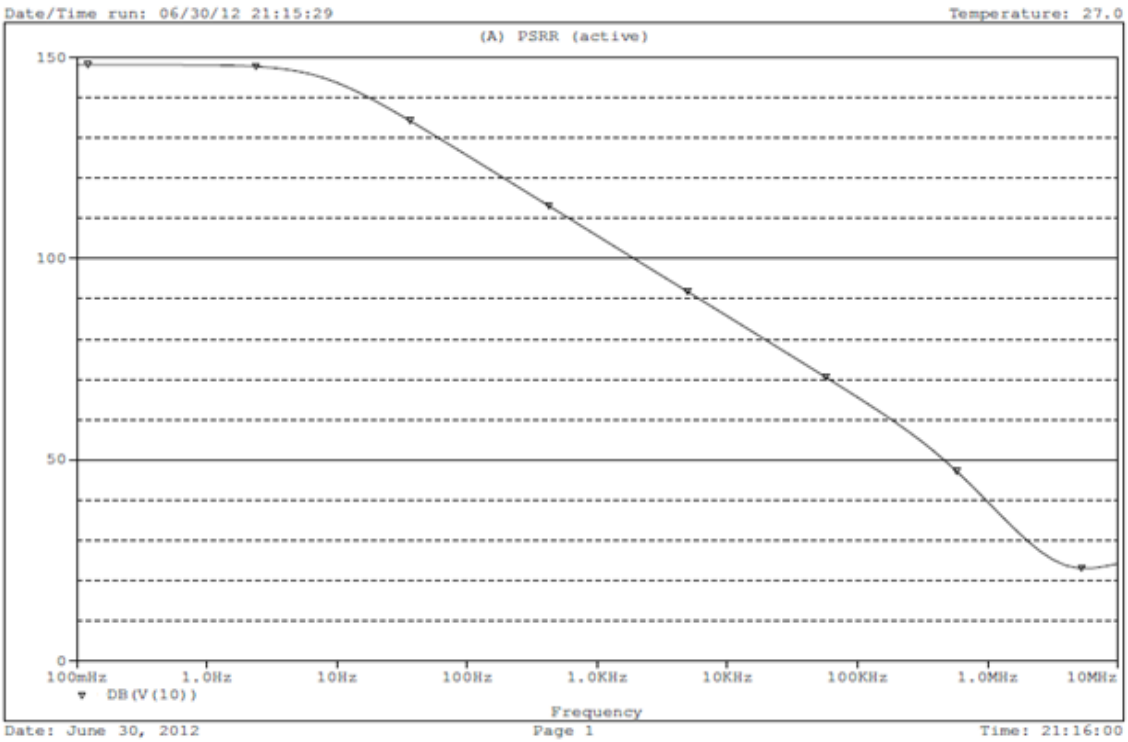


Fig. 6.10: Power supply rejection ratio

6.6 Input Output Characteristics Using Unity Gain Configuration

For linearity test op amp is biased in the unity gain follower configuration as shown in fig. 6.11. Now input dc voltage is varied from 0 volt to 1.8 volt. Now the input and output is compared. The op amp is linear for input for which output match with input.

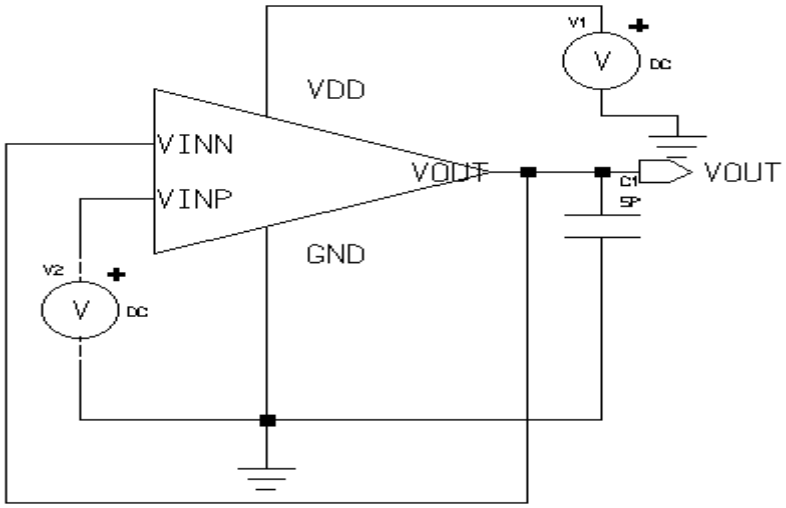


Fig. 6.11: Schematic for the simulation of input common-mode range

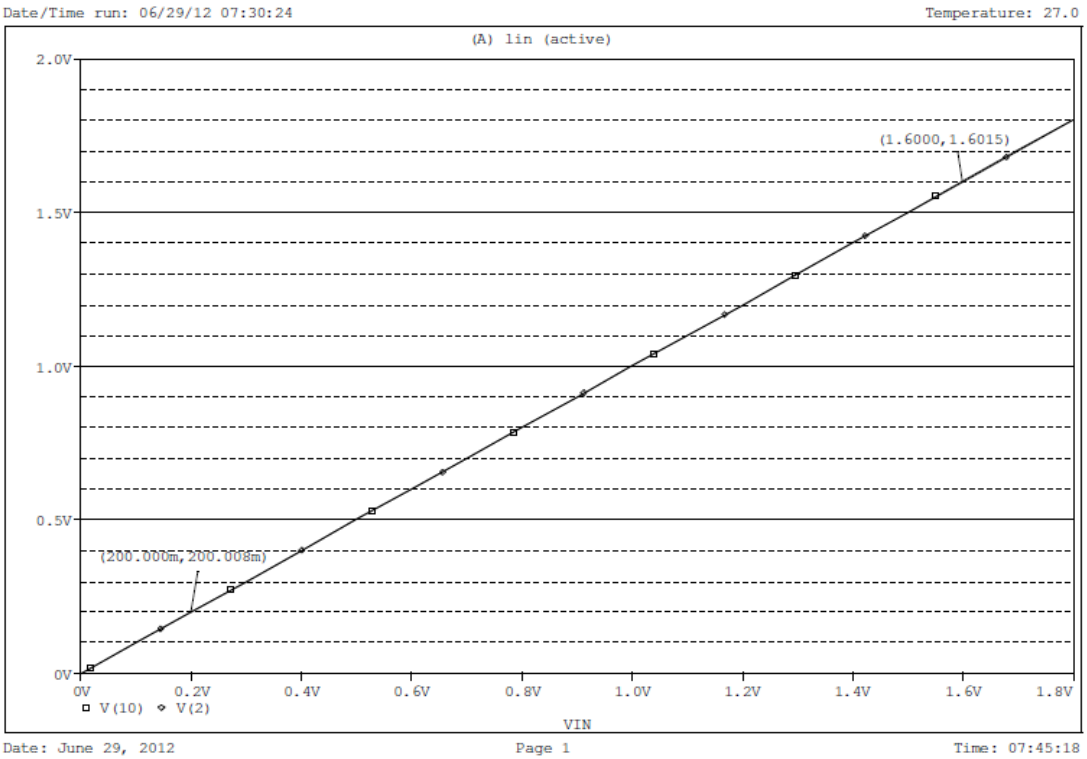


Fig. 6.12: Simulation result of input common-mode range (Linearity test)

6.7 Variation of Frequency Response with Load Capacitance

Fig. 6.13-6.15 shows the effect of variation of load capacitance (1pF, 5pF, 10pF) on the frequency response of the op amp.

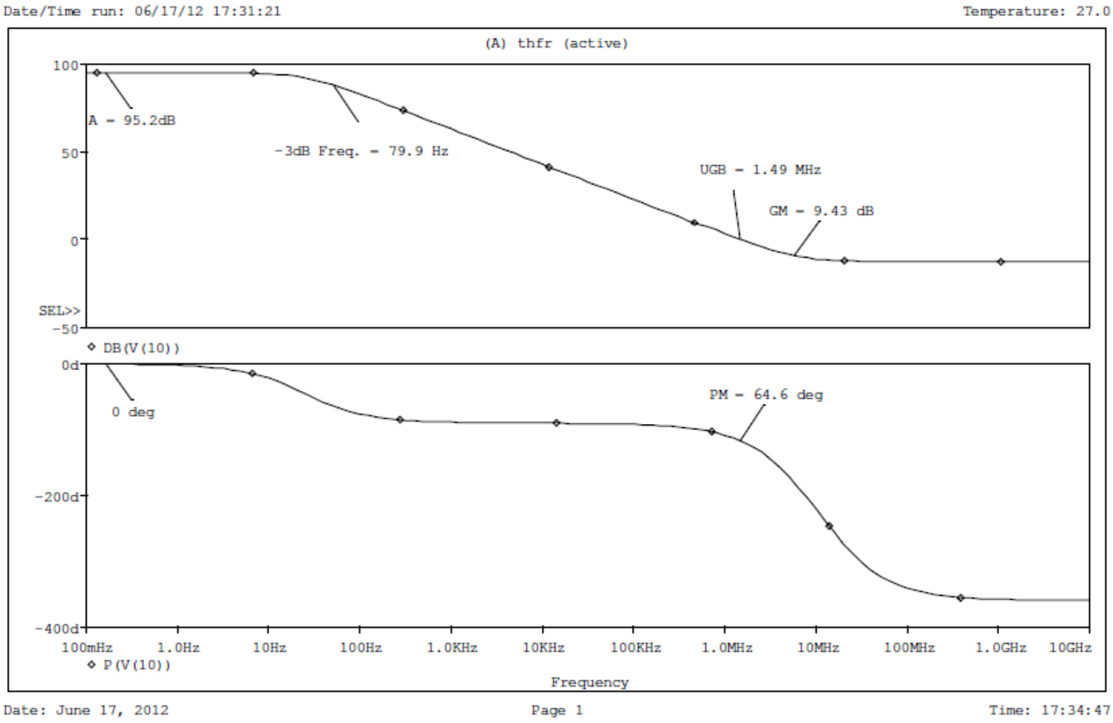


Fig. 6.13: Frequency response at load capacitance 1pF

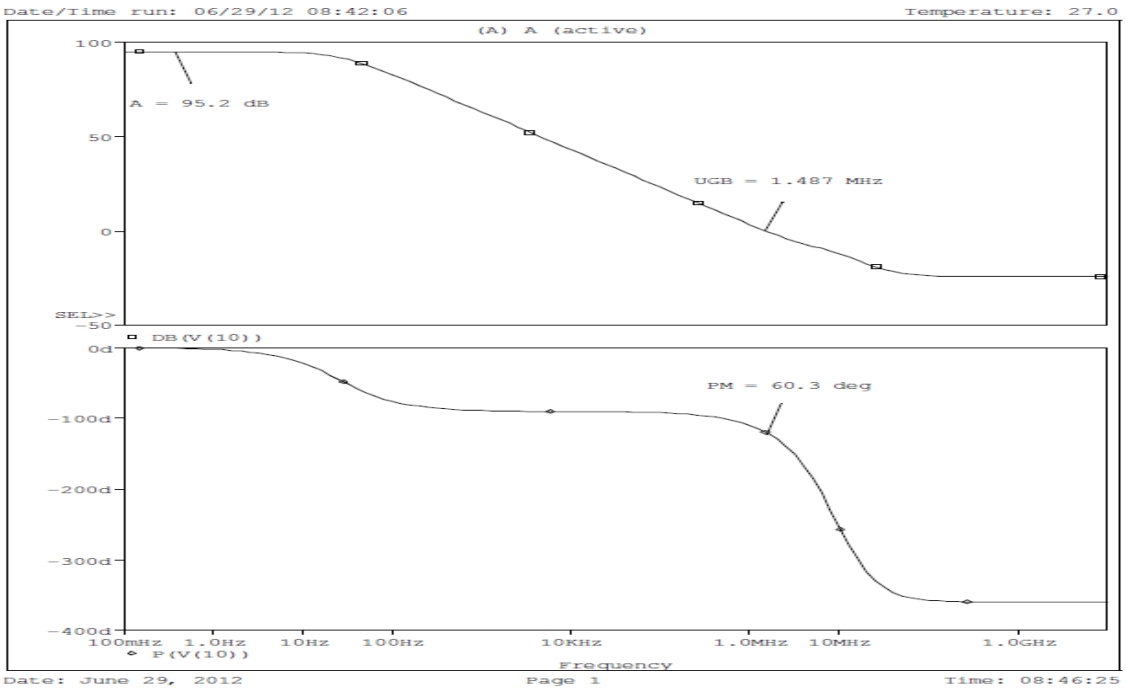


Fig. 6.14: Frequency response at load capacitance 5pF

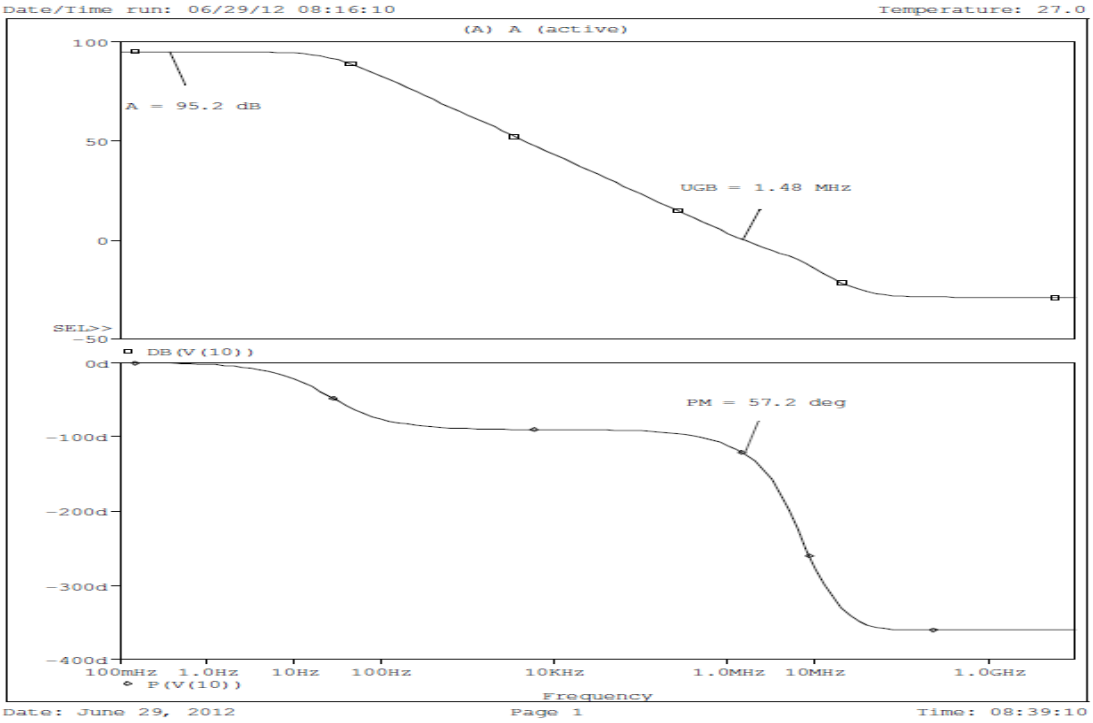


Fig. 6.15: Frequency response at load capacitance 10pF

Table IV: Variation of parameters with the Load Capacitance (C_L)

Load capacitance (C_L) (pf)	Unity gain Bandwidth (MHz)	Phase Margin (degree)
1	1.491	64.6
5	1.487	60.3
10	1.480	57.2

Table IV shows there is not very much variation on the UGB and phase margin with the variation in the load capacitance (C_L) similar is the case with the slew rate it does not change significantly with the variation in load capacitance. But these three parameters changes significantly with compensation capacitance (Cc).

6.8 Effect of Variation of Compensation Capacitance (*Cc*)

Figures given below show the effect variation of *Cc* on the frequency response.

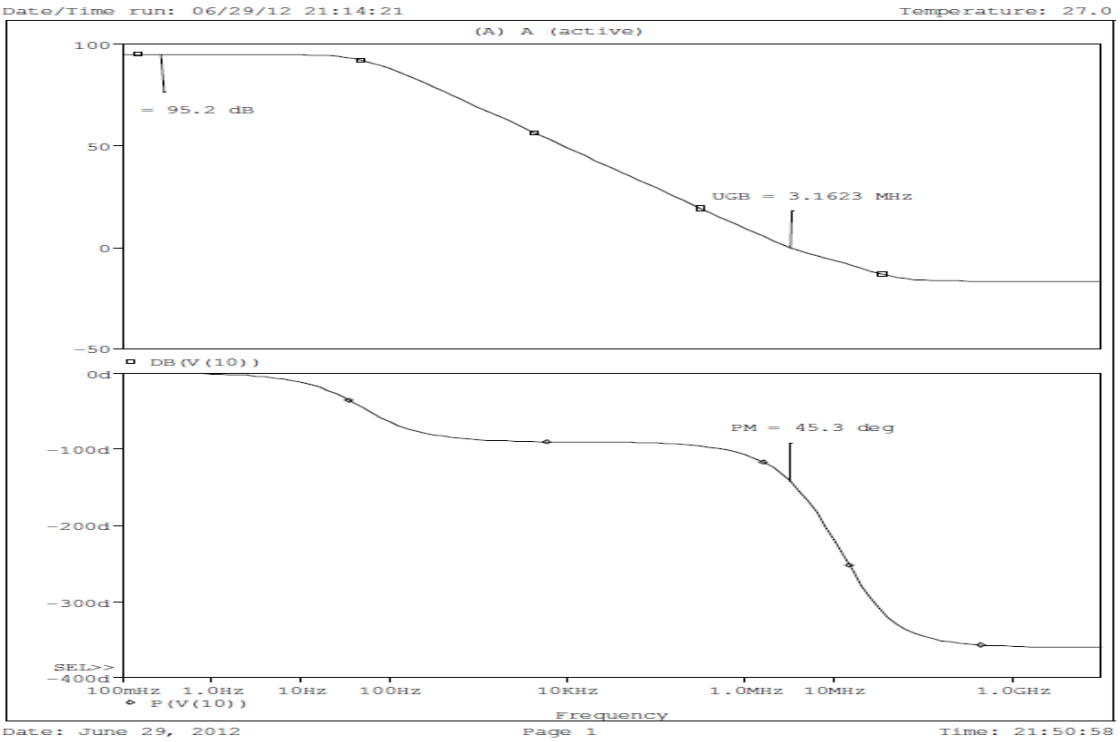


Fig. 6.16: Frequency response variation with Cc =0.1pF

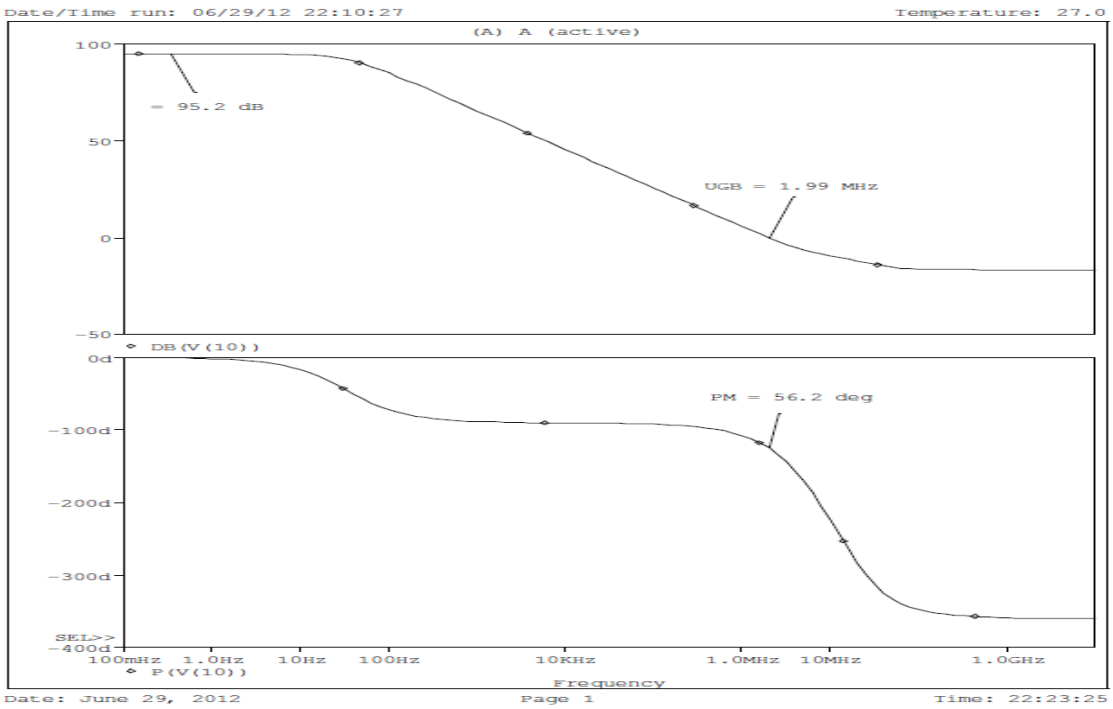


Fig. 6.17: Frequency response variation with Cc =0.25pF.

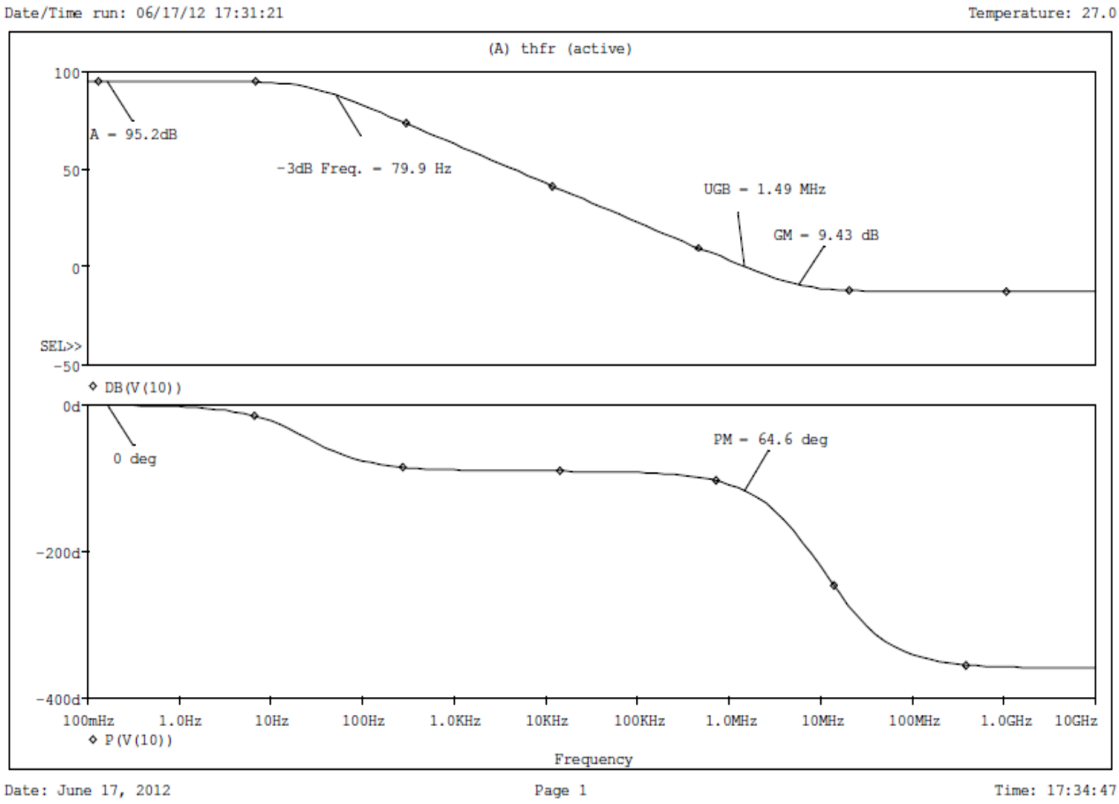


Fig. 6.18: Frequency response variation with Cc = 0.5pF

Table V: Variation of parameters the compensation capacitance (*Cc*)

Compensation Capacitor Cc (pF)	Unity Gain Bandwidth (MHz)	Phase Margin (degree)
0.1	3.16	45.3
0.25	1.99	56.2
0.5	1.49	64.6

Table V shows the unity gain bandwidth and phase margin changes with compensation capacitance.

TABLE VI: COMPARISON WITH PREVIOUS RESEARCH WORK RESULTS

PARAMETERS	UNITS	2005 [9]	2000 [10]	2000 [11]	2008 [12]	THIS WORK
SUPPLY	V	3	1	1.5	3.5	1.8
A_O	Db	55.56	70	65	65	95.2
UGB	MHz	0.17	0.19	0.23	NA	1.49
-3Db	Hz	164	45	60	127	79
PHASE MARGIN	Deg.	NA	60	62	61.5	64.6
POWER DISSIPATION	µW	66	5	5.16	104	54.2
SR^+	V/µs	0.05	0.15	0.18	0.41	11.9
SR^-	NA	NA	NA	NA	NA	8.3
CMRR	dB	85	NA	NA	92.5	99.1
PSRR	dB	NA	90	NA	80	148.2
C_L	pF	NA	7	9	10	1
C_C	pF	NA	4	2	150	0.5

CHAPTER 7

CONCLUSION AND FUTURE RESEARCH

7.1 Conclusion

In this thesis a feasible configuration of a high gain low power op-amp using Widlar architecture is proposed. This op amp uses composite cascode connections for the differential input, a common source second stage, and a current buffer. By selecting the appropriate current and choosing the W/L aspect ratios of transistors wisely, some MOS devices operate in subthreshold range while the remainder works in the active range. With the high output impedance and the low current of the composite cascode connections, a high gain stage is possible with small chip area and power dissipation. This high impedance load also leads to flexible and simple compensation schemes. The proposed op-amp shows a favorable slew rate and GBW product compared to other amplifiers driving large capacitive loads. This design is intended for applications where simplicity of layout, small cell size, and low power are important.

In present work current buffer compensation technique is used which reduces the value of compensation capacitor and improves bandwidth, phase margin CMRR, slew rate but PSRR decreases. As the compensation capacitor play an important role for power consumption and noise parameters. The power consumption decreases with the compensation capacitor value, current buffer approach has been used which is less sensitive to process variations.

The operational amplifier has been designed and simulated using PSPICE simulator in 0.18µm, Level 7, CMOS process technology parameter with a supply voltage of 1.8V. The operational amplifier achieves dc gain 95.2 dB, unity gain bandwidth 1.49 MHz, phase margin 64.6°. Also the power consumption, PSRR, and CMRR of the operational amplifier are obtained as 54.2µW, 148.2 dB, and 99.1 dB respectively.

7.2 Future Research

In this work, one can observe that negative slew rate is not equal to positive slew rate and negative slew rate is smaller than positive slew rate. Condition for negative slew

rate is that $I_1=I_2$ even after applying this condition negative slew rate is not equal to positive slew rate. Thus, this is one main problem or area of improvement.

The input offset bias current errors and the common mode rejection ratio is strongly dependent on the matching accuracy of the current mirrors. This random offset can be minimized by matching the current mirrors by careful layout techniques like common centroid method and unit cell layout techniques.

The design has a unity bandwidth greater than 1.48MHz. This can be further improved using the bandwidth enhancement techniques. These techniques are resistor series peaking, inductor series peaking and current feedback. One may also use their combinations too.

BIBLIOGRAPHY

[1] S. Sen and B. Leung: A class-AB high-speed low-power operational Amplifier in BiCMOS technology. IEEE J. Solid-State, vol. 31, no. 9, Sept. 1996, pp. 1325-1330.

[2] L. Bouzerara, M. T. Belaroussi: High gain and low-power load compensated cascode OTA using feed-forward technique with frequency-dependent Current Mirrors. In: Proc. International Symposium on Signals, Circuits and Systems (SCS2001), Iasi, Romania, July 2001, pp. 93-96.

[3] F. Op't Eynde and W.Sansen: Design and optimization of CMOS wideband amplifiers. In: Proc. IEEE 1989 Custom Integrated Circuits Conference, pp. 25.7.1-25.7.4.

[4] Y. Taur, "Cmos Design Near the Limit of Scaling," IBM Journal of Research and Development, vol. 46, no. 2/3, March/May 2002, pp. 213–222.

[5] L. Li, "High Gain Low Power Operational Amplifier Design and Compensation Techniques," Phd thesis, Brigham Young University, April 2007.

[6] Sarbishaei, H.; Kahookar Toosi, T.; Zhian Tabasy, E.; Lotfi, R. "A high-gain high speed low-power class AB operational amplifier", IEEE Conference 2005, Pages: 271- 274 Vol. 1.

[7] hiyuan Li; Jianguo Ma; Mingyan Yu; Yizheng Ye "Low noise operational amplifier design with current driving bulk in 0.25μm CMOS technology", IEEE Conference 2005 , Pages: 630 – 634.

[8] Vincence, V.C.; Galup-Montoro, C.; Schneider, M.C., "Low-voltage class AB operational amplifier", IEEE Conference 2001, Page(s): 207 – 211.

[9] R. G. Eschauzier, R. Hogervorst, and J. H. Huijsing, "A programmable 1.5V CMOS class-ab operational amplifier with hybrid nested miller compensation," IEEE J. Solid-State Circuits, vol. 29, no. 12, pp. 1497–1504, Dec. 1994.

[10] G. N. Lu and G. Sou, “A CMOS op amp using a regulated-cascode trans-impedance building block for high-gain, low-voltage achievement,” Proc. of IEEE International Symposium on Circuits and Systems, vol. 1, pp. 9–12, June 2007.

[11] D. J. Comer and D. T. Comer, “Using the weak inversion region to optimize input stage design of CMOS op amps,” Circuits and Systems II: Express Briefs, vol. 51, no. 1, pp. 8–14, Jan. 2004.

[12] P. R. Gray and R. G. Meyer, “Analysis and Design of Analog Integrated Circuits,” 4th edition, John Wiley & Sons, 2001.

[13] B. Razavi, “Design of Analog CMOS Integrated Circuits,” Tata McGraw-Hill, 2002.

[14] P. Gray, P. Hurst, S. Lewis, and R. Meyer, Network analysis and feedback amplifier design. New York: D. Van Nostrand Company Inc., 1949.

[15] D. J. Comer and D. T. Comer, Fundamentals of electronic circuit design. New York: John Wiley & Sons Inc., 2003.

[16] P. E. Allen and D. R. Holberg, CMOS Analog Circuit Design, 2nd Ed. NewYork: Oxford University Press, 2002.

[17] R. G. H. Eschauzier and J. H. Huijsing, “Frequency Compensation Techniques for Low-Power Operational Amplifiers,” Boston: Kluwer, 1995.

[18] B. Razavi, “Design of Analog CMOS Integrated Circuits,” Tata McGraw-Hill, 2002.

[19] K. N. Leung and P. Mok, “Analysis of multistage amplifier-frequency compensation,” IEEE Transactions on Circuits and Systems, vol. 48, no. 9, Sep. 2001, pp. 1041–1056.

[20] H.-T. Ng, R. Ziazadeh, and D. Allstot, “A multistage amplifier technique withembedded frequency compensation,” IEEE J. Solid-State Circuits, vol. 34, no. 3, Mar. 1999, pp. 339–347.

[21] P. Gray, P. Hurst, S. Lewis, and R. Meyer, Network analysis and feedback amplifier design. New York: D. Van Nostrand Company Inc., 1949.

[22] K.-J. de Langen, R. Eschauzier, G. van Dijk, and J. Huijsing, “A 1-ghz bipolar class-ab operational amplifier with multipath nested miller compensation for 76-db gain,” IEEE J. Solid-State Circuits, vol. 32, no. 4, Apr. 1997, pp. 488–498.

[23] F. You, S. Embabi, and E. Sanchez-Sinencio, “Multistage amplifier topologies with nested gm-c compensation,” IEEE J. Solid-State Circuits, vol. 32, no. 12, Dec. 1997, pp. 2000–2011.

[24] G. Palmisano, G. Palumbo, and S. Pennisi, “Design Procedure for Two Stage CMOS Transconductance Amplifier: A Tutorial,” in *Analog Integrated Circuit and Signal Processing. Norwell, MA: Kluwer, vol. 27, pp. 179–189, 2001*

[25] G. Palmisano and G. Palumbo., “A Compensation Strategy for Two-Stage CMOS Op-Amps Based on Current Buffer.” IEEE Trans. on Circuits and Systems (part I) 44(3), pp. 257–262, Mar. 1997.

[26] Rajput, S.S.; Jamuar, S.S., “Low voltage, low power, high performance current mirror for portable analogue and mixed mode applications”, IET Journal 2001, Page(s): 273 – 278.

APPENDIX

Simulations have been performed using PSpice at 180nm technology and the model files provided by MOSIS (AGILENT) used have the following parameters:

```
.MODEL NMOS NMOS (                                LEVEL   = 7
+ TNOM    = 27             TOX     = 4.1E-9
+XJ       = 1E-7           NCH     = 2.3549E17      VTH0    = 0.3750766
+K1       = 0.5842025      K2      = 1.245202E-3    K3      = 1E-3
+K3B      = 0.0295587      W0      = 1E-7           NLX     = 1.597846E-7
+DVT0W    = 0              DVT1W   = 0              DVT2W   = 0
+DVT0     = 1.3022984      DVT1    = 0.4021873      DVT2    = 7.631374E-3
+U0       = 296.8451012    UA      = -1.179955E-9   UB      = 2.32616E-18
+UC       = 7.593301E-11   VSAT    = 1.747147E5     A0      = 2
+AGS      = 0.452647       B0      = 5.506962E-8    B1      = 2.640458E-6
+KETA     = -6.860244E-3   A1      = 7.885522E-4    A2      = 0.3119338
+RDSW     = 105            PRWG    = 0.4826         PRWB    = -0.2
+WR       = 1              WINT    = 4.410779E-9    LINT    = 2.045919E-8
+XL       = 0              XW      = -1E-8          DWG     = -2.610453E-
9
+DWB      = -4.344942E-9   VOFF    = -0.0948017     NFACTOR = 2.1860065
+CIT      = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB    = 0              ETA0    = 1.991317E-3    ETAB    = 6.028975E-5
+DSUB     = 0.0217897      PCLM    = 1.7062594      PDIBLC1 = 0.2320546
+PDIBLC2  = 1.670588E-3    PDIBLCB = -0.1           DROUT   = 0.8388608
+PSCBE1   = 1.904263E10    PSCBE2  = 1.546939E-8    PVAG    = 0
+DELTA    = 0.01           RSH     = 7.1            MOBMOD  = 1
+PRT      = 0              UTE     = -1.5           KT1     = -0.11
+KT1L     = 0              KT2     = 0.022          UA1     = 4.31E-9
+UB1      = -7.61E-18      UC1     = -5.6E-11       AT      = 3.3E4
+WL       = 0              WLN     = 1              WW      = 0
+WWN      = 1              WWL     = 0              LL      = 0
+LLN      = 1              LW      = 0              LWN     = 1
+LWL      = 0              CAPMOD  = 2              XPART   = 0.5
+CGDO     = 6.7E-10        CGSO    = 6.7E-10        CGBO    = 1E-12
+CJ       = 9.550345E-4    PB      = 0.8            MJ      = 0.3762949
+CJSW     = 2.083251E-10   PBSW    = 0.8            MJSW    = 0.1269477
+CJSWG    = 3.3E-10        PBSWG   = 0.8            MJSWG   = 0.1269477
+CF       = 0              PVTH0   = -2.369258E-3   PRDSW   = -1.2091688
+PK2      = 1.845281E-3    WKETA   = -2.040084E-3   LKETA   = -1.266704E-
3
+PU0      = 1.0932981      PUA     = -2.56934E-11   PUB     = 0
+PVSAT    = 2E3            PETA0   = 1E-4           PKETA   = -3.350276E-
3    )


.MODEL PMOS PMOS (                                LEVEL   = 7
+ TNOM    = 27             TOX     = 4.1E-9
+XJ       = 1E-7           NCH     = 4.1589E17      VTH0    = -0.3936726
+K1       = 0.5750728      K2      = 0.0235926      K3      = 0.1590089
+K3B      = 4.2687016      W0      = 1E-6           NLX     = 1.033999E-7
+DVT0W    = 0              DVT1W   = 0              DVT2W   = 0
+DVT0     = 0.5560978      DVT1    = 0.2490116      DVT2    = 0.1
+U0       = 112.5106786    UA      = 1.45072E-9     UB      = 1.195045E-
21
+UC       = -1E-10         VSAT    = 1.168535E5     A0      = 1.7211984
+AGS      = 0.3806925      B0      = 4.296252E-7    B1      = 1.288698E-6
```

```
+KETA     = 0.0201833      A1       = 0.2328472      A2       = 0.3
+RDSW     = 198.7483291    PRWG     = 0.5            PRWB     = -0.4971827
+WR       = 1              WINT     = 0              LINT     = 2.943206E-8
+XL       = 0              XW       = -1E-8          DWG      = -1.949253E-
8
+DWB      = -2.824041E-9   VOFF     = -0.0979832     NFACTOR  = 1.9624066
+CIT      = 0              CDSC     = 2.4E-4         CDSCD    = 0
+CDSCB    = 0              ETA0     = 7.282772E-4    ETAB     = -3.818572E-
4
+DSUB     = 1.518344E-3    PCLM     = 1.4728931      PDIBLC1  = 2.138043E-3
+PDIBLC2  = -9.966066E-6   PDIBLCB  = -1E-3          DROUT    = 4.276128E-4
+PSCBE1   = 4.850167E10    PSCBE2   = 5E-10          PVAG     = 0
+DELTA    = 0.01           RSH      = 8.2            MOBMOD   = 1
+PRT      = 0              UTE      = -1.5           KT1      = -0.11
+KT1L     = 0              KT2      = 0.022          UA1      = 4.31E-9
+UB1      = -7.61E-18      UC1      = -5.6E-11       AT       = 3.3E4
+WL       = 0              WLN      = 1              WW       = 0
+WWN      = 1              WWL      = 0              LL       = 0
+LLN      = 1              LW       = 0              LWN      = 1
+LWL      = 0              CAPMOD   = 2              XPART    = 0.5
+CGDO     = 7.47E-10       CGSO     = 7.47E-10       CGBO     = 1E-12
+CJ       = 1.180017E-3    PB       = 0.8560642      MJ       = 0.4146818
+CJSW     = 2.046463E-10   PBSW     = 0.9123142      MJSW     = 0.316175
+CJSWG    = 4.22E-10       PBSWG    = 0.9123142      MJSWG    = 0.316175
+CF       = 0              PVTH0    = 8.456598E-4    PRDSW    = 8.4838247
+PK2      = 1.338191E-3    WKETA    = 0.0246885      LKETA    = -2.016897E-
3
+PU0      = -1.5089586     PUA      = -5.51646E-11   PUB      = 1E-21
+PVSAT    = 50             PETA0    = 1E-4           PKETA    = -3.316832E-
3    )
```