

**DELHI TECHNOLOGICAL UNIVERSITY**

**DEPARTMENT OF ELECTRONICS AND COMMUNICATION  
ENGINEERING**

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**CERTIFICATE**

*This is to Certify that the major project work entitled, “**DESIGN OF HIGH GAIN LOW POWER AMPLIFIER**” submitted by **RAM MOHAN OJHA (12/VLSI/2K10)** in partial fulfilment of the requirements for the award of degree of **Master of Technology in VLSI Design and Embedded System at Delhi Technological University** is an original work carried out under my supervision and has not been submitted for the award of any other degree to the best of my knowledge and belief.*

Mr. Deva Nand  
(Assistant Professor)

Prof. Rajiv Kapoor

**Project Guide**

**Head of Department of E&C Engg.**

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**RAM MOHAN OJHA**  
Roll No.: 12/VLSI/2K10  
M.Tech. (VLSI Design &  
Embedded System)

## **ABSTRACT**

The analog electronics circuits have been developed much better from the past few decades. The design of analog amplifier has become the field of attraction due to various changes in technology. Amplifier circuits are analog circuit which can be used anywhere in houses like in electronic appliances. A variety of these devices such as Operational Amplifier, Fully Differential Amplifier, Current Feedback and Current Conveyors are spread all over in the integration of such electronic devices. In analog processing system Operational Amplifier is considered as a key element.

A CMOS single output two stage operational amplifier is presented which operates at 1.8 V power supply. It is designed to meet a set of provided specifications. The unique behavior of MOS transistor in sub-threshold region allows designer to work at both low input bias current and also at low voltage. This op-amp has very low standby power consumption with a high driving capability and operates at low voltage so that the circuit operates at low power. The op-amp provides a gain of 95.2 dB, -3db bandwidth of 80 Hz, phase margin of  $64.6^{\circ}$  and a unity gain bandwidth of 1.49 MHz for a load of 1 pF capacitor. This op-amp has a PSRR of 148.2 dB. It has a CMRR (dc) of 99.1 dB, and an output slew rate of 11.9 V/ $\mu$ s. The power consumption for the op-amp is 54.2  $\mu$ W. The presented op-amp has Input Common Mode Range (ICMR) of 0.2V to 1.3V. The op-amp is designed in the 180 nm technology using the 180 nm technology library.

The described op-amp is a simple two stage single ended op-amp which employs composite cascode technique. The input stage of the op-amp is a differential amplifier with an NMOS pair. The second stage of the operational amplifier is a simple PMOS common source amplifier. The second stage is used to increase the voltage swing at the output. The schematic of the operational amplifier has been designed and simulation is done using PSPICE simulator thereafter results are compared with the previous reported design.

# **TABLE OF CONTENTS**

Certificate .....	i
Acknowledgement .....	ii
Abstract .....	iii
Table of contents .....	iv
List of figures .....	viii
List of tables .....	xi
Chapter 1            Introduction .....	1
1.1    Background .....	1
1.2    Motivation .....	3
1.3    System Overview .....	5
1.4    Applications .....	6
1.5    Thesis Organization .....	6
Chapter 2            Literature Review .....	8
2.1    Introduction .....	8
2.2    MOSFET Operation .....	9
2.2.1    Strong Inversion Region .....	11
2.2.2    Moderate Inversion Region .....	12
2.2.3    Weak Inversion Region .....	12
2.3    Operational Amplifier Overview .....	13
2.3.1    Introduction .....	13
2.3.2    Operational Amplifier .....	14
2.3.3    Operational Amplifier Performance Parameters .....	18
2.4    Stability Consideration .....	23
2.4.1    Feedback Circuit Theory .....	24
2.4.2    Stability .....	25

Chapter 3	Operational Amplifier Compensation .....	30
3.1	Introduction .....	30
3.2	Basic Frequency Compensation Techniques of Operational Amplifier ....	31
3.2.1	Parallel Compensation .....	31
3.2.2	Pole Splitting – Single Capacitor Miller Compensation .....	31
3.2.3	Single Capacitor Miller Compensation with a Nulling Resistor ...	34
3.3	Other Multistage Operational Amplifier Compensation Techniques .....	35
3.3.1	Nested Miller Compensation .....	36
3.3.2	Reversed nested Miller compensation .....	37
3.3.3	Multipath NMC .....	37
3.3.4	Nested Gm-C compensation .....	38
3.3.5	Single Miller Feed-Forward Compensation .....	39
3.3.6	Nonstandard NMC Schemes .....	40
3.3.7	No Capacitor Feed Forward .....	41
3.3.8	Negative Miller Capacitance Compensation .....	42
Chapter 4	Operational Amplifier Design Methodology .....	44
4.1	Introduction .....	44
4.2	Weak Inversion Technique for Low Power Design .....	47
4.3	Parameter Extractions of MOS in Subthreshold Region .....	47
4.3.1	Subthreshold Slope Factor ‘n’ Extraction .....	48
4.3.2	I <sub>o</sub> Extraction .....	49
4.3.3	Calculation Channel Length Modulation Coefficient, $\lambda$ .....	50
4.4	Optimized Design Approaches .....	51
4.4.1	Nulling Resistor Approach .....	53
4.4.2	Voltage Buffer Approach .....	53
4.4.3	Current Buffer Approach .....	54

	4.4.4	Comparison of Design Approaches Based on Performance Parameter .....	55
	4.4.5	Advantage /Disadvantage with Current Buffer Approach .....	56
	4.5	Designing of Operational Amplifier Using gm/ID Method .....	56
Chapter 5		Proposed 2-Stage Operational Amplifier .....	61
	5.1	Introduction .....	61
	5.2	Selection of Circuit Topology .....	61
	5.3	The Composite Cascode Connection .....	63
	5.4	Practical Composite Cascode Circuit .....	64
	5.5	Circuit Realization .....	65
	5.5.1	Input Differential Composite Cascode Stage .....	66
	5.5.2	Composite Cascode Current Mirror .....	67
	5.5.3	Second Composite Cascode Stage .....	67
	5.5.4	Current Buffer .....	68
	5.5.5	Schematic of CMOS Operational Amplifier .....	69
Chapter 6		Simulation Results .....	71
	6.1	AC Response .....	71
	6.2	Transient Results .....	72
	6.3	Step Response .....	74
	6.4	Common Mode Rejection Ratio .....	75
	6.5	Power Supply Rejection Ratio .....	77
	6.6	Input Output Characteristics Using Unity Gain Configuration .....	78
	6.7	Variation of Frequency Response with Load Capacitance .....	79
	6.8	Effect of Variation of Compensation Capacitance (Cc) .....	81
Chapter 7		Conclusion And Future Research .....	84
	7.1	Conclusion .....	84
	7.2	Future Research .....	84

Bibliography .....	86
Appendix .....	89

## LIST OF FIGURES

FIGURE	DESCRIPTION	PAGE NO.
Fig.1.1	Operating voltage trend in CMOS technology.....	2
Fig.1.2	General Structure of op-amp.....	5
Fig.2.1	Power-supply ( $V_{dd}$ ), threshold voltage ( $V_t$ ), and gate-oxide thickness ( $t_{ox}$ ) vs. channel length for CMOS.....	9
Fig 2.2	Operating regions of a MOS device.....	10
Fig 2.3	General operational amplifier.....	14
Fig 2.4	Thevenin amplifier model .....	16
Fig 2.5	Ideal op-amp model.....	16
Fig 2.6	Open loop frequency curve.....	18
Fig 2.7	Showing unity gain bandwidth (UGB), gain margin (GM), phase margin (PM).....	19
Fig 2.8	Typical op amp input noise spectrum.....	22
Fig 2.9	Showing $R_i$ , $R_{id}$ and $R_o$ .....	23
Fig 2.10	General negative feedback system.....	24
Fig 2.11	Negative feedback system.....	26
Fig 2.12	General frequency response of op-amp.....	27
Fig 3.1	Implementation of pole-splitting (Miller Compensation).....	31
Fig. 3.2	Miller equivalent of circuit in Fig. 2.12.....	33
Fig. 3.3	Pole splitting.....	33
Fig. 3.4	Addition of $R_z$ in series with compensation capacitor.....	34
Fig. 3.5	Structure of a three-stage NMC amplifier.....	36
Fig. 3.6	Block diagram of the basic RNMC.....	37
Fig 3.7	Multipath NMC (MNMC).....	37
Fig 3.8	Nested Gm-C compensation (NGCC).....	39



Fig 3.9	Single Miller Feed-Forward Compensation (SMFFC).....	39
Fig. 3.10	No capacitor feed forward (NCFF).....	41
Fig. 3.11	Op-amp bandwidth extension method [23].....	42
Fig. 4.1	Typical two stage op-amp.....	44
Fig. 4.2	CMOS differential input stage.....	44
Fig. 4.3	Common source amplifier stage.....	45
Fig. 4.4	Source follower.....	46
Fig. 4.5	$\ln(I_D)$ and $V_{GS}$ curve in weak inversion region.....	49
Fig. 4.6	$I_D$ and $V_{GS}$ curve in weak inversion region.....	50
Fig. 4.7	Plot between $I_D$ vs $V_{DS}$ for NMOS in sub-threshold.....	51
Fig. 4.8	Two-stage op amp.....	52
Fig. 4.9	RC compensation block.....	53
Fig. 4.10	Voltage buffer compensation block.....	54
Fig. 4.11	Current buffer compensation block.....	55
Fig. 4.12	Circuit diagram of two stage op-amp.....	57
Fig. 4.13	$g_m/I_D$ Vs $I_D/(W/L)$ curve for NMOS.....	58
Fig. 5.1	Composite cascode amplifier.....	63
Fig. 5.2	Practical composite cascode stage.....	64
Fig. 5.3	Op amp input differential composite cascode stage.....	66
Fig. 5.4	Op amp composite cascode current mirror.....	67
Fig. 5.5	Op amp second composite cascode stage.....	68
Fig. 5.6	Current buffer.....	68
Fig.5.7	Schematic of two stage operational amplifier.....	69
Fig. 6.1	Configuration for simulating the open loop frequency response of op-amp.....	71
Fig. 6.2	Frequency response of op amp.....	72
Fig. 6.3	Schematic for the simulation of the transient response.....	73

Fig. 6.4	Output and Input signals for transient analysis.....	73
Fig. 6.5	Schematic for the simulation and measurement of the slew rate.....	74
Fig. 6.6	Slew Rate for the rising and falling edge with unity gain configuration.....	74
Fig. 6.7	Schematic for the simulation of common mode gain and CMRR.....	75
Fig. 6.8	Common mode rejection ratio CMRR.....	76
Fig. 6.9	Schematic for the simulation of PSRR.....	77
Fig. 6.10	Power supply rejection ratio.....	77
Fig. 6.11	Schematic for the simulation of input common-mode range.....	78
Fig. 6.12	Simulation result of input common-mode range (Linearity test).....	78
Fig. 6.13	Frequency response at load capacitance 1pF.....	79
Fig. 6.14	Frequency response at load capacitance 5pF.....	79
Fig. 6.15	Frequency response at load capacitance 10pF.....	80
Fig. 6.16	Frequency response variation with $C_c = 0.1\text{pF}$ .....	81
Fig. 6.17	Frequency response variation with $C_c = 0.25\text{pF}$ .....	81
Fig. 6.18	Frequency response variation with $C_c = 0.5\text{pF}$ .....	82

## LIST OF TABLES

<b>TABLE NO.</b>	<b>DESCRIPTION</b>	<b>PAGE NO.</b>
TABLE I	Comparison of design approaches.....	55
TABLE II	Comparison of Performance of Various Op-Amp Topologies.....	62
TABLE III	Operational Amplifier Devices Sizes.....	70
TABLE IV	Variation of parameters with Load Capacitance ( $C_L$ ).....	80
TABLE V	Variation of parameters with compensation capacitance ( $C_c$ ).....	82
TABLE VI	Comparison with previous research work results.....	83