DELHI TECHNOLOGICAL UNIVERSITY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

DELHI-110042

CERTIFICATE

This is to Certify that the major project work entitled, "**DESIGN OF HIGH GAIN LOW POWER AMPLIFIER**" submitted by **RAM MOHAN OJHA** ***(12/VLSI/2K10)*** *in partial fulfilment of the requirements for the award of degree of* ***Master of Technology*** *in* ***VLSI Design and Embedded System*** *at* ***Delhi Technological University*** *is an original work carried out under my supervision and has not been submitted for the award of any other degree to the best of my knowledge and belief.*

Mr. Deva Nand
(Assistant Professor)

Project Guide

Prof. Rajiv Kapoor

Head of Department of E&C Engg.

ACKNOWLEDGEMENT

I express my sincere gratitude to my project guide “Mr. Deva Nand”, Assistant Professor, Department of Electronics and Communication Engineering, for giving valuable guidance during the course of this investigation for his ever encouraging and timely moral support. His enormous knowledge and intelligence always help me unconditionally to solve various problems.

I am greatly thankful to “Dr. Rajiv Kapoor”, Head of Department (Electronics and Communication Engineering), Delhi Technological University for his perpetual encouragement, generous help and inspiring guidance.

I would like to extend my gratitude and my sincere thanks to “Dr. Neeta Pandey”, Associate Prof. E&C Deptt. for her timely comments, guidance, and support. She is my source of inspiration. Her trust and support inspired me in the most important moments of making right decisions.

I express my feelings of thanks to the entire faculty and staff of Department of Electronics and Communication Engineering, Delhi Technological University, Delhi for the help and moral support which went along way successful completion of my thesis work.

Next, I'd like to thank to all my friends for all the good times at the lab and for their help, criticism and suggestions.

I am thankful to the Almighty God who bestowed upon me his grace and was always with me whenever I felt lonely.

RAM MOHAN OJHA
Roll No.: 12/VLSI/2K10
M.Tech. (VLSI Design &
Embedded System)

ABSTRACT

The analog electronics circuits have been developed much better from the past few decades. The design of analog amplifier has become the field of attraction due to various changes in technology. Amplifier circuits are analog circuit which can be used anywhere in houses like in electronic appliances. A variety of these devices such as Operational Amplifier, Fully Differential Amplifier, Current Feedback and Current Conveyors are spread all over in the integration of such electronic devices. In analog processing system Operational Amplifier is considered as a key element.

A CMOS single output two stage operational amplifier is presented which operates at 1.8 V power supply. It is designed to meet a set of provided specifications. The unique behavior of MOS transistor in sub-threshold region allows designer to work at both low input bias current and also at low voltage. This op-amp has very low standby power consumption with a high driving capability and operates at low voltage so that the circuit operates at low power. The op-amp provides a gain of 95.2 dB, -3db bandwidth of 80 Hz, phase margin of 64.6^0 and a unity gain bandwidth of 1.49 MHz for a load of 1 pF capacitor. This op-amp has a PSRR of 148.2 dB. It has a CMRR (dc) of 99.1 dB, and an output slew rate of 11.9 V/μs. The power consumption for the op-amp is 54.2 μW. The presented op-amp has Input Common Mode Range (ICMR) of 0.2V to 1.3V. The op-amp is designed in the 180 nm technology using the 180 nm technology library.

The described op-amp is a simple two stage single ended op-amp which employs composite cascode technique. The input stage of the op-amp is a differential amplifier with an NMOS pair. The second stage of the operational amplifier is a simple PMOS common source amplifier. The second stage is used to increase the voltage swing at the output. The schematic of the operational amplifier has been designed and simulation is done using PSPICE simulator thereafter results are compared with the previous reported design.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES