"Managing Reactive Power Using Cascaded Multilevel D-STATCOM in Sub-Transmission/11kV Distribution System"

A Dissertation Submitted in the Partial Fulfilment for the Degree of

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in

Power System Engineering

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CERTIFICATE

It is certified that **Mr. Tapesh Vishnoi** Roll No. **11/P.Sy./09**, student of **M.Tech. Power System Engineering**, Department of Electrical Engineering, Delhi Technological University, has submitted the dissertation entitled **"Managing Reactive Power Using Cascaded Multilevel D-STATCOM in Subtransmission/11kV Distribution System"** under my guidance towards partial fulfilment of the requirements for the award of the degree of Master of Technology (Power System Engineering).

The dissertation is a bonafide work record of project work carried out by him under my guidance and supervision. His work is found to be outstanding and his discipline impeccable during the course of the project.

I wish him success in all his endeavours.

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TAPESH VISHNOI

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ABSTRACT

This thesis investigates the problems associated with 11kV distribution system in terms of delivery of clean power and their solutions, in particular the reactive power compensation. The abnormalities in the distribution system has been modelled and analysed. Any deviation from the ideal condition has been computed in the time domain at every instant. The deviation so computed has been compensated by use of the D-STATCOM in the real time. A detailed model of 3-phase bridge D-STATCOM for line voltage upto 11kV has been developed using cascaded multilevel voltage source converter structure (VSCs). A same phase multilevel PWM control has been developed for the multilevel inverter for the medium voltage distribution system. The scheme has been replaced for the control of the D-STATCOM so that it maintains the reactive power and THD under control by keeping all the voltage and current waveforms as per their standard sinusoidal forms. The proposed system has been presented with the mathematical equations and block diagrams for detailed illustrations of the control loops. A SIMULINK model using MATLAB/SIMULINK platform has been used to present the proposed system. Simulation result for different operating condition has been obtained and analysed for viewing the merit of the proposed control technique. The obtained results corroborate the effectiveness of control scheme.

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INTRODUCTION

1.1 General

An electric distribution system is part of a power system deriving power from the bulk power source and delivering power to the loads. Distribution systems are, in general, divided into six parts, namely, sub transmission circuits, distribution substations, distribution or primary feeders, distribution transformers, secondary circuits or secondary and consumer's service connections and meters or consumer's services. The present chapter discusses about the power quality issues associated with the distribution system, how their mitigation is done using custom power devices. With the advent of power electronics, the IGBT Switches have emerged as most promising candidate for customer power devices for power quality improvement. A single available such switch has as maximum of voltage 1.2 kV, where as the distributed system looks forwarded to 11kV distributed system. To provide compensation to such level of voltage a structure having multilevel structure is required. The following section deals with multilevel structure based VSI/D-STATCOM.

1.2 Power Quality Issues

Power Quality problems are referred as deviation of the electrical parameter such as current, voltage and frequency from their standard magnitude. These standards may vary from country to country but in general for power the current and voltage should be near sinusoidal and frequency of the oscillating supply should be constant. Along these factors a consumer should also get an uninterrupted supply. So, improved PQ power system can be defined as the uninterrupted distribution of supply following the standard waveform norms even in abnormal conditions caused by human or natural adversaries [1].

Many industrial loads such as semiconductor manufacturing industries, healthcare industries, financial organisation, air traffic control etc. are categorized as sensitive loads as a little

deviation from the standard supply can cause huge damages to the consumers [2]. So for these types of loads electric power quality is of high concern. However conventionally used distributed system faces many types of problems arise due to loading perturbations and abnormal switching conditions. Thus maintaining the power quality is apprehensive for the electric engineers.

The various power quality problems and their effects are as follows [3]:

1.2.1 Poor Load Factor: A load with high X/R ratio causes a poor load factor which makes the reactive component of the supply current high and the magnitude of the supply current also increases. This high reactive current causes a voltage drop in the system, also as the magnitude of supply current increases the ohmic loss (I^2R losses) also increases.

1.2.2 Harmonic Contents in Loads: The switching of nonlinear loads and power electronic equipments causes the generation of harmonics in the distributed system. These harmonics currents cause additional losses in the system in form of heating of the equipments which in long run can permanently damage the system. Some time these harmonics may also lead to mal-operation of the system as various switching devices as the timer circuitry is disturbed by these harmonics.

1.2.3 Unbalanced Loads: In a healthy power system the 3-phases should be equal in magnitude and 120^0 degree spatial apart from each other. If the load connected to any of the phase is unbalanced, it causes the unbalance in the other phase also as the unbalanced supply current flows through the supply impedance. This imbalance causes the trouble in operation of the induction machine as the negative sequence voltage creates a flux in opposition of the main rotor flux and produces a negative torque. Also the decomposed zero sequence voltage can cause extra loss in the system.

1.2.4 Notching in Load Voltage: Notching is the periodic voltage distortion produced during the commutation of current from one phase to another in power electronic converter. The large phase controlled rectifiers cause notches in the phase voltage as they provide finite inductance in the supply. Due to this there are periods where line to line voltage falls to zero. Firing angle

of the rectifier does play a very important role in the place of notch in the waveform. This notching can cause abnormal operation of protective devices which can interrupt the whole system.

1.2.5 DC Offset in Load Voltage: Geomagnetic disturbances and half wave rectification produce the DC offset in the power system. The DC output of the power electronic loads such as rectifier cause the supply to have a DC offset. This offset can cause the flux excursion of the distribution transformer. DC current also enhances the corrosion of metallic structure as it causes the metallic ions to flow in the direction of the current flow which involve the earth as return path.

1.2.6 Voltage Sag/Swell: The short duration voltage variation caused by faults, energization of large loads that require large inrush current and intermittent loose connection produces voltage sag and swells in the system. As the name suggest voltage sag and swell are the decrement and increment of the fundamental frequency voltage from the standard value of the fundamental frequency voltage. These can cause the mal-operation of protective devices.

1.2.7 Short time Overvoltage/Undervoltage: Sustained transient usually oscillatory transient sustaining for more than one minute in the system can cause an increase or decrease in magnitude of the voltage. Switching on the large capacitive load pushes heavy reactive power to system which in turn causes the overvoltage. Undervoltage is the result of opposite events. Sustained overvoltages may damage the home appliances.

1.2.8 Voltage Flicker: Rapid variation in current magnitude as in the case of arc furnaces causes the rapid variation of the supply voltage. The term is referred as the voltage flicker. Due to this flicker the light intensity from the incandescent lamps vary rapidly which can have adverse effect on human health as it may lead to migraine and headache to the human observer.

1.2.9 Power Frequency Variation: As the load in the system changes very rapidly, the supply frequency of a system having low inertia system may also vary as according to torque, current and speed characteristics of the generation system. This change may throw the system out of synchronism and may lead to complete system failure.

The passive filters are included in the distribution system to filter out the distortions in the distributed system but their performance is restricted. However, load conditions are ever changing in the distribution system hence, a varying compensation is needed for the distribution system. The custom power devices are therefore required to be installed to provide active compensation.

1.3 Custom Power (PQ Improvement Devices)

As the power electronics controller based shunt and series FACTS devices are used for the enhancing the transmission capabilities of the transmission system, similarly shunt and series power electronics devices can be used for addressing the power quality issues in distributed system which witness huge variety of problems [4]. The power electronic based devices work as compensating devices in distribution system. These custom power devices enhance the power quality while keeping the frequency, voltage and current under specific limits. The various operation performed by these controllers to improve the PQ problems includes the low phase unbalances, low flicker, low harmonic distortion and maintenance of the values of voltage, current and frequency within specified limits. These devices can also sustain the supply in case of power interruption if provided with DC power back up.

These compensating devices are connected in shunt, series or a combination of both. The controller of these devises can be implemented for the mitigation of one or many power quality issue. The custom power devices can be broadly classified in two types namely: **(i)** network reconfiguring type and, **(ii)** compensating type.

1.3.1 Network Configuration Type Devices

Network reconfiguring type custom powers are used for fast current limiting and current breaking during the faults. They can transfer the load to the alternate feeder in case of abnormalities in the system. The main devices belonging to this family are:

1.3.1.1 Solid State Current Limiter (SSCL): This GTO base device limits the fault current by inserting an inductor in the faulty line. As the system detects normal conditions the inductor is removed from the line.

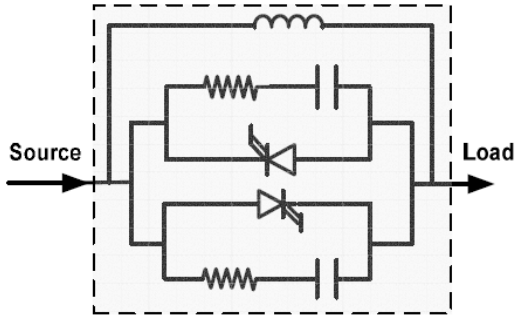


Figure 1.1 Basic Configuration of SSCL.

1.3.1.2 Solid State Circuit Breaker (SSCB): The fault current can be diverted from the healthy system very rapidly with the use of this devise. The system also incorporates the auto reclosing function to restore the supply in case of normal system condition is restored. This circuit consists of a combination of GTO and thyristor switches which performs very fast in comparison to its mechanical counterpart.

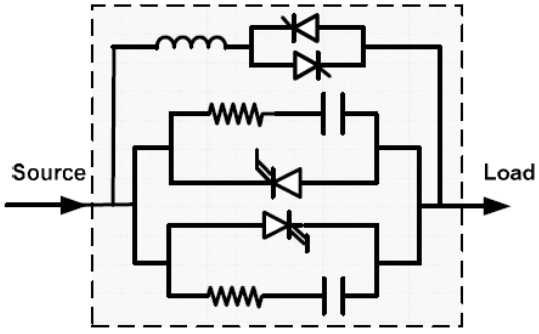


Figure 1.2 Basic Configuration of SSCB.

1.3.1.3 Solid State Transfer Switch (SSTS): This thyristor based device is used to transfer the load to an alternative feeder in case of any abnormalities. This device is usually employed to protect sensitive loads.

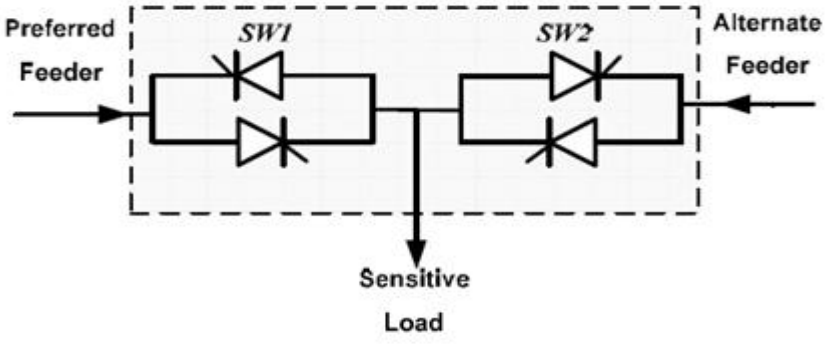


Figure 1.3 Basic Configuration of SSTS.

1.3.2 Compensating Devices

The compensating devices are used for the mitigation of power quality issues. They are used for active filtering, power factor correction, load balancing and voltage regulation to name a few. They can be installed as shunt, series or hybrid combination to compensate the power quality problems. Shunt devices are popular in those applications which demands greater ease of protection. These devices are operated in such manner that they provide balanced and harmonic free current to the upfront utility devices. They can also be controlled to correct the unbalance and distortion in the source currents in such a manner that it appears that a balance load is connected to the ac system. Similarly the series device work on improving the power quality issues related to voltages. These devices operate in such a way as to provide balance, undistorted and regulated voltage at the load end. These compensating devices family members with their specific function are presented in the following section:

1.3.2.1 Distribution STATCOM (D-STATCOM): This shunt connected device is the low level avatar of FACTS device STATic COMpensator (STATCOM). The opportunity to work at low voltage enable the device to perform harmonic filtering, power factor improvement, load balancing, reactive power compensation etc. when connected as load compensator. When connected to distribution system it can also perform the voltage regulation [5]. In this mode it can sustain the desired voltage against any demand of reactive power by the load connected to the distributed system.

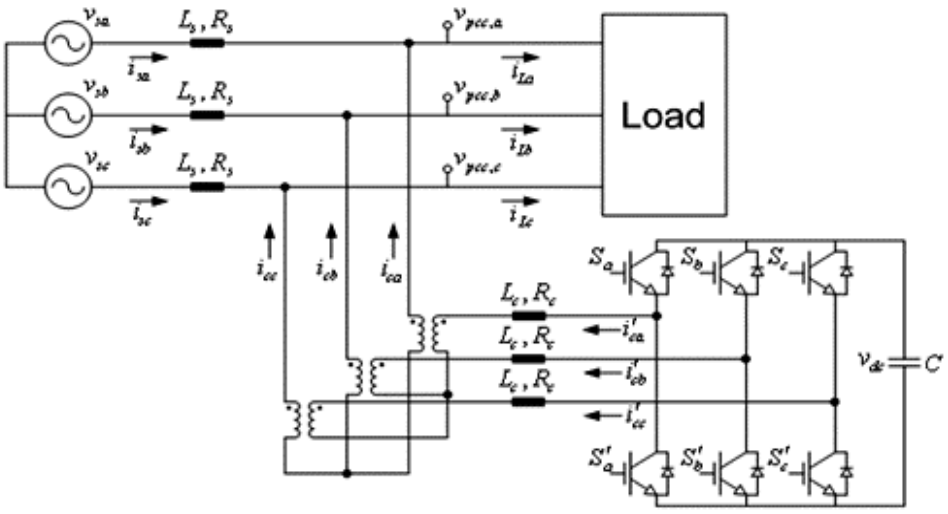


Figure 1.4 Schematic Diagram of D-STATCOM.

The main difference in operating the D-STATCOM and STATCOM is that the STATCOM is required to inject a set of three balanced quasi-sinusoidal voltage which are phase displaced 120^0. On the contrary a D-STATCOM can inject component of current to compensate reactive power, unbalance in currents and harmonic currents as per the requirement to eliminate power quality problems in the concerned system.

1.3.2.2 Dynamic Voltage Restorer (DVR): This device has the structure as that of static synchronous series compensator (SSSC) in the FACTS devices. This device injects a series voltage to compensate the voltage sag/swell in the supply side and also inject real or reactive power to regulate the voltage. The sensitive loads can be protected from any kind of voltage distortion with this device. The main difference between SSSC and DVR operation is that the former supplies a balance sinusoidal voltage in series; however the later is able to inject unbalance voltages and component corresponding to distortion. The DVR can also compensate the distorted voltage to clean the supply voltage.

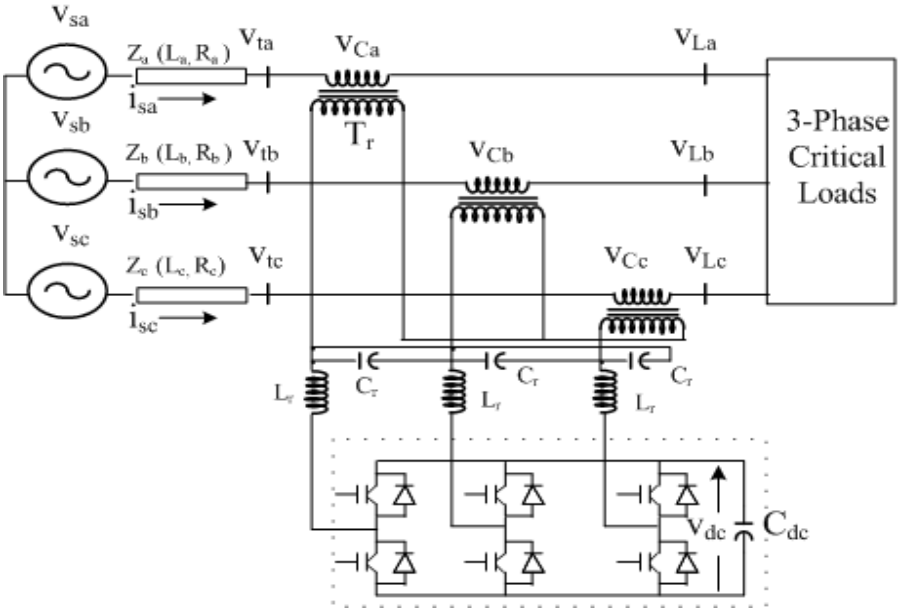


Figure 1.5 Schematic Diagram of Capacitor Supported DVR.

1.3.2.3 Unified Power Quality Conditioner: This versatile device is able to compensate any of the power quality problems as it can inject current in shunt and voltage in series simultaneously as per the system requirement. The injected current or voltage can be of any shape or type, balanced or unbalanced as desired by the system.

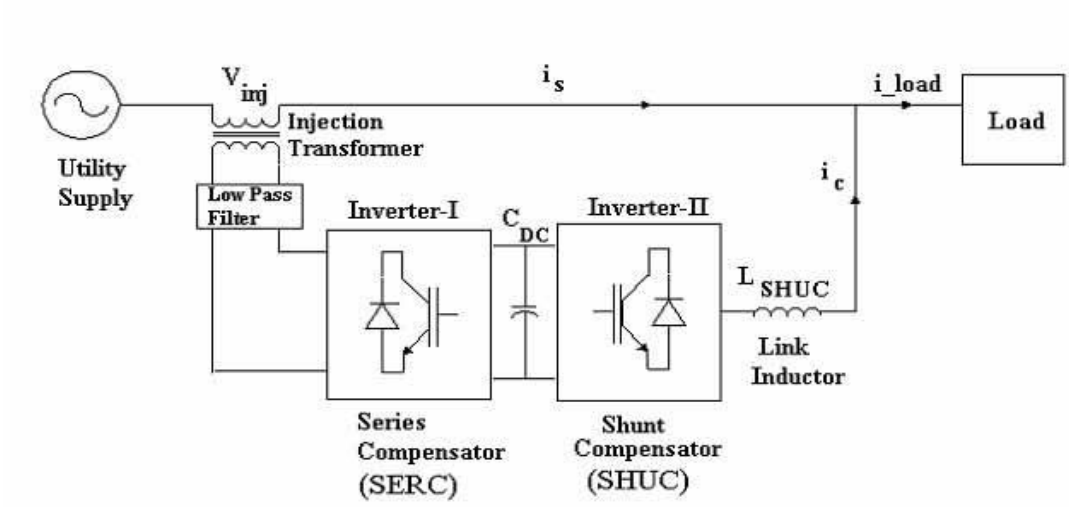


Figure 1.6 Schematic Diagram of Right Shunt UPQC Configuration.

1.4 Multilevel Structure for High/Medium Voltage System

In modern power system the power delivery is kept at a very high voltage (400kV or 765kV) to reduce the transmission losses. On the consumer side this voltage is brought down by the transformer as per the consumer requirements in two stages; sub-transmission and distribution level. Usually 66/33kV systems are termed as sub transmission systems while the systems below 33kV system are categorised as distribution system.

In present distribution system load shedding is inevitable as we have various types of loads and system requirements. With the advancement in distributed generation (DG) the distribution system requires different norms and regulations. The use of high voltage distribution not only ease the load shedding also it ensures the improved structure as there are less losses and theft of supply.

The main concern with the high/medium power distribution is the method to be adopted for improving the power quality. As the custom power requires a very fast switching for the harmonic reduction and compensating the distortion from the waveforms, the switch used in these power electronic based controllers should be of such grade that they should able to withstand high voltage and current conditions. In the present scenario the availability of such bidirectional switches is very restricted due to lack of research and manufacturing companies in this field.

This makes the multilevel structure of the power electronic based custom power a necessary requirement for mitigation of power quality issues. This multilevel structure can easily be employed with the switches of rather low ratings and provides a satisfactory performance in addressing the problems above mentioned. But the development of these converters is in initial phase and requires new methodologies for effective operation of these converters.

1.5 Organization of Dissertation

This dissertation is organised in five chapters which are arrange to give the comprehensive view of proposed work:

Chapter 2 gives the record of literature surveyed in carrying out the proposed work. In this chapter different type of multilevel structure used in control of power flow and their control technique proposed by many researchers have been discussed. The main emphasis is given on the Cascades H-Bridge multilevel inverter (CHBMI) structure and multilevel D-STATCOM as custom power.

Chapter 3 presents a mathematical model of PLL, an integral part of control schemes adopted for these power electronic based devices. A mathematical model for cascade H-bridge multilevel inverter is proposed for the system calculation. The inverter model is further enhanced to develop the multilevel D-STATCOM.

Chapter 4 presents the SIMULINK model of 3-phase bridge D-STATCOM, multilevel inverter for different levels and multilevel D-STATCOM. The results for different load conditions are obtained in graphical form and detail analysis is done of the obtained results.

Chapter 5 presents the main conclusions of dissertation and future scope of proposed work. This chapter extends the horizon for the further advancement that can be done in the related field.

In the last detailed information of all the references studied and used in forming the dissertation is given.

CHAPTER 2

LITERATURE SURVEY

CHAPTER 2

LITERATURE SURVEY

2.1 General

Past few years have witnessed a substantial change in the electricity distribution system. The emphasis has been given on the reliable power system distribution which holds the key in improving the power quality along with reliability. Various industries which require quality supply of voltage and current, the office and household consumers who do not want to pay money for poor power and distribution companies (DisComs) who do not want their power to get wasted in the process of distribution have to properly understand the importance of power quality. Devices varying from the simple power factor correctors to UPQC are being installed for obtaining the pure power. The connectivity of Power Quality (PQ) compensator to the LT side distribution transformer attracts lots of problem which include frequent interruptions and reconnections, large bandwidth and rating of devices, improper utilization etc. Whereas, operation of PQ compensator at HT side/11kV distribution side offer longer time of connectivity, more depth of penetration and, such PQ compensators can serve various Distributed Power Generators (DPG) which forms microgrid and are connected to 11kV distribution system. A literature search is done to select the appropriate topology of multilevel converter in carrying out the proposed work and the area identified for further research.

2.2 Literature Review

The concept of a unified converter theory [6] suggests that any power electronic converter can be observed as a matrix of switches which connects its input nodes to its output nodes. These nodes may be either DC or AC, and either inductive or capacitive; and the power flow can take place in either direction. However, basic laws of electricity enforce restrictions such as:

1) If one set of nodes (input or output) is inductive, the other set must be capacitive, so as not to create a cut set of voltage or current sources when the switches are closed.

2) The combination of open and closed switches should never open circuit an inductor, or short circuit a capacitor.

This unified set of converters is generally categorised into a number of different sets as according to their operation. In a rectifier the power flow is predominately from the AC side to

the DC side and in the inverter power flow is predominately from the DC side to the AC side. The term converter is used either when there is no predominant direction of power flow i.e. power flow is bidirectional. In general it encompasses both rectifiers and inverters [7].

2.2.1. Survey for Multilevel Converter

A multilevel converter can switch either its input or output nodes (or both) between multiple (more than two) levels of voltage or current. The multilevel voltage source converter has found many industrial applications such as ac power supplies, static VAR compensators, drive systems, etc. Among the various advantages of multilevel configuration is the harmonic reduction in the output waveform without increasing switching frequency or decreasing the converter power output and also the stress of high power operating conditions is less on every switch [8], [9], [10]. The output voltage waveform of a multilevel converter is composed of the number of levels of voltages which are obtained either from battery or synthesized by capacitors which holds the voltage across them. We can build multilevel inverter to obtain the voltage level from 3 levels to any number of levels. As the number of levels increases, the output THD decreases. However, problems of voltage unbalancing, voltage clamping requirement, circuit layout, and packaging constraints restrict the number of the achievable voltage levels [8].

Three mostly used voltage synthesis-based multilevel inverters are introduced, i.e.

1. Diode Clamped Multilevel Inverter (DCMI) [8][9],
2. Flying Capacitor Multilevel Inverter (FCMI) [8],
3. Cascade H-Bridge Multilevel Inverter (CHBMI) [8].

2.2.1.1 Diode Clamped Multilevel Inverter (DCMI)

The diode-clamped multilevel inverter uses capacitors in series to divide the dc bus voltage into a set of voltage levels. An m-level diode-clamp inverter requires m-1 capacitors on the dc bus. The obtained output is m-level phase voltage. A single-phase five-level diode-clamped inverter, which can produce a nine-level phase to phase voltage waveform, is shown in Fig. 2.1.

The dc bus consists of four capacitors, i.e., C1, C2, C3, and C4. For dc bus voltage V_{dc}, the voltage across each capacitor is $V_{dc}/4$, and voltage stress on each device will be limited to one capacitor voltage level, $V_{dc}/4$, through clamping diodes. DCMI output voltage synthesis is relatively straightforward. To explain how the staircase voltage is synthesized, point O is considered as the output phase voltage reference point. Using the five-level inverter shown in Fig. 2.1, there are five switch combinations to generate two voltage level one above and below and other at zero level.

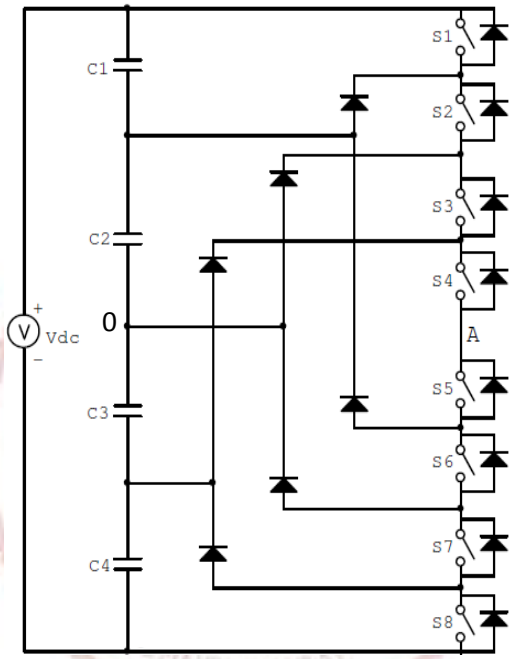


Figure 2.1 A Single Phase Five Level DCMI.

Table 2.1 shows the phase voltage level and their corresponding switch states. In the Table 1.1, state 1 represents that the switch is on and state 0 represents the switch is off. There exist four complementary switch pairs in each phase, i.e., S1-S5, S2-S6, S3-S7 and S4-S8.

Table 2.1 Diode-Clamped Five-Level Inverter Voltage Levels and Their Switch States:

Output V_{AO}	Switch State							
	S1	S2	S3	S4	S5	S6	S7	S8
$V_5 = -V_{dc}/4$	1	1	1	1	0	0	0	0
$V_4 = -Vdc/2$	0	1	1	1	1	0	0	0
$V_3 = 0$	0	0	1	1	1	1	0	0
$V_2 = Vdc/2$	0	0	0	1	1	1	1	0
$V_1 = Vdc/4$	0	0	0	0	1	1	1	1

However, due to the following disadvantages, the use of diode-clamped topology is limited to a maximum of five levels [8], [11], [14]:

1) Although the transformer can be eliminated, extra components (diodes) are required to ensure load current continuity. As the number of levels increase, the number of extra components raises sharply. These extra components do not necessarily ensure equal voltage sharing for all switches.

2) Switch utilization is not equal as outer switches receive a lower average load. This problem becomes particularly apparent as the number of levels increase and the modulation depth is small. Similarly the power flow to and from the different capacitors in a capacitor string is not balanced.

3) All switch states are not allowed. The disallowed states must be remapped to their equivalent allowed states.

4) Different equivalent states show the capacitor voltages in different directions. This must be used to control the capacitor voltages.

For the above mentioned reasons, a dedicated modulation strategy must be used to control this topology. However these strategies are often complex even after specifically customized to the topology.

2.2.1.2 Flying-Capacitor Multilevel Inverter (FCMI)

The flying capacitor inverter, or imbricated cells multilevel inverter topology was proposed in [12], [13]. A FCMI as shown in Fig. 2.2 uses a ladder structure of dc side capacitors where the voltage on each capacitor differs from that of the next capacitor. To generate m-level staircase output voltage, m-1similar capacitors are required in the dc bus. Each phase-leg has an identical structure. The size of the voltage increment between two capacitors determines the size of the voltage levels in the output waveform.

Here the switch pair-capacitor ‘cell’ is isolated and inserted within a similar cell – hence the term imbricated cells inverter. The inner pair of switches and their associated capacitor ‘fly’ as the outer pair of devices switch. The combination of conducting switches and capacitors ensures that the voltage across any blocking switch is always well defined. Table 2.2 shows the switch combination of the voltage levels and their corresponding switch states. In fact, there is

more than one combination to produce output voltages V2, V3, and V4, this provides the FCMI more flexibility than DCMI.

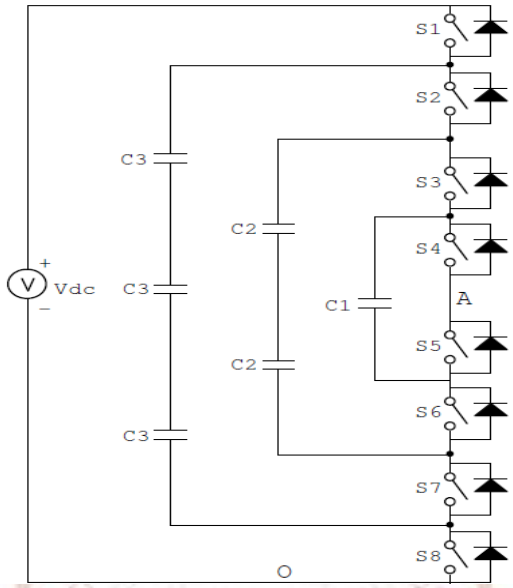


Figure 2.2 A Single-Phase Five-Level Flying-Capacitor Inverter.

Table 2.2 Switch Combination of the Voltage Levels and Their Corresponding Switch States:

Output V_{AO}	Switch State							
	S1	S2	S3	S4	S5	S6	S7	S8
$V_5 = -V_{dc}/2$	1	1	1	1	0	0	0	0
$V_4 = -V_{dc}/4$	1	1	1	0	0	0	0	1
	1	1	0	1	0	0	1	0
	1	0	1	1	0	1	0	0
	0	1	1	1	1	0	0	0
$V_3 = 0$	1	1	0	0	0	0	1	1
	1	0	1	0	0	1	0	1
	1	0	0	1	0	1	1	0
	0	1	1	0	1	0	0	1
	0	1	0	1	1	0	1	0
	0	0	1	1	1	1	0	0
$V_2 = V_{dc}/4$	1	0	0	0	0	1	1	1
	0	1	0	0	1	0	1	1
	0	0	1	0	1	1	0	1
	0	0	0	1	1	1	1	0
$V_1 = V_{dc}/2$	0	0	0	0	1	1	1	1

The flying capacitor family of converters have many advantages as following [11],[12],[14] :

1) This topology can be applied to a number of different converter types - current or voltage source, DC-DC or DC-AC. For this purpose any switch combination can be adopted.
2) As long as switch pairs receive complementary drive signals, voltage sharing is ensured. Any modulation strategy can be easily applied to this structure by phase shifting the drive signals.
3) There is no need of balancing voltages of the capacitors as conventional modulation strategy takes care of this problem, if required, the capacitor voltages can be actively controlled by an appropriate modification of the control signals.
4) This structure is not reliant on a transformer multilevel topology the switches equally shares the load by default.

However, this topology has certain limitation [11],[14]:

1) This topology requires a lot of high voltage capacitors as compared to other topologies. These capacitors are essential as they conduct the full load current for at least part of the switching cycle. To reduce the value of capacitor used in the structure, the switch frequency has to be very high.
2) Starting the converter safely may be a non-trivial task as capacitors have zero voltage across them in the initial states.
3) The topology is not inherently fault tolerant. In case of even a single component burn out, the whole of the inverter is isolated making system inoperative.

2.2.1.3 Cascaded H Bridge Inverters with Separated DC Sources (SDCSs)

This topology is configured by cascading the identical single phase bridge rectifier. [8],[11].The multilevel inverter using cascaded-inverter with SDCSs synthesizes a desired voltage level from several independent sources of dc voltages, which are provided from either batteries, fuel cells or solar cells. This configuration is getting popularity in ac power supply and adjustable speed drive applications for its easy to upgrade structure. This new inverter can avoid extra clamping diodes or voltage balancing capacitors. A single-phase two-cell series configuration of such an inverter is shown in Fig. 2.3.

The ac terminal voltages of different level inverters are connected in series. Each inverter level generates three different voltage outputs, $+V_{dc}$, $-V_{dc}$, and zero for the different firing combination of four switches, S1-S4. As the ac outputs of each level of full-bridge inverters are connected in series, the synthesized voltage waveform is the sum of the inverter outputs. In this topology, the number of output phase voltage levels is defined by m=2s+1, where s is the number of dc sources. Table 2.3 shows the switch combination of the voltage levels and their corresponding switch states.

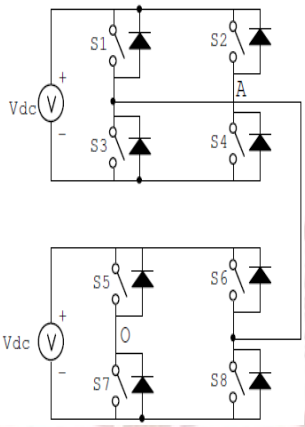


Figure 2.3 Single-Phase Structure of a Two-Cell Cascaded Inverter.

Table 2.3 Two-Cell Cascaded-Inverter Voltage Levels and Their Switch States:

Output V_{AO}	Switch State							
	S1	S2	S3	S4	S5	S6	S7	S8
$V_5 = -2V_{dc}$	0	0	0	0	0	1	1	0
$V_4 = -Vdc$	0	0	0	0	0	1	0	1
$V_3 = 0$	0	1	1	0	0	0	0	0
$V_2 = Vdc$	1	1	1	1	1	0	1	0
$V_1 = 2Vdc$	1	1	1	1	1	0	0	1

This multilevel converter structure has some very significant advantages, if its limitations are acceptable [11],[14]. Its advantages are:

1) It has perhaps the simplest architecture and the lowest component count. No transformer is needed, so capital costs are low.

2) Modularity is its main advantageous feature which makes the use of this topology in the ever expanding power system structure. This flexibility of modular structure is not only open to its component devices but the control for the system is also modular.

3) If a module fail (or be removed), it must fall short circuited, or be bypassed. The converter can continue to operate, at full current capacity, but at reduced voltage rating..

And the limitations of this topology are as follows:

1) The access to DC bus capacitors is limited, which narrows its area of application to either those with only reactive power flow, or those where the power source or load can be both modular and isolated.

2) On the DC side if self supported system using the capacitors to be employed, the voltage balancing across all the capacitor is rather complex.

3) Practically in case of module failure, or say, if fault tolerance is required, the converter will need a more conservative voltage rating — a potential cost penalty.

Table 2.4 Comparison of Power Component Requirements Per Phase Leg Among Three Multilevel Inverters[11][15]:

Inverter Configuration	Diode – Clamp	Flying Capacitor	Cascade Inverter
Main Switching Devices	2(m-1)	2(m-1)	2(m-1)
Main Diodes	2(m-1)	2(m-1)	2(m-1)
Clamping Diodes	(m-1)(m-2)	0	0
DC Bus Capacitors	(m-1)	(m-1)	(m-1)/2
Balancing Capacitors	0	(m-1)(m-2)/2	0

2.2.2 Modulation Technique

Pulse width modulation (PWM) strategies used in a conventional inverter can be modified to use in multilevel converters. The advent of the multilevel converter PWM modulation methodologies can be classified according to switching frequency as illustrated in Fig. 2.4. The three multilevel PWM methods most discussed in the literature have been multilevel carrier-based PWM, selective harmonic elimination, and multilevel space vector PWM; all are extensions of traditional two-level PWM strategies to several levels.

2.2.2.1 Hysteresis Control: In hysteresis band modulating scheme the pulses are obtained by calculating the error between the desired output and the measured output. As this error exceeds a certain bound (leaves the hysteresis band), the state of the switches is changed, so as to drive the error back within that bound. In this manner switching pulses are obtained to drive the inverter. This basic requirement of is to integrate the controlled output quantity of the inverter

by the load, or as part of the controller. As in a voltage source hysteretic inverter, the output current (the measured and subsequently controlled quantity) will be integrated by an inductive load.

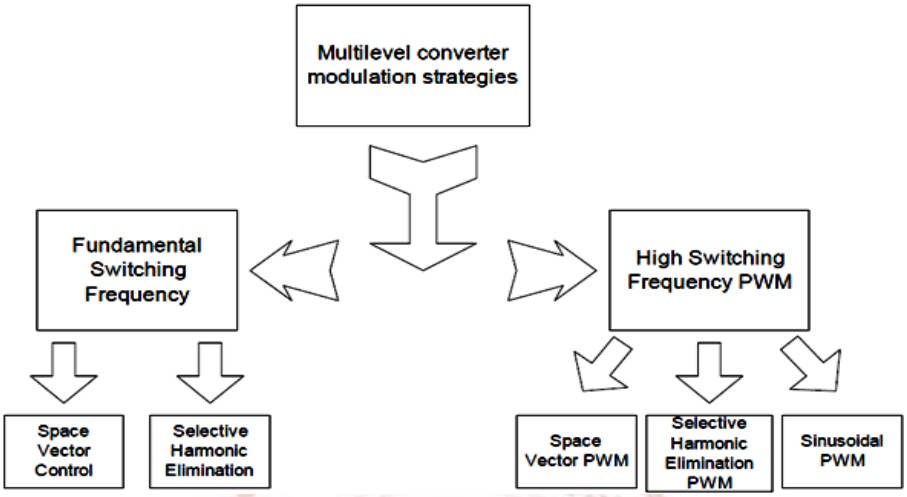


Figure 2.4 Classification of PWM Multilevel Converter Modulation Strategies.

The advantages offered by this technique include simplicity to implement, closed loop nature and low distortion. This method gives bounded, predictable error and fast transient response to change at either the input or the output. But variable nature of switching period limits its usefulness to low power, high switching frequency applications as this variable nature causes a continuous and wide output spectra. Subharmonics can also be present as the switching instants are asynchronous or acyclic.

To eliminate sub-harmonics quarter wave symmetry is used at each zero crossing by resetting the error and forcing a switching, and hence a reflection of the pattern, at 90 degrees [16]. This method offers discrete spectra without sub-harmonics. Modulation of the width of the hysteresis band also restricts variation the switching frequency [17], [18].This places upper and lower limits on the switching frequency, but does not address the problem of sub-harmonics.

2.2.2.2 Multilevel carrier-based PWM: Many multilevel carrier-based PWM techniques as a means for controlling the active devices in a multilevel converter. The most popular and easiest technique to implement uses several triangle carrier signals and one reference, or modulation, signal per phase. Fig. 2.5 illustrates three major carrier-based techniques used in a conventional inverter that can be applied in a multilevel inverter: sinusoidal PWM (SPWM), third harmonic

injection PWM (THPWM), and space vector PWM (SVM). SPWM is a very popular method in industrial applications [11] [14][19].

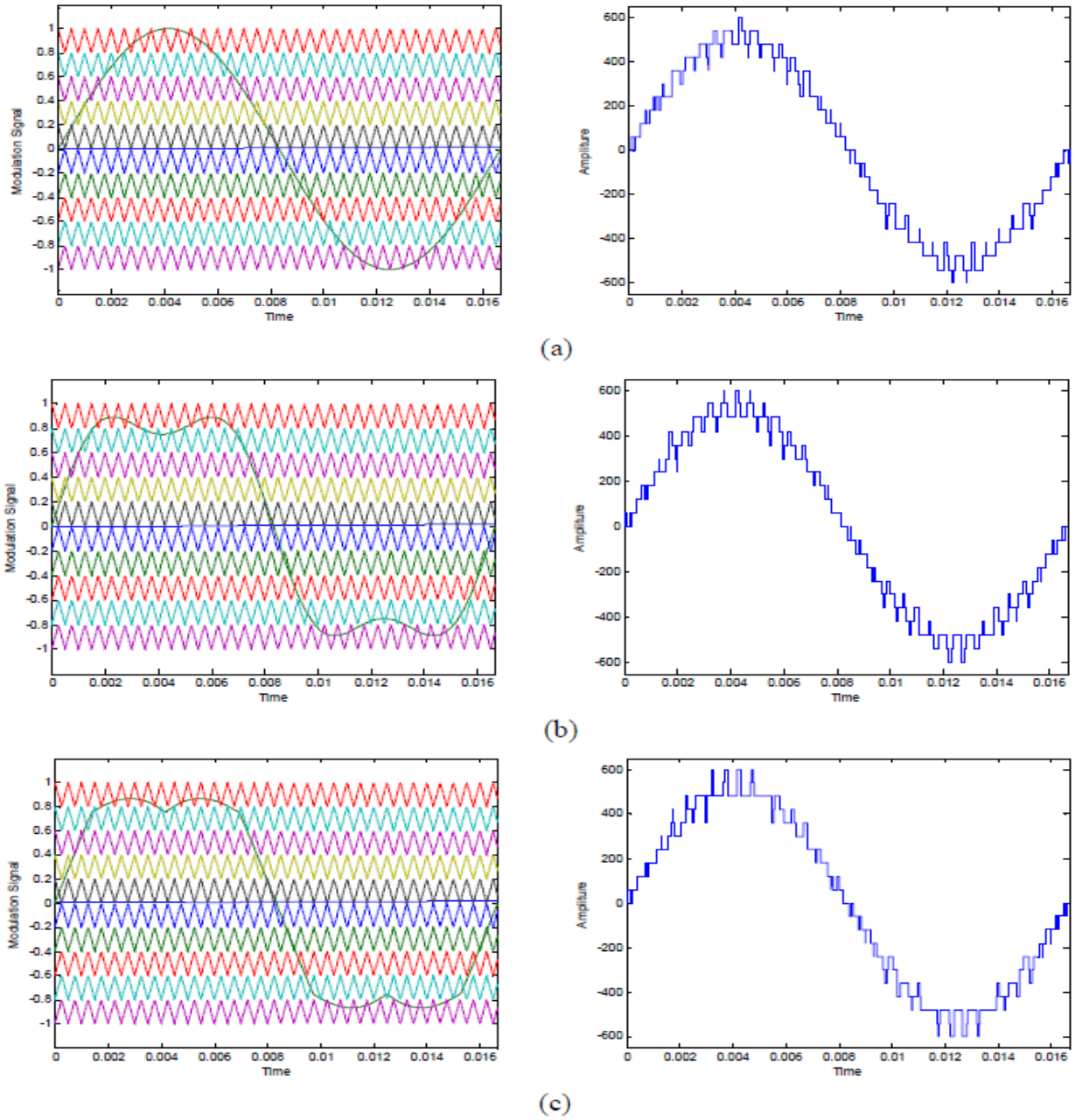
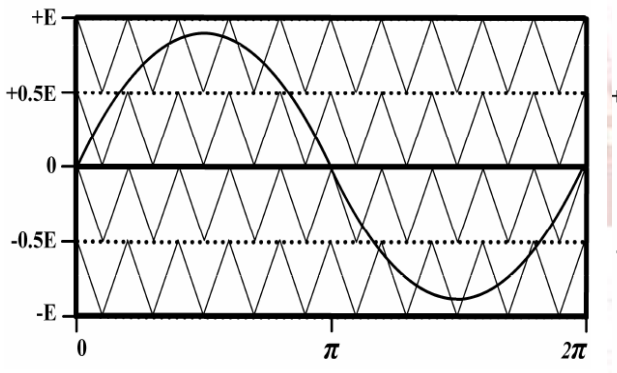


Figure 2.5. Simulation of Modulation Signals and Their Line-Line Output Voltage Using Five Separate dc Sources (60 volts each dc source) Cascaded Multilevel Inverter with Three Major Conventional Carrier-Based PWM Techniques at Unity Modulation Index and 2 kHz Switching Frequency. (a) SPWM, (b) THPWM, (c) SVM.

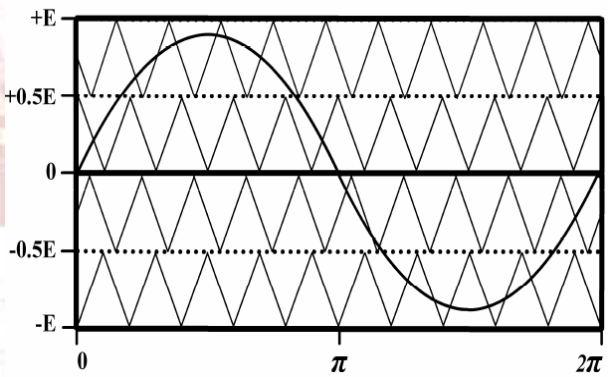
In order to achieve better dc link utilization at high modulation indices, the sinusoidal reference signal can be injected by a third harmonic with a magnitude equal to 25% of the fundamental;

its line-line output voltage is shown in Fig. 2.5 (b). As can be seen in Fig. 2.5(b) and (c), the reference signals have some margin at unity amplitude modulation index. Obviously, the dc utilization i.e. the ratio of the output fundamental voltage to the dc link voltage of THPWM and SVM are better than SPWM in the linear modulation region [14][19].

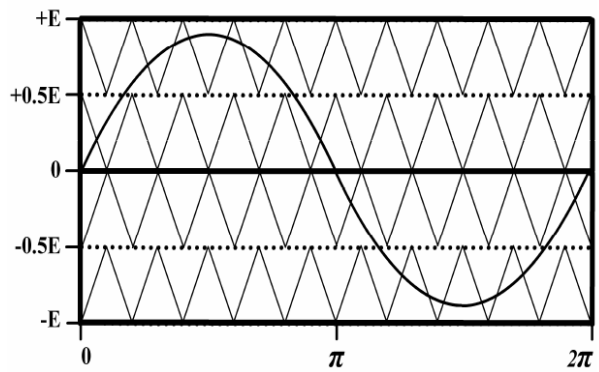
A. Sinusoidal PWM (SPWM) Technique: The pulse width modulation schemes are simple to implement as well as the provide flexibility in control. This basic principle of this scheme is to compare the reference signal (V_r) with a high frequency carrier wave (V_c) i.e. usually triangular or Inverted U type. When $V_r > V_c$, the PWM output will be high (state +1) and, for $V_r < V_c$ it will be low (state -1). In multilevel PWM generation the reference signal is compared by these carriers for definite bands. Thus, different SPWM can be achieved by different techniques of arranging carrier wave as shown in Fig. 2.6 and table 2.5 gives the description of carrier wave [19].



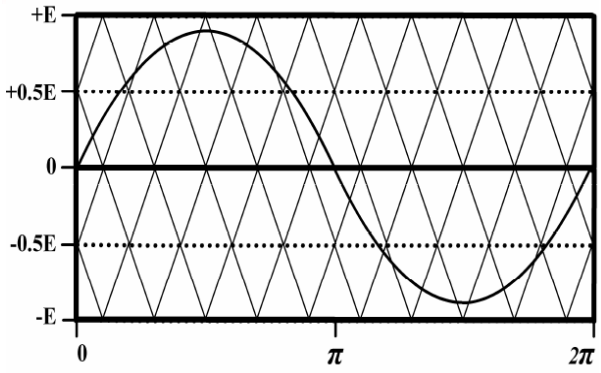
(a) PD-SPWM



(b) PS –SPWM



(c) POD –SPWM



(d) APOD- SPWM

Figure 2.6 Different Type of PWM Techniques.

Table 2.5 Different Arrangements of Carrier Wave for SPWM Technique:

Type of SPWM	Meaning	Description
PD	Phase Disposition	All carriers have same phase (Fig. 2.6 a)
PS	Phase Shifted	For each carrier, phase displacement equals $360/(N-1)^0$ and is successively added on the next carrier (Fig. 2.6 b)
POD	Phase Opposition Disposition	All carriers located above zero reference have the same phase, but they have displaced 180^0 phase displacement respect to those located below zero reference (Fig. 2.6 c)
APOD	Alternative Phase Opposition Disposition	A 180^0 phase displacement is imposed between each carrier (Fig. 2.6 d)

B. Subharmonic PWM : Unlike SPWM which does not modulate the signal at zero crossing, the SH-PWM scheme modulates the signal even at zero crossings. SH-PWM for m multiple levels is extended as m-1 carriers with the same frequency f_c and the same amplitude A_C are disposed such that the occupied bands are contiguous [20]. The reference waveform has peak-to-peak amplitude A_m, a frequency f_m, and its zero centred in the middle of the carrier set. Continuously comparing the reference signal with each of the carrier signals, the active device corresponding to that carrier is switched on when the reference is greater than a carrier signal and it is switched off when the reference is less than a carrier signal. In multilevel inverters, the amplitude modulation index, m_a, and the frequency ratio, m_f, are defined as:

$$\boldsymbol{m_a = \frac{A_m}{(m-1)A_c}} \quad \textbf{(2.1)}$$

$$\boldsymbol{m_f = \frac{f_c}{f_m}} \quad \textbf{(2.2)}$$

Fig. 2.7 demonstrates a set of carriers (m_f = 21) for a six-level diode-clamped inverter and a sinusoidal reference, or modulation, waveform with an amplitude modulation index of 0.8. The resulting output voltage of the inverter is also shown in the same Fig. [24].

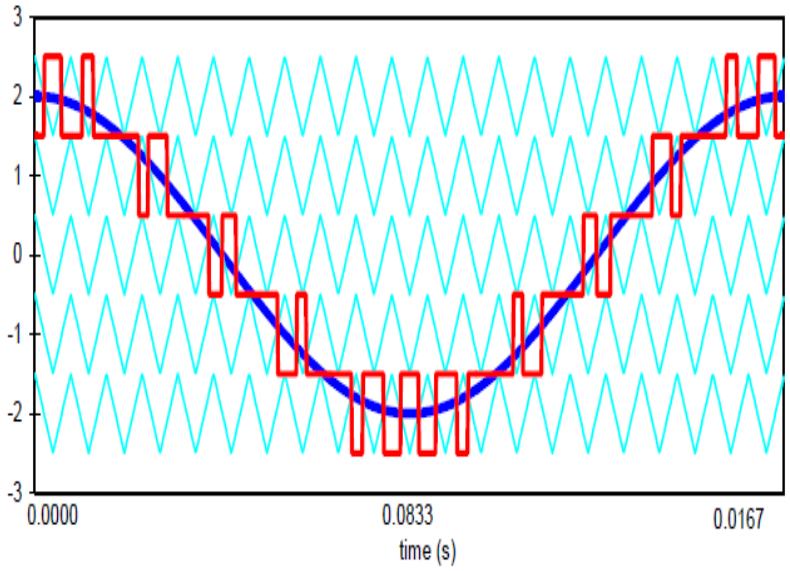


Figure 2.7 Multilevel Carrier-Based SH-PWM Showing Carrier Bands, Modulation Waveform, and Inverter Output Waveform (m = 6, m_f = 21, m_a = 0.8).

C. Switching Frequency Optimal PWM: One another method for multilevel inverter is switching frequency optimal PWM (SFO-PWM) which is similar to SH-PWM except that a zero sequence (triplen harmonic) voltage is added to each of the carrier waveforms [21]. In this method the instantaneous average of the maximum and minimum of the three reference voltages (V_a^*,V_b^*,V_c^*) is obtained and, then this value is subtracted from each of the individual reference voltages i.e.

$$\boldsymbol{V_{offset}} = \frac{\mathbf{max}(V_a^*,V_b^*,V_c^*)+\boldsymbol{min}(V_a^*,V_b^*,V_c^*)}{2} \quad \textbf{(2.3)}$$

$$\boldsymbol{V_{aSFO}^*} = \boldsymbol{V_a^*} - \boldsymbol{V_{offset}} \quad \textbf{(2.4)}$$

$$\boldsymbol{V_{bSFO}^*} = \boldsymbol{V_b^*} - \boldsymbol{V_{offset}} \quad \textbf{(2.5)}$$

$$\boldsymbol{V_{cSFO}^*} = \boldsymbol{V_c^*} - \boldsymbol{V_{offset}} \quad \textbf{(2.6)}$$

All of the three reference waveforms in the carrier band are centred because of this addition of the triplen offset voltage which makes it equivalent to using space vector PWM [22, 23]. Fig. 2.8 and 2.9 depicts the SH- PWM and SFO- PWM generation which utilize different frequencies for different triangular wave carrier bands. This method is highly effective to balance the device switching for all the levels in a diode clamped inverter [24].

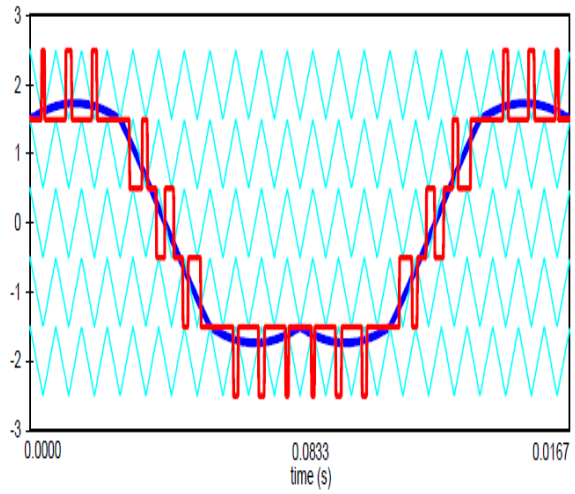


Figure 2.8 Multilevel Carrier-Based SFO-PWM Showing Carrier Bands, Modulation Waveform and Inverter Output Waveform (m = 6, m_f = 21, m_a = 0.8).

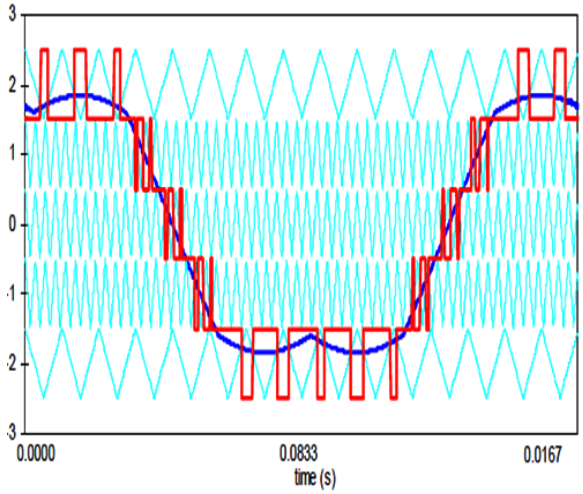


Figure 2.9 SFO-PWM where Carriers Have Different Frequencies (m_a = 0.85, m_f = 15 for $Band_2$, $Band_{-2}$; m_f= 55 for $Band_1$, $Band_{-1}$, $Band_0$, ϕ = 0.10 rad).

D. Modulation Index Effect on Level Utilization: A multilevel inverter is unable to make use of all of its levels at very low modulation indices [25]. Fig. 2.10 presents the simulation results of output voltage waveform at amplitude modulation indices of 0.5 and 0.15. Fig. 2.10 (a) clearly shows the unused band for amplitude modulation indices less than 0.6 in a six-level inverter which indicates that the switches in this band are not functioning. Fig. 2.10 (b) shows how at modulation index less than 0.2 a multilevel inverter operates as traditional two-level inverter as only the middle switches change state.

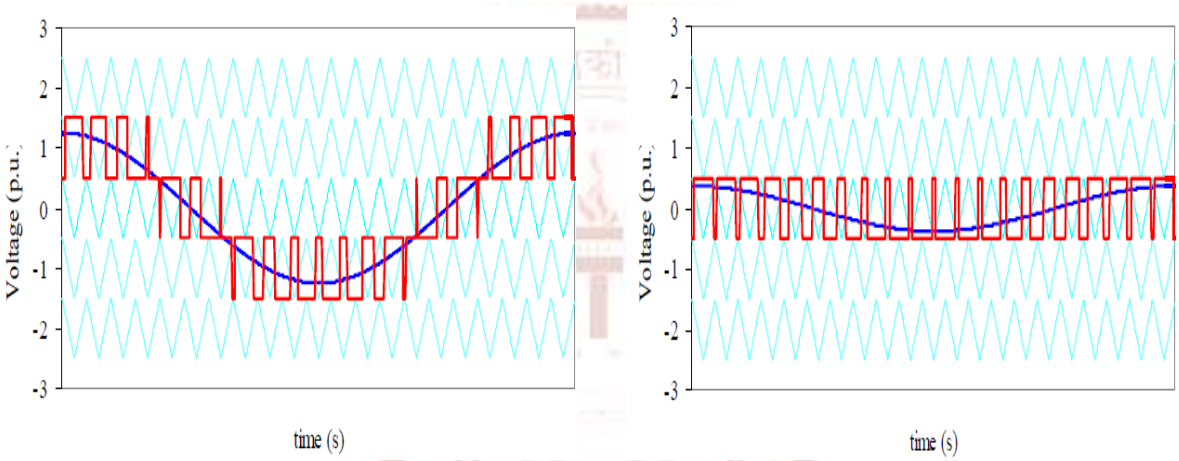
The minimum modulation index m_{amin} for which a multilevel inverter controlled with SH-PWM makes use of all of its levels, m, is

$$\boldsymbol{m_{amin} = \frac{m-3}{m-1}} \qquad \textbf{(2.7)}$$

Table 2.6 shows that the maximum modulation index before pulse dropping (overmodulation) occurs are 1.000 for SH-PWM and 1.155 for SFO-PWM [25]. Thus it can be observed whenever a multilevel inverter operates at modulation indices much less than 1.000, not all of its levels are utilized for the generation of the output voltage. Also as the number of levels in the inverter increases, level usage is also prone to suffer [14],[25].

Table 2.6. Modulation Index Ranges Without Level Reduction (Min) or Pulse Dropping Because of Overmodulation (Max):

Levels	SH-PWM		SFO-PWM	
	Min	Max	Min	Max
3	0.000	1.000	0.000	1.155
4	0.333	1.000	0.385	1.155
5	0.500	1.000	0.578	1.155
6	0.600	1.000	0.693	1.155
7	0.667	1.000	0.770	1.155
8	0.714	1.000	0.825	1.155
9	0.750	1.000	0.866	1.155
10	0.778	1.000	0.898	1.155
11	0.800	1.000	0.924	1.155
12	0.818	1.000	0.945	1.155
13	0.833	1.000	0.962	1.155



(a) SH-PWM, m = 6, m_a = 0.5 **(b) SH-PWM, m = 6, m_a = 0.15**

Figure 2.10 Level Reductions in a Six-Level Inverter at Low Modulation Indices.

Even during low modulation periods, all multiple levels can be used by rotating level usage in the inverter after each modulation cycle. Taking advantage of the redundant output voltage states in such manner reduces the switching stresses on some of the inner levels by using the unused outer voltage levels [26].

For low modulation indices use of redundant line-line voltage states are available in a diode - clamped inverters [26]. However these inverters do not have any phase redundancies. The available number of redundant states in an m-level diode-clamped inverter for an output voltage state (i, j, k) can be calculated as,

$$N_{\substack{redundancies \\ available}} = m - 1 - [\max(i, j, k) - \min(i, j, k)] \quad (2.8)$$

As the modulation index is increased, more redundant states can be obtained. Table 2.7 shows the number of distinct and redundant line-line voltage states available in a six-level inverter for different output voltages [25],[26].

Table 2.7 Six-Level Inverter Line-Line Voltage Redundancies:

max(i,j,k)-min(i,j,k)	# Distinct States	# Redundancies per Distinct State	Total # of States
0	1	5	6
1	6	4	30
2	12	3	48
3	18	2	54
4	24	1	48
5	30	0	30
Total	*91*	---	*216*

E. Increasing Switching Frequency at Low Modulation Indices: Even after making switching frequency double to sufficiently rotate the level usage in odd – level inverter in case of amplitude modulation indices less than 0.5, the thermal losses remain within the limits of the device. The modulation index at which frequency doubling can be accomplished varies with the levels in even level inverter [25]. As the switching frequency increases, inverter is able to compensate for higher frequency harmonics. This yields a waveform that follows reference more closely.

Table 2.8 Increased Switching Frequency Possible at Lower Modulation Indices [25]:

Inverter Levels	Modulation Index, m_a		Frequency Multiplier
	Min	Max	
3	0.000	0.500	2X
4	0.000	0.333	3X
5	0.250	0.500	2X
	0.000	0.250	4X
6	0.200	0.400	2X
	0.000	0.200	5X
7	0.333	0.500	2X
	0.167	0.333	3X
	0.000	0.167	6X
8	0.285	0.428	2X
	0.142	0.285	3X
	0.000	0.142	7X
9	0.25	0.500	2X
	0.125	0.250	4X
	0.000	0.125	8X
10	0.333	0.444	2X
	0.222	0.333	3X
	0.111	0.222	4X
	0.000	0.111	9X
11	0.333	0.500	2X
	0.200	0.333	3X
	0.000	0.200	5X
12	0.272	0.454	2X
	0.181	0.272	3X
	0.090	0.181	5X
	0.000	0.090	11X
13	0.333	0.500	2X
	0.250	0.333	3X
	0.167	0.250	4X
	0.0833	0.167	6X
	0.000	0.0833	12X

To accomplish this doubling of inverter frequency, a prototype of a seven-level diode-clamped inverter with an amplitude modulation index of 0.4 is switched such as that the reference waveform is centred in the upper three carrier bands and lower three carrier bands from one cycle to next cycle. Half of the switches "rest" in every other cycle and not endorse any switching losses. However, this method is limited to only three-wire systems as the diode-clamped inverter has line-line redundancies and no phase redundancies. Synchronization of transition for all three phases while moving from one carrier set to the next set is essential at the discontinuity. In this process of frequency doubling, all three phases add or subtract the following number of states (or levels) every other reference cycle [14],[25]:

$$\boldsymbol{h_a(j+1) = h_a(j) + (-1)^j . \frac{[m-1]}{2}} \quad \textbf{(2.9)}$$

At modulation indices closer to zero, even more increase in the switching frequency is possible by rotating the reference waveform among the carrier bands for a few cycles before returning to a previous set of switches for use. The switches are able to absorb higher losses as they "rest" for a few cycles. In redundant switching each of the three phases in the seven-level inverter will have three change states of switch pairs at the end of every reference cycle which results in additional switching losses. However, this redundant switching loss is around five percent of the total switching loss compared to the switching loss associated with the normal PWM switching [25].

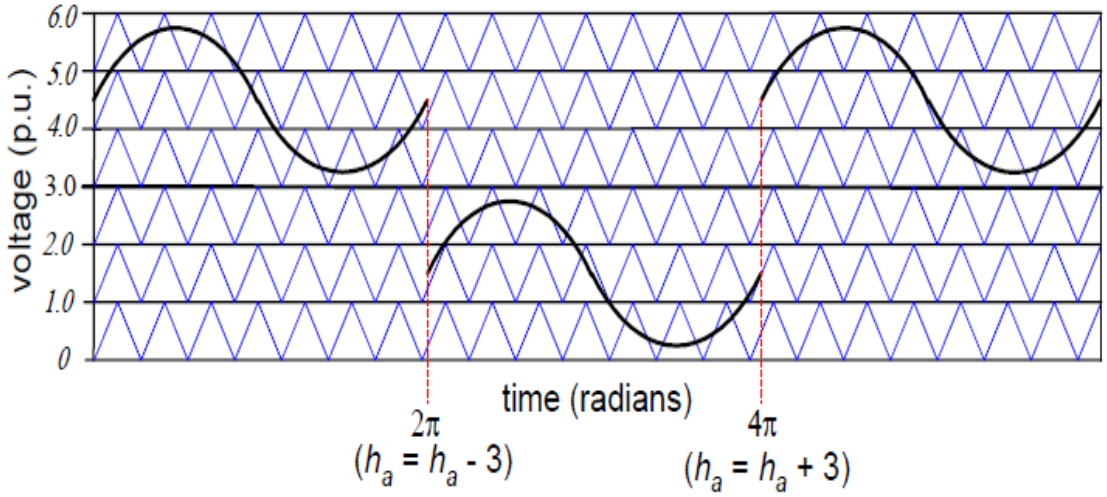


Figure 2.11 Reference Rotation among Carrier Bands Rotation at Low Modulation Indices (m_a< 0.5).

To increase the carrier frequency by a factor of three, two methods of rotating the reference waveform among three different regions (top, middle, and bottom) for modulation indices less than 0.333 in a seven-level inverter are shown in Fig. 2.12 and Fig. 2.13. Former is preferred to later as it requires only four redundant states switching as against of eight redundant states switching of later in every three reference cycles. In general preferred one will have ½ of the redundant switching losses that the alternate method would have.

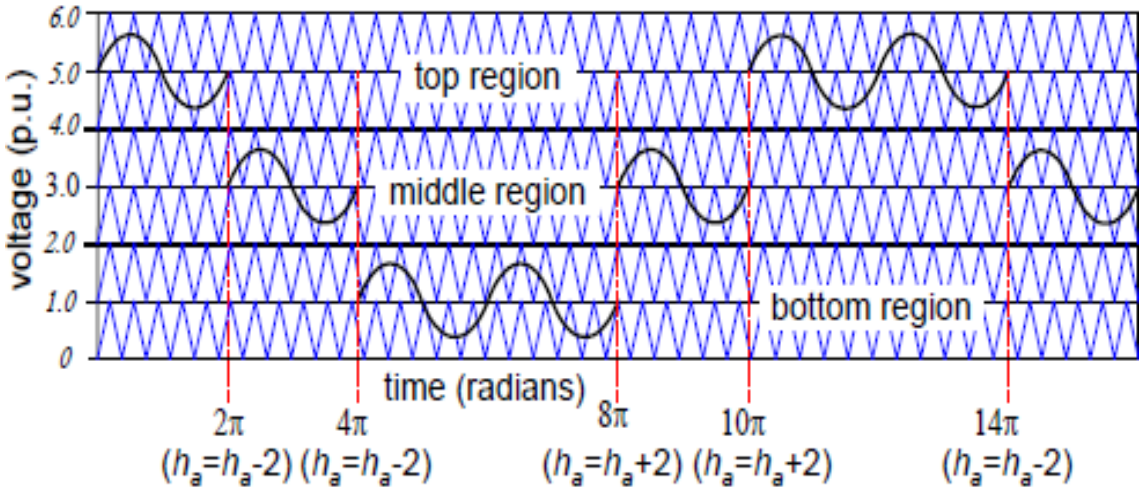


Figure 2.12 Preferred Method of Reference among Carrier Bands with 3× Carrier Frequency at Very Low Modulation Indices.

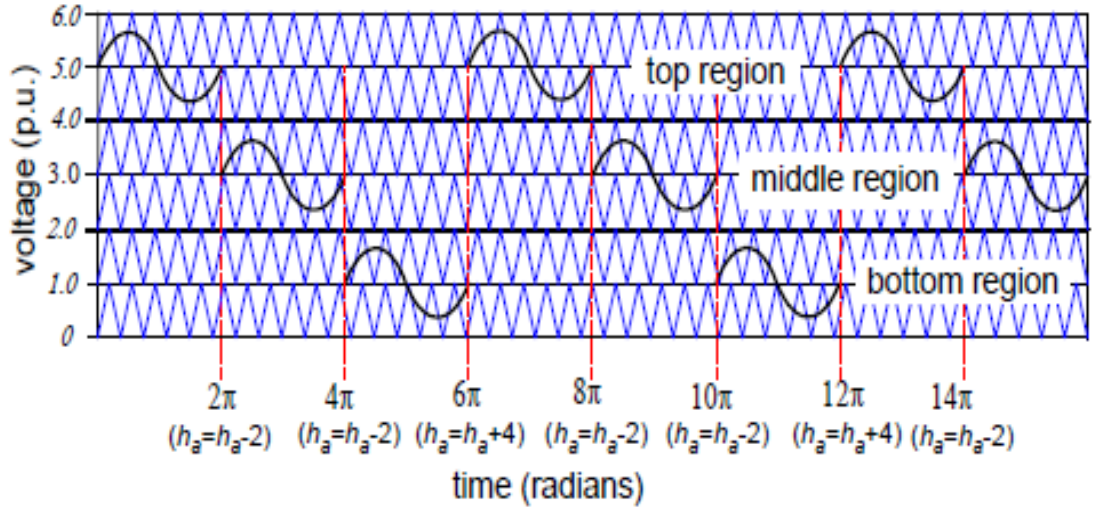


Figure 2.13 Alternate Method of Reference Rotation among Carrier Bands with 3× Carrier Frequency at Very Low Modulation Indices.

The cascaded H-bridges inverter has phase redundancies in addition to the line-line redundancies [25][26] . As the output voltage in each phase of a three-phase inverter can be generated independently of the other two phases when only phase redundancies are used, phase redundancies can be easily exploited compared to line-line redundancies. In a cascaded inverter each active device's duty cycle is balanced over (m-1)/2 modulation waveform cycles regardless of the modulation index is obtained using these phase redundancies [27]. The pulse rotation technique with a PWM output voltage waveform represents a more effective means of controlling a driven motor at low speeds [28,29]. In this control the output waveform can have a high switching frequency even though individual levels can still switch at a constant switching frequency of 60 Hz.

F. Multilevel space vector PWM: The two-level space vector pulse width modulation technique has been extended to more than three levels for the diode-clamped inverter [30]. Fig. 2.14 shows what the space vector d-q plane looks like for a six-level inverter. Fig. 2.15 represents the equivalent dc link of a six-level inverter as a multiplexer that connects each of the three output phase voltages to one of the dc link voltage tap points [31].

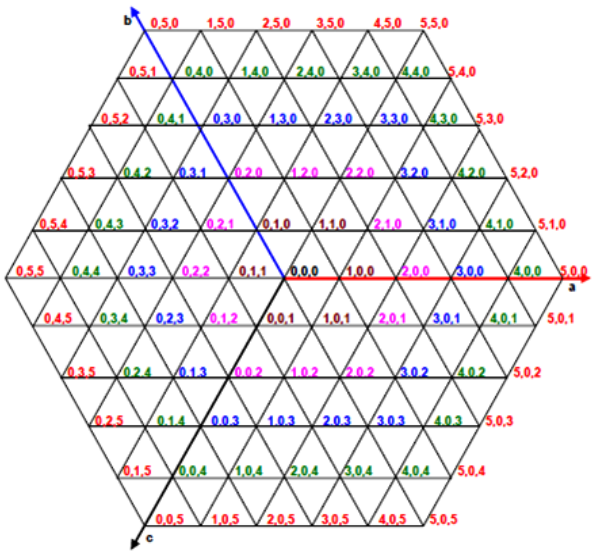


Figure 2.14 Voltage Space Vector for a Six–Level Inverter.

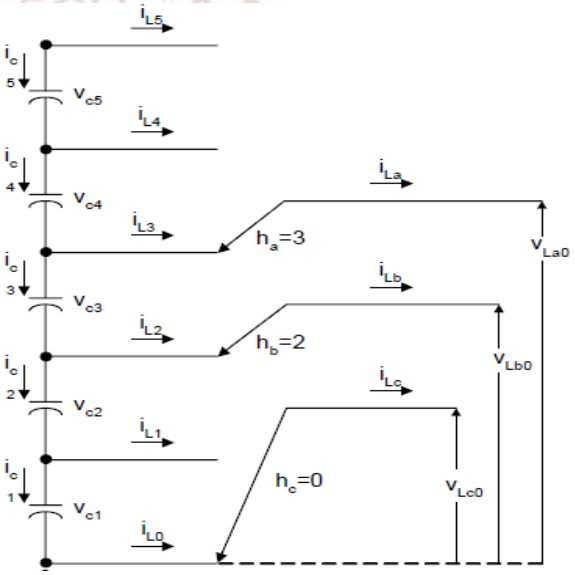


Figure 2.15 Multiplexer Model of a Diod-Clamped Six-Level Inverter.

A specific three-phase output voltage state of the inverter is represented with a specified point on the space vector plane. For example V_{an} = $3V_{dc}$, V_{bn} = $2V_{dc}$, and V_{cn}= $0V_{dc}$ is represented with (3, 2, 0). Fig. 2.15 shows the corresponding connections between the dc link and the

output lines for this point in a six-level inverter. An algebraic equation to represent the output voltages in terms of the switching states and dc link capacitors has been given as [32]. For n = m-1 where m is the number of levels in the inverter:

$$\boldsymbol{V_{abc0} = H_{abc} V_c}\ , \qquad \textbf{(2.10)}$$

$$\textbf{where } \boldsymbol{V_c = [V_{c1}\ V_{c2}\ V_{c3}\ \dots\ V_c]^T, H_{abc} = \begin{bmatrix} h_{a1} & h_{a2} & h_{a3} & \dots & h_{an} \\ h_{b1} & h_{b2} & h_{b3} & \dots & h_{bn} \\ h_{c1} & h_{c2} & h_{c3} & \dots & h_{cn} \end{bmatrix}, V_{abc0} = \begin{bmatrix} V_{a0} \\ V_{b0} \\ V_{c0} \end{bmatrix}, and}$$

$$\boldsymbol{h_{aj} = \sum_{j}^{n} \delta(h_a - j)}$$

where h_a is the switch state and j is an integer from 0 to n, and where $\delta(x) = 1$ if $x \geq 0$, $\delta(x) = 0$ if $x < 0$.

The point (3, 2, 0) on the space vector plane can also represent the switching state of the converter. Each integer indicates the number of upper switches with state ON in each phase leg for a diode-clamped converter. As an example, for $h_a = 3$, $h_b = 2$, $h_c = 0$, the H_{abc} matrix for his particular switching state of a six-level inverter would be

$$\boldsymbol{H_{abc} = \begin{bmatrix} 0 & 0 & 1 & 1 & 1 \\ 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}}$$

States for which a particular output voltage can be generated by more than one switch combination are termed redundant switching state. These states are possible even at lower modulation indices, or at any point other than those on the outermost hexagon. For an output voltage state (x, y, z) in an m-level diode-clamped inverter, the number of redundant states available can be calculated as m – 1 – max(x, y, z) [32]. As the voltage vector in the space vector plane gets closer to the origin (or the modulation index decrease), redundant states also increase. For a six-level diode-clamped inverter, the zero voltage states are (0, 0, 0), (1, 1, 1), (2, 2, 2), (3, 3, 3), (4, 4, 4), and (5, 5, 5) i.e. equal to the number of levels, m. The number of possible switch combinations is equal to the cube of the level (m^3). The number of distinct or unique states for an m-level inverter can be given by

$$\boldsymbol{m^3 - (m-1)^3 = \left[6 \sum_{n=1}^{m-1} n\right] + 1} \qquad \textbf{(2.11)}$$

Therefore, the number of redundant switching states for an m-level inverter is $(m-1)^3$. Table 2.9 summarizes the available redundancies and distinct states for a six-level diode-clamped inverter.

Table 2.9 Line-Line Redundancies of Six-Level Three-Phase Diode-Clamped Inverter [30]:

Redundancies	Distinct States	Redundant States	Unique State Coordinates: (a, b, c) where 0≤ a,b,c ≤5
5	1	5	(0,0,0)
4	6	24	(0,0,1),(0,1,0),(1,0,0),(1,0,1),(1,1,0),(0,0,1)
3	12	36	(p,0,2),(p,2,0),(0,p,2),(2,p,0),(0,2,p,),(2,0,p) where p≤2
2	18	36	(0,3,p),(3,0,p),(p,3,0),(p,0,3),(3,p,0),(0,p,3) where p≤3
1	24	24	(0,4,p),(4,0,p),(p,4,0),(p,0,4),(4,p,0),(0,p,4) where p≤4
0	30	0	(0,5,p),(5,0,p),(p,5,0),(p,0,5),(5,p,0),(0,p,5) where p≤5
Total	*91*	*125*	*216 total states*

In multilevel PWM, three triangle vertices, V_1, V_2, and V_3, to a reference point V* are opted as to minimize the harmonic components of the output line-line voltage [33,34]. The respective time duration, T_1, T_2, and T_3, required of these vectors is obtained by solving the following equations:

$$\overrightarrow{\boldsymbol{V_1}}\boldsymbol{T_1} + \overrightarrow{\boldsymbol{V_2}}\boldsymbol{T_2} + \overrightarrow{\boldsymbol{V_3}}\boldsymbol{T_3} = \boldsymbol{V^*T_s} \quad \textbf{(2.12)}$$

$$\boldsymbol{T_1 + T_2 + T_3 = T_s} \quad \textbf{(2.13)}$$

where T_S is the switching period. (2.11) can be broken-up into the real and imaginary part of used terms:

$$\boldsymbol{V_{1d}T_1 + V_{2d}T_2 + V_{3d}T_3 = V_d^*T_1} \quad \textbf{(2.14)}$$

$$\boldsymbol{V_{1q}T_1 + V_{2q}T_2 + V_{3q}T_3 = V_q^*T_{s1}} \quad \textbf{(2.15)}$$

Equations (2.12) through (2.15) can then be solved for T_1, T_2, and T_3 as follows:

$$\begin{bmatrix} \boldsymbol{T_1} \\ \boldsymbol{T_2} \\ \boldsymbol{T_3} \end{bmatrix} = \begin{bmatrix} \boldsymbol{V_{1d}} & \boldsymbol{V_{2d}} & \boldsymbol{V_{3d}} \\ \boldsymbol{V_{1d}} & \boldsymbol{V_{2d}} & \boldsymbol{V_{3d}} \\ \boldsymbol{1} & \boldsymbol{1} & \boldsymbol{1} \end{bmatrix}^{-1} \begin{bmatrix} \boldsymbol{V_d^*T_s} \\ \boldsymbol{V_d^*T_s} \\ \boldsymbol{T_s} \end{bmatrix} \quad \textbf{(2.16)}$$

Some others proposed space vector methods do not require the nearest three vectors, but these methods generally make the control algorithm more complex. Redundant switch levels can be used to improved DC bus utilization [35]. Fig. 2.16 presents the sinusoidal reference voltage (circle of points) and the inverter output voltages in the d-q plane.

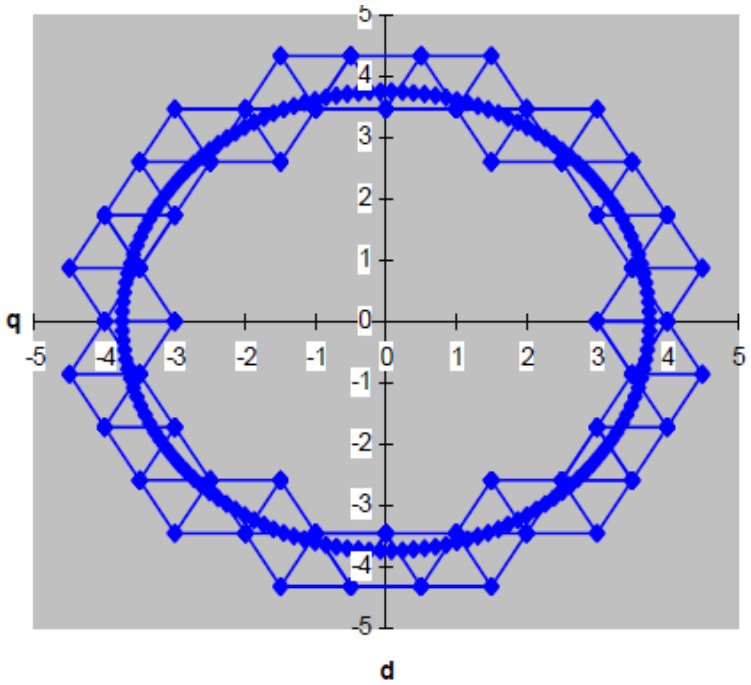


Figure 2.16 Sinusoidal Reference and Inverter Output Voltage States in d-q Plane.

The equations for the currents through the dc link capacitors can be given as

$$\boldsymbol{i_{cn} = -i_{Ln}}\text{ , and} \qquad \textbf{(2.17)}$$

$$\boldsymbol{i_{c(n-j)}| = -i_{L(n-j)} + i_{L(n-j+1)}}\text{ ,} \qquad \textbf{(2.18)}$$

where j=1,2,3.....n-1.

The choice of redundant switching states can be used to determine which capacitors will be charged/discharged or unaffected during the switching period. However, this method of capacitor voltage balancing is quite complicated in selecting which of the redundant states to use. Constant use of redundant switching states increases switching frequency on the expense of lower efficiency of the inverter. Optimized space vector switching sequences for multilevel inverters have been proposed in [36].

G. Selective harmonic elimination virtual stage PWM method: The proposed selective harmonic elimination method made use of Fourier Transform [37-38]. For a stepped waveform with s steps, the Fourier Transform follows:

$$\boldsymbol{V(\omega t) = \frac{4V_{dc}}{\pi}\sum_{n=1}^{\infty}[\cos(n\theta_1) + \cos(n\theta_2) + \ \ldots + \ \cos(n\theta_s)]\sin\frac{(n\omega t)}{n}},\qquad \textbf{(2.19)}$$

where n=1,3,5 ...

From (2.17), the magnitudes of the Fourier coefficients when normalized with respect to V_{dc} are as follows:

$$\mathbf{H(n)} = \frac{\mathbf{4}}{\boldsymbol{\pi n}}[\mathbf{cos(n\theta_1) + cos(n\theta_2) + \ ... + \ cos(n\theta_s)}], \qquad \mathbf{(2.20)}$$

where n = 1,3,5,7 ...

The conducting angles θ_1, θ_2 , ... θ_s can be chosen to cancel the predominant lower frequency harmonics for minimising the total harmonic distortion in voltage.

Virtual stage PWM method achieves a wide range of modulation index with minimized THD [39-41]. In this method Unipolar Programmed PWM and the fundamental frequency switching scheme are combined to utilize the advantages of both schemes. In Unipolar Programmed PWM, the switches connected to the involved DC voltage are switched "on" and "off" several times per fundamental cycle. The output voltage waveform shape is determined by the switching pattern. For fundamental switching frequency method, the switching angles are equal to the number of DC sources. However, for the Virtual Stage PWM method, the number of switching angles is not equal to the number of DC voltages as shown in Fig. 2.18 for four switching angles; only two DC voltages are used.

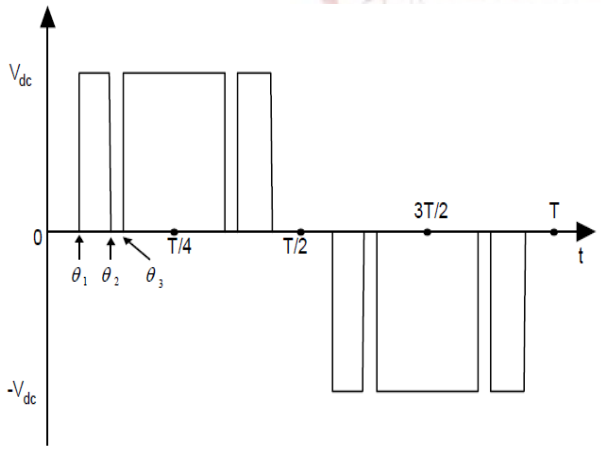


Figure 2.17 Unipolar switching output waveform.

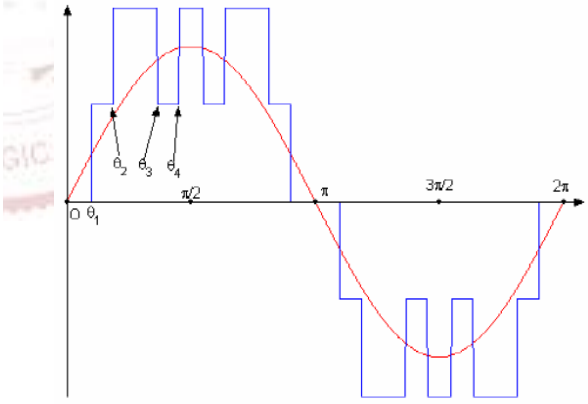


Figure 2.18 Output waveform of Virtual Stage PWM control.

Bipolar Programmed PWM and Unipolar Programmed PWM could be used for modulation indices too low for the applicability of the multilevel fundamental frequency switching method. Virtual Stage PWM will produce output waveforms with a lower THD most of the time even for low modulation indices [41].

For cancelling the 5th, 7th , 11th and 13th harmonics equations from (2.18) will be as follows:

$$\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) + \cos(5\theta_4) + \cos(5\theta_5) = 0$$

$$\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) + \cos(7\theta_4) + \cos(7\theta_5) = 0$$

$$\cos(11\theta_1) + \cos(11\theta_2) + \cos(11\theta_3) + \cos(11\theta_4) + \cos(11\theta_5) = 0 \quad (2.21)$$

$$\cos(13\theta_1) + \cos(13\theta_2) + \cos(13\theta_3) + \cos(13\theta_4) + \cos(13\theta_5) = 0$$

$$\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4) + \cos(\theta_5) = 5m_a$$

Newton's method using numerical solution can be used to solve these equations but it needs good initial guesses, and solutions are not guaranteed. The resultant method employing elimination resultant theory has been proposed in to solve the transcendental equations for switching angles [42-44]. However, as the number of DC voltages or the number of switching angles increases, the degrees of the harmonic current characterized polynomials in these transcendental equations become bulky. Thus, these methods are employed with is solved by Newton's method to compute the fundamental frequency switching angle.

H. SVC [45]: This conceptually different control strategy based on the space-vector theory works with low switching frequencies and does not generate the mean value of the desired load voltage in every switching interval as in SVM. In this method a voltage vector is delivered to load to minimize the space error or distance to the reference vector. The high density of vectors makes complex modulation scheme involving the three vectors adjacent to the reference. This method is simple and attractive for high number of levels. The error in terms of the generated vectors with respect to the reference will be high for low number of levels; eventually increasing the load current ripple.

I. Direct Torque Control (DTC) [46]**:** The DTC technique which was developed for low-voltage two level inverters as a substitute to the field oriented method to effectively control torque and flux in ac drives have been applied in multilevel inverters along with hysteresis current control [47].

J. Capacitor Balancing Techniques: A diode-clamped multilevel inverter would have to sacrifice its output voltage performance to obtain balanced voltages for real power conversion.

Additional voltage balancing circuits as back-to-back rectifier/inverter system and dc chopper etc. can be used proper voltage balancing control [48, 49].

Voltages balance is easier for capacitor-clamped structure when the load current is dc for their application in high-voltage dc/dc conversions [51]. However, when applied to power conversion in which no real power is involved, such as reactive power compensation, the voltage balancing and ripple in capacitor-clamped inverter become difficult as each phase leg has its own floating capacitors that handle the phase current [50], [51].

2.2.3 Multilevel D-STATCOM

The cascaded inverter can be used for universal power conditioning of power systems as, it is able to provide reactive and harmonic compensation [48],[52]. A multilevel inverter based D-STATCOM provides lower costs, higher performance, less electromagnetic interference (EMI), and higher efficiency than the traditional PWM inverter based D-STATCOM for both series and parallel compensation. Due to losses in the circuit component and limited controller resolution, a slight voltage imbalance can occur even in self- balancing cascaded multilevel D-STATCOM. A control scheme for reactive and harmonic compensation with ensures dc voltage balance is proposed in the literature [48].

A laboratory prototype of 30kVar STATCOM based on a 17-level cascaded H-bridges inverter, has been used for suppression of harmonics by multi-pulse optimization incorporating switching-pattern swapping technique to equalise the exchanged power sharing among inverter cells by controlling the fundamental output voltages across them [53]. Direct power control (DPC) based custom power devices employed with multilevel inverter enhance custom power devices capacity, flexibility of choosing voltage vectors and harmonics minimizing capability[54].

Hysteresis current control technique can be adopted for controlling the injected current by the FCMLI-based D-STATCOM [55]. This scheme also allows preferential charging or discharging of the flying capacitors to balance their voltage. The reported state feedback control-based compensating technique resulted in balanced and distortion free source currents and regulated terminal voltages in multilevel inverters based D-STATCOMs for systems with non-stiff source. Switching strategies have been proposed FCMLI-based D-STATCOM as well

as DCMLI-based D-STATCOM, which ensures an efficient utilization of all output voltage states of the inverter for tracking the reference [56]. Other schemes for nullifying the effect of the dc component in the system neutral current on the dc capacitor voltages are developed [58].

In the voltage control mode, a distribution static compensator (D-STATCOM) employed with cascaded multilevel inverters which are controlled with phase-shifted multicarrier unipolar pulse width modulation (PWM) technique, reduces the ripple magnitude in the switching function and allows the use of smaller carrier amplitude under closed loop. This technique increases the forward gain and, in this way, improves the tracking characteristics. However, the mathematics to obtain the condition for smooth modulation is quite complex as it uses the Bessel's function representation of the PWM output and the switching condition of the multilevel inverter- controlled system [57]. The sliding-mode control of cascaded H-bridge multilevel-inverter (CHBMLI)-controlled systems using multiband hysteresis modulation have been proposed in the literature [58]. This technique swaps each cell sequentially to provide the self-balancing capability to capacitors supported system [58]. The multiband hysteresis modulation shifts the switching components toward higher frequencies. Thus, the switching ripple content in the output controlled voltage is reduced.

Reference current tracking and dc-link voltage maintaining can be simultaneously achieved under unbalanced conditions by decoupling the STATCOM into three single-phase systems. The average active power in each phase can be adjusted to a target value determined by the dc-link voltage control loop [59]. Addressing the problem of unbalance capacitor voltages using zero-sequence voltage and negative-sequence current allows the STATCOM to operate flexibly under normal power system condition and does not need wide margin of dc capacitor voltage under large asymmetrical condition [60].

With the use of individual voltage balancing strategy the converters can be commutated at fundamental line frequencies while maintaining the delivered reactive power equally distributed among all the H-bridges of the converter [64]. Small signal model of the controller can balance individual dc capacitor voltages when H-bridges run with different switching patterns and have parameter variations. This feedback control strategy based controller can work well in all operation regions: the capacitive mode, the inductive mode, and the standby mode without having any restriction on the cascade number [65].

Besides these many system have been proposed in literature to address the specific power quality problem such as mitigation of flicker caused by arc furnace , fault imbalance, reactive power control etc. [61-65].These system are designed for FACTS devices but by using proper power electronics device they can work as custom power.

Different type of multilevel inverter and their control strategies have been elaborated for different levels and the scope for their use in electric system. These systems have their own merit and demerits. However, some converter shows a promising future of improve power quality in the case of high voltage distribution.

2.3 Identified Research Areas

As we learn from the suggested readings the Cascaded H- Bridge Multilevel Inverter based D-STATCOM extends its use in power quality improvement as compared to its DCMI and FCMI counterpart for its various advantages upon two other topologies. The control of CHBMI is proposed by many researchers. However, these control strategies compromise on different levels as some are rather complex to implement or if they are simple they do not provide as sufficient control on the system. Thus, we find some research areas as:

Need of developing a new scheme to control the cascaded H- Bridge multilevel inverter, which is easier to implement and do not compromise with system performance even in harsh abnormal conditions occurring in the systems. Control Scheme which can be adopted for wide range of operation such as capacitive or inductive and increase number of voltage level.

2.4 Conclusions

In this chapter we have studied the various type of inverter and their control strategies. Among all inverter CHBMI shows a promising future. So this topology is used as the main concern in coming chapters. The research gap between the existing control schemes have been found on the basis of their performance and ease of implementation. However, new control scheme which have all the inherent qualities of previous generation but without any complexities is required in future works. For this a new controller is proposed in the upcoming chapters.

CHAPTER 3

MODELLING OF THE MULTILEVEL D-STATCOM

CHAPTER 3

MODELLING OF THE MULTILEVEL D-STATCOM

3.1 General

An accurate and well-defined model is a prerequisite for designing a system with superior control. As discussed in previous chapters, a cascaded multilevel H- bridge multilevel inverter (CHBMI) based D-STATCOM have many advantages over diode clamped multilevel inverter (DCMI) and fly capacitor type multilevel inverter (FCMI). Ease of control, and flexibility for future upgradation are one of the key advantages offered by CHBMI based D-STATCOM. However, these cascaded-multilevel VSCs have excessive number of controlled variables, so to reduce the complexities in design; a model based on practical assumptions and proposed variable definitions is proposed in this chapter. The model is designed in such a manner that it can be utilized for any number of levels of cascaded bridge inverter. In the later part of the chapter the model of the proposed control scheme is also presented.

3.2 Modelling of the CHBMI based Multilevel D-STATCOM

A multilevel D-STATCOM system is composed of three main parts: a multilevel-cascaded VSC with separated DC source, the coupling (inter-phase) inductors and a controller. The coupling inductors filter out the current harmonic components that are generated in system due to modulation techniques used to control the converters. Beside this they also serve as the reactive power coupler between the AC and DC side of the system.

A multilevel-cascaded converter is employed with a number of identical H-bridge converters, whose output terminals are connected in series as shown for phase a in Fig. 3.1. It can be observed that each H-bridge includes four IGBT switches with anti-parallel diodes and a dc-link capacitor. The output voltage is summation of those H-bridge converters, i.e.,

$$V_{kn} = V_{k1} + V_{k2} + V_{k3} + ... + V_{kN} \quad (3.1)$$

where k, is the phase notation a, b or c and,

N is the number H bridge converter per phase.

Assuming $v_{dc1} = v_{dc2} = v_{dc3} = \ldots = v_{dcN} = V_{dc}$ in the steady state conditions, each H-bridge module can produce three different voltage levels: −Vdc, 0, Vdc. With reference to the upper bridge, it is possible to set $v_{a1} = +V_{dc}$ by turning on power switches S_{11} and S_{14} and $v_{a1} = -V_{dc}$ by turning on power switches S_{12} and S_{13}. Moreover, it is possible to set $v_{a1} = 0$ by turning on either S_{11} and S_{12} or S_{13} and S_{14}, the lower bridge operates in a similar manner. Therefore, total number of output-phase voltage levels and the maximum number of line-to-line voltage levels that can be synthesized are equal to 2N+1 and 4N+1 respectively. It should be noted that the switching states of S_{x1}, S_{x2} (x = 1, 2, 3, … , N) must be complementary to those of S_{x3}, S_{x4} (x = 1, 2, 3, … , N) in order to avoid short circuit of the H-bridge.

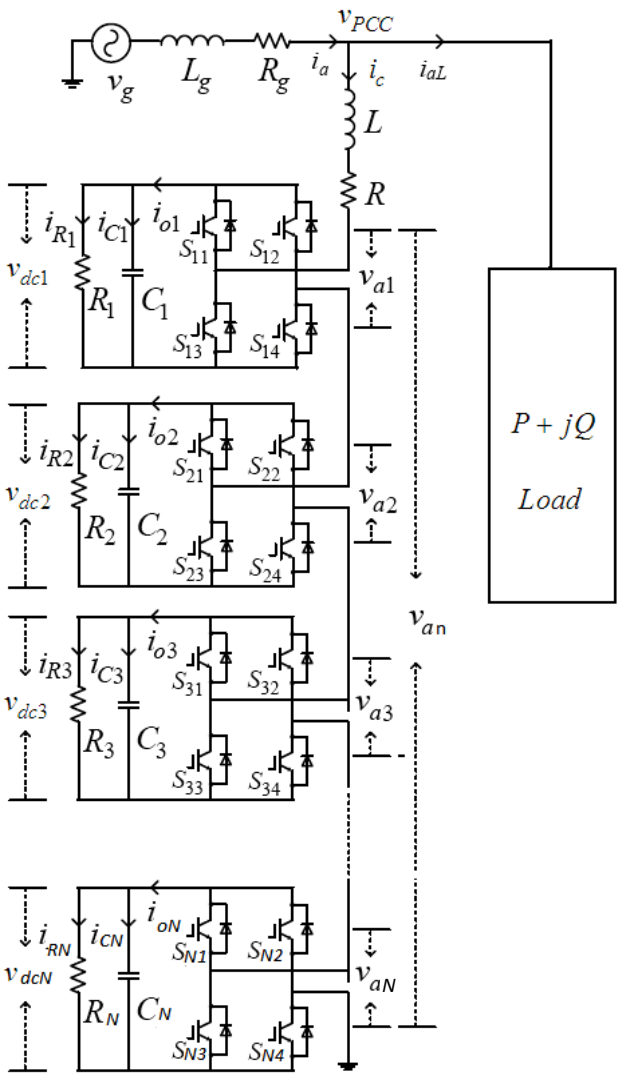


Figure 3.1 Schematic Diagram of the Proposed DSTATCOM Based on Cascaded H-bridge Multilevel Inverter.

To derive the state-space equations for the multilevel DSTATCOM, the switching functions are defined for individual H-bridges, as denoted by:

$$S_1 = S_{11} \cdot S_{14} - S_{12} \cdot S_{13},$$
$$S_2 = S_{21} \cdot S_{24} - S_{22} \cdot S_{23},$$
$$S_3 = S_{31} \cdot S_{34} - S_{32} \cdot S_{33}, \quad (3.2)$$
$$\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots$$
$$S_n = S_{N1} \cdot S_{N4} - S_{N2} \cdot S_{N3}$$

The value of S_x (x = 1, 2, 3, …. , N) indicates the dynamic process of charging and discharging between the dc-link capacitors C_1, C_2 and C_3. Supposing the D-STATCOM current i_c is positive, then the capacitor Cx (x = 1, 2, 3, …, N) is charging if $S_x = 1$, discharging if $S_x = -1$, and not undergoing any of these processes if $S_x = 0$. Complementary phenomenon appears if the inverter current is negative.

The following assumptions are made for deriving the mathematical model of the cascaded H-bridge inverters.

a) The grid is assumed to be AC current source at fundamental frequency;

b) The power losses of the whole system are categorized as series loss and parallel loss. The series loss and losses in interfacing inductor are represented as equivalent series resistance (ESR) whereas parallel losses pertains to shunt connected resistances across the dc link capacitors, corresponding to the active power loss of the H-bridge, including blocking loss, capacitor loss and absorbing circuit loss, etc.

The differential equation describing the dynamics of the coupling inductor between the cascaded H-bridge inverter and the grid can be derived as:

$$\boldsymbol{v_{PCC} = Ri_c + L\frac{di_c}{dt} + S_1 v_{dc1} + S_2 V_{dc2} + S_3 v_{dc3} + \cdots + S_N v_{dcN}} \quad (3.3)$$

where the variable v_{PCC} represents grid voltage at the point of common coupling (PCC), *L* represents the inductance of the coupling inductor and *R* represents the equivalent series resistance (ESR). The variables v_{dc1}, v_{dc2}, v_{dc3} and v_{dcN} are actual voltages across the dc-link capacitors of the cascaded H-bridge inverter, which may not equal to the reference voltage V_{dc}^* during dynamic process.

According to the Kirchoff 's law, the currents flowing into the dc-link capacitors C1, C2 and C3 can be expressed as:

$$\boldsymbol{i_{c1} = C_1 \frac{dv_{dc1}}{dt} = i_{o1} - i_{R1} = S_1 i_c - \frac{v_{dc1}}{R_1}}$$

$$\boldsymbol{i_{c2} = C_2 \frac{dv_{dc2}}{dt} = i_{o2} - i_{R2} = S_2 i_c - \frac{v_{dc2}}{R_2}}$$

$$\boldsymbol{i_{c3} = C_3 \frac{dv_{dc3}}{dt} = i_{o3} - i_{R3} = S_3 i_c - \frac{v_{dc1}}{R_3}} \quad \textbf{(3.4)}$$

$$\vdots \qquad \vdots \qquad \vdots$$

$$\boldsymbol{i_{cN} = C_N \frac{dv_{dcN}}{dt} = i_{oN} - i_{RN} = S_N i_c - \frac{v_{dc1}}{R_N}}$$

where R_1, R_2 and R_3 are the equivalent resistance of each H-bridges, representing the parallel losses. The variables i_{o1}, i_{o2} and i_{o3} represent the total dc-link current and i_{R1}, i_{R2} and i_{R3} represent the current in the dc-link resistance of the individual H-bridge module. The equations (3.3)-(3.4) can be rearranged as:

$$\boldsymbol{\frac{di_c}{dt} = \frac{v_{PCC}}{L} - \frac{R}{L} i_c - \frac{S_1 v_{dc1}}{L} - \frac{S_2 v_{dc1}}{L} - \frac{S_3 v_{dc3}}{L} - \dots - \frac{S_N v_{dcN}}{L}}$$

$$\boldsymbol{\frac{dv_{dc1}}{dt} = \frac{S_1 i_c}{C_1} - \frac{v_{dc1}}{R_1 C_1}}$$

$$\boldsymbol{\frac{dv_{dc2}}{dt} = \frac{S_2 i_c}{C_2} - \frac{v_{dc2}}{R_2 C_2}} \quad \textbf{(3.5)}$$

$$\boldsymbol{\frac{dv_{dc3}}{dt} = \frac{S_3 i_c}{C_3} - \frac{v_{dc3}}{R_3 C_3}}$$

$$\vdots \qquad \vdots \qquad \vdots$$

$$\boldsymbol{\frac{dv_{dcN}}{dt} = \frac{S_N i_c}{C_N} - \frac{v_{dcN}}{R_N C_N}}$$

Let the vector of state variables be denoted with $X = [i_c \; v_{dc1} \; v_{dc2} \; v_{dc3} \; .... \; v_{dcN}]^T$ and the input vector with $U = [v_{PCC} \; 0 \; 0 \; .... \; 0]^T$. Then (3.5) can be expressed in compact matrix form:

$$\mathbf{X = AX + BU} \quad \textbf{(3.6)}$$

where matrices A and B can be represented as:

$$A = \begin{bmatrix} -\frac{R}{L} & -\frac{S_1}{L} & -\frac{S_2}{L} & -\frac{S_3}{L} & \dots\dots\dots & -\frac{S_N}{L} \\ \frac{S_1}{C_1} & -\frac{1}{R_1C_1} & 0 & 0 & \dots\dots\dots & 0 \\ \frac{S_2}{C_2} & 0 & -\frac{1}{R_2C_2} & 0 & \dots\dots\dots & 0 \\ \frac{S_3}{C_3} & 0 & 0 & -\frac{1}{R_2C_2} & \dots\dots\dots & 0 \\ \vdots & \vdots & \vdots & \vdots & \dots\dots\dots & \vdots \\ \frac{S_N}{C_N} & 0 & 0 & 0 & 0 & -\frac{1}{R_NC_N} \end{bmatrix}$$

$$B = \begin{bmatrix} \frac{1}{L} & 0 & 0 & 0 & \dots\dots\dots & 0 \\ 0 & 0 & 0 & 0 & \dots\dots\dots & 0 \\ 0 & 0 & 0 & 0 & \dots\dots\dots & 0 \\ \vdots & \vdots & \vdots & \vdots & \dots\dots\dots & \vdots \\ 0 & 0 & 0 & 0 & \dots\dots\dots & 0 \end{bmatrix}$$

3.3 Control Strategy for the D-STATCOM

The proposed control scheme for the system is developed in two phase. In the first phase a simple and easy to implement control scheme for the multilevel inverter is developed. This control scheme is later developed for advanced control of Multilevel D-STATCOM. This approach gives proper insight of the switching pulse generation and the D-STATCOM operation and control. The controller is designed in such a manner that it can also be upgraded as the voltage level of the distribution generation increases.

3.3.1 Control of the Cascaded H- Bridge Multilevel Inverter

The control of the CHBMI comprises of the PWM signal generation unit for creating the switching input to the bridge. As in a leg of multiple H-bridge is represented as a phase, the switching pulse for all the bridges are to be generated in such manner that full system voltage requirement for all the bridge contribute to synthesize the desired level of voltage. In any case when system is operated at lower voltage level, the H-bridge at higher level should be bypassed accordingly. The scheme should also be capable of keeping all the phases (a, b and c) in balance as any imbalance can disturb the switching pattern. This can severely affect the system performance and the full utilization of the system is not achievable. Fig. 3.2 shows the schematic diagram of the proposed system.

In the first step a reference signal for the control of inverter is generated. The reference signal is comprised of three sinusoidal signals which are 120^0 phase apart from each other, thus creating

a balanced signal unit. Each of these signals is processed for the generation of pulses in different phase legs. This approach makes the switching of all three phases balance.

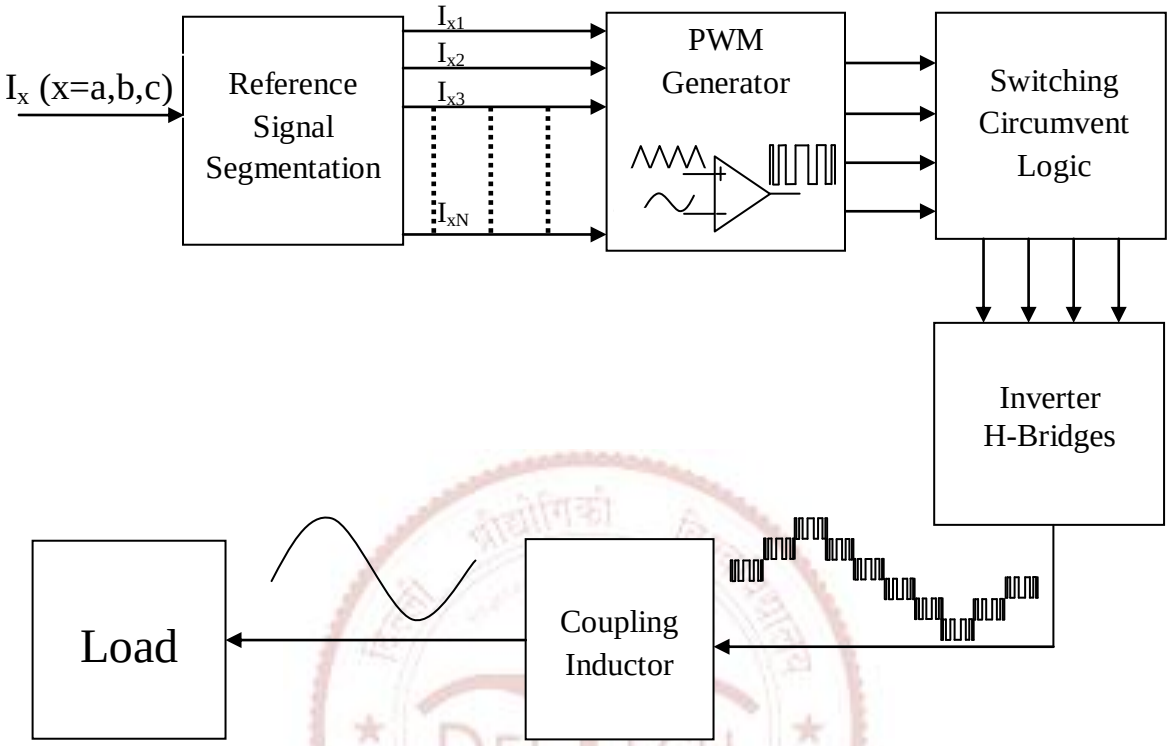


Figure 3.2 Schematic Diagram of Control Module for the CHBMI.

The reference signal is divided into as many signals as required for the desired level generation. The split signals are fed into PWM generators where they are compared to a triangular wave of high frequency. The modulation index for the PWM generator is chosen according to the (2.1). The switching pulses are continuously generated for each segmented signal to generate the desired level of voltage.

However, when the voltage level is low the upper bridges have to be bypassed. To obtain such characteristic of the switching pulse, a switching circumvent logic for a level is applied. This logic modifies the PWM switching pulse in such manner that the level, that is to be bypass, has both of its gate drive combination S_{X1} and S_{X2} or S_{X3} and S_{X4} on at the same instant. Thus, there is short circuit in this particular case and the contribution of corresponding H-bridge is zero as no current flows by the DC source.

The firing of IGBTs in every H- bridges generates a particular level of voltage. These levels are then synthesized to obtain the multilevel voltage output. This voltage waveform has very low THD as it follows the sine wave. The waveform can be further smoothen with the help of filters. The ripples in the generated wave are later eradicated with the inter-phase inductor. An addition filter can also be used for the harmonic filtration.

3.3.2 Control of the Multilevel D-STATCOM

The controller of the D-STATCOM requires additional accessaries in the Cascade H- bridge multilevel inverter as it has to provide online management of the reactive power. The reactive power requirement in the system is to be calculated and compensated using the device. As mentioned in reported text that the reactive power can be managed by injection/absorption of reactive current, this requires the calculation of the active and reactive components of the voltage and current. Also the injected power should be in synchronism with the power flowing in the mains, for this purpose the reactive power generated requires the use of PLL which keeps a track of all the phases of system voltages and currents. The controller for the proposed scheme is shown in Fig. 3.3.

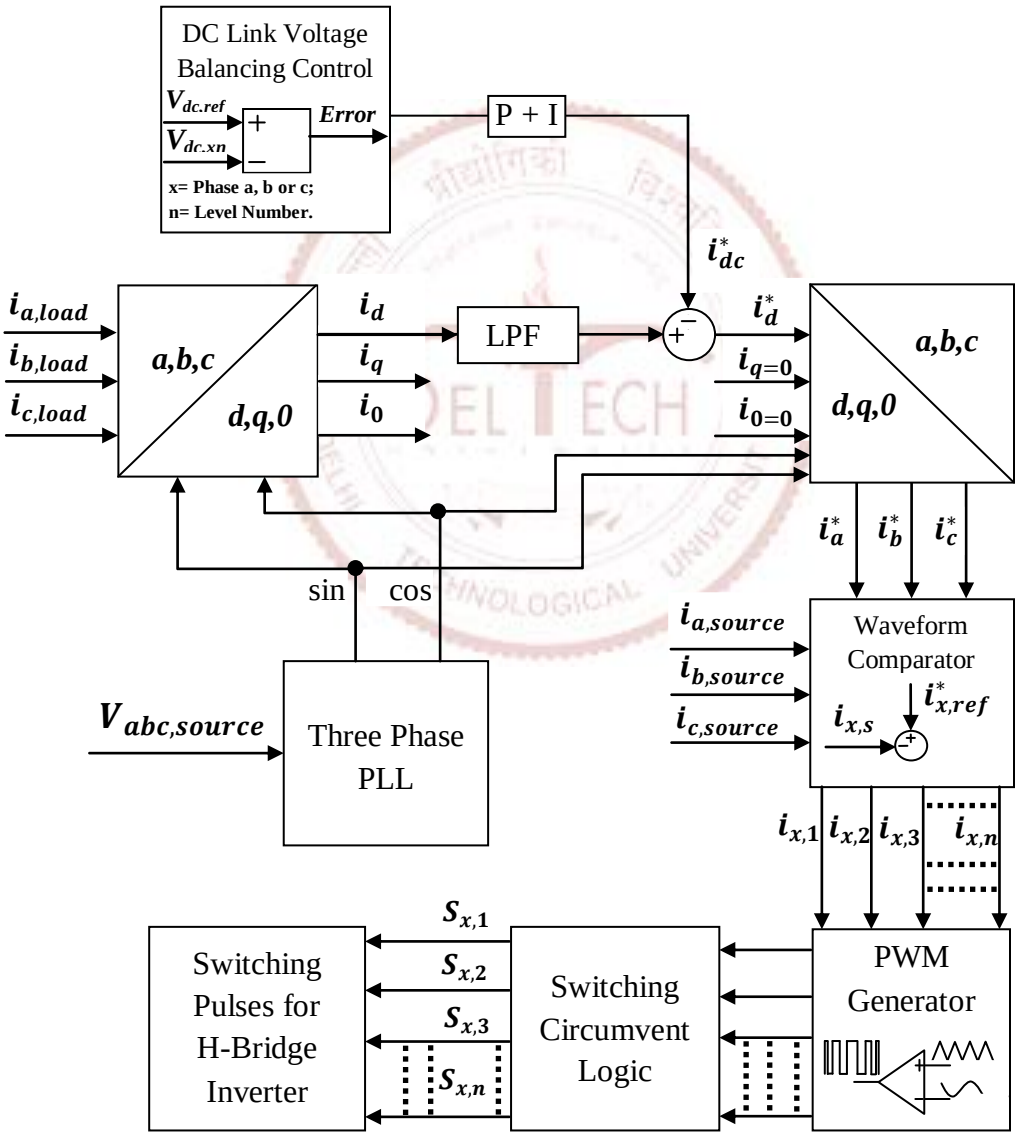


Figure 3.3 Schematic Diagram of Control Module for CHBMI based D-STATCOM.

Phase Locked Loop: Since active and reactive components of power are derived by using the phase angle of the source voltage, the synchronization of the multilevel D-STATCOM to the source becomes less critical. For this reason phase locked loops are employed in the system to track the phase of the source side and synchronizing it with the generated reference waveform at every instant .The mathematical presentation of the PLL can be explained for an arbitrary source voltage as:

$$\boldsymbol{v_s(t) = V_1 \sin(\omega_0 t + \varphi_1) + \sum_{n=2}^{N} V_n \sin(n\omega_0 t + \varphi_n)} \quad \textbf{(3.7)}$$

where φ_1 and φ_n are the initial phase angle of the fundamental and the nth order harmonic component, respectively. The DC offset can be neglected for the preciseness. The phase angle of the fundamental component voltage can be expressed as:

$$\boldsymbol{\varphi_1 = \Delta\theta_1 + \theta_1} \quad \textbf{(3.8)}$$

where θ_1 and $\Delta\theta_1$, are the estimated phase angle of the fundamental supply voltage and the estimation error, respectively, obtained from the PLL. Substituting (3.8) into (3.7) yields:

$$\boldsymbol{v_s(t) = V_1 cos(\Delta\theta_1) \sin(\omega_0 t + \varphi_1) + V_1 sin(\Delta\theta_1) cos(\omega_0 t + \varphi_1) + \sum_{n=2}^{N} V_n sin(n\omega_0 t + \varphi_n)} \quad \textbf{(3.9)}$$

Thus the original signal can be obtained by adjusting coefficients $V_1 \cos(\Delta\theta_1)$ and $V_1 \sin(\Delta\theta_1)$ in the (3.9). Also as the (3.9) indicate that the pre-knowledge of the phase angle of the original signal is not required.

De-coupled control of active and reactive power: This technique enables the decoupled control of active and reactive power. The current and voltage are transformed in the synchronising rotating reference frame to obtain active and reactive power. When the reference frame is synchronised with the phase voltage, the d-axis and q-axis components of load current represents the active and reactive power respectively. These components can be utilized for the regulation of the corresponding power transaction between the source, load and compensating device.

The mathematical formulation for the decoupled control of active power and reactive power is possible with the use of Clarke and Parks' transformation. If the current at the point of common

coupling be $i_{a,l}$, $i_{b,l}$ and $i_{c,l}$, then mathematical modelling for the management of reactive power can be presented as:

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 1/2 & 1/2 \\ 0 & \sqrt{3}/2 & \sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} i_{a,l} \\ i_{b,l} \\ i_{c,l} \end{bmatrix} \quad \textbf{(3.10)}$$

Here i_α, i_β and i_0 represent the α axis, β axis and zero sequence current respectively. One motivation of using $\alpha\beta 0$ transformation is separation of zero sequence current. As no zero sequence current flow in case of three phase three wire system, i_0 can be eliminated from the system, thus resulting in simplification. Also in case of a balanced three phase four wire system, this component is zero. Hence (3.10) can be modified as:

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 1/2 & 1/2 \\ 0 & \sqrt{3}/2 & \sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_{a,l} \\ i_{b,l} \\ i_{c,l} \end{bmatrix} \quad \textbf{(3.11)}$$

This equation can be used to obtain the direct axis, i_d and quadrature axis, i_q components of the current by the rotating i_α and i_β with the reference wave generated by the PLL.

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \cos(\omega_1 t) & -\sin(\omega_1 t) \\ \sin(\omega_1 t) & \cos(\omega_1 t) \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \quad \textbf{(3.12)}$$

To filter the ripple, if any, in the calculated components of the current, the obtained components can be passed through a low pass filter. For the balancing the dc bus the voltage across the dc bus, say V_{dc}, is compared with a reference dc signal, $V_{dc,ref}$ and an error signal is generated. This error is controlled with the use of a PI controller.

$$i_{dc}^* = (K_P + K_I)(V_{dc} - V_{dc,ref}) \quad \textbf{(3.14)}$$

Thus the total active current requirement of the system can be obtained by summing the two dc component.

$$i_d^* = i_d + i_{dc}^* \quad \textbf{(3.15)}$$

By controlling only one current component corresponding power can be controlled. In the proposed, scheme direct axis current is used to generate α axis and β axis current component. These components are the indicators of the active power flowing in the system as they are synchronised with the source voltage.

$$\begin{bmatrix} i_{\alpha}^{*} \\ i_{\beta}^{*} \end{bmatrix} = \begin{bmatrix} \cos(\omega_1 t) & \sin(\omega_1 t) \\ -\sin(\omega_1 t) & \cos(\omega_1 t) \end{bmatrix} \begin{bmatrix} i_{d}^{*} \\ 0 \end{bmatrix} \quad \textbf{(3.16)}$$

This obtained α axis and β axis currents are used to produce the three phase reference current using the inverse Clarke transformation such as:

$$\begin{bmatrix} i_{a,lref}^{*} \\ i_{b,lref}^{*} \\ i_{c,lref}^{*} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_{\alpha}^{*} \\ i_{\beta}^{*} \end{bmatrix} \quad \textbf{(3.17)}$$

As explained this reference current have only active power required by the load. Comparing these values with the phase currents of the source ($i_{x,s}$; x= a,b,c) gives the value of reactive current flowing in the system. Thus, reactive power can be managed with taking the difference of two current as the reference waveform generating the PWM pulses.

$$\begin{bmatrix} i_{a,switch}^{ref} \\ i_{b,switch}^{ref} \\ i_{c,switch}^{ref} \end{bmatrix} = \begin{bmatrix} i_{a,s} \\ i_{b,s} \\ i_{c,s} \end{bmatrix} - \begin{bmatrix} i_{a,lref}^{*} \\ i_{b,lref}^{*} \\ i_{c,lref}^{*} \end{bmatrix} \quad \textbf{(3.18)}$$

These reference signals are segmented for the inputs to the PWM generator. The PWM generator switching pulses are generated in the same manner as explained in section 3.3.1. These PWM switching pulses trigger the various H-bridges' IGBTs of the D-STATCOM to synthesized the desired voltage level for reactive power management.

3.4 Conclusion

The step by step modelling of the proposed control scheme gives deep insight of the system behaviour. The presented model indirectly tackles the compensation of the reactive power as the load active current requirement of the system is obtained by separating it from the reactive

component. However, the switching pulses are generated as per the demanded reactive power by the load which is measured by the difference of desired active current for the load and the source current. This approach is highly effective as at any instant the source sees only active power at PCC. All of the reactive power demand is met with the D-STATCOM. Also employing current as a reference signal for PWM generation increase the system performance as it provides fast switching for the inverter circuit. The proposed system has simple mathematical formulation which can easily be implemented in MATLAB/SIMULINK environment. The MATLAB models for the cascaded H-bridge multilevel inverter as well as multilevel D-STATCOM based on these equations are presented in the next chapter.

CHAPTER 4

PERFORMANCE EVALUATION OF THE PROPOSED SYSTEM

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PERFORMANCE EVALUATION OF THE PROPOSED SYSTEM

4.1 General

This chapter presents the MATLAB/SIMULINK modelling and control of the multilevel structure used for power quality enhancement. The present chapter is divided in two sections. In the first section multilevel inverter topologies for different level is presented. The control scheme for different level inverters is developed as per the mathematical model presented in the previous chapter. The motivation behind this section is to corroborate the validity of generated PWM pulses and their application for switching the cascaded H-bridges as to synthesize the desired voltage level.

In the second section the multilevel cascaded H-bridge multilevel D-STATCOM is discussed for the concerned issue of reactive power management. The control scheme developed for the multilevel inverter is modified to suite for the D-STATCOM as the D-STATCOM is connected to the system as current controlled device whereas the inverter modelled behaves as voltage controlled device.

4.2 Cascade H-bridge Multilevel Inverter

Fig. 4.1 depicts the SIMULINK model of the 11 kV cascaded multilevel inverter feeding power to various loads. Different level inverter structure will be studied in the coming section. The inverter and different loads is connected trough resistive-inductive loads.

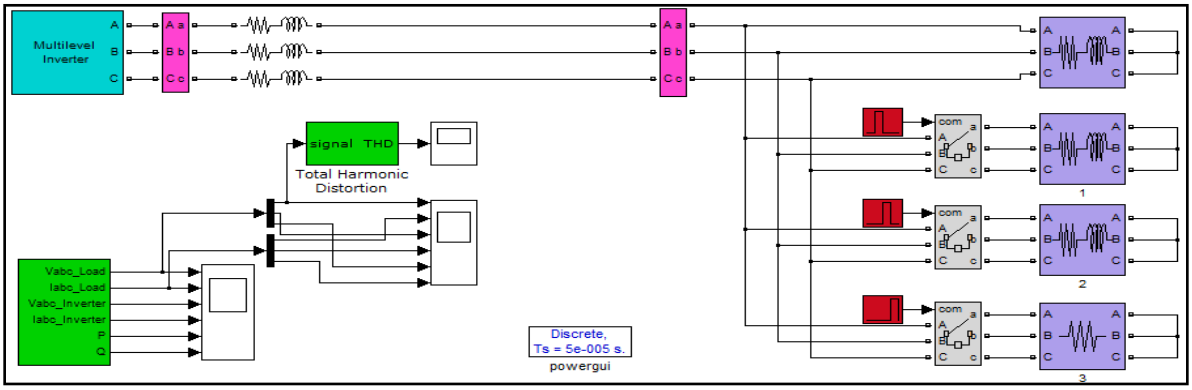

Figure 4.1 SIMULINK Model for Multilevel Inverter.

The switching of the loads is done at different instant to evaluate the performance of the system under load perturbations and dynamics of the system in response to their load switching between Point of Common Coupling (PCC) and loads. By varying the loads at different times many loading conditions can be obtained. The measurement unit is showed for the calculation of different parameters.

4.2.1 Three Level Inverter

4.2.1.1 Model Description

The model consists of single H-bridge in each phase leg as shown in Fig. 4.2.1. All the three H-bridge are connected at the same node with the ground. One H-bridge has two arms with two IGBTs in each arm. The IGBT have the snubber resistance of 100kΩ and snubber capacitance of infinity. This IGBT provides very low ohmic loss as the resistance of the device in running condition is of only 1mΩ. The forward voltage for the device as well as diode is set to be zero. Internal inductance of the diode is also set to the zero for the application purpose. Fall time and the rise time of the device are 1microsecond and the 2 microsecond respectively.

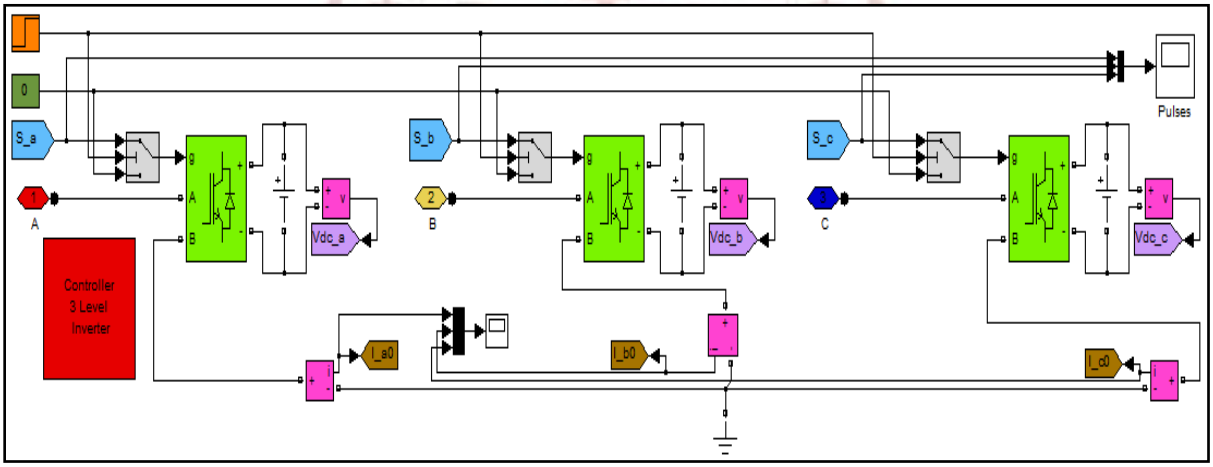

Figure 4.2.1 SIMULINK Model of Three Level Cascaded H-Bridge Multilevel Inverter.

Each H- Bridge is connected to DC voltage source of 11000 kV at its DC side for the generation of the AC voltage for the load. The switching is done through the subsystem shown as controller. The inside view of the controller is depicted in Fig. 4.2.2. The controller as mentioned above is modelled as per the scheme presented in the previous chapter. The PWM generator is developed as to produce PWM pulses at desired frequency of switching. The output

pulses from the PWM generator are fed into the switching circumvent circuit as the level generation requires the bypassing of the current.

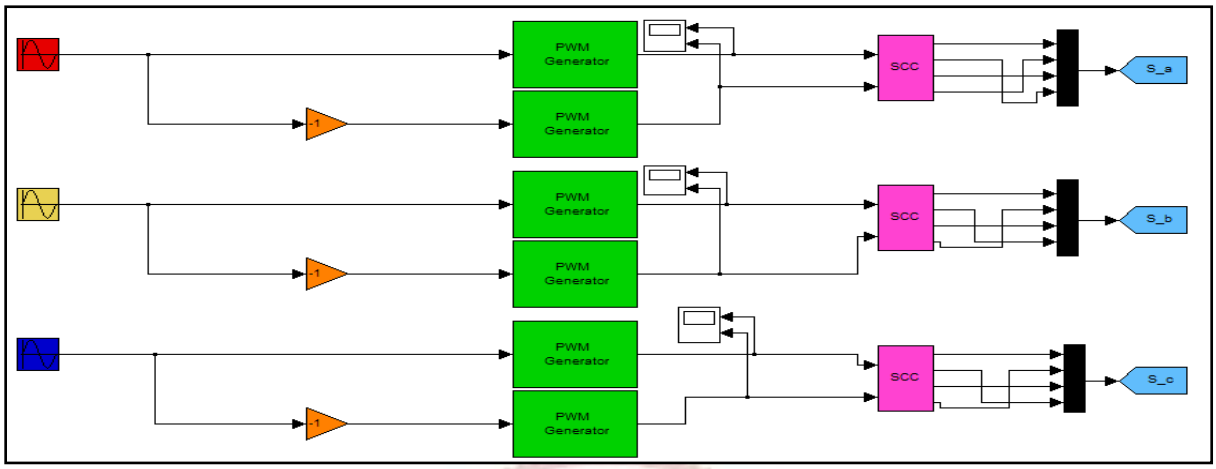

Figure 4.2.2 Controller for Three Level Cascaded H-Bridge Multilevel Inverter.

4.2.1.2 Results and Discussion

Fig. 4.3 demonstrates the various waveforms for the different parameters obtained from the switching of inverter. Power electronic devices are switched in at time 0.0 second with a load impedance of 7.80 + j5.70 Ω connected to the inverter. The voltage of 11kV (peak value) having three level (-11, 0, 11) kV is generated across the inverter terminal. A current of 930 A flows in the line and the voltage across the load is obtained to be 10.7kV. The current waveform has two peaks as the current due to reactive load. The active and reactive powers for this load are 3.88 MW and 1.59 MVAr respectively. At 0.25s load impedance is varied to 3.9 + j2.85 Ω, the multi-step voltage across the load is found to be 10.5kV. Active and reactive powers demanded by the load are 7.29MW and 2.98MVAr for this load. The current waveform follows the same pattern as previous load but with increased amplitude (1800 ampere). As the load impedance is varied to -0.266+ j4.089 Ω at 0.50 second, the multi-step voltage across load becomes 10.3kV. The current waveform increases to 2200 A with a notch at peak value due to highly inductive load. The transients also observed in the current of different phase, However, the same is subsided in 3 to 4 cycle of load current. The reactive power increases to level of 5.5MVAr, the active power demand of the system marginally increase to 7.41 MW. When a less reactive load of 4.255+j1.198 Ω is inserted in the system which causes an active and reactive power of 8.71MW and 1.56 MVAr in the circuit. The multi-step levels of the voltage are less visible as the waveform becomes near sinusoidal for this load. This 10.9 kV

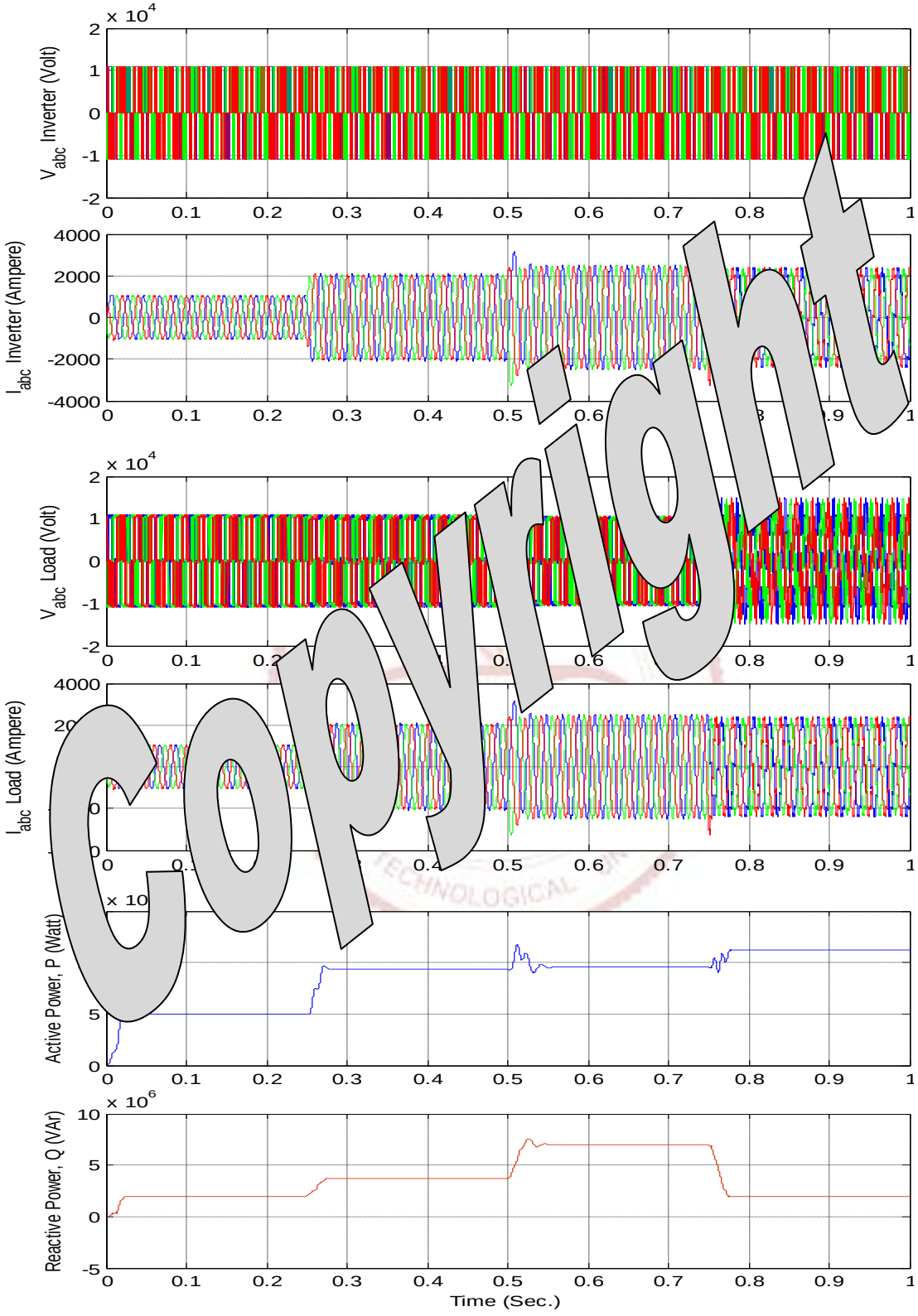

Figure 4.3 Simulated Results for Three Level Cascade H-Bridge Inverter.

voltage waveform has less distortion than voltage obtained from the previous case. However, current waveform gets highly distorted when connected to purely resistive load which is devoid of inductor that acts as the current filter.

When the resistive load is removed from the system the voltage is disturbed and the system is again made to have a load of 7.8 +j5.7Ω, the waveform for voltage shows some transient behaviour as the load is again reactive. The transients in the system take few cycles to recover it to its previous value of 10.7kV.

4.2.2 Five Level Inverter

4.2.2.1 Model Description

The model consists of two H-bridge in each phase leg as shown in Fig. 4.4.1. The model is developed from the three level inverter by cascading similar H-Bridges in every leg of the three level inverter. The voltage across one bridge is set to be 5500 volts. Controller for the switching also has one more input for PWM generator and one more switching circumvent circuit (SCC) in each phase as shown in Fig. 4.4.2.

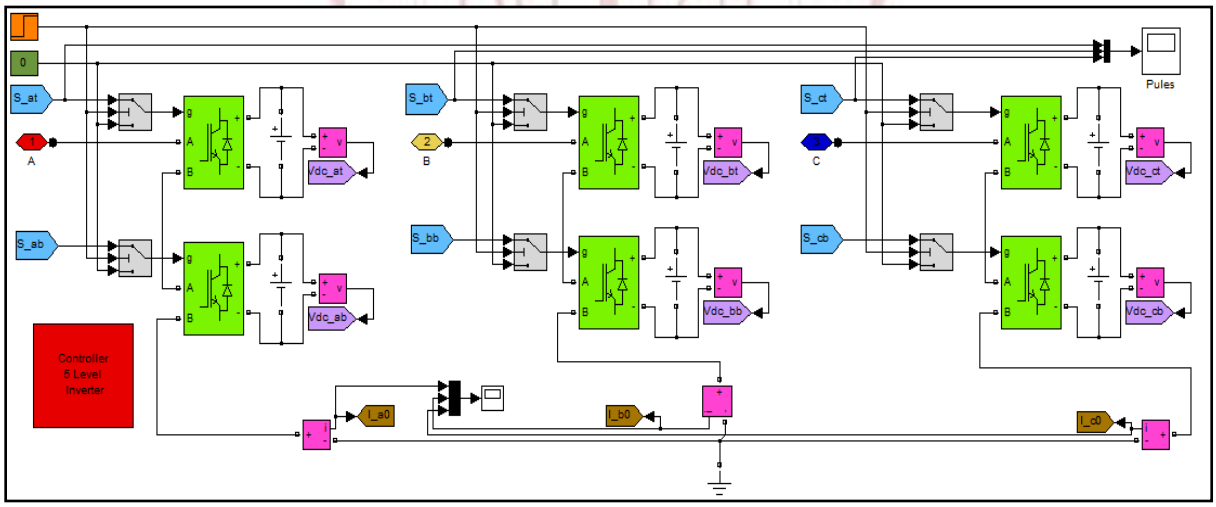

Figure 4.4.1 SIMULINK Model of Five Level Cascaded H-Bridge Multilevel Inverter.

4.2.2.2 Results and Discussion

Fig. 4.5 demonstrates the various waveforms for the different parameters obtained from the switching of inverter. Power electronic devices are switched in at time 0.0 second with a load impedance of 7.80 + j5.70 Ω connected to the inverter. The voltage of 11kV (peak value) having three level (-11, 0, 11) kV is generated across the inverter terminal. A current of 1100 A

flows in the line and the voltage across the load is obtained to be 10.7kV. The current waveform is almost sinusoidal without any measure peak. The active and reactive powers for this load are 5.2 MW and 2.2 MVAr respectively. At 0.25second load impedance is varied to 3.9 + j2.85 Ω, the multi-step voltage across the load is found to be 10.5kV. Active and reactive powers demanded by the load are 10.34MW and 4.11 MVAr for this load. The current waveform follows the same pattern as the previous connected load but with increased amplitude (2115 A). As the load impedance is varied to -0.266+ j4.089 Ω at 0.50 second, the multi-step voltage across load becomes 1015kV. The current waveform has increased amplitude of 2600 A. A transient in current in current is also observed in different phase. However, this transient is subsided in 3 to 4 cycle of load current. The reactive power increases to level of 7.65MVAr, the active power demand of the system marginally increase to 10.55 MW. When a less reactive load of 4.255 +j1.198 Ω is inserted in the system, active and reactive powers become 12.31 MW and 2.1 MVAr in the circuit. The multi-step levels of the voltage are less visible as the waveform becomes near sinusoidal for this load. This 10.9 kV voltage waveform has less distortion than voltage obtained for the previous loads. However, current waveform is highly distorted as the reactance of the load which was also acting as the current filter is less in this case. A notch is also visible at the peak of this current waveform.

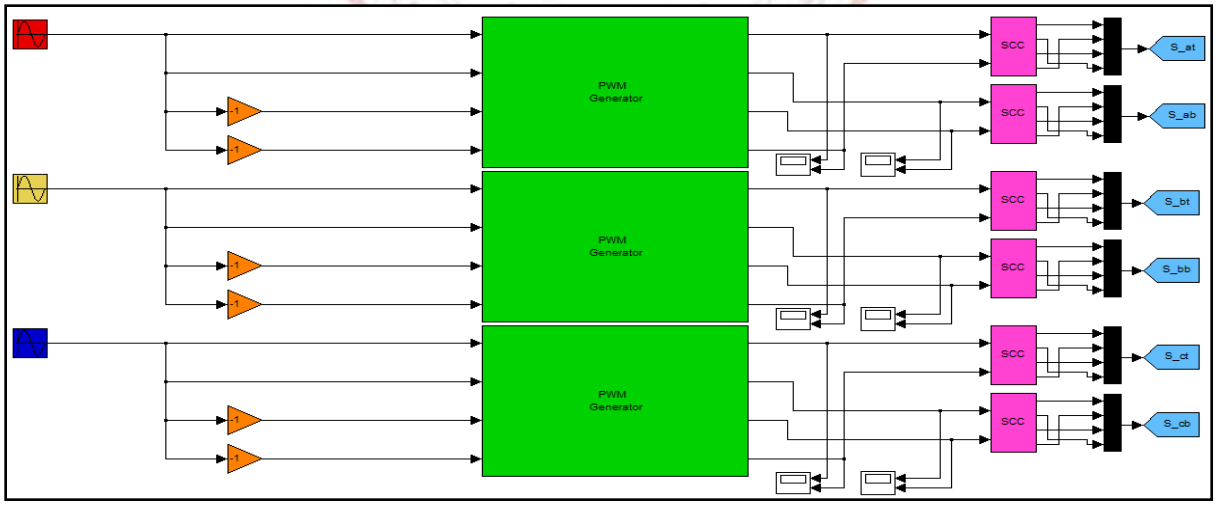

Figure 4.4.2 Controller for Five Level Cascaded H-Bridge Multilevel Inverter.

The difference in the magnitude of the voltage, current and two powers of five level and three level inverter is because of the different harmonic components.

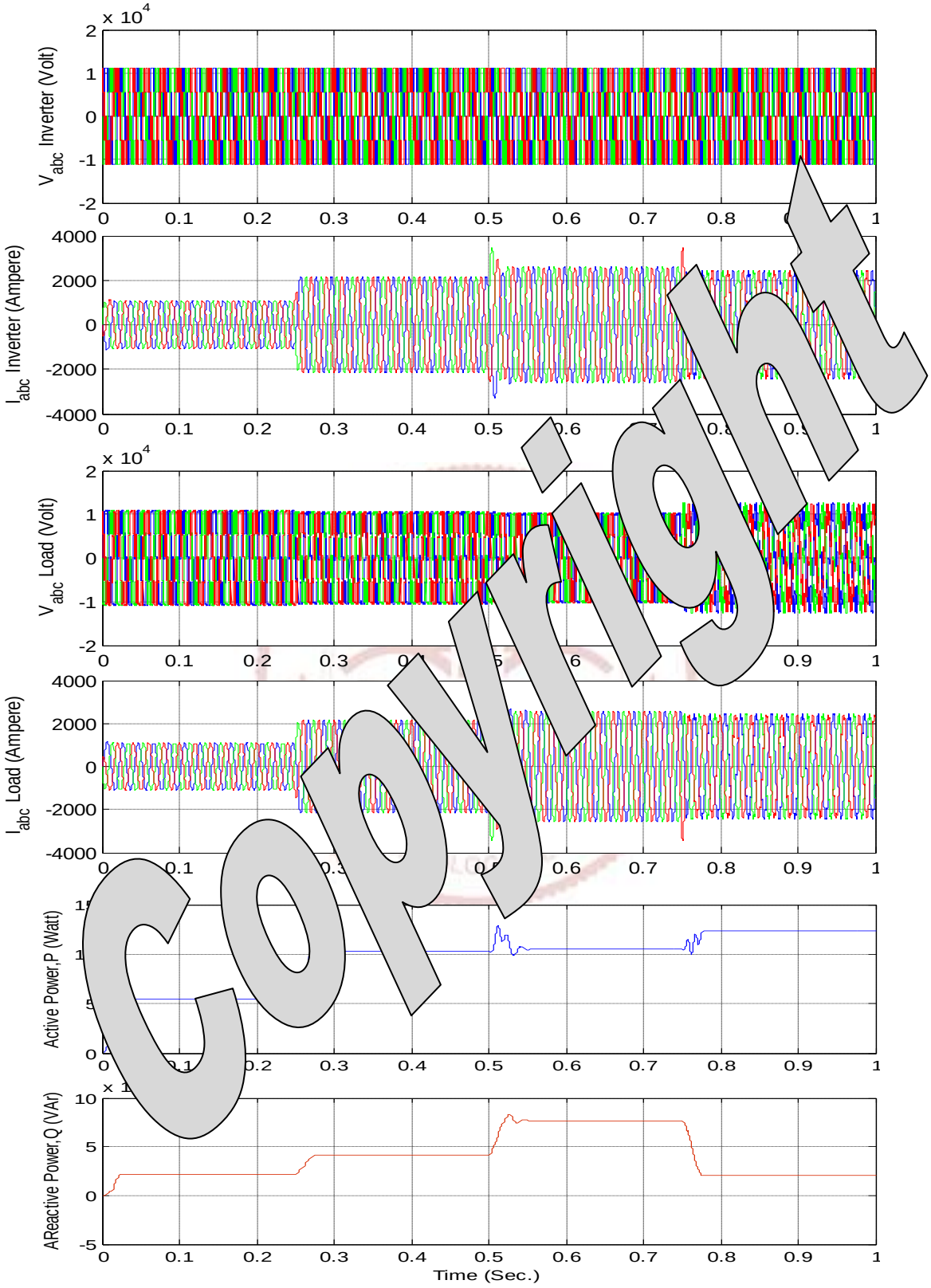

Figure 4.5 Simulated Results for Five Level Cascade H-Bridge Inverter.

When the resistive load is removed from the system the voltage is disturbed beyond 1.0 second and the system is again made to have a load of 7.8 +j5.7Ω, the waveform for voltage shows some transient behaviour as the load is again reactive. This causes unbalance in the system which takes few cycles to recover it to its previous value of 10.7kV.

4.2.3 Seven Level Inverter

4.2.3.1 Model Description

The model consists of three H-bridge in each phase leg as shown in Fig. 4.6.1. The model is developed from the five level inverter by cascading similar H-Bridges in every leg of the five level inverter. The voltage across one bridge is set to be 3667 V. Controller for the switching also has one more input for PWM generator for each phase as shown in Fig. 4.6.2.

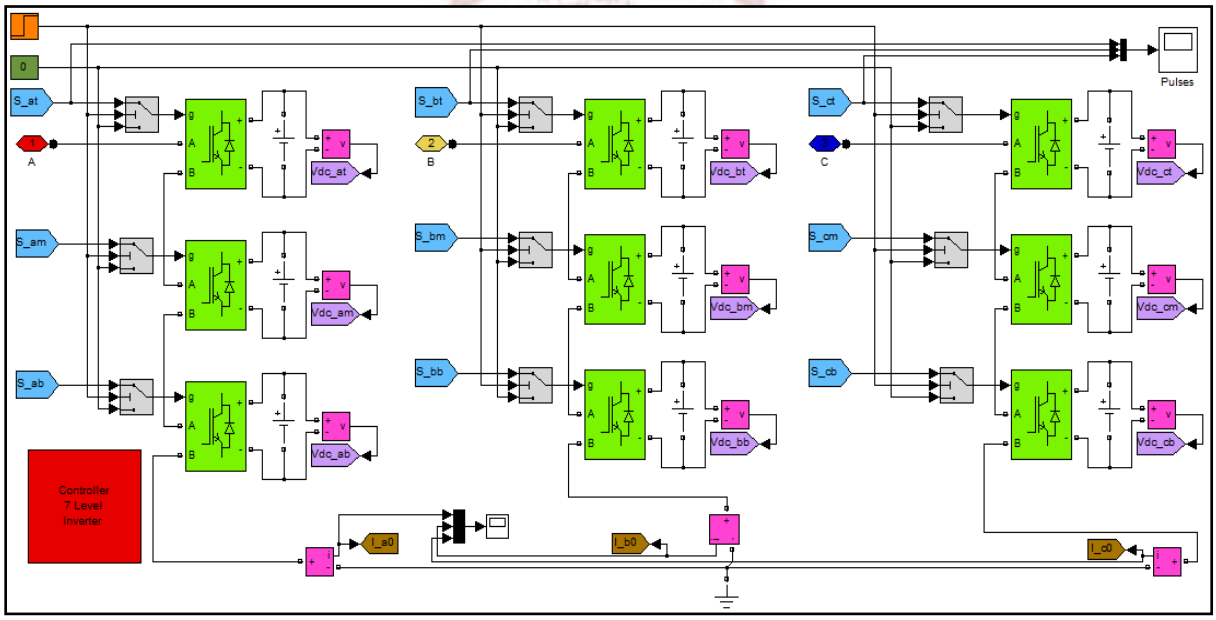

Figure 4.6.1 SIMULINK Model of Seven Level Cascaded H-Bridge Multilevel Inverter.

4.2.3.2 Results and Discussion

Fig. 4.7 demonstrates the various waveforms for the different parameters obtained from the switching of inverter. Power electronic devices are switched on at time 0.0 second with a load impedance of 7.80 + j5.70 Ω connected to the inverter. The voltage of 11kV (peak value) having three level (-11, 0, 11) kV is generated across the inverter terminal. A sinusoidal current having very low harmonics of 1085 A flows in the line and the voltage across the load is obtained to be 10.7kV. The active and reactive powers for this load are 5.2 MW and 2.2 MVAr

respectively. At 0.25second load impedance is varied to 3.9 + j2.85 Ω, the multi-step voltage across the load is found to be 10.3kV. Active and reactive powers demanded by the load are 10.02MW and 3.97 MVAr for this load. The current waveform follows the same pattern as previous load but with increased amplitude (2100 A). As the load impedance is varied to -0.266+ j4.089 Ω at 0.50 second, the multi-step voltage across load becomes 10.2kV. The current waveform has increased amplitude of 2550 A. A transient is also observed in the current of different phase. However, this unbalance is removed in 3 to 4 cycle of load current. The reactive power increases to level of 7.43MVAr, the active power demand of the system marginally increase to 10.23 MW. A less reactive load of 4.255+j1.198 Ω causes an active and reactive power of 12.31 MW and 2.1 MVAr in the circuit. The multi-step levels of the voltage are less visible as the waveform becomes near sinusoidal for this load. This 10.8 kV voltage waveform has less distortion than voltage obtained for the previous loads. However, current waveform with amplitude of 2300 A is highly distorted as the reactance of the load which was also acting as the current filter is less in this case. A notch is also visible at the peak of this current waveform.

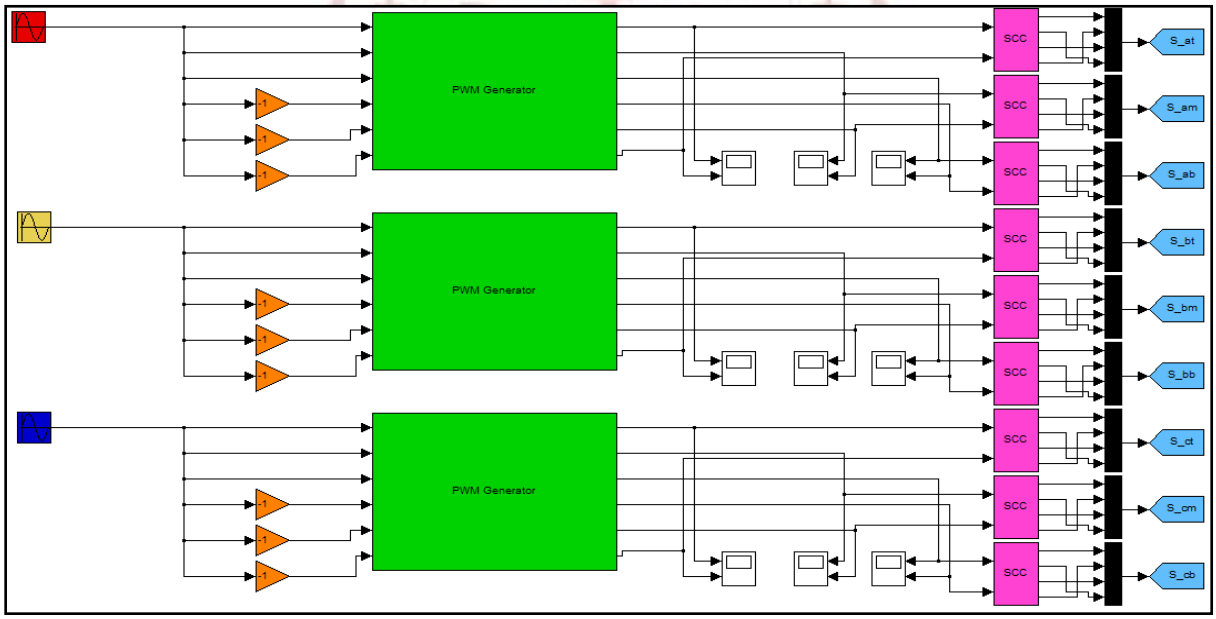

Figure 4.6.2 Controller for Seven Level Cascaded H-Bridge Multilevel Inverter.

The difference in the magnitude of the voltage, current and two powers of seven level inverter is different from the previous cases due to different harmonic components. The efficiency of this level with different level in terms of %THD is discussed in the coming text.

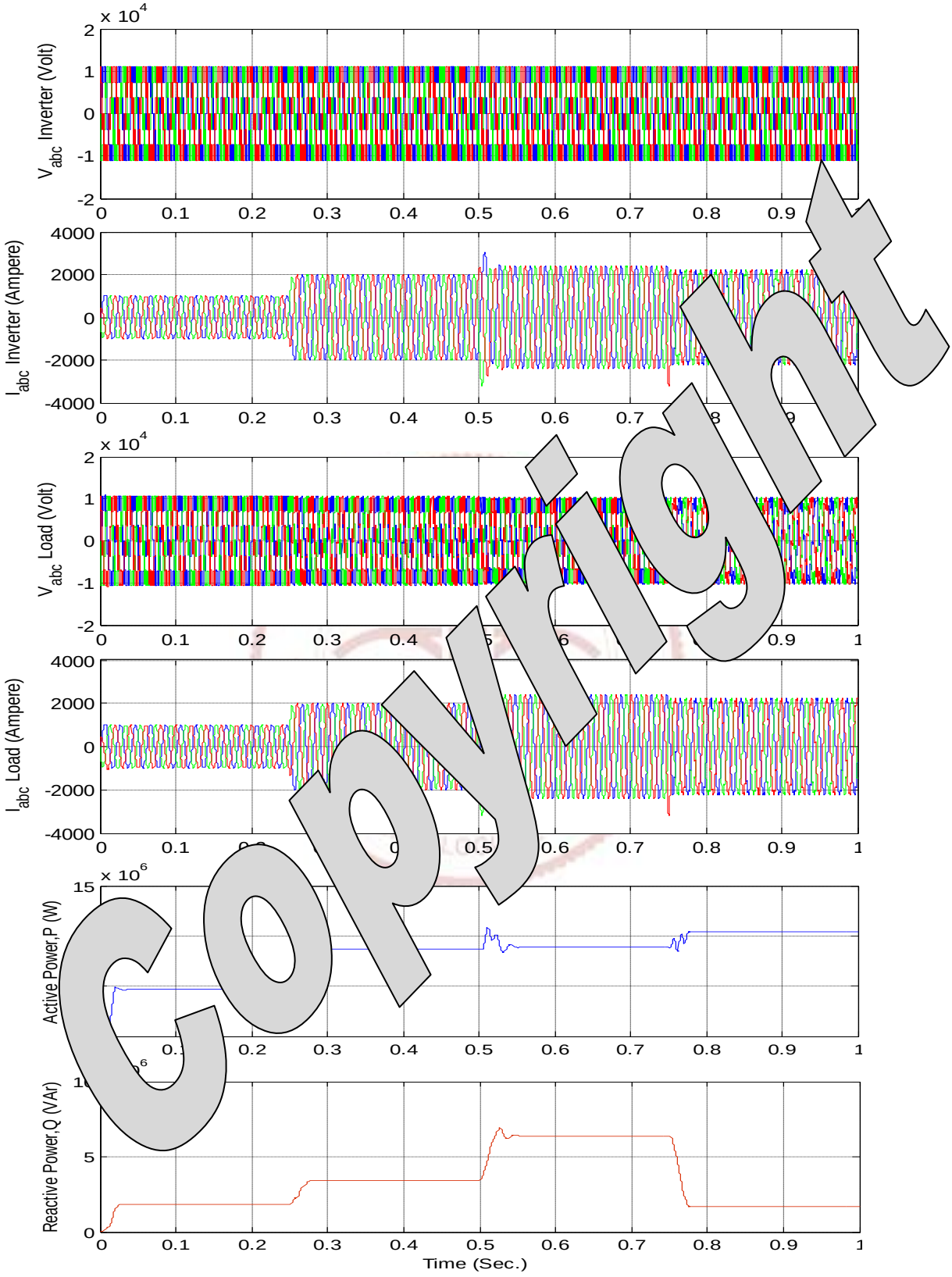

Figure 4.7 Simulated Results for Seven Level Cascade H-Bridge Inverter.

4.2.4 Nine Level Inverter

4.2.4.1 Model Description

The model consists of four H-bridge in each phase leg as shown in Fig. 4.8.1. The model is developed from the seven level inverter by cascading similar H-Bridges in every leg of the seven level inverter. The voltage across one bridge is set to be 2750 V. Controller for the switching also has one more input for PWM generator and switching circumvent circuit in each phase as shown in Fig. 4.8.2.

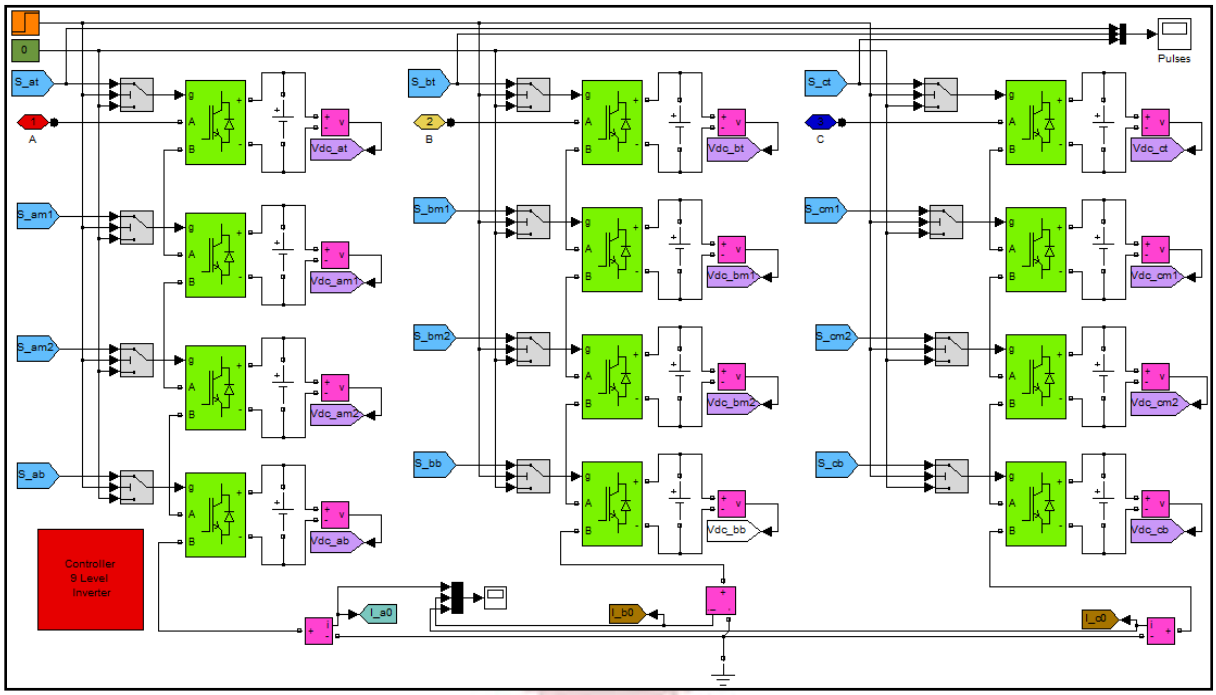

Figure 4.8.1 SIMULINK Model of Nine Level Cascaded H-Bridge Multilevel Inverter.

4.2.4.2 Results and Discussion

Fig. 4.9 demonstrates the various waveforms for the different parameters obtained from the switching of inverter. Power electronic devices are switched on at time 0.0 second with a load impedance of 7.80 + j5.70 Ω connected to the inverter. The voltage of 11kV (peak value) having three level (-11, 0, 11) kV is generated across the inverter terminal. A sinusoidal current having very low harmonics of 1100 A flows in the line and the voltage across the load is obtained to be 10.7kV. The active and reactive powers for this load are 5.4 MW and 2.2 MVAr respectively. At 0.25s load impedance is varied to 3.9 + j2.85 Ω, the multi-step voltage across the load is found to be 10.5kV. Active and reactive powers demanded by the load are 10.18

MW and 4.17 MVAr for this load. The current waveform follows the same pattern as previous load but with increased amplitude (2115 A). As the load impedance is varied to -0.266 + j4.089 Ω at 0.50 second, the multi-step voltage across load becomes 10.1kV. The current waveform has increased amplitude of 2600 A. A transient has been observed in the current of different phases. However, this unbalance is removed in 3 to 4 cycle of load current. The reactive power increases to level of 7.66 MVAr, the active power demand of the system marginally increase to 10.34 MW. A less reactive load of 4.255+j1.198 Ω causes an active and reactive power of 12.1 MW and 2.16 MVAr in the circuit. The multi-step levels of the voltage are less visible as the waveform becomes near sinusoidal for this load. This 10.9 kV voltage waveform has less distortion than voltage obtained for the previous loads. However, current waveform with amplitude of 2350 A is highly distorted as the reactance of the load which was also acting as the current filter is less in this case.

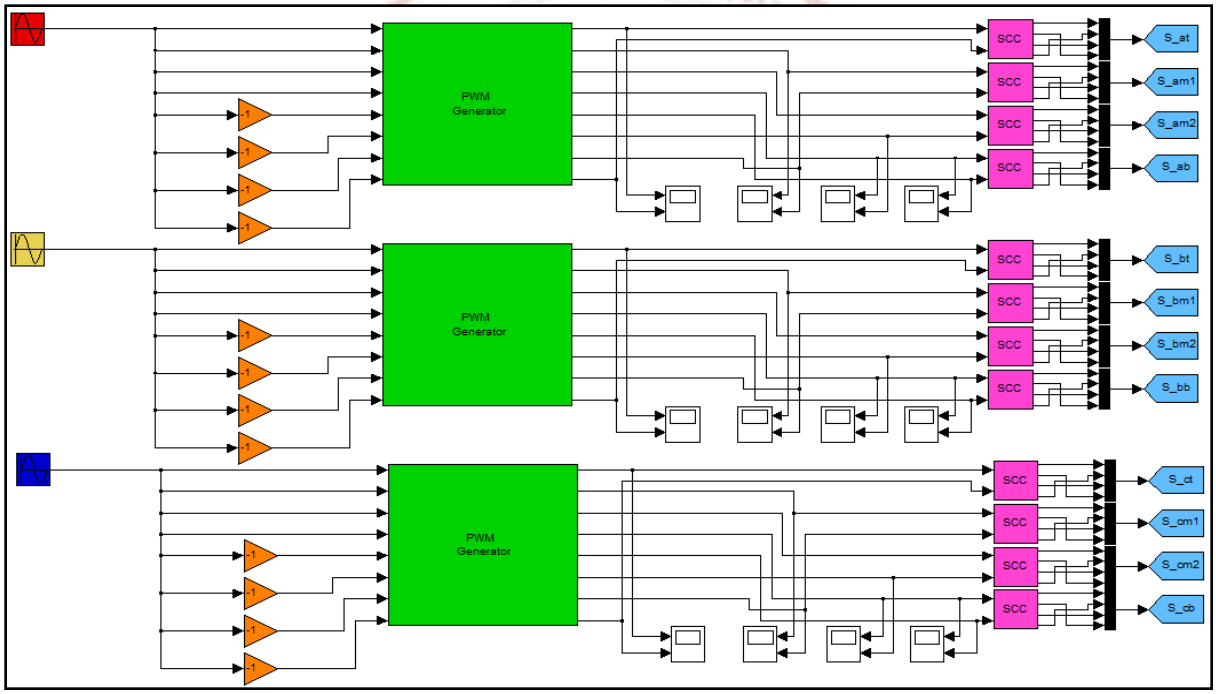

Figure 4.8.2 Controller for Nine Level Cascaded H-Bridge Multilevel Inverter.

The difference in the magnitude of the voltage, current and two powers of different levels is because of the different harmonic components. An initial look in the various waveforms gives the cue of superior performance of nine level inverter over its lesser level counterpart. The removal of resistive load causes a transient behaviour in the system as voltage takes some time to settle as per the requirement of more reactive load.

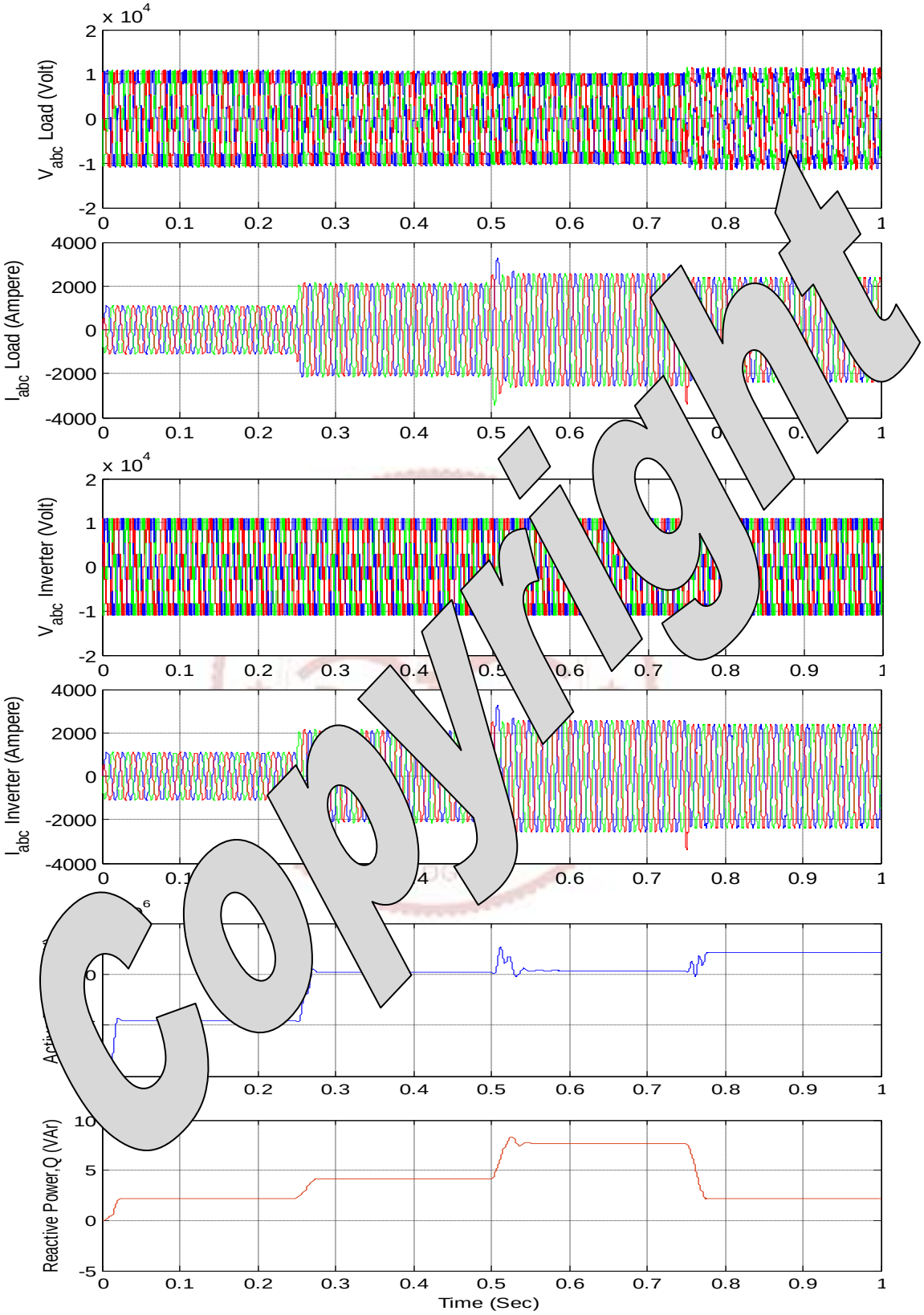

Figure 4.9 Simulated Results for Nine Level Cascade H-Bridge Inverter.

4.2.5 Eleven Level Inverter

4.2.5.1 Model Description

The model consists of five H-bridge in each phase leg as shown in Fig. 4.10.1. The model is developed from the nine level inverter by cascading similar H-Bridges in every leg of the nine level inverter. The voltage across one bridge is set to be 2250 V. Controller for the switching also has one more input for PWM generator and SCC in each phase as shown in Fig. 4.10.2.

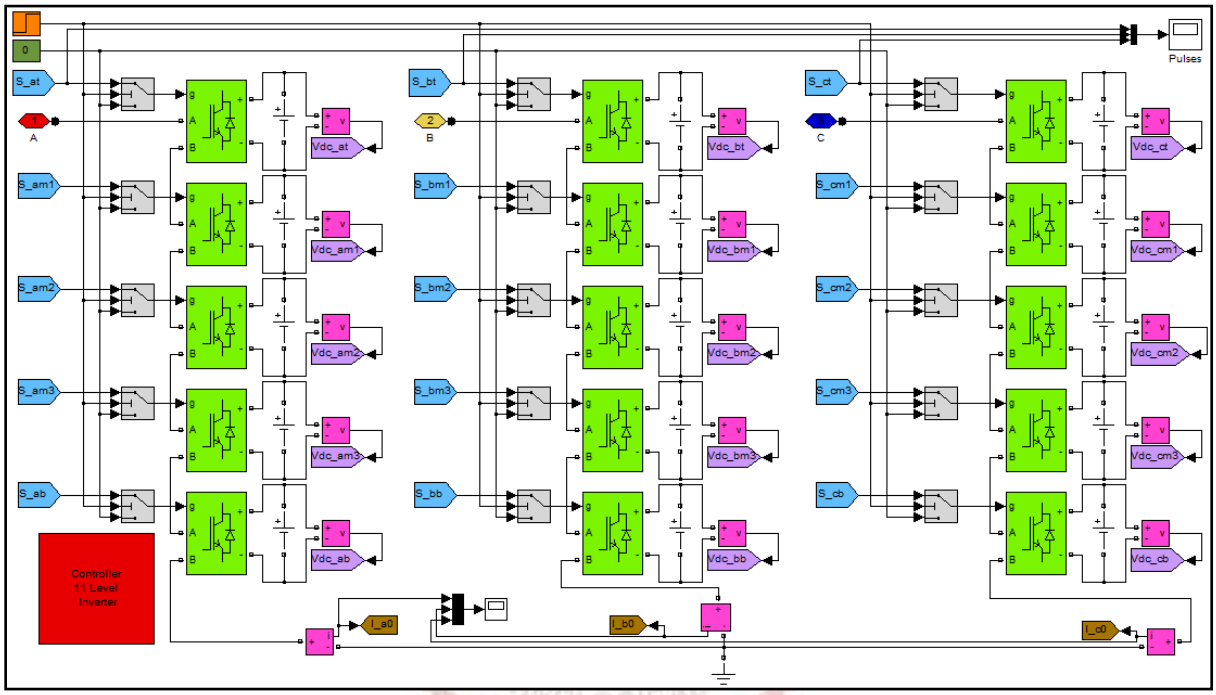

Figure 4.10.1 SIMULINK Model of Eleven Level Cascaded H-Bridge Multilevel Inverter.

4.2.5.2 Results and Discussion

Fig. 4.11 demonstrates the various waveforms for the different parameters obtained from the switching of inverter. Power electronic devices are switched on at time 0.0 second with a load impedance of 7.80 + j5.70 Ω connected to the inverter. The voltage of 11kV (peak value) having three level (-11, 0, 11) kV is generated across the inverter terminal. A sinusoidal current having very low harmonics of 1100 A flows in the line and the voltage across the load is obtained to be 10.7kV. The active and reactive powers for this load are 5.28 MW and 2.11 MVAr respectively. At 0.25s load impedance is varied to 3.9 + j2.85 Ω, the multi-step voltage across the load is found to be 10.4kV. Active and reactive powers demanded by the load are 9.27 MW and 3.94 MVAr for this load. The current waveform follows the same pattern as

previous load but with increased amplitude (2120 A). As the load impedance is varied to -0.266 + j4.089 Ω at 0.50 second, the multi-step voltage across load becomes 10.04kV. The current waveform has increased amplitude of 2540 A. There is also an unbalance of current in the current of different phases. However, this unbalance is removed in 2 to 3cycle of load current. The reactive power increases to level of 7.37 MVAr, the active power demand of the system marginally increase to 10.12 MW. A less reactive load of 4.255+j1.198 Ω causes an active and reactive power of 11.82 MW and 2.0 MVAr in the circuit. The multi-step levels of the voltage are less visible as the waveform becomes near sinusoidal for this load. This 10.9 kV voltage waveform has less distortion than voltage obtained for the previous loads. However, current waveform with amplitude of 2355 A is highly distorted as the reactance of the load which was also acting as the current filter is less in this case.

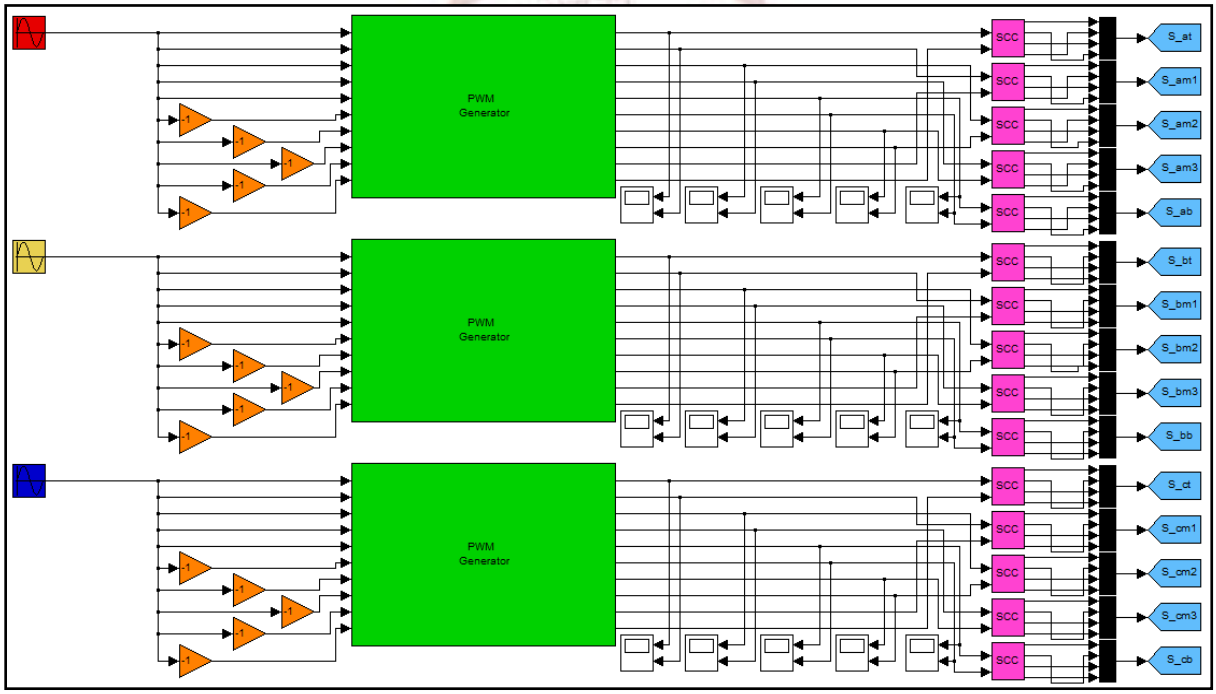

Figure 4.10.2 Controller for Eleven Level Cascaded H-Bridge Multilevel Inverter.

The difference in the magnitude of the voltage, current and two powers of different levels is because of the different harmonic components.

When the resistive load is removed from the system the voltage is disturbed and the system is again made to have a load of 7.8 +j5.7Ω, the waveform for voltage shows some transient behaviour as the load is again reactive. This causes unbalance in the system which takes few cycles to recover it to its previous value of 10.7kV.

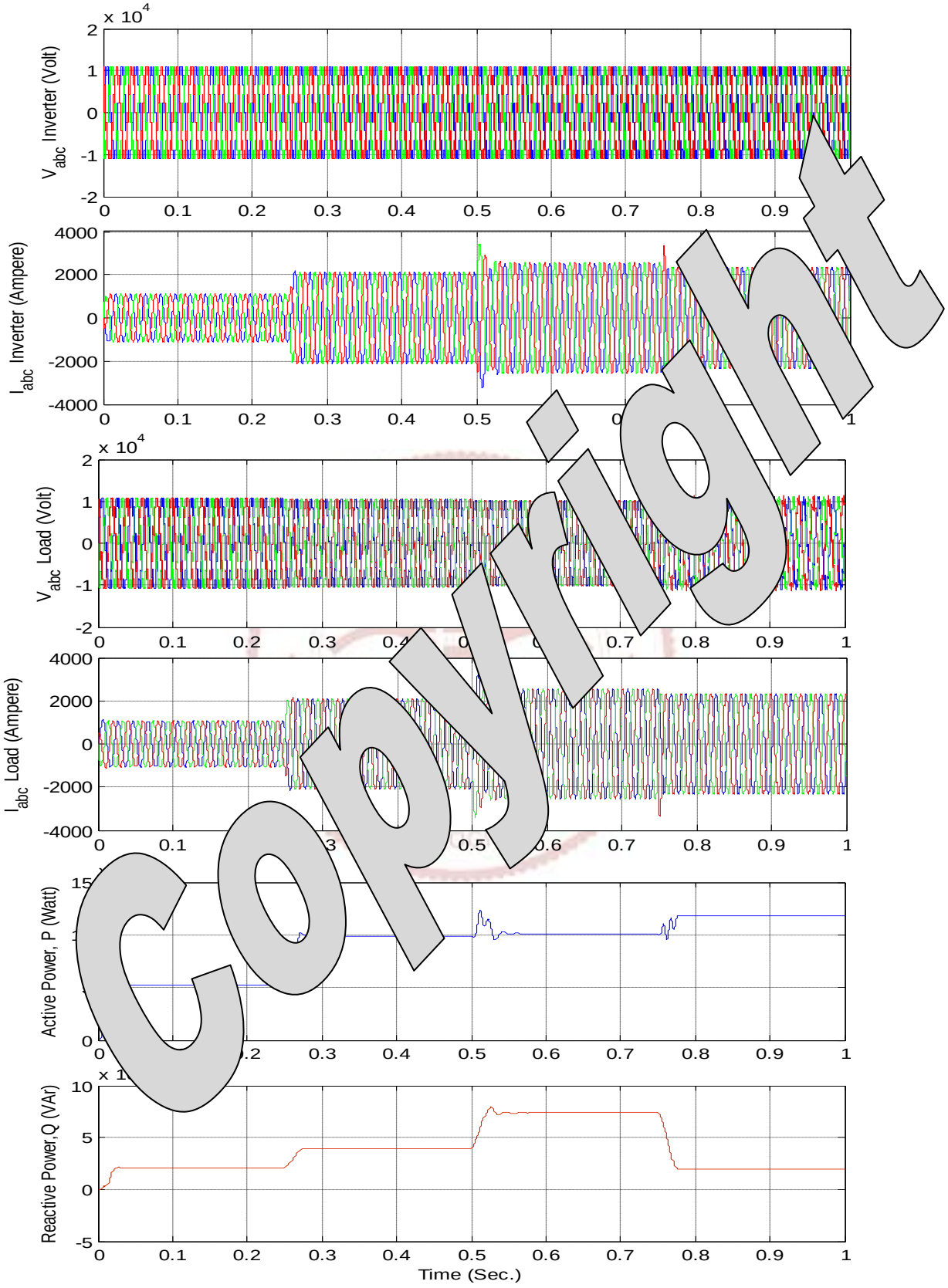

Figure 4.11 Simulated Results for Eleven Level Cascade H-Bridge Inverter.

The difference in the performance of the different inverter shown in previous text is shown in the table 4.1, table 4.2 and table 4.3.Table 4.1 shows the variation in % THD in load voltage of phase A for different load impedances as the number of level changes. Phase B and phase C have almost the same values so the result obtained for them are not presented. Table 4.2 shows the variation in % THD in load current of phase A for different load impedances as the number of level changes. The current in the inverter is equal to the load current as there is no node presented in the proposed system, so the result will obviously are equal as obtained for load current. Table 4.3 illustrate the comparison of % THD in inverter voltage of phase

Table 4.1 Comparison of %THD in Load Voltage (Phase A) of Different Cascaded H- Bridge Level Inverters for 11kV (Phase to Phase) Voltage:

Load Impedance (R + jX)Ω	Three Level Inverter	Five Level Inverter	Seven Level Inverter	Nine Level Inverter	Eleven Level Inverter
7.80+j5.70	68.52	25.64	18.03	13.[illegible]	11.61
3.90+j2.85	67.84	25.52	17.82	[illegible]	11.47
-0.266+j4.089	69.87	26.29	[illegible]6	[illegible]	11.82
4.255+j1.198	40.97	17.17	[illegible]3	8.44	6.34

As shown in table 4.1, THD in load voltage for single inverter does not vary significantly for different reactive load. However, the variation is very much visible when the load is made to be resistive from the inductive load. As in many cases the 11 Level inverter shows improved performance.

Table 4.2 Comparison of [illegible] Load Current (Phase A) of Different Cascaded H- Bridge Level Inverters for 11kV (Phase to Phase) Voltage:

Load Impedance (R + jX)	Three Level Inverter	Five Level Inverter	Seven Level Inverter	Nine Level Inverter	Eleven Level Inverter
7.80+j[illegible]	[illegible]40	1.51	1.42	1.34	1.38
3.90+j2.[illegible]	[illegible].16	1.05	0.95	0.82	0.89
-0.266+j4.0[illegible]	[illegible].62	1.14	1.15	1.06	1.00
4.255+j1.198	10.99	3.70	2.72	2.12	2.46

As shown in table 4.2, THD in load current for a single inverter does not vary significantly for different reactive load. However, the variation is very much visible when the load is made to be resistive from the inductive load. The increased THD is caused because of the absence of

inductor in load which was also acting as the filter for the current harmonics. Again, 11 Level inverter shows improve performance for the current also.

Table 4.3 Comparison of %THD in Inverter Voltage (Phase A) of Different Cascaded H- Bridge Level Inverters for 11kV (Phase to Phase) Voltage:

Load Impedance (R + jX)Ω	Three Level Inverter	Five Level Inverter	Seven Level Inverter	Nine Level Inverter	Eleven Level Inverter
7.80+j5.70	69.58	25.83	18.30	13.[illegible]	11.8[illegible]
3.90+j2.85	67.65	25.83	18.28	13.5[illegible]	1.82
-0.266+j4.089	69.61	25.81	18.27	[illegible]53	[illegible]80
4.255+j1.198	40.51	25.83	18.[illegible]9	[illegible]	1.82

As shown in table 4.3, THD in inverter voltage for a single inverter does not vary significantly for different reactive load. The variations are marginal even [illegible] highly reactive load. However, the variation is very much visible when load is made to be resistive from the inductive load.

4.3 Cascade H- Bridge Based Multilevel D-STATCOM

For managing the reactive power, the multilevel inverter proposed in the previous section can operated in two D-STATCOM configurations: (i) voltage control source (ii) current control source. When the multilevel inverter is used as voltage controlled source, it compensate the reactive power keeping the reference voltage and power angle, δ. The reactive power can be transacted both way (D-STATCOM to grid and load to D-STATCOM) by changing the power angle, δ of the voltage of the source. As a current control source D-STATCOM can compensate reactive power by injection of the required decoupled current in the system. The first method is quite complex as the voltage of both side along with the load angle be adjusted for desired result. Controlling voltage in itself is very cumbersome. However, in the second method only one variable (current) is to be controlled as per the system requirement.

The various level D-STATCOMs and its PWM generation controllers can be modelled with the multilevel inverters and their controllers have been shown in previous section. As per inference drawn from the previous section, the 11-level cascaded H- bridge multilevel inverter converter could be a better contender for enhanced performance than its lesser level counterpart. Due to

this motivation only the 11-level CHBMI based D-STATCOM is used for the demonstration of reactive power compensation.

The SIMULINK model for the proposed system is presented in Fig. 4.12.1. The 11kV (phase to phase) source and the load have a source impedance of 0.1+ j0.034 Ω in each phases. The cascaded H-bridge having batteries of 3kV each at the DC bus is connected in tandem, and the three phase structure is connected in shunt with the interphase inductor of 0.1 + j1.319 Ω in each phases coupled to the P.C.C. A ripple filter is also used which smoothens voltage output end of D-STATCOM injected in the system by filtering the switching harmonics.

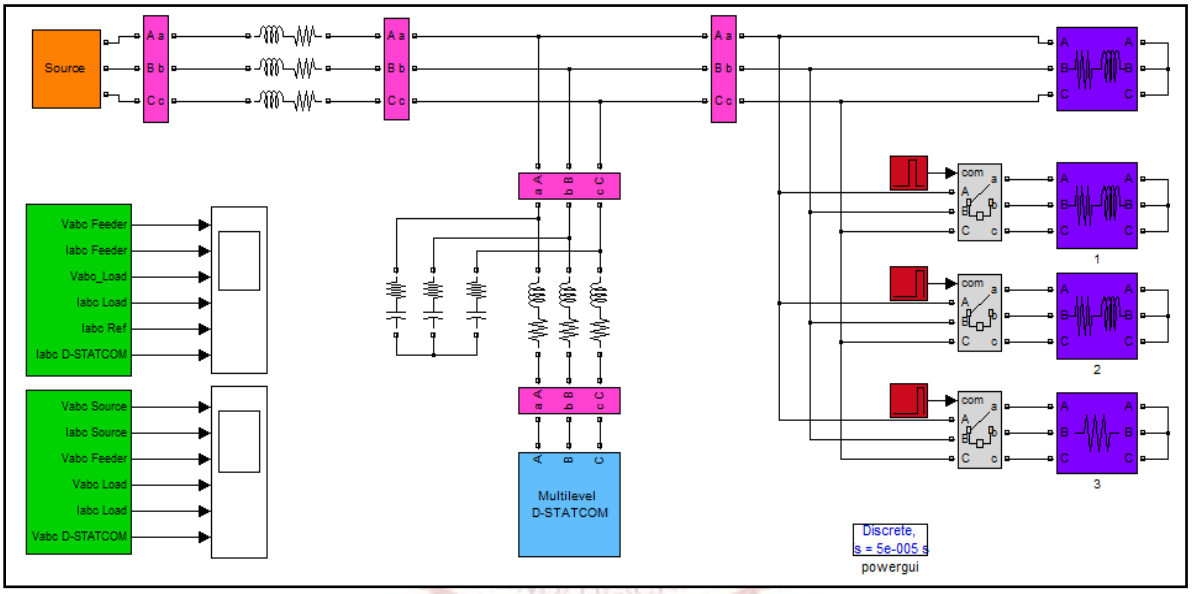

Figure 4.12.1 SIMULINK Model of Distribution System Employed With 11-Level Cascaded H-Bridge Multilevel D-STATCOM.

The two operation of the D-STATCOM are presented in the following sections.

4.3.1 Application of D-STATCOM for Reactive Power Compensation

4.3.1.1 Control Strategy

A stiff source of constant power frequency is considered for supplying the power to the load. Fig. 4.12.2 depicts the controller of the D-STATCOM which is modelled on the basis of SRF theory dealt in mathematical equations (3.7)-(3.18) in previous chapter. The indirect current control is adopted for the compensation various PQ components with ease of operation. The generated reference current is compared with the feeder current which is forced to become

purely sinusoidal in presence of compensating device. Load current is decomposed for the generation of reference currents using SRF Theory. Such decomposition decouples the current into the active and reactive fundamental frequency components, and the components corresponding to harmonic frequencies using the abc to dq transformation and synchronisation of sine-cosine reference waveform to phase voltage utilizing a fast PLL. High frequency ripples in the d-q frame are filtered by a low pass filter. The reactive power component is forced to zero to have only fundamental component of active power component of current while reverse Park and Clarke transformations. This current is compared with the feeder current to produce the input signal for generation of PWM, which is modelled with the 11 level multilevel inverter controller explained in previous section. The controller for the 11-level multilevel inverter is shown in Fig.4.12.2 as a subsystem in PWM generation for the D-STATCOM.

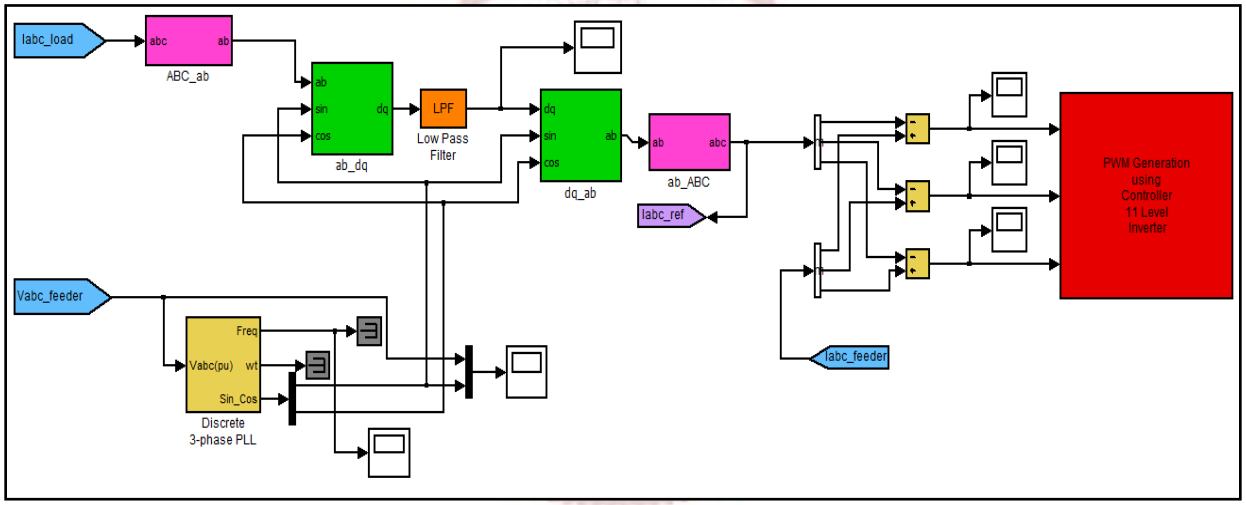

Figure 4.12.2 Controller of the Multilevel D-STATCOM for Reactive Power Compensation Having Controller for the 11- Level Inverter as a Subsystem.

4.3.1.2 Result and Discussion

The performance of the system has been depicts in Fig. 4.13-Fig.4.18. Fig.4.13 shows the operation of proposed 11level D-STATCOM for the reactive power compensation demonstrated in the SIMULINK environment. The system is operated for a total time of 2 second and results are concluded for various load perturbations. Load impedances of the 10.2+j31.4 Ω, 5.1+j15.7Ω, 3.46+j15.84 Ω and 9.84+j3.06 Ω changed at switching instant of t=0.0sec., 0.50sec., 0.75sec and 1.0 sec. respectively. The load impedance beyond t=1.25 sec. is fixed at 10.2+j31.4 Ω. The varying load demands different power transaction (active &

reactive) for different periods from the mains. For sake of clarity Fig. 4.13 is segregated corresponding to different load perturbations and shown in Fig.4.14 to Fig.4.17.

These figures provide a more detailed insight of the voltage and current profile in the system. In the beginning the load demands active and reactive power of 1.04MW and 1.07 MVAr respectively from the mains. All this power is supplied by the source as D-STATCOM is not switched in till 0.2sec. Thus, a lagging current flows in the circuit. As the D-STATCOM is switched in at t=0.2 sec., all the reactive power of the system is supplied by the D-STATCOM and the current and voltage at the feeder bus become in phase as shown in Fig.4.1.4 and the source current reduces to 220 A from 275 A, thus alleviating the burden from the source.

Fig. 4.15 depicts the D-STATCOM performance when load impedance varies to 5.1+j15.7Ω from 10.2+j31.4 Ω, during the time interval of t=0.5sec. to 0.75sec., both the active power and reactive power demand of the load is doubled. All of the reactive power is supplied by the D-STATCOM where as, only the active power demand is drawn from the feeder. The current and voltage of the feeder remain in phase.

As shown in Fig.4.16, when the load impedance is made highly reactive with an assigned value of 3.46 + j15.84Ω at 0.75sec., the reactive power demanded by the load (2.35 MVAr) is fully supplied by the D-STATCOM and the feeder supplies only active power.

In the last section (shown in Fig.4.17) from t=1.0sec. to 1.25sec., when the load becomes nearly resistive (9.84+j3.06Ω) the reactive power injected by the D-STATCOM also reduces. The demanded reactive power amount to 0.9MVAr in the present case, which is also successfully met by the D-STATCOM. Finally the load is again made slightly reactive at 1.25 s, to revisit the system dynamics when load changes from resistive to reactive suddenly. D-STATCOM instantly compensates this perturbation too and required power is met by it without any major transition in the source voltage and current values.

Fig.4.18 depicts the instantaneous active and reactive power distribution in the system for the different loads.

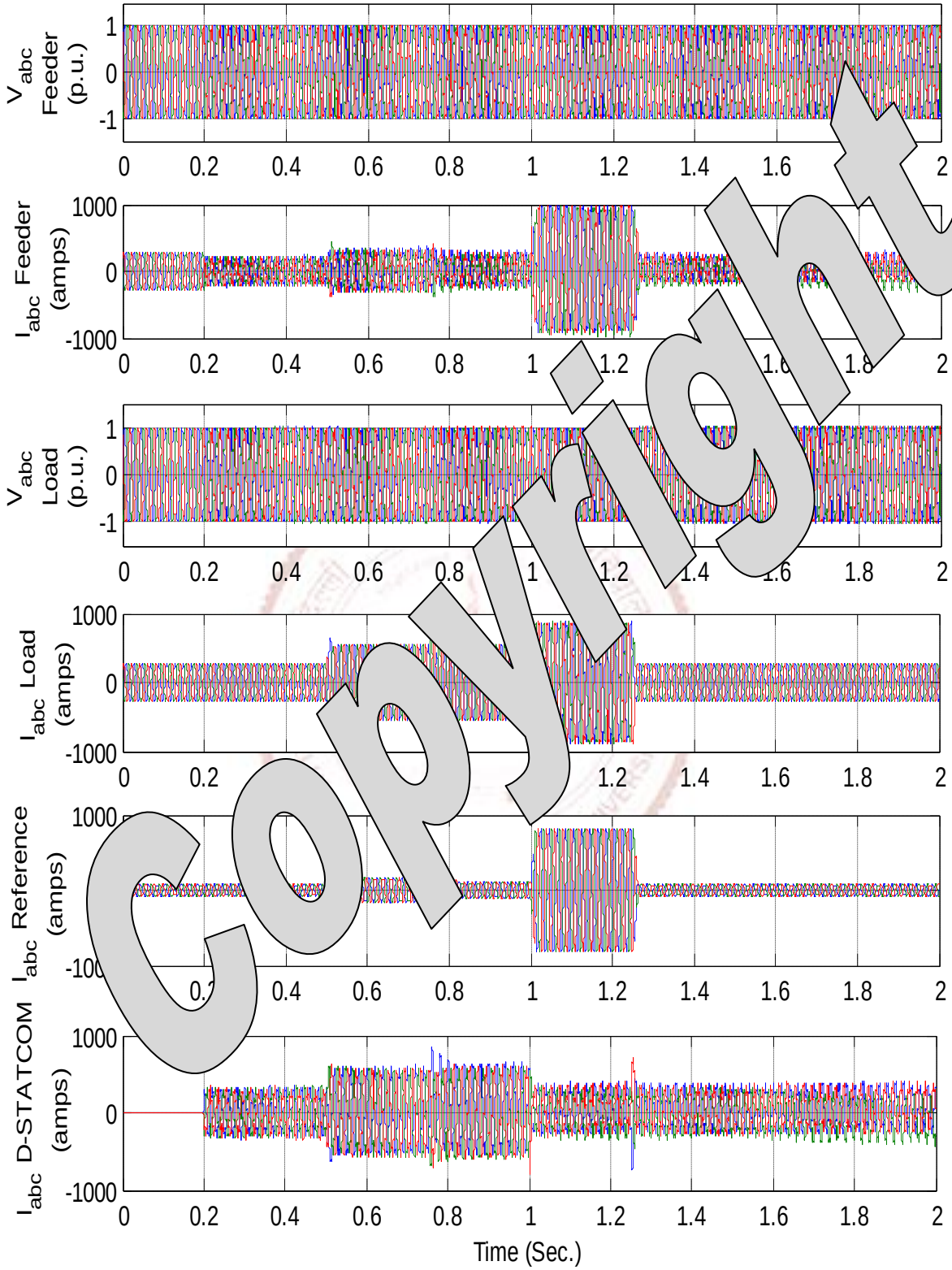

Figure 4.13 Simulated Results of the eleven level Cascaded Multilevel Inverter Based D-STATCOM for Different Loads with Load switching instants t= 0.5, 0.75, 1.0 and 1.25 Second and D-STATCOM Switching Instant = 0.2 Second.

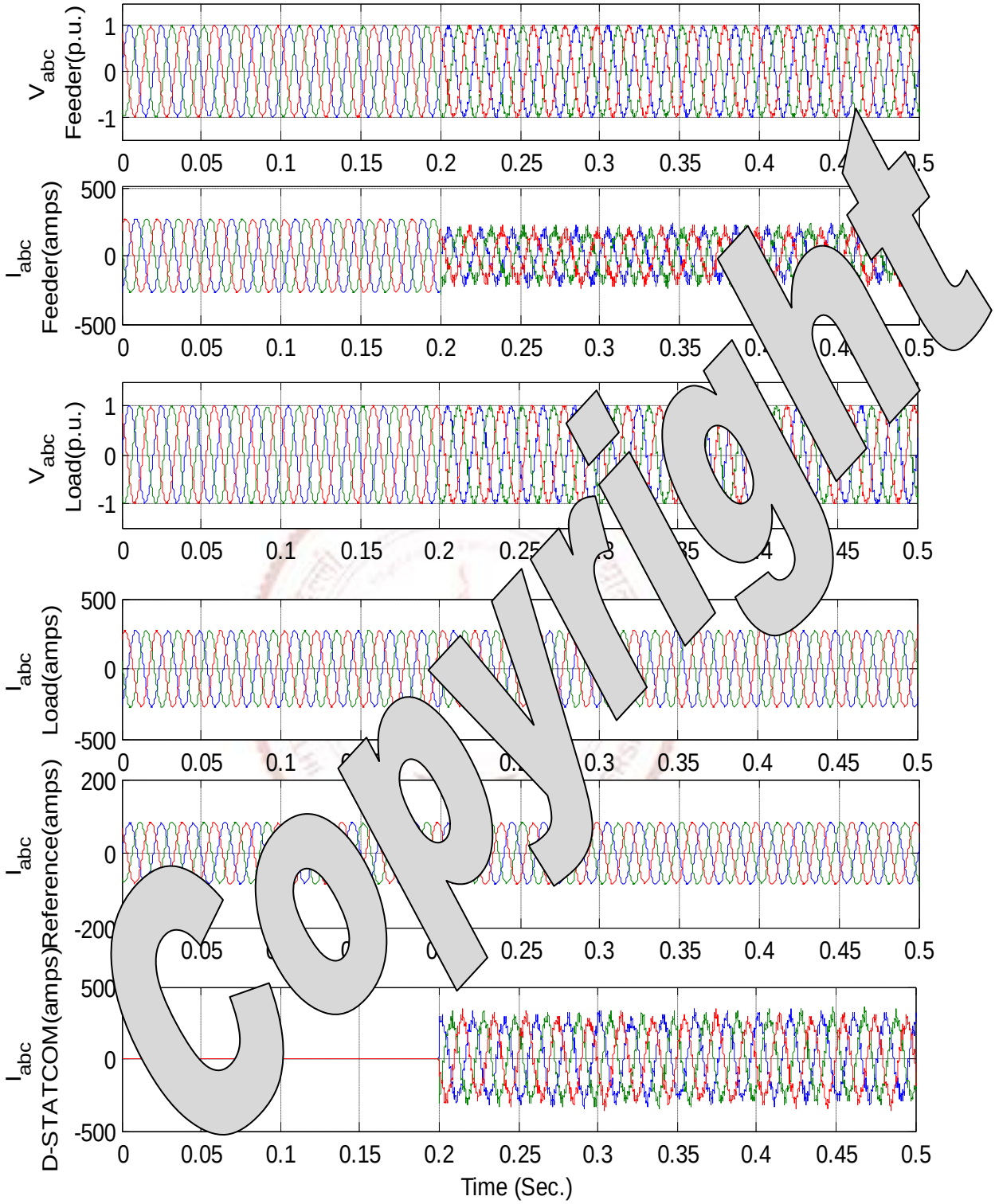

Figure 4.14 Simulated Result for the Proposed CHBMI based D-STATCOM for load impedance of 10.2+j31.4 Ω (Switching Instant of D-STATCOM = 0.2 Second).

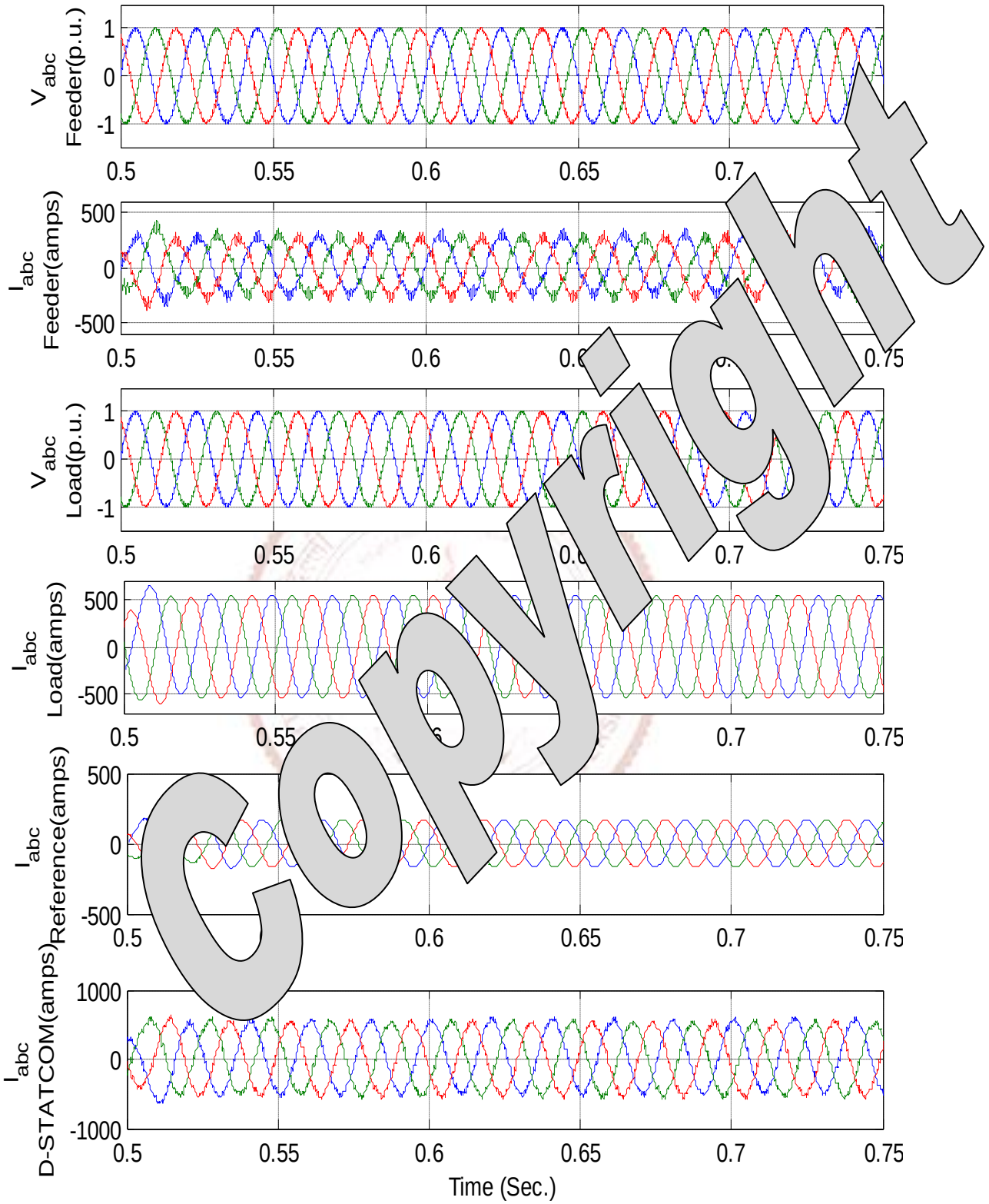

Figure 4.15 Simulated Result for the Proposed CHBMI based D-STATCOM for load impedance of 5.1+j15.7 Ω.

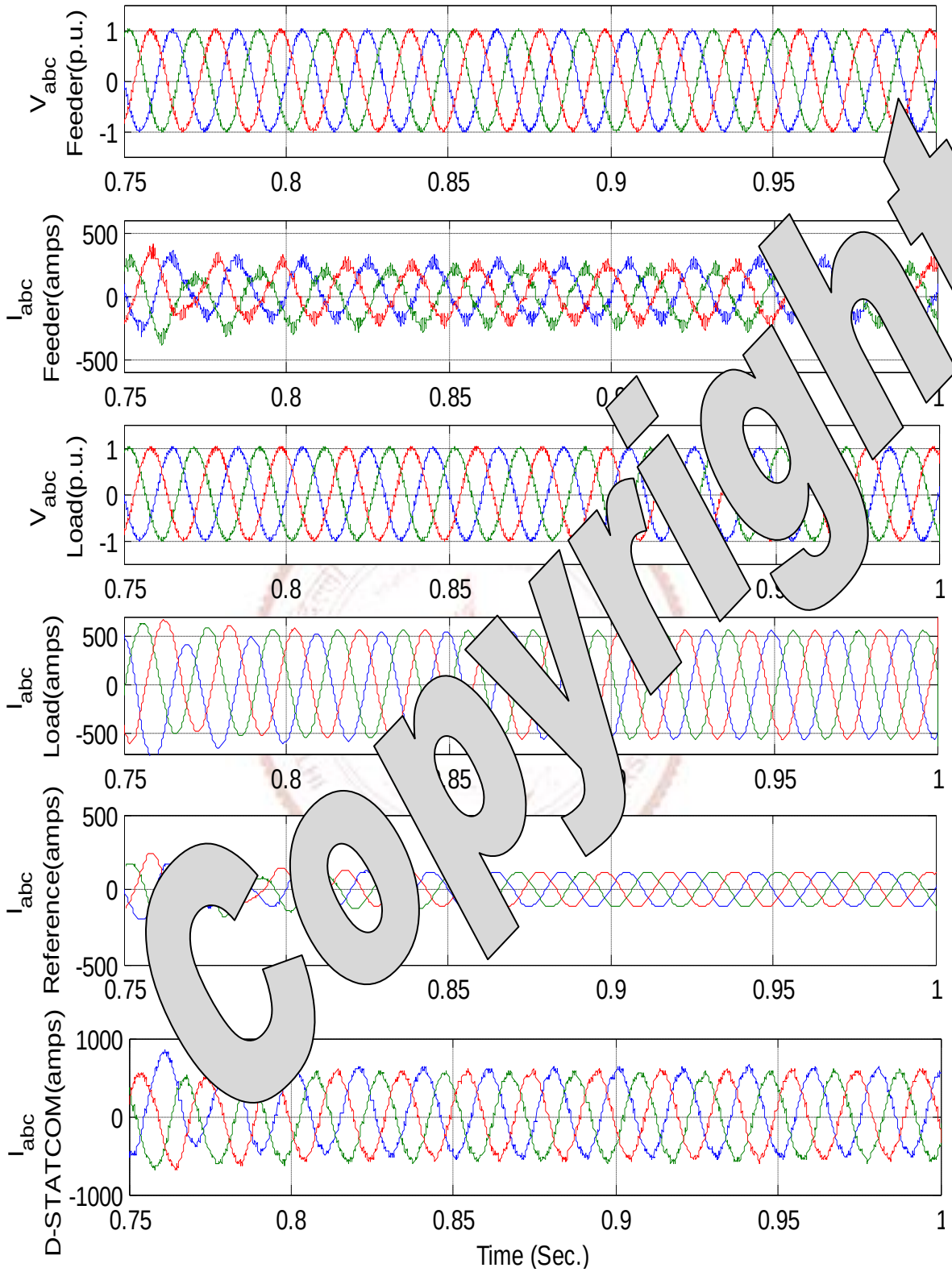

Figure 4.16 Simulated Result for the Proposed CHBMI based D-STATCOM for load impedance of 3.46+j15.84 Ω.

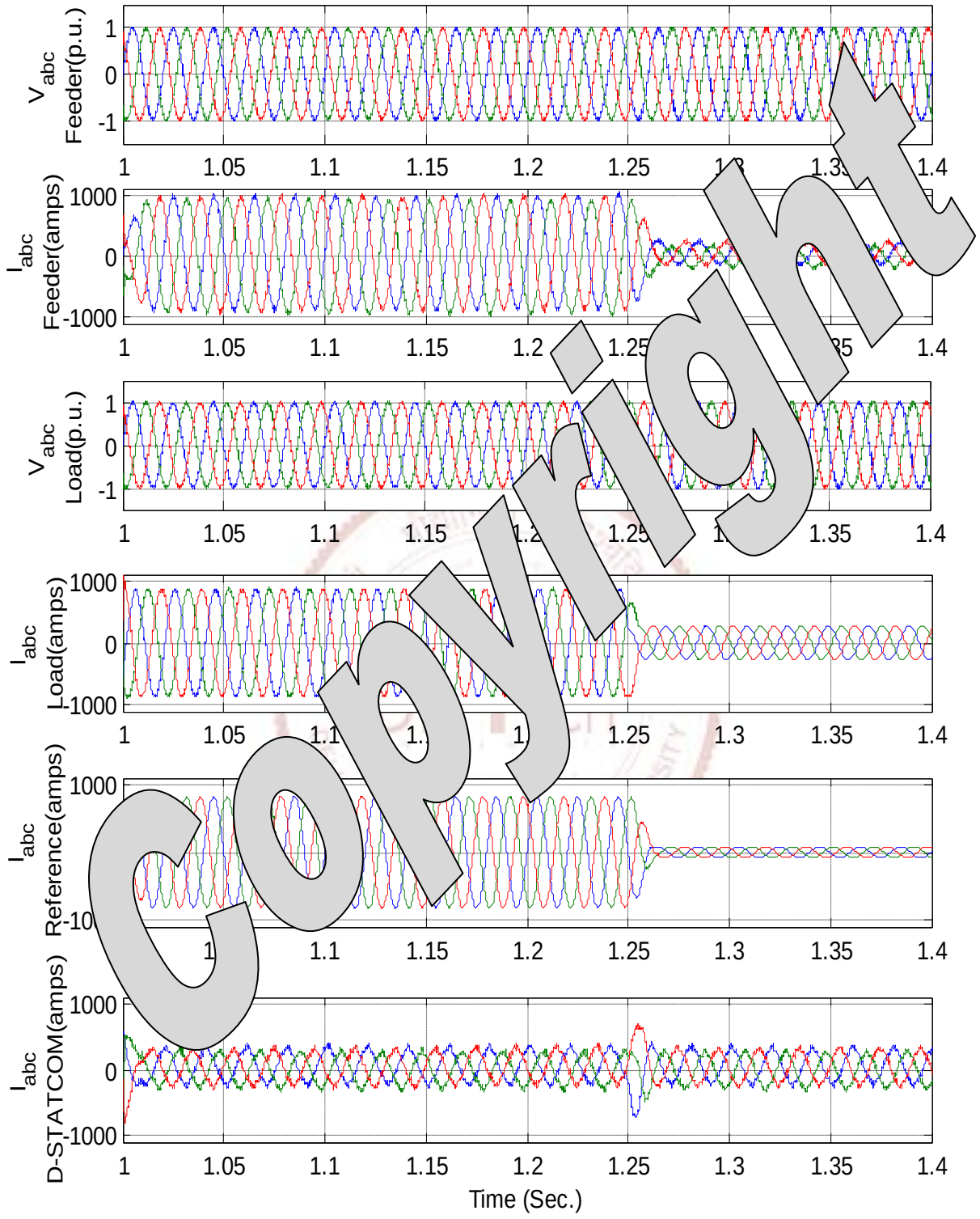

Figure 4.17 Simulated Result for the Proposed CHBMI based D-STATCOM for load impedance of 9.84+j3.06 Ω and 10.2+ j31.4 Ω (Load Transition Instant = 1.25 Second).

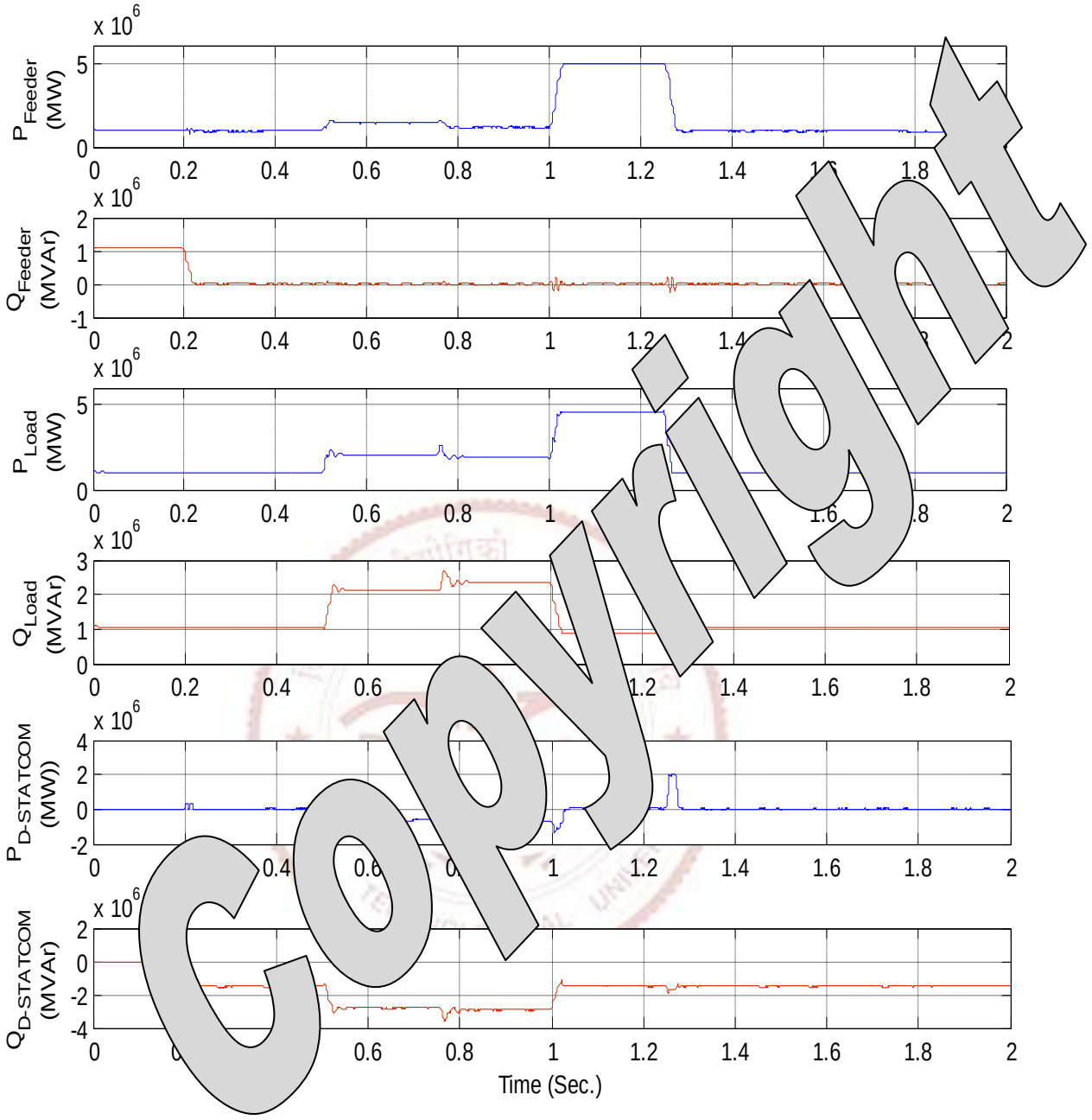

Figure 4.18 Active and Reactive Power Requirements for the Proposed System.

4.3.2 Application of D-STATCOM for Selective Harmonic Mitigation

Fig. 4.19 shows the model of proposed D-STATCOM with a thyristor converter load to evaluate the performance of D-STATCOM for selective harmonic mitigation. The controller shown in Fig.4.20 employs two SRF extractor tuned to 5^{th} and 7^{th} harmonic frequencies as to compute the quantum of harmonics. The selective compensation is chosen for the fact that multilevel converters are suited for the compensation of low harmonic frequency component as

they can be compensated at lower PWM frequencies. The SRF extractor is tuned individually to prominent harmonics (5^{th} and 7^{th}) for their mitigation from source current.

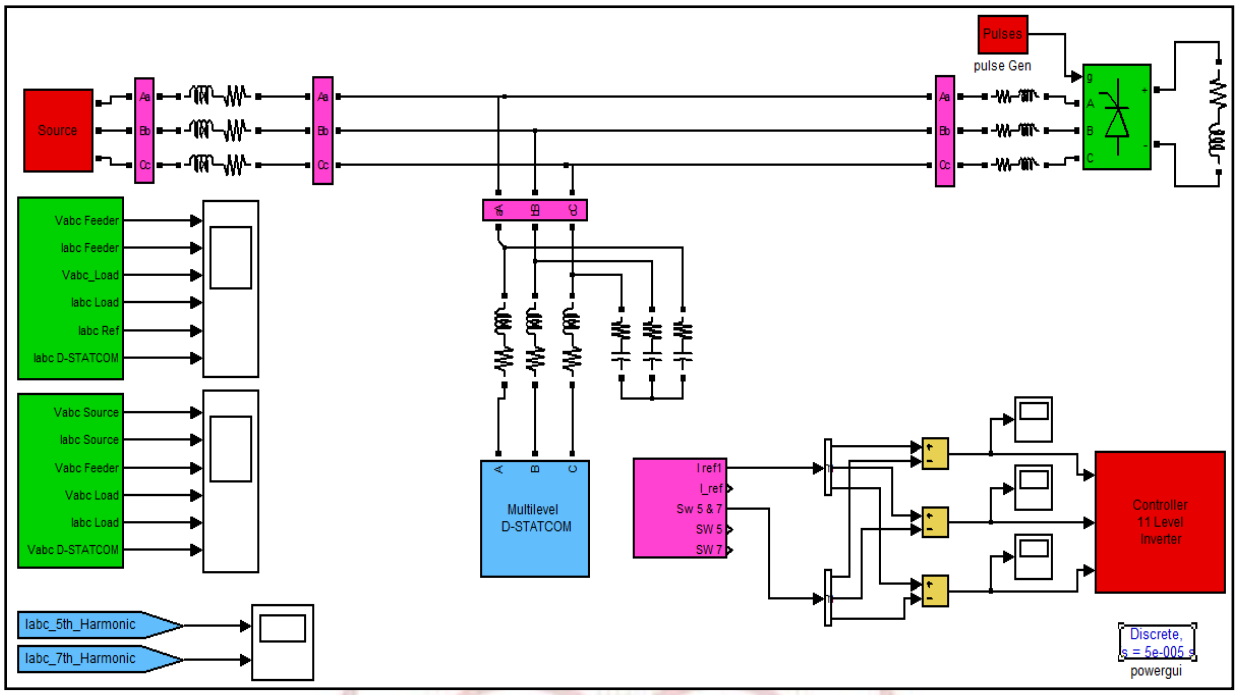

Figure 4.19 SIMULINK model of the CHBMI based D-STATCOM along with its controller for the Selective Harmonic Mitigation

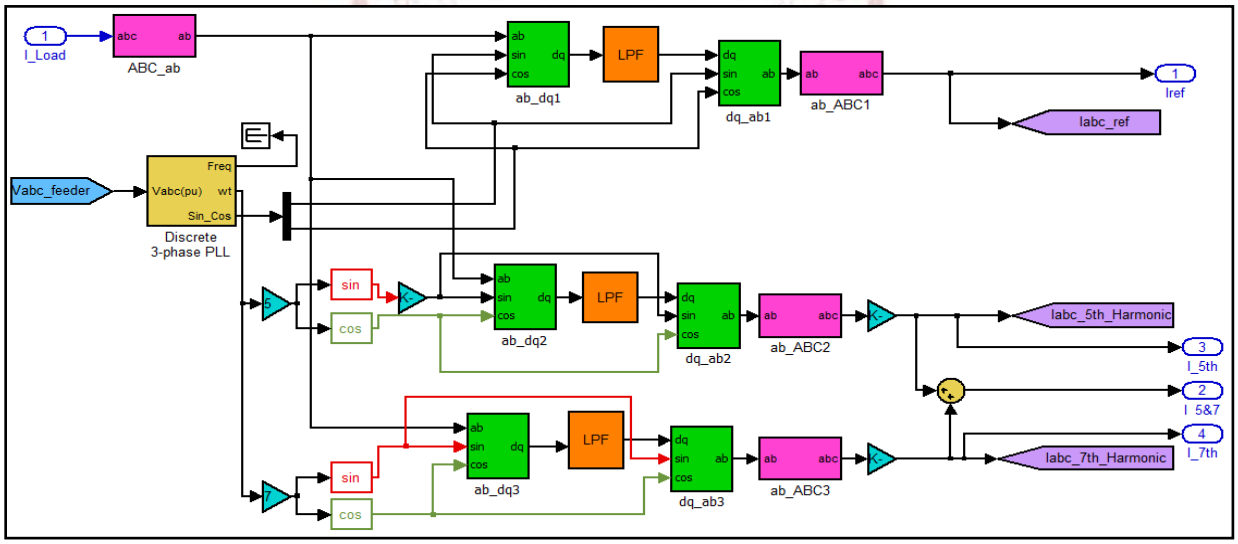

Figure 4.20 Controller for the CHBMI based D-STATCOM for Selective Harmonic Mitigation.

4.3.2.1 Control Strategy

Fig. 4.20 shows the inside view of the controller used for the selective harmonic mitigation. The load current is Clarke and Park transformed into the decoupled components to extract the 5^{th}

and 7th harmonic current, while running the PLL at 5th and 7th harmonic frequencies. A low pass filter is employed at d-q frame to smoothen the ripples corresponding to frequencies other than dc components to extract separately the 5th and 7th harmonic components present in the load current. The generated currents corresponding to 5th and 7th harmonic frequencies may be used for selective harmonic compensation using direct current control of the DSTATCOM. The direct current control compares the reference currents with the D-STATCOM current to produce the PWM signals.

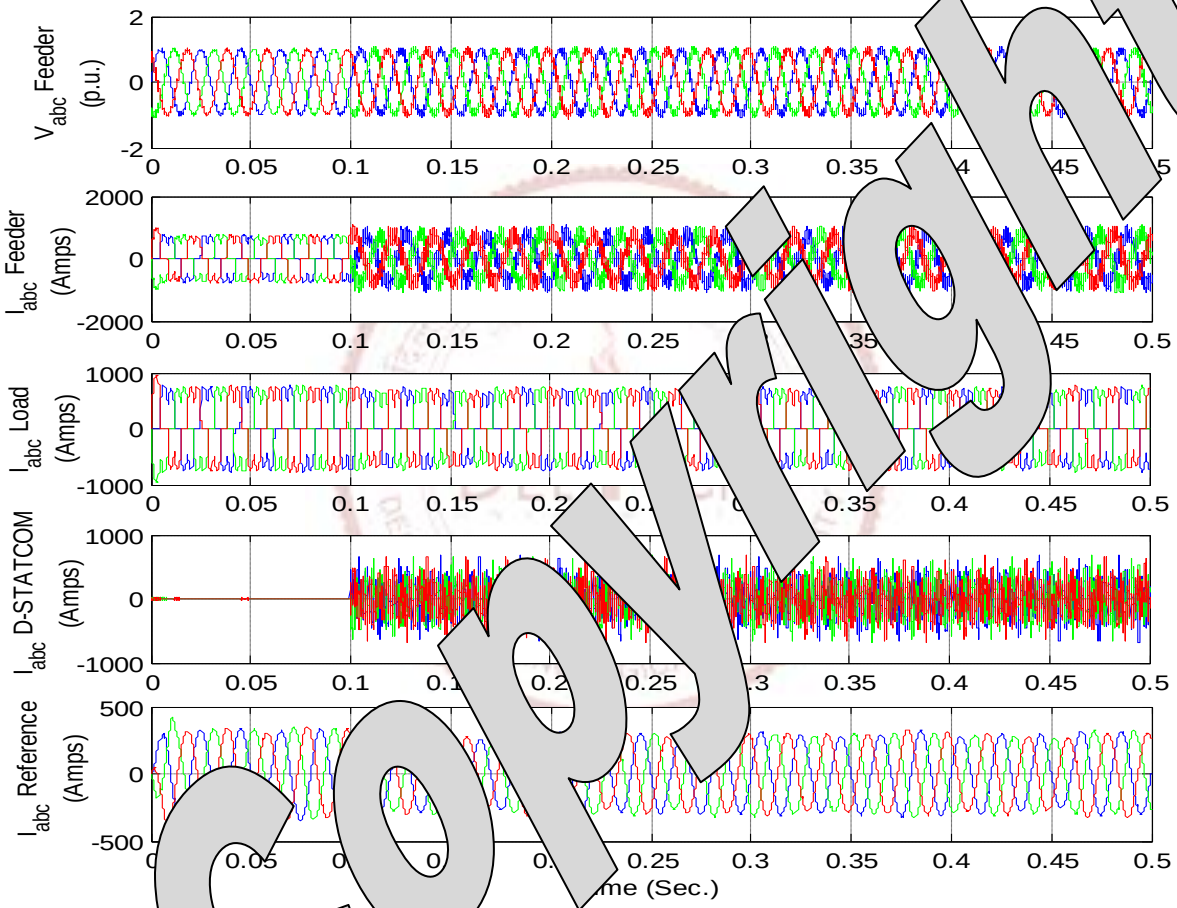

Figure 4.21 Simulated Results for the Mitigation of Selective Harmonics (5th and 7th) by the CHBMI based D-STATCOM

4.3.2.1 Results and Discussion

Fig.4.21 depicts the results for the proposed controller for the mitigation of 5th and 7th harmonics. The thyristor converter is considered as connected load which inject large harmonic contents at the PCC. It may be evident from Fig.4.21 from t=0.0s to t=0.2s, when the D-STATCOM is not switched in, the feeder current follows the load current and is contaminated

with huge harmonic components. As the D-STATCOM is switched in at t=0.2 sec., it starts compensating 5^{th} and 7^{th} harmonics almost instantaneously. It may be observed that 5^{th} and 7^{th} harmonics are nearly eliminated and the %THD of feeder current reduces from 31.1% to 18.63%. Further details are provided in Table 4.4 gives the quantum of 5^{th} and 7^{th} harmonic current magnitude in the feeder currents. The value of %THD is observed as 17.12%, 31.69% and 18.63% for compensation of only 5^{th} harmonic component, only 7^{th} harmonic component and compensation of both (5^{th} and 7^{th}) harmonics respectively.

Table 4.4 Percentage (%) Contamination of the Harmonics in Feeder Current (e he P ed System in Case of Different Harmonic Mitigation:

Harmonic Order	Contamination of Specific Harmoni %)			
	Without Mitigation	5^{th} Harmonic Mitigation	7^{th} Harm itiga	Bo 5^{th} and 7^{th}) H nonics Mitigation
5^{th}	27.21	**2.53**	9	**0.86**
7^{th}	5.22	2.93	0	**1.23**
11^{th}	9.36	7.92	8.0	6.88
13^{th}	3.33	1.69	2.71	2.08
17^{th}	4.46	3.6	4.98	4.08
19^{th}	2.76	2.4	2.59	2.25

4.4 Conclusion

The performance of the ca ded ridg multile inverter is evaluated for different configuration. Among the on ns th ighest level configuration i.e. eleven level in this th ws v prom g r s. This model is later configured for modelling of D-STATCO or managi ctive wer in a sub-transmission/11 kV distribution system. The s m perf anc the management of reactive power and selective harmonic mitigation is pr ed w he help of simulation in SIMULINK/PSB with load perturbations. The results prese s chapter prove the effectiveness of the present topology and its control.

CHAPTER 5

MAIN CONCLUSION AND FUTURE SCOPE OF THE WORK

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5.1 General

The main objective of the work has been focused on modelling and development of a controller for the cascaded H-bridge multilevel D-STATCOM. The developed structure of the model and the switching sequence is developed and simulated in the MATLAB/SIMULINK platform. Various operating conditions and results have been presented and discussed in the previous chapter.

5.2 Main Conclusion

The cascaded H-bridge multilevel inverter based D-STATCOM model and its control has been thoroughly investigated. The main focus of the study has been towards the development of a control scheme that work with simplicity and is easy to implement, offer faster dynamics, robust in operation and have flexibility for future upgradation. Step by step efforts have been made in the desired direction. The main conclusions dealt in the thesis work are:

- SIMULINK/PSB Modelling of various cascaded H-bridge multilevel inverters with the controller for different levels.
- Comparative study of the cascaded multilevel inverters for different level of voltages, their dynamic performance and the THD.
- Investigation in the inverter structure and controller are designed to provide the flexibility in future upgradation.
- A controller based on current control technique is developed as it provides the faster dynamics and easy control.
- Various simulated results are obtained to prove the validation and effectiveness of the chosen scheme for the implementation in the D-STATCOM.
- A simulation study of reactive power compensation using multi level D-STATCOM model and its controller using SIMULINK/PSB.
- Controller model dynamics shows the effectiveness of controller for the real time control of the reactive power.
- Faster dynamics of the control algorithm.
- Selective harmonic elimination with multilevel inverters and improvement of THD has also been studied.
- Simulated results prove the efficacy of the controller in selective harmonic elimination.

5.3 Suggestions for Future Work

The areas in which the presented work can be extended and further advancements, these are listed as follows:

- The laboratory prototype of the proposed system can be developed to validate the design, model and control techniques.
- The self supported DSTATCOM model may be developed employing the capacitor at dc bus, and maintaining constant average voltage at each capacitor based on the levels of the voltages.
- The scheme is presented taking one problem of either management of reactive power or harmonic mitigation at one time. A controller addressing more than one power quality problem can be designed.
- The proposed scheme can be extended for the operating the multilevel D-STATCOM structure in the voltage mode separately and combining with the presented current control scheme. This method may provide the faster harmonic mitigation based on current control mode and; management of reactive power and voltage regulation in voltage control mode simultaneously or separately.

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