CHAPTER 1

INTRODUCTION

1.1 Introduction:

For introducing Chua's circuit, one definitely needs to know about chaos. This chaos theory was introduced by a mathematician named H. Poincare in 1905. In mathematics chaos theory describes the behaviour of a certain dynamical systems i.e. system whose state evolves with time that may exhibit dynamics that are highly sensitive to initial condition.

Chua's circuit is the simplest autonomous circuit that exhibits chaos. Chaos is characterized by a stretching and folding mechanism. Nearby trajectories of a dynamical system are repeatedly pulled apart exponentially and folded back together. Since the discovery of Chua's circuit, it is always served as the main prototype circuit for studying chaos in electronic systems.

1.2 Chua circuit:

Chua's circuit was invented by Leon CHUA IN 1983. While on a visit to Japan, having witnessed a futile attempt at producing chaos in an electrical analog of Lorenz's equation Leon Chua was prompted to develop a chaotic electronic circuit. He realized that chaos could be produced in piecewise linear circuit if it possessed at least two unstable equilibrium points- one to provide stretching and the other to fold trajectories. With this insight, he systematically identified those third order piecewise linear circuits containing a single voltage controlled non linear resistor that could produce chaos. Specifying that the driving point characteristics of the voltage controlled non linear resistor N_R should be chosen to yield at least two unstable points, he invented Chua's circuit.

Soon after its conception, the rich dynamical behaviour of chua's circuit was confirmed by computer simulation and experiment. Since then, there has been an intensive effort to understand every aspect of the dynamics of the circuit with a view to develop it as a paradigm for learning, understanding and teaching about non linear dynamics and chaos.

While differential equations and mechanical system provide convenient frameworks in which to examine bifurcation and chaos, electronic circuits are unique, in being easy to build, easy to measure and easy to model. Furthermore they operate in real time, and parameter values are easily adjusted. Just as the linear parallel RLC resonant circuits the simplest paradigm for understanding periodic steady state phenomena in linear

circuits, so chua's circuit presents an attractive paradigm for studying non periodic phenomena in nonlinear circuits. The importance of chua circuit and its relative is that they can exhibit every type of bifurcation and attractor that has been reported till date in third order continuous time dynamical systems. While exhibiting a rich variety of complex dynamical behaviour , the circuit is simple enough to be constructed and modelled by using standard electronic parts and simulators.

Moreover, this remarkable circuit is the only physical system for which the presence of chaos has been proven mathematically.

1.3 Chaos theory:

Chaos is characterized by a stretching and folding mechanism. Nearby trajectories of a dynamical system are repeatedly pulled apart exponentially and folded back together. Since the discovery of Chua's circuit, it is always served as the main prototype circuit for studying chaos in electronic systems.

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CHAPTER 2

LITERATURE REVIEW

The first time that chaos is found in history is in 1885 in Sweden. King Oscar I1 had question about a 'three-body problem'. Three planets in space, which moves in regard to each other by mutual gravitation forces. The person who would solve this question would receive a price. The same question, but then with two planets, was years before solved by Newton. But this case is much more difficult.

A mathematician named Henri Poincare sends in an opinion of what he thinks is the answer. Moments before publication he noticed he has made a mistake. He explained that the problem in some way is unsolvable. The reason why this problem is unsolvable is that a very small difference in the start position or velocity can make a huge difference in the final result. With this conclusion Poincare had the chaos principle.

Edward Lorenz has also an important place in the history of chaos. In the sixties he developed computer models. One of these models is of the earth atmosphere at the Northern hemisphere. He made a lot of calculations to six decimal places. When he rounded off these numbers to three decimal places, the result was astonishing. In the beginning the old and new calculations coincided, but after some time the results were totally different. The conclusion is that the results of his calculation are strongly depended on the starting point. A small different in the start position can lead to large differences in the final result. When he repeated the process many times, by which he used the results as starting points. The differences in the results are plotted in a three dimensional graph, a butterfly appears then. This graph is also called the Lorenz attractor.
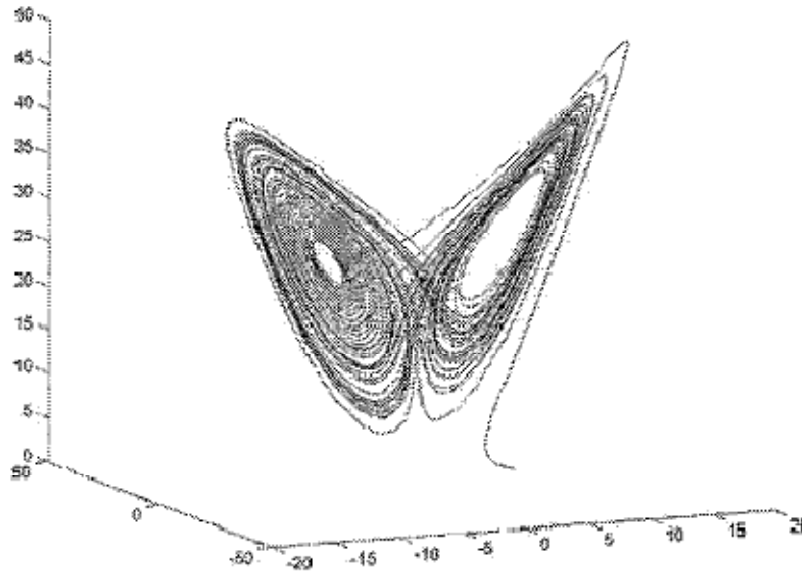
Fig. 2.1: The Lorenz Attractor

The first observations of chaos in electronical circuits are in 1927 by Van der Pol and Van der Mark. They see it in non linear oscillators. In 1980 Ueda and Akamastu find chaos in negative resistance oscillators. But the circuit of Chua is bit more special because of its simplicity and university. Since its discovery Chua's circuit has served as the main prototype circuit for studying chaos in electronic systems.[Matsumoto[4],1984]

Several realizations of this circuit have been introduced in the literature [Cruz &Chua,[5,21] 1992; Kennedy[2,20] 1992, 1995; Rodriguez – Vazquez & Delgado-Restituto, 1993; Zhong[7], 1994; Elwakil & Kennedy,[23] 1999a, [24]1999b, [25]2000]. These various implementations were concerned with two main design aspects of Chua's circuit. The first aspect is the realization of the voltage controlled non linear resistor [Cruz &Chua,[5,21]1992; Kennedy,[2,20]1992; Zhong,[7]1994; Elwakil &Kennedy,[24]1999b,[25]2000] and the second aspect is the removal of the inductor as it is generally difficult to integrate [Rodriguez-Vazquez &Delgado-Restituto,1993; Morgul,[6]1995;Elwakil & Kennedy, [23]1999a].

The chaotic nature of Chua's circuit was observed by Matsumoto in 1983 using computer simulation, following the instructions of Chua who had invented this circuit and had explained

its operating principles to Matsumoto moments before he was rushed to the hospital for a major surgery and who did not participated in the early phases of this research.

In acknowledging his subsidiary role as a computer programmer, Matsumoto named this circuit Chua's circuit.

The first experimental Chua's circuit which confirms the presence of chaos was due to Zhong and Ayrom [17] in 1984. A second experimental circuit was reported by Matsumoto shortly after and was designed by Tokunaga who is also responsible for obtaining all of the experimental results presented in that paper. The global bifurcation landscape of Chua's circuit was obtained by Komuro and a team of students of Matsumoto. The colorful bifurcation landscape in this paper was drawn by a professional artist.

The first rigorous proof of the chaotic nature of Chua's circuit was given, when the authors proved that there exist some parameters (α, β) such that the Chua's circuit satisfies Shil'nikov's theorem and therefore has infinitely many horseshoe maps. Although the authors are listed in alphabetical order as a compromise to Matsumoto's tradition of ordering his name first in earlier publications on Chua's circuit, the rigorous proof of the main theorem is due to Komuro. However since the limiting cantor set from a horseshoe map is not an attractor, this result does not imply that the double scroll Chua's attractor [1] is directly related to the chaotic phenomena associated with the horse shoe map. This unsatisfactory situation has now been resolved by a recent proof that a 2D geometrical model of Chua's circuit gives rise to a double horse shoe map which generates strange attractors.

Another milestone was achieved in 1990 when a canonical circuit was discovered which is qualitative equivalent of a 21- parameter family C of continuous odd symmetric piecewise-linear vector fields.

Inspired by a question posed by professor J. Neirynck in 1991 on whether this canonical circuit is unique, a systematic search has since been completed by several researchers, including A. Huang and Lj. Kokarev, where many more distinct canonical circuits has been found. The universal Chua's circuit presented in this paper is therefore only one among many qualitatively equivalent circuits in the class C.

CHAPTER-3

CHUA'S CIRCUIT

3.1General:

Chua's circuit is one of the most popular nonlinear dynamical systems used to investigate the dynamic behavior in all possible states: Periodic, quasi-periodic and chaotic. It is very simple electronic circuit capable to exhibit a rich dynamical behavior. It was introduced in 1987 by Leon O. Chua (Chua and Desoer, 1987, Santoboni, 1999), since then; the ease of construction of the circuit has made it a natural real-world example of a chaotic system. It was the first physical implementation of chaos which has been rigorously proved (Kapitaniac, 2000). Any autonomous circuit made from standard components (resistors, capacitors, inductors) must satisfy three criteria in order to show chaotic behavior:-

i)   at least one non linear element

ii)   one or more locally active resistor

iii)   three or more energy storage elements

Chua's circuit is the simplest electronic circuit meeting these criteria (Itohand Hayashi, 1998). This circuit has been studied extensively since its initial proposal, and serves as a test platform for many research areas that involve bifurcation processes including chaos. (Calvo et al., 2001). The robustness, ease of implementation, and its nonlinear behavior contribute to the success between theoretical and experimental researches of chaos theory.

$$c_1 \frac{dv_1}{dt} = \frac{1}{R}(v_2 - v_1) - f(v_1) \qquad\qquad 3.1.1$$

$$C_2 \frac{dv_2}{dt} = \frac{1}{R}(v_1 - v_2) + i_L \qquad\qquad 3.1.2$$

$$L\frac{di_L}{dt} = -v_2 - R_o i_L \qquad\qquad 3.1.3$$

The equations shown above are differential equations of Chua's circuit.

In the figure shown below it is shown how Chua circuit looks like. Where C_1 and C_2 are the parameters of the conductors. R is the changeable resistance, R_o is the internal resistance of the coil and L is the constant value of the coil.

N_R is the value of the negative resistance. The measured values are V_1, V_2 and I_L. These values can be measured, which will give experimental results. But they can also theoretically be calculated by the differential equations above.
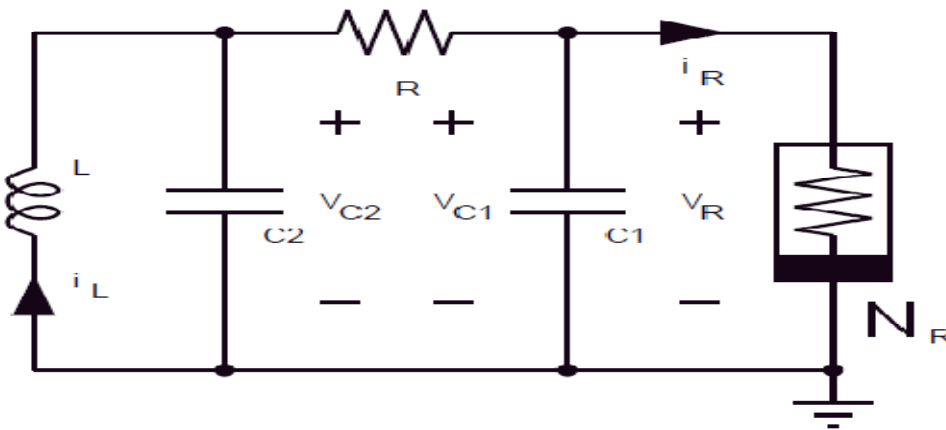
Fig. 3.1: Chua's Circuit Schematic. The circuit consists of a linear inductor L, a linear resistor R, two linear capacitors C_1 and C_2 and a nonlinear resistor N_R.
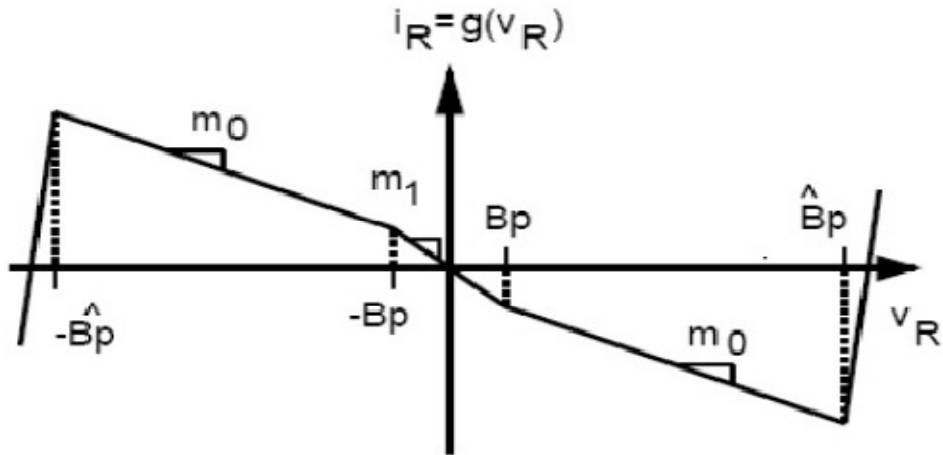
Fig. 3.2: The i-v characteristic of the nonlinear resistor N_R. Every physically realizable nonlinear resistor is eventually passive – the outermost segments must lie within the first and third quadrants of the v-i plane for sufficiently large |v| and |i|.

The state equations for Chua's circuit are shown below

$$C_1 \frac{dv_{c_1}}{dt} = \frac{v_{c_2} - v_{c_1}}{R} - i_R \qquad\qquad 3.1.4$$

$$C_2 \frac{dv_{c_2}}{dt} = \frac{v_{c_1} - v_{c_2}}{R} + i_L \qquad\qquad 3.1.5$$

$$L \frac{di_L}{dt} = -v_{c_2} \qquad\qquad 3.1.6$$

In above equations

$$i_R = g(v_R) = g(v_{c_1})$$

It is a piecewise linear function

$$g(v_R) = m_0 v_R + \frac{1}{2}(m_1 - m_0)[|v_R + B_p| - |v_R - B_p|] \qquad\qquad 3.1.7$$

It can be inferred that the slopes in the inner and outer regions are m_1 and m_0 respectively; $\pm Bp$ denote the breakpoints.

It is difficult to obtain precise values of the inductor needed to build the circuit. Also, the inductor is quite bulky and it cannot be integrated on a chip. Moreover, many commercially available inductors have a core that is added to increase the inductance (and hence reduce the number of windings needed). But, this is known to have the effects of adding distortion to the signal via hysteresis.

The sensitive dependence on initial conditions for the chaotic circuit, this would be largely undesirable. One solution is to simulate the inductor using a gyrator which uses a two op-amp implementation of the gyrator. In this paper, we use a simpler synthetic inductor implementation. Specifically:

1) We use only one op-amp for the synthetic Inductor.

2) All components are off-the-shelf (a parts list is included at the end of this paper).

3.2 The Non-Linear Resistor Concept and Chua Diode:

The term Chua's diode is a general description for a two-terminal nonlinear resistor with a piecewise linear characteristic. In the literature, Chua's diode is defined in two forms. As shown in fig. 3.3a the first type of Chua's diode is a voltage-controlled nonlinear element characterized by $I_R = f(V_R)$, and the other type is a current-controlled nonlinear element characterized by
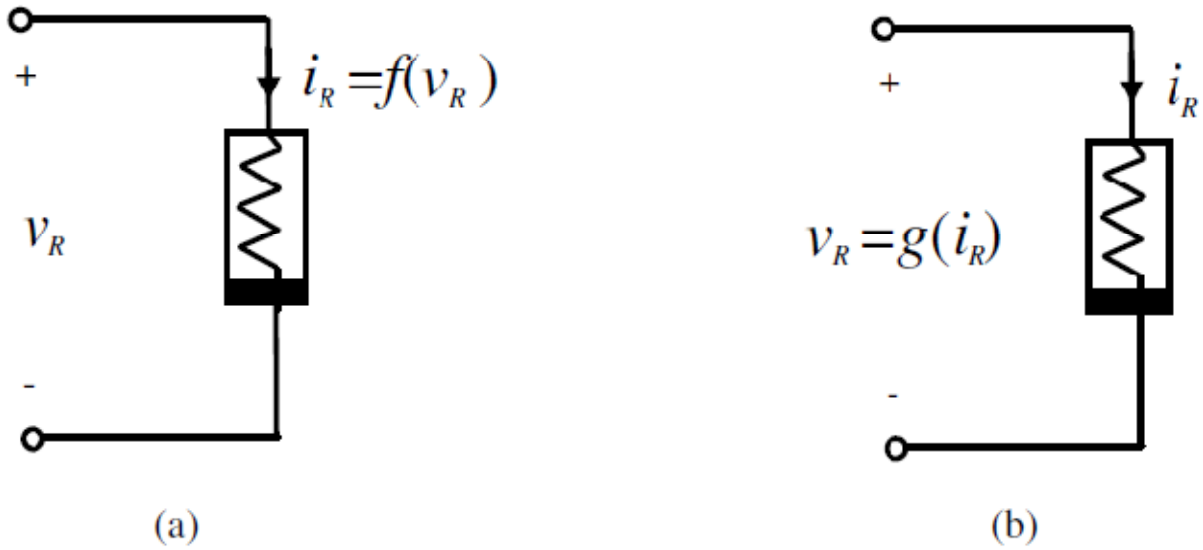
$V_R = g(I_R)$.

$$i_R = f(v_R)$$

$$v_R$$

$$v_R = g(i_R)$$

$$i_R$$

(a)   (b)

Fig. 3.3 (a) Voltage-controlled Chua's diode, 3.3(b) current-controlled Chua's diode.

Chaotic oscillators designed with Chua's diode are generally based on a single, three - segment, odd symmetric, voltage-controlled piecewise linear, nonlinear resistor structure. Such a voltage-controlled characteristic of Chua's diode is given in Fig.3.4
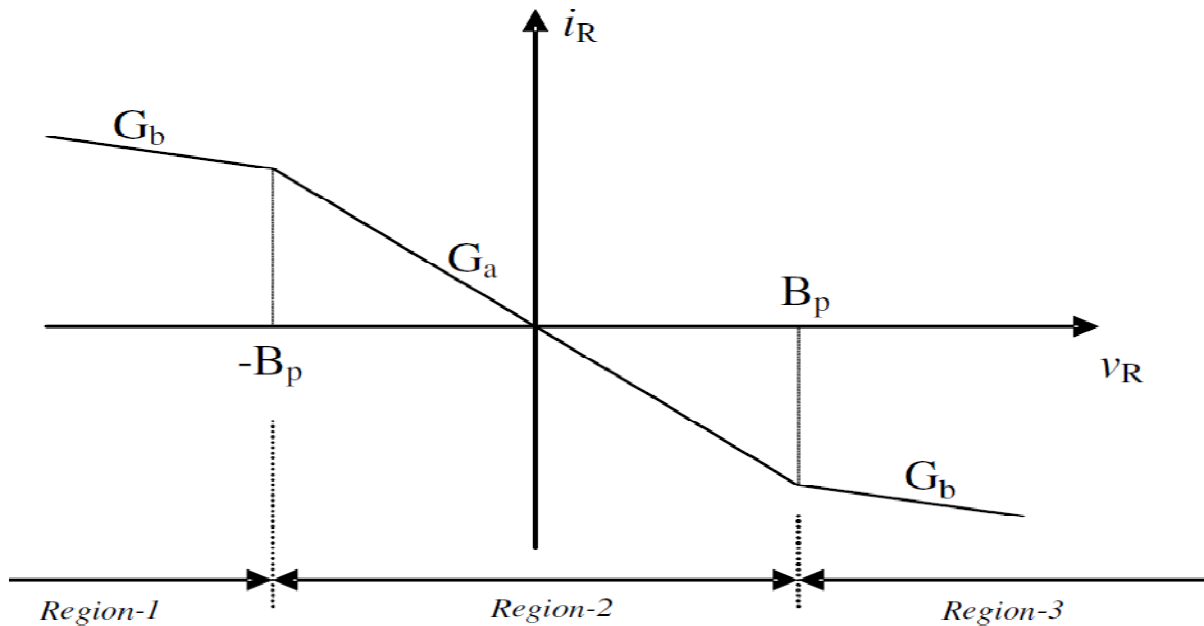

Fig. 3.4 : Three-segment odd-symmetric voltage-controlled piecewise-linear characteristic of Chua's diode.

This characteristic is defined by

$$i_R = f(v_R) = G_b v_R + 0.5(G_a - G_b)[|v_R + B_p| - |v_R - B_p|] \qquad \text{3.2.1}$$

$$= \begin{cases} G_b v_R + (G_b - G_a)B_p, & v_R < -B_p \\ G_a v_R, & -B_p \le v_R \le B_p \\ G_b v_R + (G_a - G_b)B_p, & v_R > B_p \end{cases}$$

In this definition, Ga and Gb are the inner and outer slopes, respectively, and $\pm Bp$ denote the breakpoints. Now, let us demonstrate why Eq. (3.2.1) defines the ($v - i$) characteristic of Fig. 3.4. For this Piecewise Linear (PWL) analysis, our starting point is the "concave resistor" concept.

The concave resistor is a piecewise-linear voltage controlled resistor uniquely specified by (G, Bp) parameters.

3.3 Circuit topology and realization of chua diode:

This section discusses several circuitry designs of Chua's diode. After giving various circuit realizations for Chua's diode, we compare these realizations with respect to circuit design issues.

This section discusses several circuitry designs of Chua's diode. A realization of Chua's diode proposed by Kennedy, which is designed by connecting two voltage-controlled negative impedance converters in parallel, has been accepted as the standard for discrete implementation. This op amp–based nonlinear resistor structure with its simulated dc characteristic is shown in Fig.3.5.
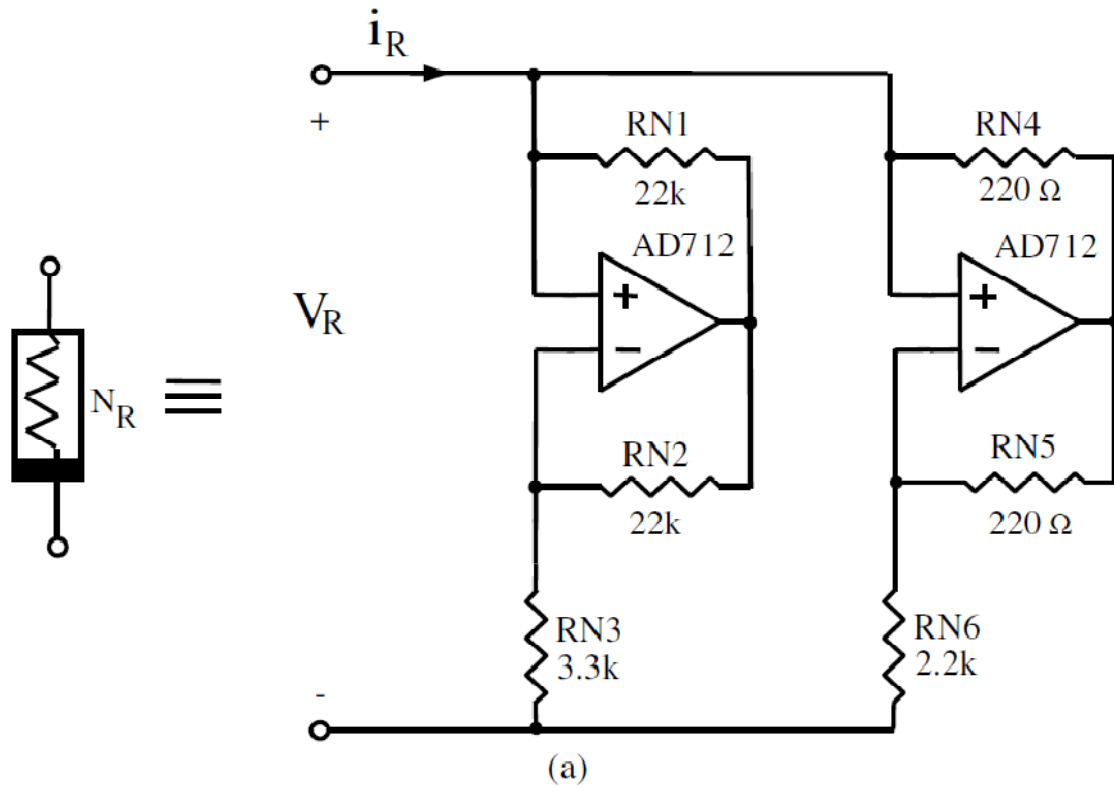
(a)

Figure: 3.5 (a) The op amp–based nonlinear resistor structure implemented by Kennedy
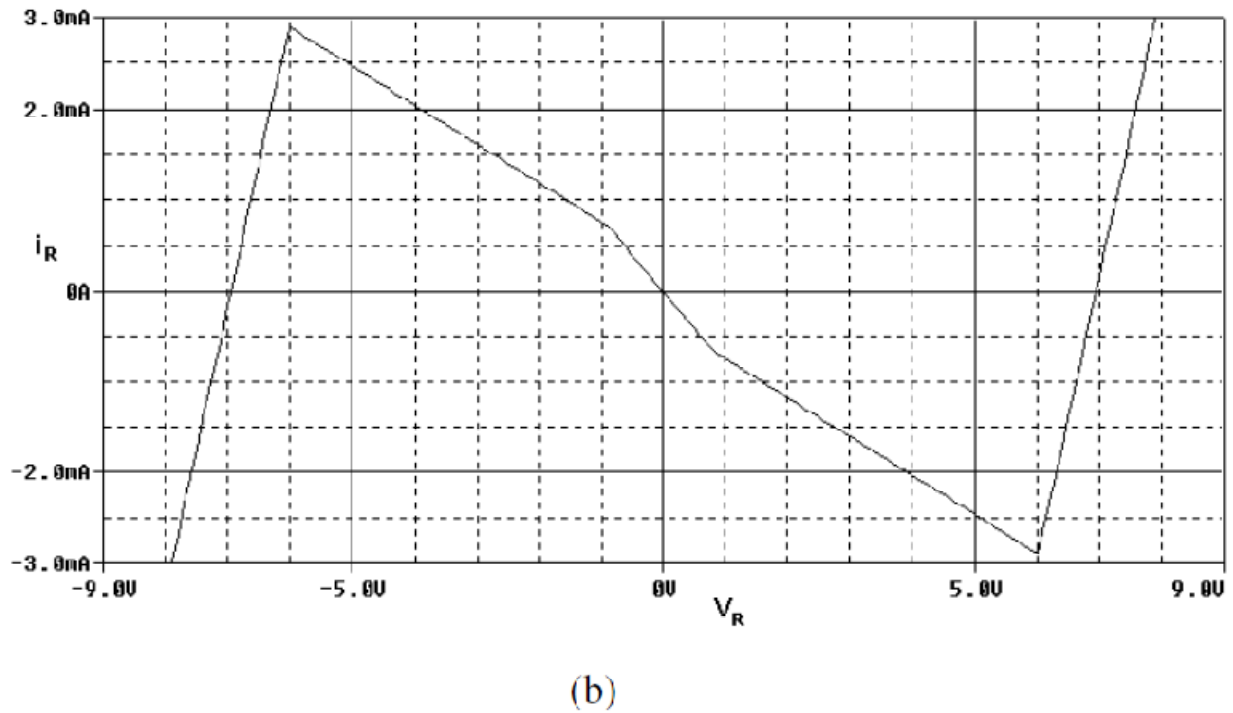

(b)

Fig.3.5 (b) simulated v-i characteristic of the nonlinear resistor of Fig. 3.5(a).

As shown in Fig. 3.5(a), this realization uses two op amps, operating in both their linear and nonlinear region, and six resistors. The slopes and breakpoints are chosen as Ga @ –0.756mA/V, Gb @ –0.409 mA/V and Bp = 1 V with the circuit parameters in Fig. 3.5(a). As Chua's circuit has a simple and easily configurable circuit structure, most of the experimental studies with it in the literature have been performed using this standard VOA-based implementation.

3.4 Software used :

Software which has been used in this proect is **multisim**. This is the software of national instrument company. In this software near about all components are available for making different types of electrical circuits. Function generator and cathode ray oscillscope, some non linear compnents as diodes, transistors, operation amplifiers are available in this software. There are also linear components as resistors, inductors, capacitors we can also varry the values of these component.

CHAPTER 4
REALIZATION OF CHUA CIRCUIT WITH DIFFERENT VALUE OF R10

4.1 Simulation and results of realization of chua circuit with different value of R10:
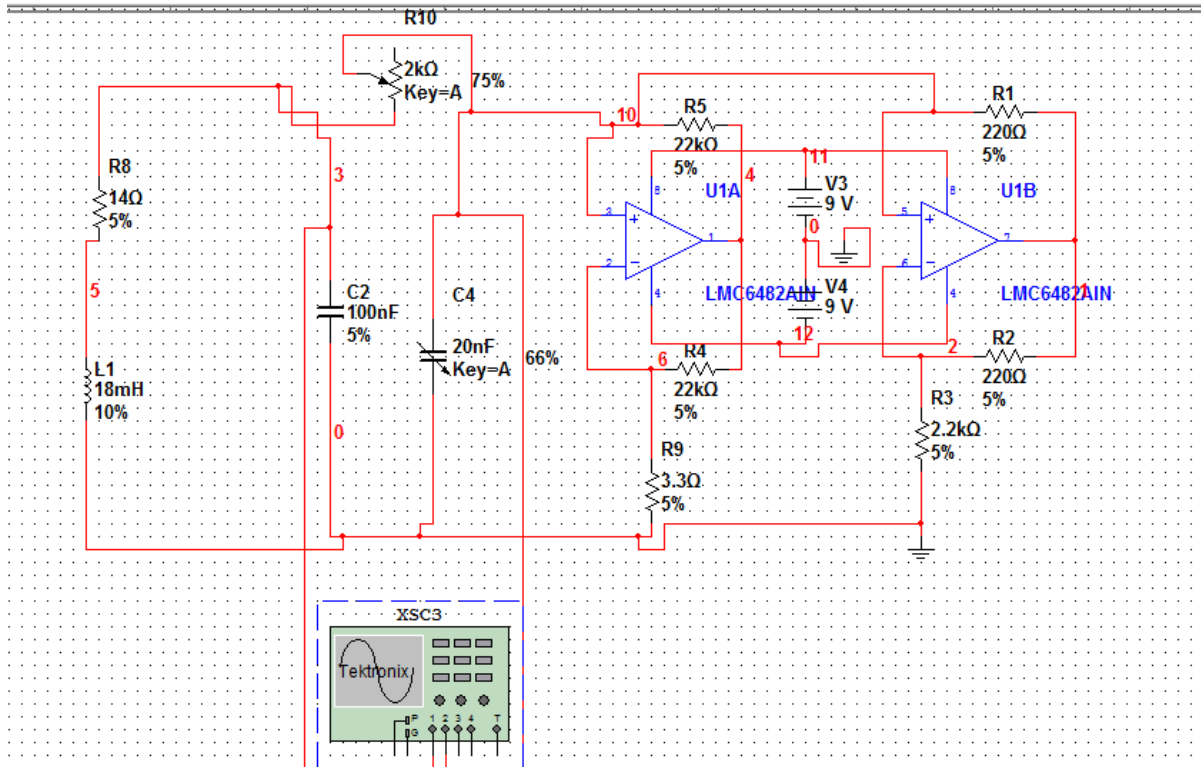

Fig.4.1: Screen Capture of multisim simulation of chua's circuit

The circuit is built from different electronically components so that the theory can be compared with the experiments.

The inductor and negative resistor are simulated by different OP-Amps, resistors and condensators. The adjustable resistor R can vary between one thousand and tow thousand.

First it is analysed how the outcoming voltage V_1 and V_2 change when the resistor changes. The system has a lot of stable points there is a periodic solution for V_1 and V_2 . The V_1-V_2 plot of a double loop are given above.

In Chua circuit using Inductor output is obtained across potentioter with different values of resistor R10. As we see in figures at the 1.1k ohm value value of R10 a saturate limit cycle is obtained. After increasing the values of R10 we get chaos.

4.2 V_1-V_2 Characteristic :
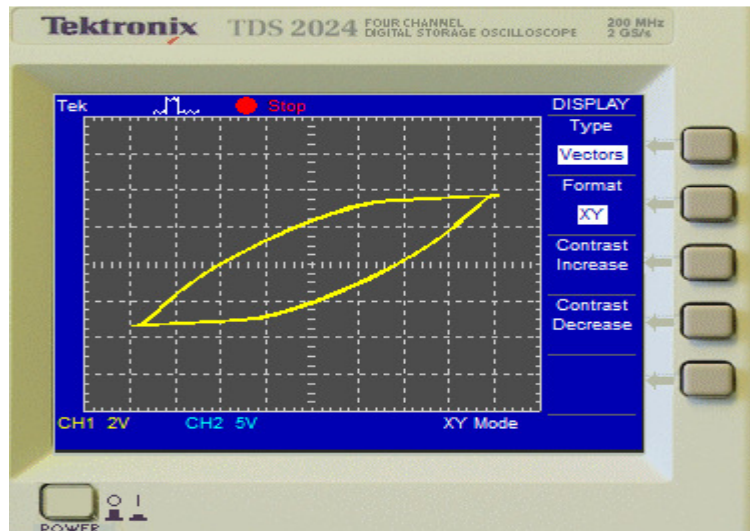
Fig.4.2. Limit cycle with R10 equal to 1.1k ohm.
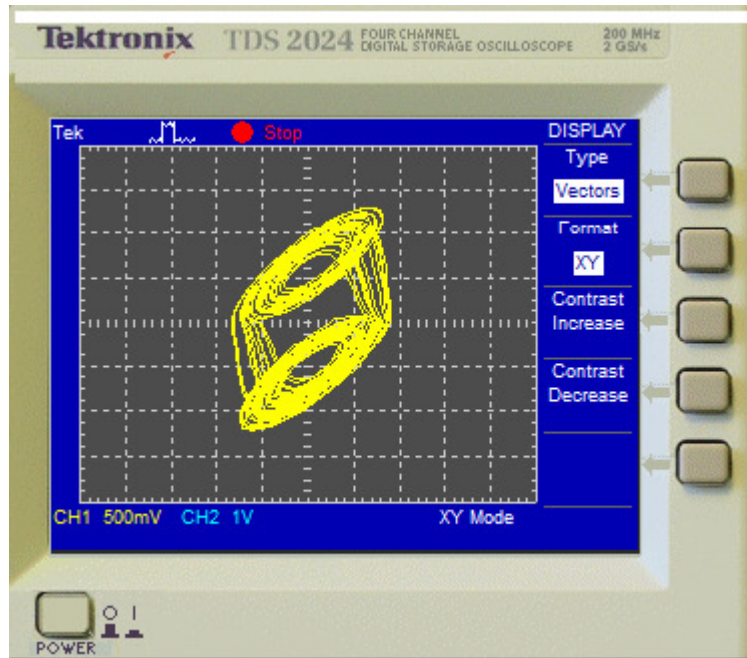
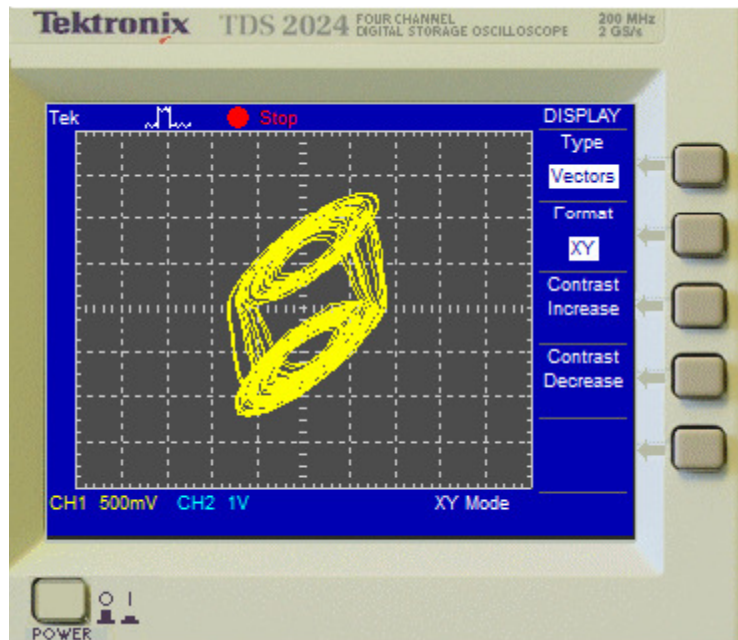**Fig.4.3. Double scroll chua's attractor with R10 equal to 1.2k ohm.**

Fig.4.4. Double scroll chua's attractor with R10 equal to 1.3k ohm.
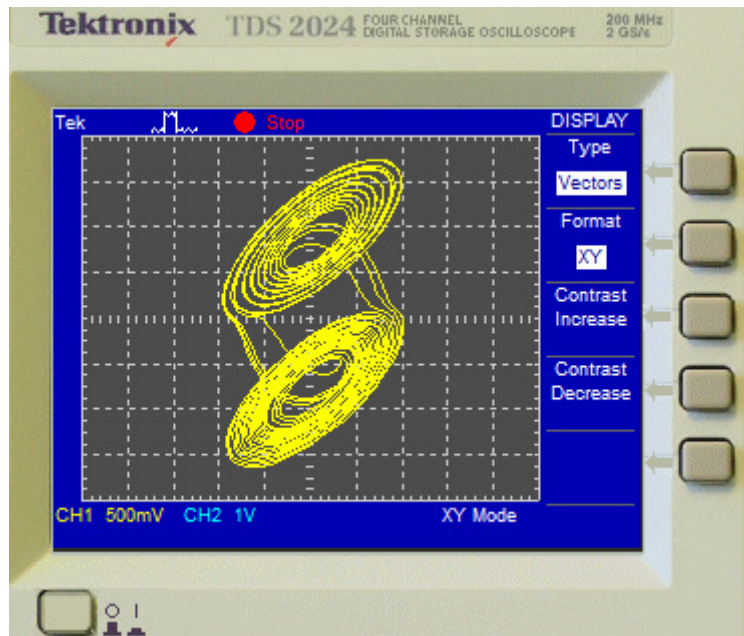
\

Fig.4.5. Double scroll chua's attractor with R10 equal to 1.5k ohm.

Fig.4.6. Double scroll chua's attractor with R10 equal to 1.6k ohm.

4.3 V_1(t)-V_2(t) Characteristic :

Here yellow waveform represents the channel 1st voltage V_{c1}(voltage across capacitor C_2) w.r.t. time and blue waveform represents channel 2nd voltage V_{c2}(voltage across capacitor C_4) w.r.t. time when the value of R10 is 75% of 2 kΩ.
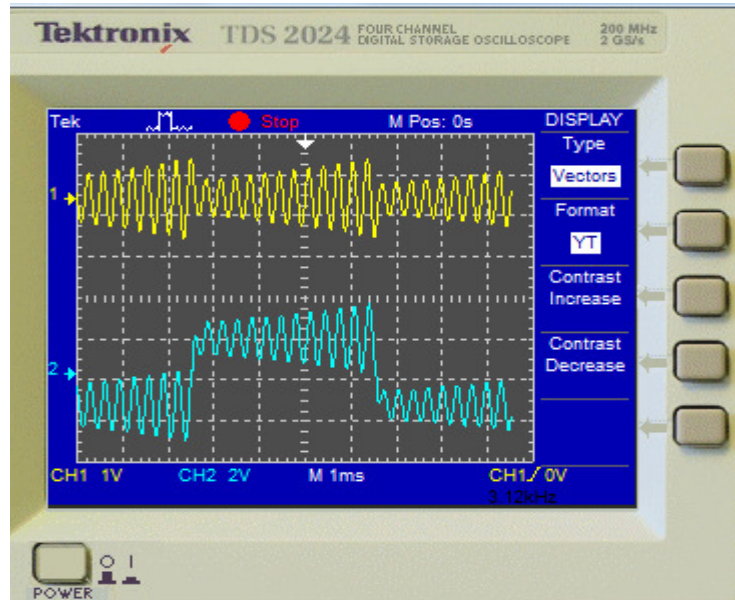

Fig.4.7 Y(t) format when realization of chua circuit as in fig.4.1

CHAPTER 5
REALIZATION OF INDUCTORLESS CHUA CIRCUIT

5.1 Simulation and results of realization of inductorless chua circuit:
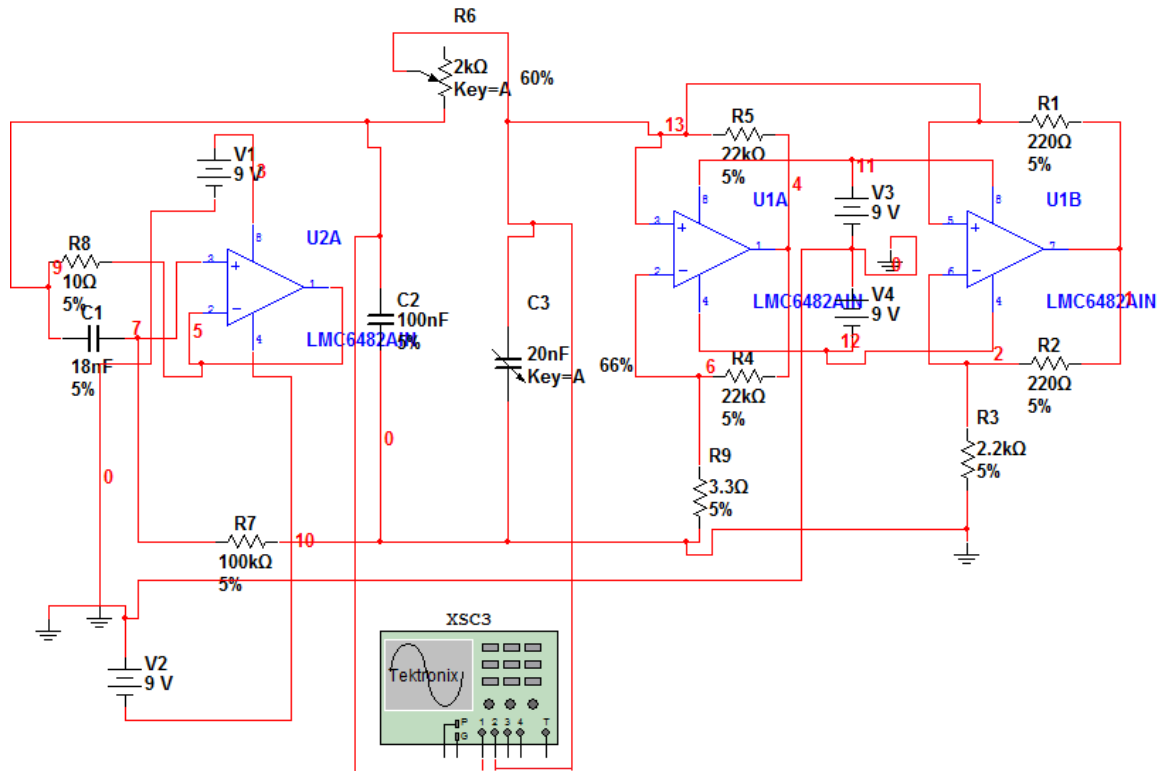

Fig.5.1:Chua's ciruit screen capture from Multisim's schematic editor. The 18 mh inductor has been replaced with single op-amp synthetic inductor and the chua diode has been made by using two op-amp implementation.
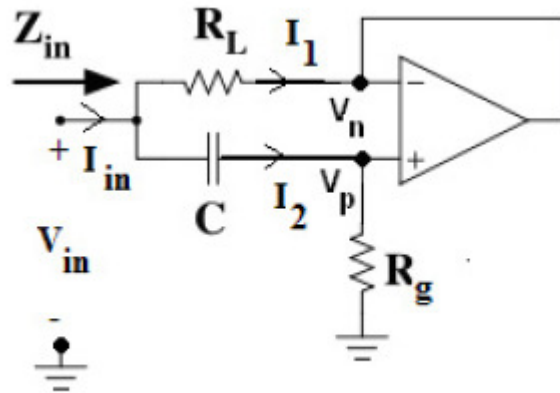
5.2 The Synthetic Inductor Impedance :

Fig. 5.2: The synthetic inductor circuit.

The goal is to derive an expression for Zin. We assume the op-amp is operating in the linear region. In above fig.5.2 shows the modified version of the synthetic inductor. If $R_L = 10^{-4}R_G$ (so that $R_L \ll R_G$). In fig. 5.2 we have:

$$Z_{in} = R_L + jwR_LR_GC \qquad\qquad 5.2.1$$

In case, $R_L = 10$, Rg = 100k and C = 18nF, so we have the equivalent circuit of Fig. 5.3 for an 18mH inductor.
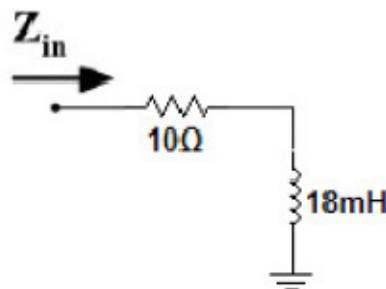

Fig.5.3: 18mH synthetic inductor circuit.

5.3 The Synthetic Inductor Impedance Derivation:

We will now derive the equivalent impedance of the synthetic inductor, as seen from its input terminals. Using Thevenin's theorem, we can write an expression for Zin in above fig.

$$Z_{in} = \frac{V_{in}(j\omega)}{I_{in}(j\omega)}$$

$$= \frac{V(j\omega)}{I_1(j\omega) + I_2(j\omega)}$$

$$= \frac{V_{in}(j\omega)}{\frac{V_{in}(j\omega) - V_n(j\omega)}{R_L} + \frac{V_{in}(j\omega)}{R_g + \frac{1}{j\omega c}}} \qquad 5.2.2$$

Assuming this using is operating in the linear region:

$$V_n(j\omega) = V_p(j\omega)$$

$$V_n(j\omega) = \frac{R_g}{R_g + \frac{1}{j\omega c}} \cdot V_{in}(j\omega) \qquad 5.2.3$$

Substituting for Vn(jω) in (5.2.2) from (5.2.3) and simplifying

$$Z_{in} = \frac{V_{in}(j\omega)}{\frac{V_{in}(j\omega) - \frac{R_g}{R_g + \frac{1}{j\omega c}} V_{in}(j\omega)}{R_L} + \frac{V_{in}(j\omega)}{R_g + \frac{1}{j\omega c}}}$$

$$= \frac{1}{\frac{1 - \frac{R_g}{R_g + \frac{1}{j\omega c}}}{R_L} + \frac{1}{R_g + \frac{1}{j\omega c}}}$$

$$= \frac{R_L}{1 - \frac{R_g}{R_g + \frac{1}{j\omega c}} + \frac{R_L}{R_g + \frac{1}{j\omega c}}} \qquad 5.2.4$$

Let $R_L = 10^{-4} R_g$ (so that $R_L << R_g$). Then substituting for RL in the denominator of (5.2.4):

$$Z_{in} = \frac{R_L}{1 - \frac{R_g}{R_g + \frac{1}{j\omega c}} + \frac{10^{-4} R_L}{R_g + \frac{1}{j\omega c}}}$$

$$\approx \frac{R_L}{1 - \frac{R_g}{R_g + \frac{1}{j\omega c}}}$$

$$= \frac{R_L + (R_g + \frac{1}{j\omega c})}{R_g + \frac{1}{j\omega c} - R_g}$$

$$= \frac{R_L (R_g + \frac{1}{j\omega c})}{\frac{1}{j\omega c}}$$

$$= j\omega c R_L (R_g + \frac{1}{j\omega c})$$

$$= R_L + j\omega R_L R_g C \qquad 5.2.5$$

Thus, if $R_L = 10^{-4} R_g$ (so that $R_L << R_g$), we have:

$$Z_{in} = R_L + j\omega R_L R_g C \qquad 5.2.6$$

Fig. 5.2 shows the circuit equivalent of eqn. 5.2.6

If R_L = 10, Rg = 100k and C = 18nF, we have the equivalent circuit of Fig. 5.2 for an 18mH inductor.

The difference between chua circuit using inductor and inductor less chua circuit is that inductor is replaced by one resistor R8 of 10 ohm, one capacitor of 18nf , and one op-amp U2A (LMC 6482 AIN). here we use inductorless chua circuit. In CRO we get output by taking different values of potentiometer R6. At 1.2k ohm of R6 we get limit cycle and by increasing the value of R6 we obtained chaos.
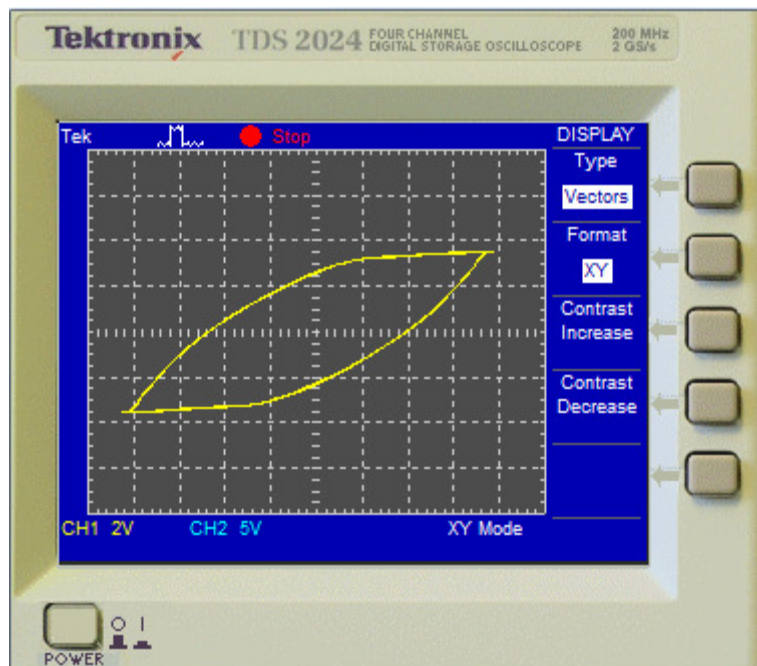
5.4 V1–V2 Characteristics :
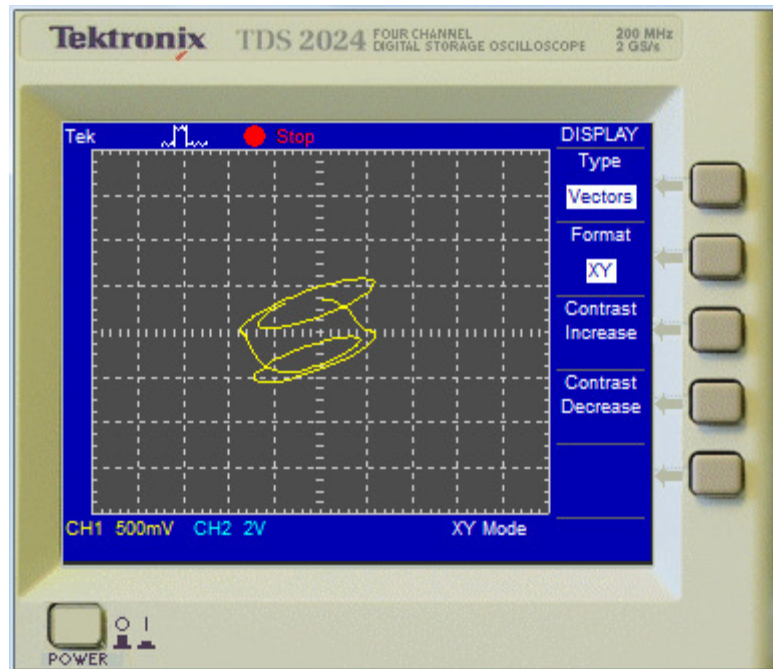

Fig. 5.4: Limit cycle with R6 equal to 1.2 kohm

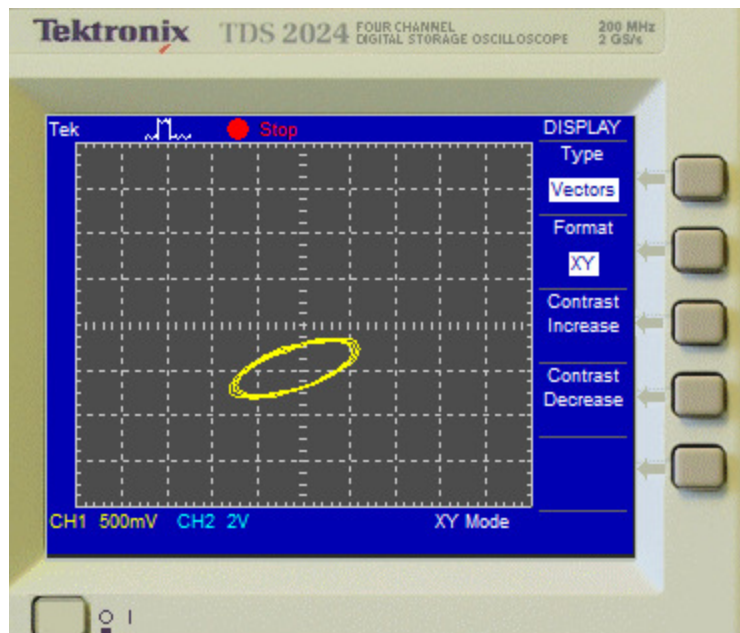**Fig.5.5: Double scroll chua's attractor with R6 equal to 1.3 kohm**

Fig. 5.6: Spiral chua's attractor with R6 equal to 1.6 kohm

5.5 V$_1$(t)-V$_2$(t) Characteristic :

Here yellow waveform represents the channel 1st voltage V$_{c1}$(voltage across C$_2$) w.r.t. time and blue waveform represents channel 2nd voltage V$_{c2}$(voltage across C$_3$) w.r.t. time. When the value of R6 is 80% of 2 kΩ.
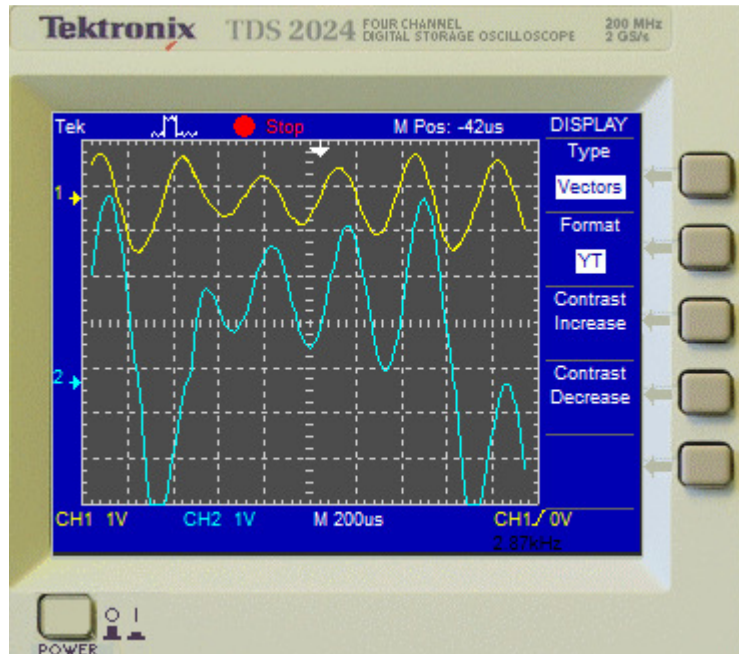

Fig.5.7: Y(t) format when realization of chua circuit as in fig.5.1

CHAPTER 6

SIMULATION OF INDUCTOR USING GIC

6.1 Inductance simulator using GIC:

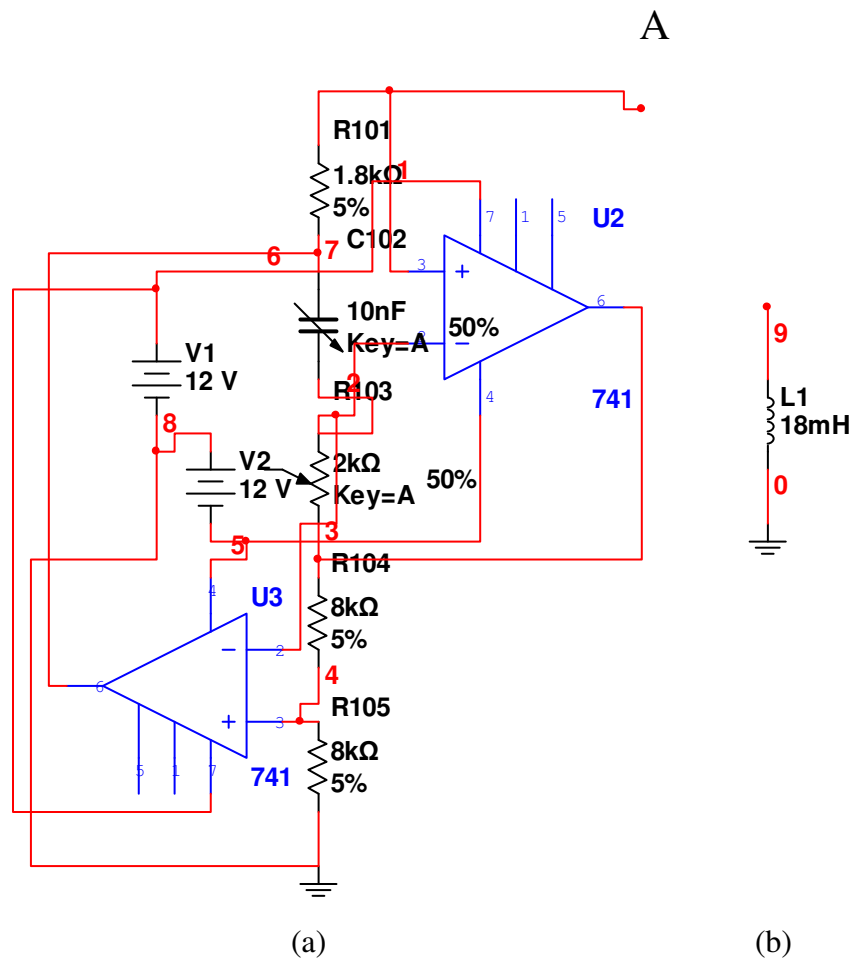(a)   (b)

Fig.6.1(a)Inductance simulated using GIC (b)Simple Inductor which is simulated in fig.6.1(a)

6.2 Generealised impedance convertor :

Impedance converters are active RC circuits designed to simulate frequency-dependent elements such as inductances for use in active filter synthesis. Among the various configurations, one that has gained prominence is the GENERALIZED IMPEDANCE CONVERTERS (GIC), which can be used not only to simulate inductances, but also to synthesize frequency-dependent resistances.
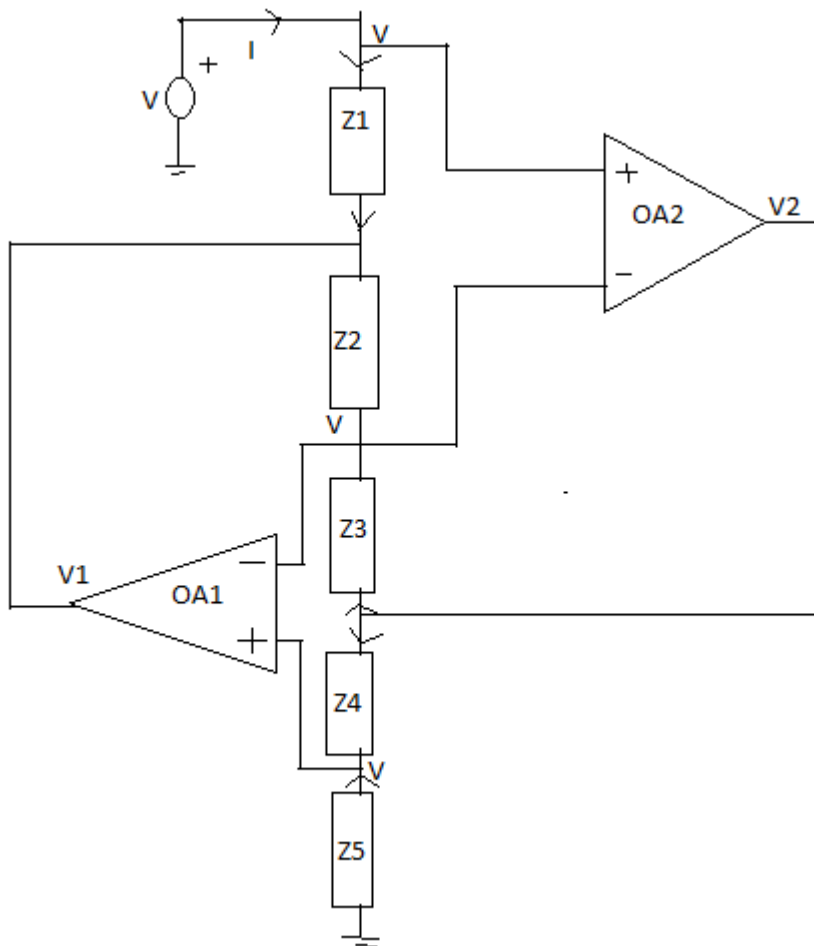

Fig. 6.2: Finding the equivalent impedance of a GIC toward ground

To find the equivalent resistances Z seen looking into node A, we apply a test voltage V as in fig 6.2, we find the resulting current I, and then let

$$Z = V/I.$$

Exploiting the fact that each op amp keeps $V_n = V_p$, we have labelled the voltages at the input nodes of both op amps as V. By ohm's law, we have

$$I = (V - V_1)/(Z_1)$$

Summing current at the node common to Z_2 and Z_3 and at the node common to Z_4 and Z_5 we obtain, respectively,

$$\frac{V_1 - V}{Z_2} + \frac{V_2 - V}{Z_3} = 0$$

$$\frac{V_2 - V}{Z_4} + \frac{0 - V}{Z_5} = 0$$

Eliminating V_1 and V_2, and solving for the ratio $Z = V/I$, we get

$$Z = \frac{Z_1 Z_3 Z_5}{Z_2 Z_4} \qquad\qquad\qquad 6.1.1$$

Depending on the type of the components we use for Z_1 through Z_5, we can configure the circuits for various impedances types.The most interesting and useful one as follows:

Alls Z_s are resistances, except Z_2 which is a capacitance. Letting $Z_2 = 1/j\omega C_{102}$ in eqn. 6.1.1 Then

$$Z = \frac{R_{101} R_{103} R_{105}}{(1/j\omega C_{102}) R_{104}} = j\omega L$$

$$L = \frac{R_{101} R_{103} R_{105} C_{102}}{R_{104}}$$

The above circuit indicates the simulation of a grounded inductance. If desired, this inductance can be varied by varying capacitance C_{102} and R_{103}.

A popular GIC application is the realization of inductorless filters starting from passive RLC filter prototypes. To this end we first design an RLC filter meeting the given specicications, then we replace its inductances with synthetic inductances realized with GICs.Note ,however,that this direct one to one replacement is applicable only if the inducatnces in the prototype are of the grounded type.

A classical example is offered by the band pass prototype as shown in below fig. This is a band pass filter because low-frequency signals are shunted by L, high frequency signals are shunted by C, and intermediate-frequency signals are passed because of resonance.Once the filter specifications are known, we first find a set of RLC values meeting the specification, then we replace the original inducatnce with a GIC inductor simulator to end up with a circuit containing only resistances and capacitances.The result is the dual-amplifier band pass.

6.3 Simulation for Vin-Vout characteristic of inductor :
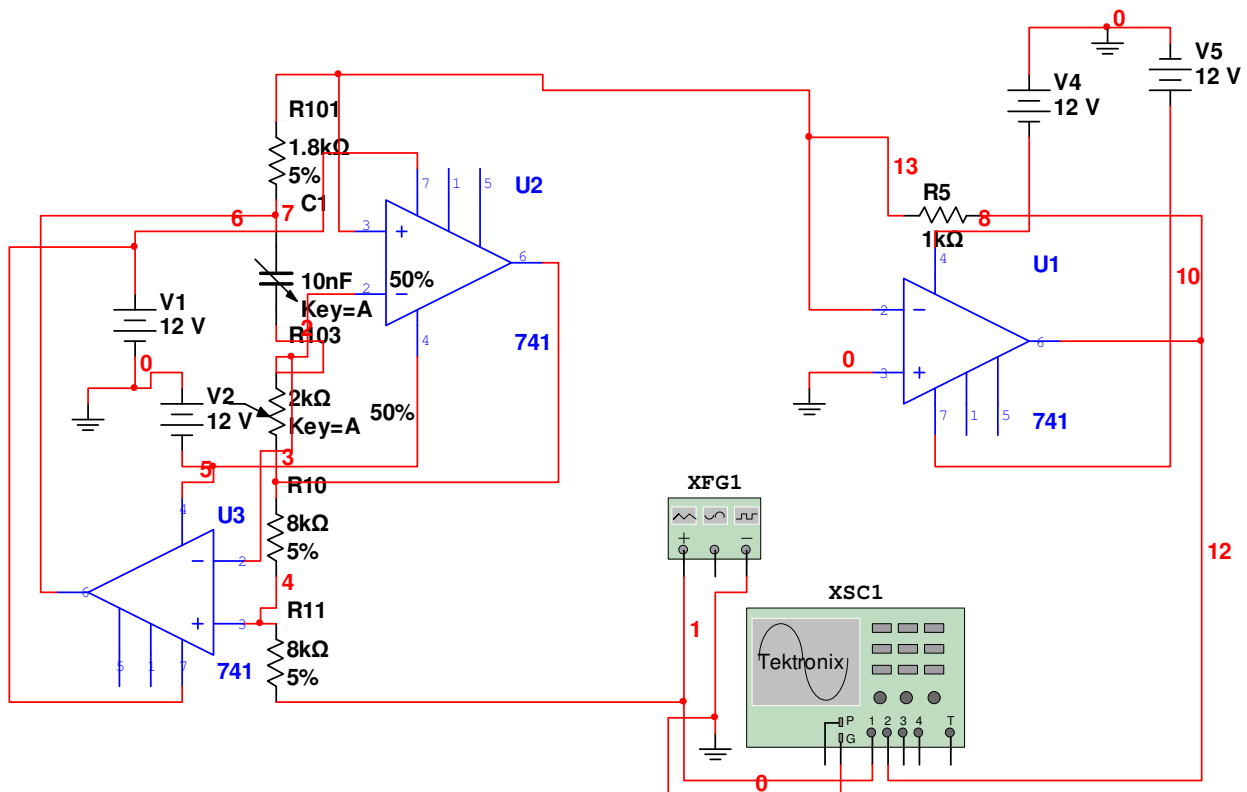
6.4 Vin-Vout characteristics:

Here the input voltage V_{in} is represented by yellow wave and output voltage V_{out} is represented by green wave in CRO. Hence its prove that the V_{out} is leading than V_{in} due to inductive property.
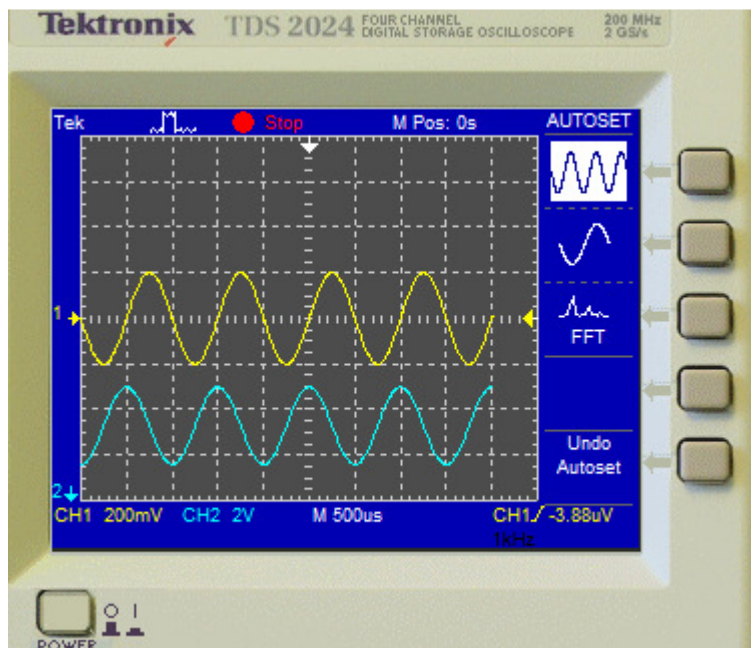

Fig.6.3: Vin-Vout characteristics of inductor simulated by GIC

6.5 Simulation and results of Realization Of Chua's circuit Using GIC:
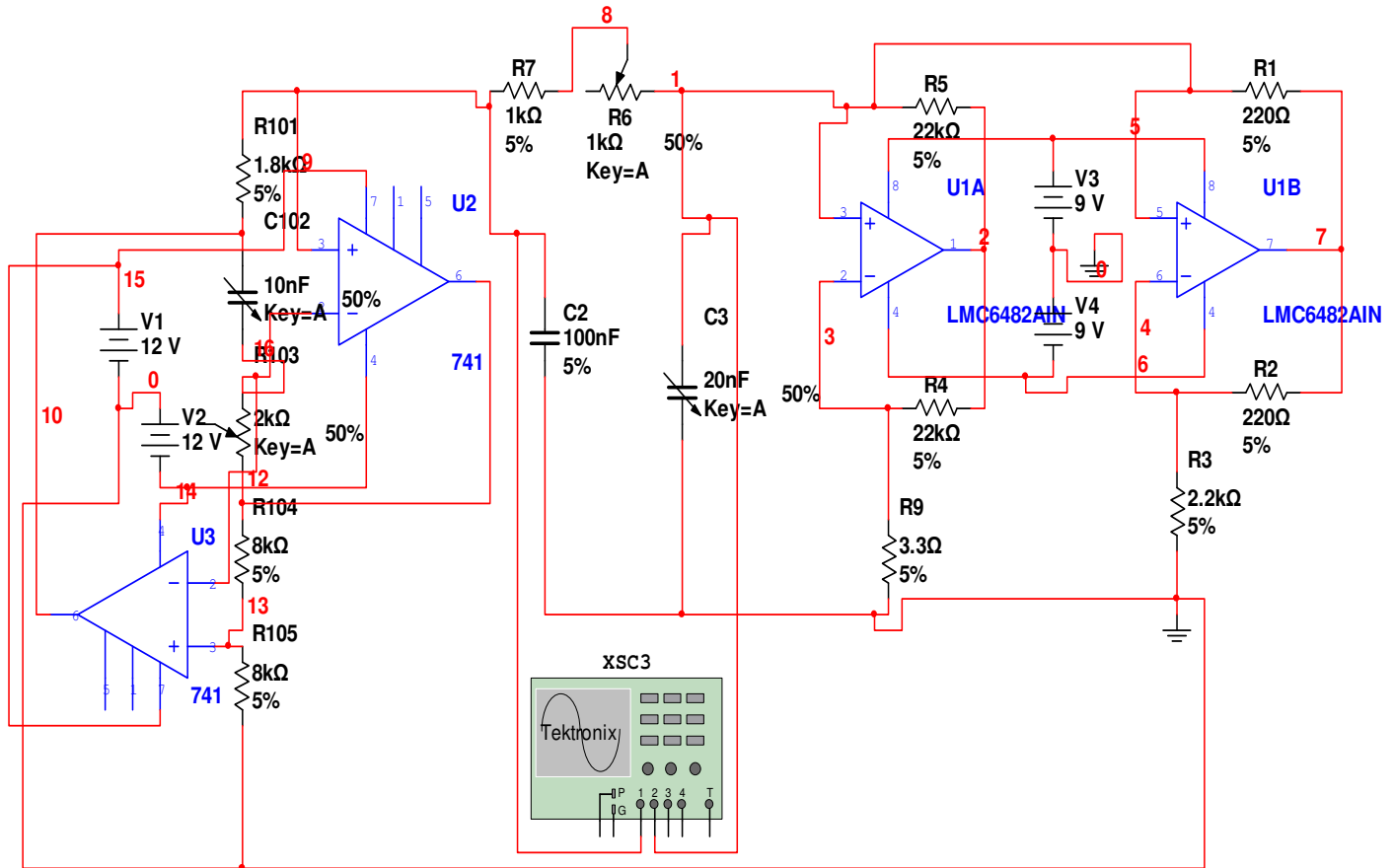
Here the inductor is replaced by GIC in which the value of resistor R$_{101}$ is 1.8 kΩ, C102 is a variable capacitor, R103 is also a variable resistor, R104 has 1.8 kΩ, and R105 has also 1.8kΩ. There are two IC's 741 used for making the GIC circuit.

When the value of capacitor C102 is varied from 5 nf to 9.5 nf then the limit cycle is obtained and after it chaos formed.

6.6 V1–V2 Characteristics:
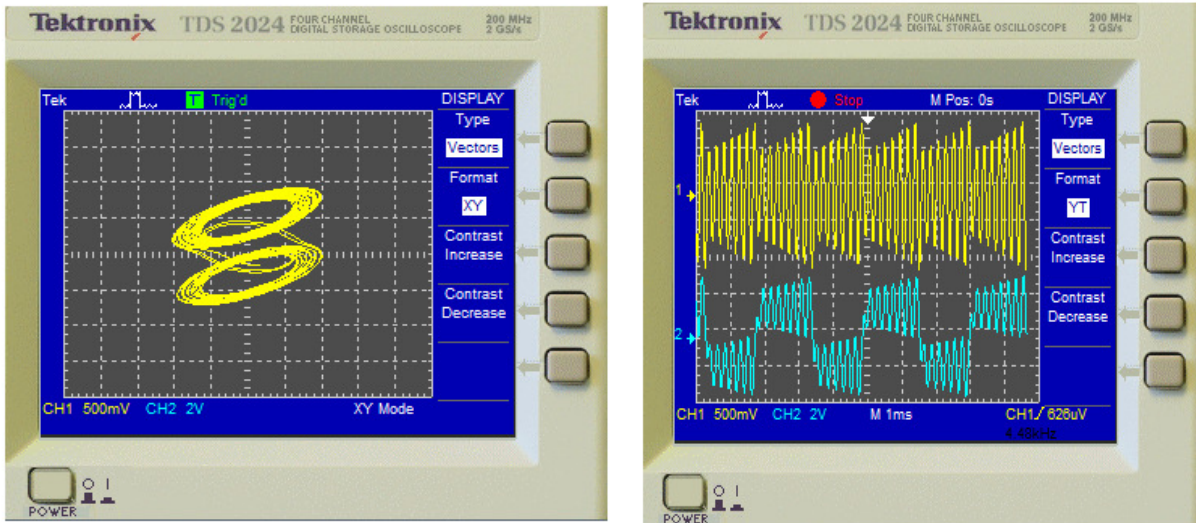
(a)   (b)

Fig.6.4 (a) Double scroll attractor with C102 equal to 2.5nf   (b).Y(t) format of realization of Chua's circuit as in fig.6.4(a)
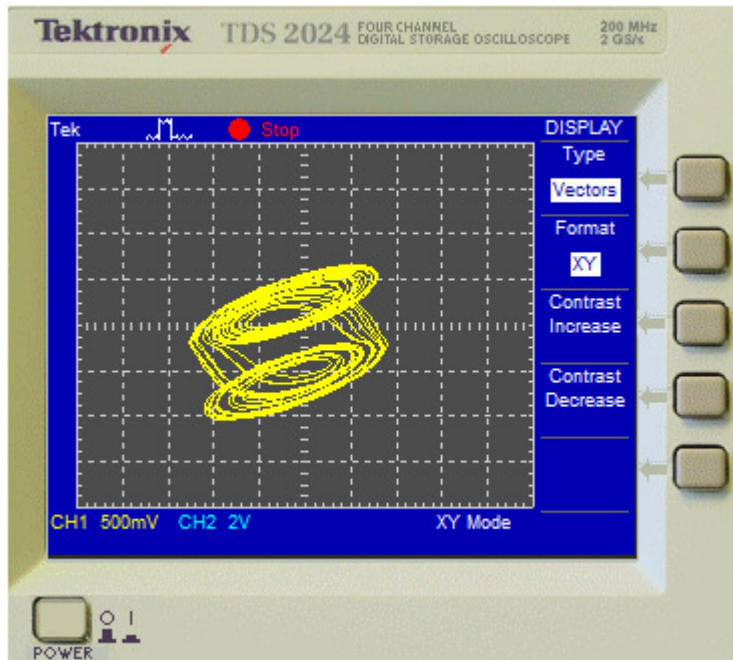
Fig.6.5:Double scroll chua's attractor with C102 equal to 3.5nf
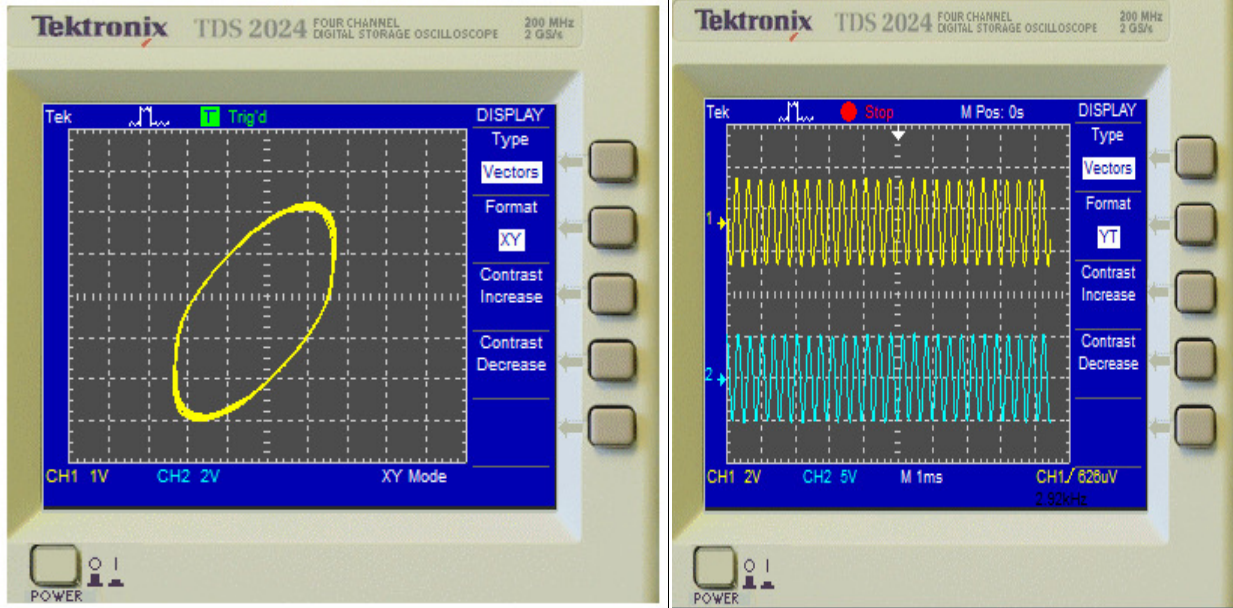
(a)   (b)

Fig.6.5: (a)Spiral chua's attractor with C102 equal to 4.5nf (b)Y(t) format format of realization of Chua's circuit as in fig.6.5(a)
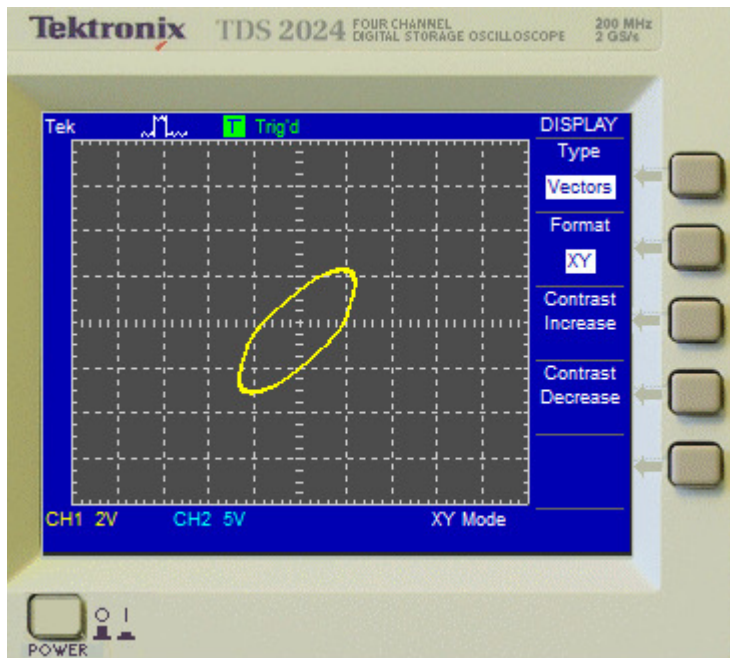
Fig.6.6: Spiral chua's attractor with C102 equal to 6nf
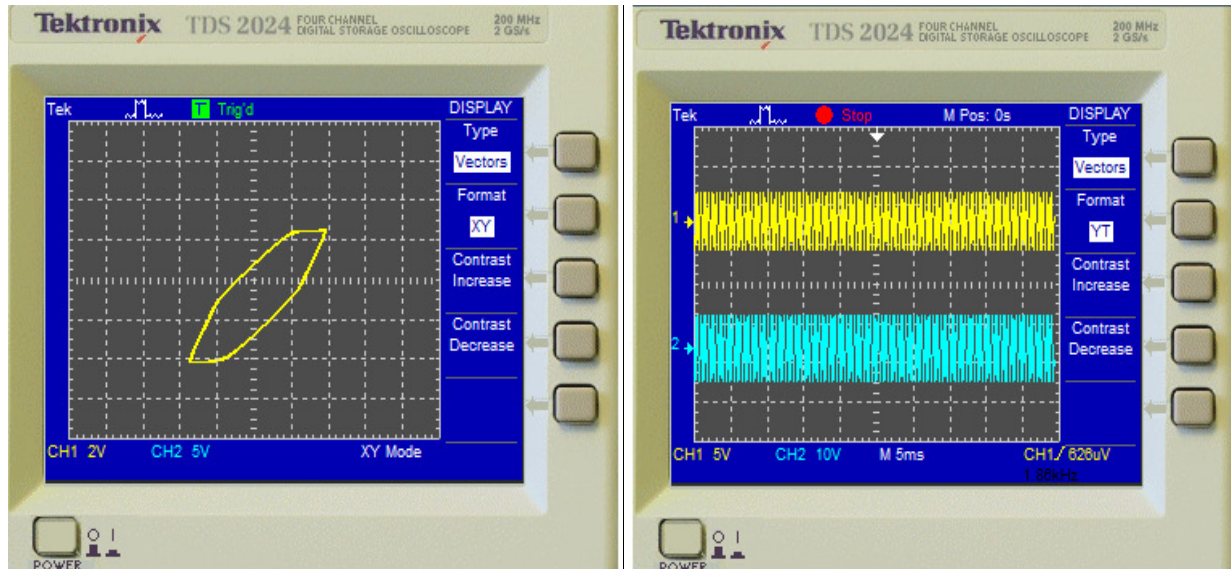
(a)   (b)

Fig.6.7: (a)Limit cycle with C102 equal to 9nf (b)Y(t) format format of realization of Chua's circuit as in fig.6.7(a)

CHAPTER 7

SIMULATION OF INDUCTOR USING OTA

7.1 Inductor simulator using OTA:

(a)   (b
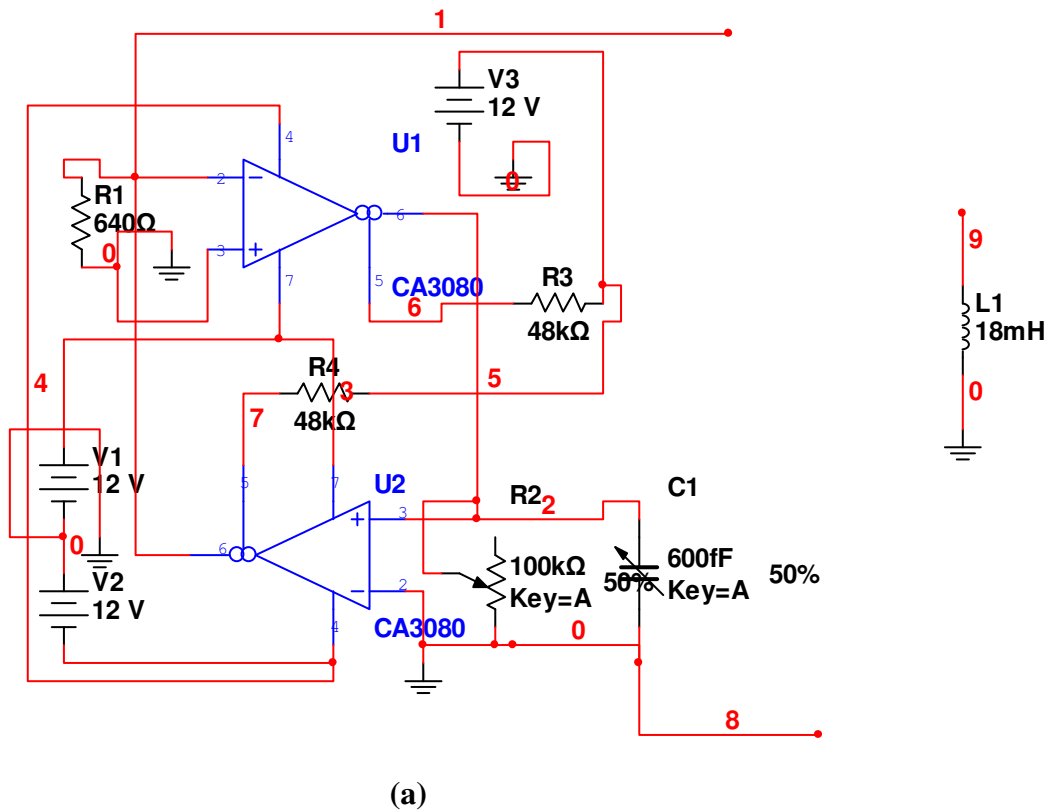
Fig.7.1(a) Inductor simulated by OTA (b)Real inductor which is simulated in fig.7.1(a)

7.2 Idealized gyrator–based inductances:

An ideal gyrator is a linear two port network that neither stores nor dissipates energy. Given input and output voltages, V_1 and V_2, respectively, and corresponding input and output currents, I_1 and I_2, the positive senses of which are delineated in below Fig. the terminal volt-ampere characteristics of an ideal gyrator are given by

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} 0 & g \\ -g & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

7.2.1

(a)   (b)
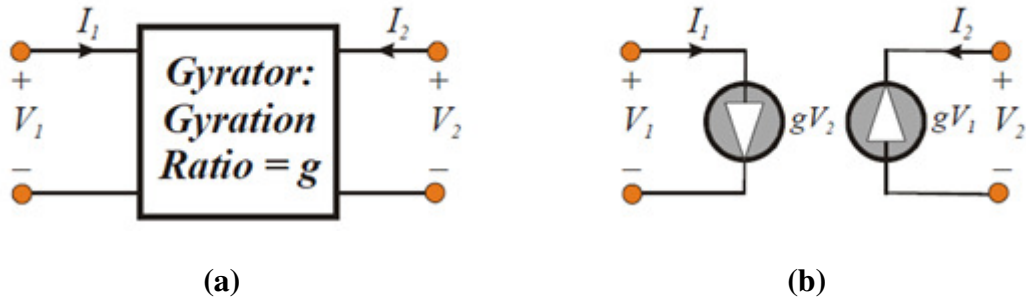
Fig. 7.2: (a) Symbolic Representation Of An Ideal Gyrator.(b) The Two Port Equivalent Circuit Of The Gyrator

Where g is a designable transconductance parameter known as the gyration ratio of the active network. In above equation it suggests, as is diagrammed in Fig. (7.2b), that only two voltages controlled current sources is required in the corresponding two port equivalent circuit. If the gyrator in Fig. (7.2a) is terminated at its output port in a capacitance, C, as showing Fig. (7.2a), the electrical model in Fig. (7.2b) produces driving point input impedance, $Zi(s)$, given by

$$Z_i(s) = \frac{V_1(s)}{I_1(s)} = \frac{sC}{g^2}$$

7.2.2

(a)   (b)
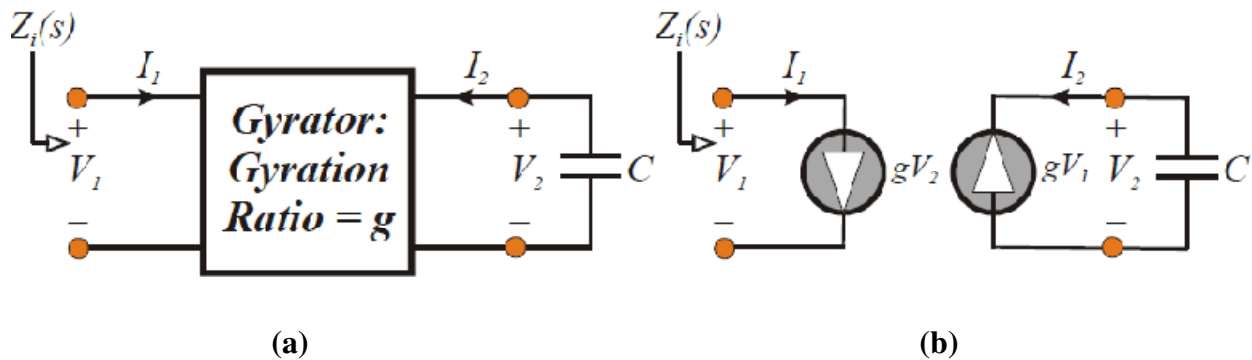
Fig.7.3. (a). Ideal Gyrator Terminated At Its Output Port In A Capacitance, C. (b). The Two Port Equivalent Circuit of the Terminated Gyrator in (a).

Clearly, the input impedance predicted by by below is inductive, where the effective inductance, *L*, is observed to be

$$L = \frac{C}{g2} \qquad\qquad 7.2.3$$

It follows that the ideal gyrator is capable of transforming an ideal capacitance incident with its output port to an input port inductance whose value is inversely proportional to square of the network gyration ratio. Because the gyrator modelled in Fig. (7.3) is ideal and therefore lossless, the quality factor of the synthesized inductor is infinitely large.

Operational transconductance amplifiers (OTAs), whose electrical characteristics emulate voltage controlled current sources, provide a logical foundation for the network realization of a gyrator. Given the electrical symbol and model of the OTA shown in Fig. (7.4a), a gyrator–based inductor assumes the topological form offered in Fig. (3b). Observe in the latter diagram that the input and output currents, I_1 and I_2, subscribe to the metric in (7.2.1), whence the effective inductance given by (7.2.3) is forged at the input port of the network at hand. A laudable attributes of the OTA–based approach toward realizing active inductances is that the individual OTA transconductances, *g*, can be adjusted through the application of externally applied bias voltage or current (not shown in the subject diagram). This flexibility effectively allows for electronically tuneable active inductances.
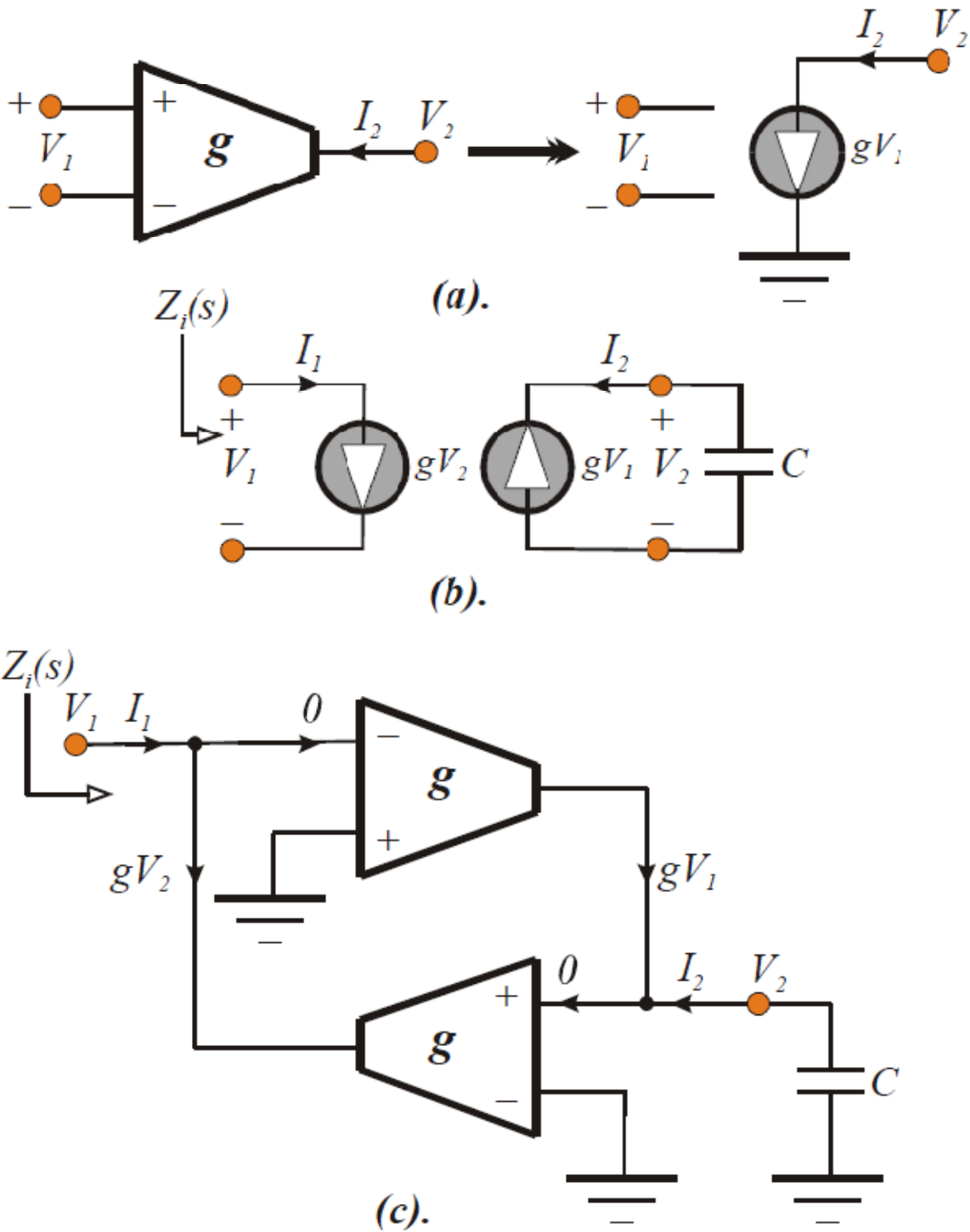
Fig.7.4. (a). Electrical Model of an Ideal Operational Transconductor (OTA). (b). the Electrical Equivalent Circuit of A Capacitive Terminated Ideal Gyrator (c). The Tran conductor Realization of the Capacitive Terminated Ideal Gyrator.

7.3 Practical Gyrator Based Inductance:

Unfortunately, the linearized model of an OTA is not the lossless and memory less structure set forth in Fig. (7.4a). In particular, an OTA has an input resistance, Ri, which in MOS technology circuits can be extremely large but in bipolar circuits is only moderately large (tens of thousands of ohms). An output resistance, Ro, in the range of at least the high tens to several hundreds of thousands of ohms also prevails. Due account must also be made of shunt input capacitance, Ci, and shunt output capacitance, Co. In submicron MOS technology circuits, Ci derives largely from gate-source and gate-source overlap capacitances and has a value typically in the range of tens to the low hundreds of femptofarads. In bipolar OTA structures, Ci derives from the depletion and diffusion components of base-emitter junction capacitance and from Miller multiplication of the base-collector junction transition capacitance.

The output capacitance, Co, which is usually dominant in common source MOS transistor circuit architectures, is determined primarily by drain-bulk capacitance and is generally of the order of the tens to a few hundreds of femptofarads. In bipolar circuits, Co is the collector-substrate capacitance and depending on the extent of Miller multiplication of the base–collector junction capacitance, it may not be the dominant energy storage element. The value of Co in either device technology can also be impacted significantly by requisite common mode bias compensation circuitry.

Finally, C_f, represents the net feedback capacitance between the input and output ports of OTA. Because an OTA is usually a multistage topology, C_f is generally of the order of at most a few femptofarads. Nevertheless, it is a troublesome energy storage element because at best, it establishes an OTA right half plane zero serving to degrade phase margin. At worst, it can incur significant under damping or even outright instability in gyrator and other feedback networks.

The upshot of the foregoing disclosures is the OTA macro model abstracted in Fig. (7.5).
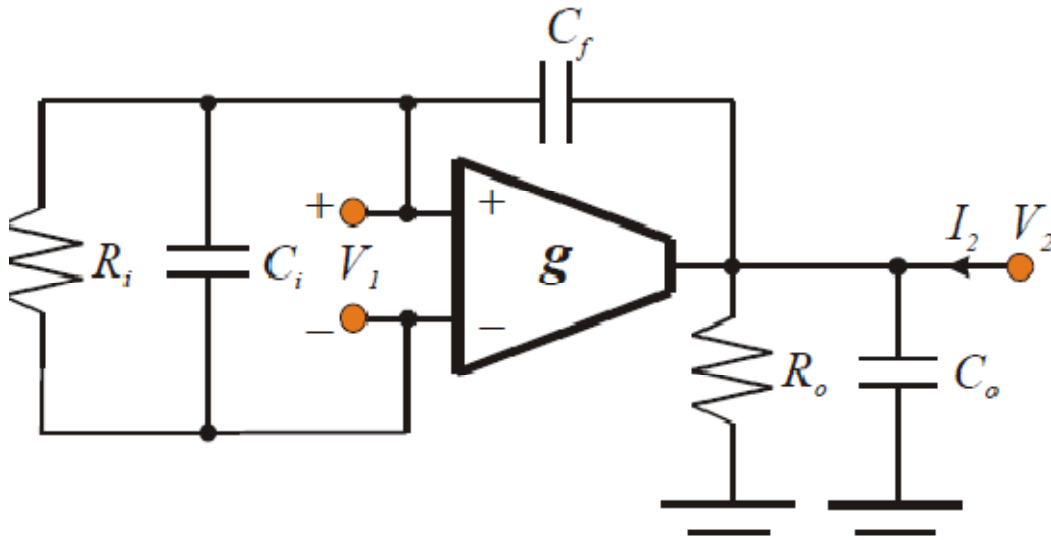
Fig. (7.5). The High Frequency Macro model of the Operational Transconductor Depicted in Fig. (7.4a).

7.4 Analysis of the ota-based gyrator active inductance :

The OTA macromodel in Fig. (7.5) gives rise to the circuit in Fig. (7.6a) as a first order approximation of the small signal high frequency electrical characteristics for the active inductor in Fig. (7.4b). In the interest of generality, the transconductances of the individual OTAs are not taken as identical. Recalling the OTA macromodel of Fig. (7.4a), the circuit in Fig. (7.6a) is electrically equivalent to Fig. (7.6b). in the latter network, the indicated capacitances are given by

$$\begin{cases} C_1 = C_{i1} + C_{02} \\ C_0 = C_{i2} + C_{01} \\ C_F = C_{f1} + C_{f2} \end{cases}$$
7.4.1

While the model resistances are,

$$R_I = R_{i1} \| R_{02}$$
7.4.2

$$R_0 = R_{i2} \| R_{01}$$
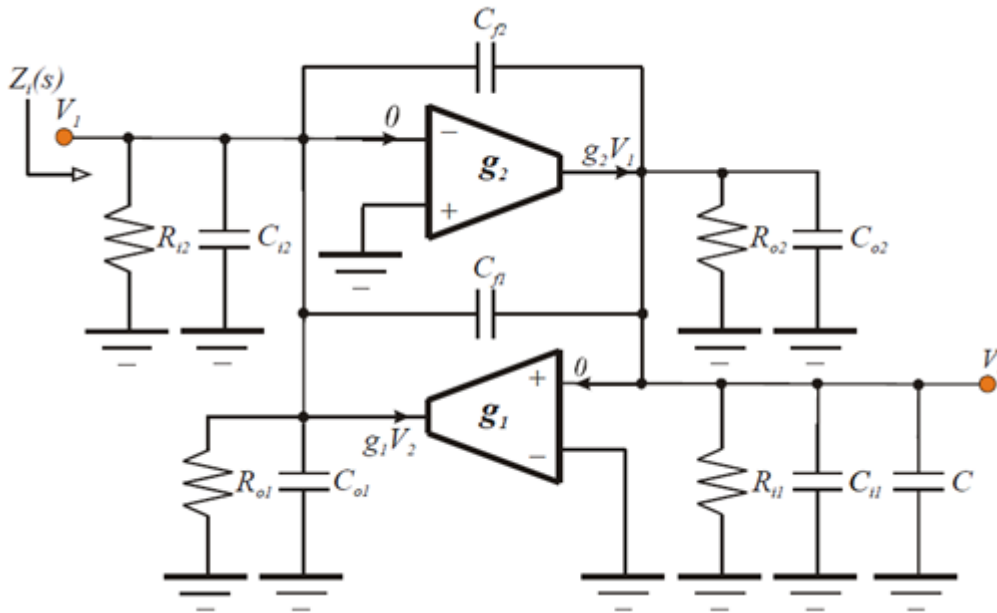
(a)
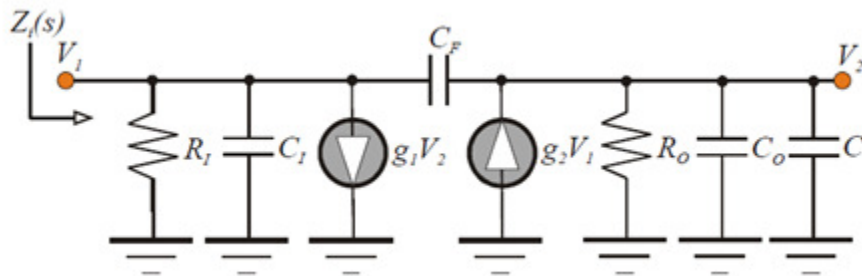
(b)

Fig. 7.6: (a). The Gyrator–Based Active Inductor With Resistive And Capacitive Input Port, Output Port, And Feedback Elements Incorporated. (b). the Linearized High Frequency Two Port Equivalent Circuit Of the Network in (a).

Note that if the operational transconductors in Fig. (7.6a) are identical and no additional circuit elements are appended to either the input or the output ports of each transconductor, $C_I = C_O$, and $R_I = R_O$.

An analysis of the model at hand produces the driving point input impedance function,

$$Z_i(s) = \frac{R_e + sL_e}{1 + \left(\frac{2\xi}{\omega_n}\right)s + \left(\frac{s}{\omega_n}\right)^2}$$

$$7.4.3$$

Where

$$R_e = \frac{R_1}{1 + g_1 g_2 R_1 R_0} \approx \frac{1}{g_1 g_2 R_0}$$

$$7.4.4$$

is the low frequency resistive component of the input impedance, and

$$L_e = \frac{R_1 R_0 (C_0 + C_F + C)}{1 + g_1 g_2 R_1 R_0} \approx \frac{C_0 + C_F + C}{g_1 g_2}$$

$$7.4.5$$

It is the low frequency value of the effective input inductance produced by the gyrator. The approximations in the foregoing two relationships reflect the presumption that the resistances, R_I, and/or R_O, are sufficiently large to ensure $g_1 g_2 R_I R_O \gg 1$. Since R_I and R_O very large and C_O and C_F very small collapse the network in Fig. (7.6a) to its simplified counterpart in Fig. (7.4b), it is not surprising that (7.4.5) corroborates with (7.2.3) for the case of $g_1 = g_2$. Unfortunately, the electrical synergy between the actual and simplified circuits degrades with increasing signal frequency since (7.4.3) indicates undamped resonance at a frequency, ω_n, which can be shown to be

$$\omega_n = \sqrt{\frac{1}{L_e\left[C_1 + \frac{C_F(C_0 + C)}{C_0 + C_F + C}\right]}}$$

$$7.4.6$$

The last term in the bracketed expression in the denominator on the right hand side of (7.4.6) is smaller than C_F, which itself is a small capacitance. Accordingly, (7.4.6) eqn. suggests that the inductance produced at the input port of the circuit in Fig. (7.6a) effectively resonates with the

net shunt input capacitance, C_I. The damping factor, ζ, (which is the inverse of twice the quality factor, Q, of the circuit in (7.4.3) derives from

$$\frac{2\xi}{\omega_n L_e} = \frac{1}{Q\omega_n L_e} = \frac{1}{R_1} + \frac{C_1 + C_F}{R_0(C_0 + C_F + C)} + \frac{(g_2 - g_1)C_F}{C_0 + C_F + C}$$

7.4.7

Observe that $g_2 \; g_1$ and a sufficiently large feedback capacitance, C_F result in a negative damping factor, which is tantamount to network instability. Fortunately, $g_2 \geq g_1$ precludes right half plane poles and therefore ensures asymptotically stable circuit responses. To the extent that g_2 is approximately equal to g_1 and R_O is very large, (7.4.7) eqn. delivers an approximate damping factor of

$$\xi \approx \frac{\omega_n L_e}{2R_1}$$

7.4.8

As expected, a progressively smaller input resistance, R_I, which appears directly in shunt with the resonant circuit comprised of the generated inductance, Le, and the shunt input capacitance, C_I, serves to increase the damping factor, thereby circumventing potential oscillation problems. In addition to bracketing the relative stability of the system undergoing investigation, the damping factor in (7.4.7) and (7.4.8) sets the degree to which the frequency dependence of the effective port resistance and port inductance are rendered nominally constant over the signal passband of interest. To clarify this contention, write (7.4.3) in this form,

$$Z_i(s) = \frac{R_e + sL_e}{1 + \left(\frac{2\xi}{\omega_n}\right)s + \left(\frac{s}{\omega_n}\right)^2} = (R_e + sL_e)F(s)$$

7.4.9

With *F(s)* understood to be the second order lowpass function,

$$F(s) = \frac{1}{1 + \left(\frac{2\xi}{\omega_n}\right)s + \left(\frac{s}{\omega_n}\right)^2}$$

7.4.10

Obviously, frequency invariant resistance and frequency invariant inductance require *F(s) = 1*,

Which is satisfied only for low signal frequencies and approximated only for appropriate damping factors and suitably large undamped resonant frequencies? Indeed, ζ larger than the inverse of root two precludes $|F(j\omega)| > 1$, but constrains the *3–dB* bandwidth of $|F(j\omega)|$ to a frequency smaller than ω_n. On the other hand, ζ smaller than the inverse of root two increases function bandwidth at the price of incurring response peaking in excess of one within the passband.

The optimum designable constraint appears to be ζ equal to the inverse of root two that imposes a maximally flat constraint on $|F(j\omega)|$; that is, $|F(j\omega)|$ displays no maxima above unity and is constant to within three decibels of unity for all signal frequencies in the closed interval,

$$0 < \omega < \omega_n.$$

It follows the eqn.(7.4.8) that

$$R_1 \approx \frac{\omega_n L_e}{\sqrt{2}} \qquad\qquad\qquad 7.4.11$$

is a reasonable constraint for ensuring nominally constant resistance and inductance over the widest possible passband.

7.5 Design constraints and guidelines:

In order to formulate guidelines appropriate to a meaningful design of the gyrator–based active inductor, it is useful to introduce the frequency normalization, *y*, such that

$$y \triangleq \frac{\omega}{\omega_n} = \frac{f}{f_n} \qquad\qquad\qquad 7.5.1$$

Under steady state sinusoidal excitation conditions, impedance therefore becomes

$$Z_i(jy) = Re[Z_i(jy) + jIm[Z_i(jy)],$$

7.5.2

Where the equation of ζ becomes,

$$R_e[Z_i(jy) = \frac{(1-y^2)R_e + 2\xi y^2 \omega_n L_e}{(1-y^2)^2 + (2\xi y)^2} \approx \frac{(1-y^2)Re + (2\xi y)^2 R_1}{(1-y^2)^2 + (2\xi y)^2}$$

7.5.3

And

$$I_m[Z_i(jy) = \frac{y[(1-y^2)\omega_n L_e - 2\xi R_e]}{(1-y^2)^2 + (2\xi y)^2} \approx \frac{\omega_n L_e y(1 - \frac{R_e}{R_1} - y^2)}{(1-y^2)^2 + (2\xi y)^2}$$

7.5.4

The last expression verifies that the input impedance is not inductive over all signal frequencies since a normalized crossover frequency, say y_{co}, exists for which $Im[Zi(j\omega)]<0$ for $y \geq y_{co}$. This normalized crossover frequency is

$$y_{C0} = \frac{f_{C0}}{f_n} = \sqrt{1 - \frac{R_e}{R_1}} \approx 1$$

7.5.5

Where the approximation reflects the fact from (7.4.4) that, $Re << R_I$. In short, the electrical nature of the drive point input impedance changes from inductive to capacitive at nominally the undamped resonant frequency of the gyrator circuit. Since the objective at hand is the realization of circuit inductance it follows that the utility of the structure proposed in Fig. (7.6a) is limited to signal frequencies that are smaller than the undamped resonance predicted by 7.4.6. On a positive note, above eqn. 7.4.11 confirms that unconditional circuit stability, in the sense of a

positive real input impedance, is virtually assured as long as the damping factor, ζ, subscribes to the inequality,

$$\xi > \sqrt{\frac{R_e}{4R_1}}$$
                                                                                            7.5.6

This inequality is relatively easy to satisfy in view of the fact that $Re << R_I$ and ζ is chosen to be approximately *0.707*.

Using 7.5.3 and 7.5.4, the quality factor, $Q(y)$, of the actively synthesized inductor is given approx. by,

$$Q(y) \approx \frac{\omega_n L_e y (1 - \frac{R_e}{R_1} - y^2)}{(1-y^2)Re + (2\xi y)^2 R_1}$$
                                                                                            7.5.7

Over the normalized frequency range, $y < 1$, where the input impedance is inductive, (7.5.7) can be approximated as,

$$Q(y) \approx \frac{\omega_n L_e y}{R_e (2\xi y)^2 R_1}$$
                                                                                            7.5.8

Which displays a maximum at,

$$y_m = \frac{f_m}{f_n} \frac{\sqrt{R_e R_I}}{\omega_n L_e}$$
                                                                                            7.5.9

Recalling (7.5.3), (7.5.9) implies that the frequency at which the inductor quality factor is maximized is

$$f_m \approx \frac{1}{2\Pi L_e} \sqrt{\frac{R_1}{g_1 g_2 R_0}} \qquad\qquad 7.5.10$$

The actual value of the maximum quality factor, *Qm*, derives from substituting 7.5.9 into 7.5.8 :

$$Q_m \triangle Q(y_m) \approx \frac{1}{2} \sqrt{g_1 g_2 R_1 R_0} \qquad\qquad 7.5.11$$

Since resistance R_I is selected to prescribe a damping factor commensurate with maximally flat inductance over the frequency passband, it follows that the shunt output resistance, R_O, determines the maximum Q of the synthesized inductor. Note therefore that the largest possible Value of maximum Q is essentially dictated by the ability to realize an operational transconductor characterized by very large shunt output resistance. Equivalently, the value of Q_m is limited by the degree to which the output port of a transconductor emulates an ideal current source.

The ratio, *fm/Qm*, is a useful design figure of merit for it effectively stipulates the requisite shunt output resistance corresponding to a desired inductance value and given operational transconductor parameters. This ratio also complements the solution to the problem of determining the engineering practicality of realizing the desired inductance specifications.
 Note that

$$\frac{f_m}{Q_m} \approx \frac{1}{\Pi L_e g_1 g_2 R_0} \qquad\qquad 7.5.12$$

Which is independent of the shunt input resistance, R_I. Consider, for example, that the operational transconductors in Fig. (7.6a) have $g_1 = g_2 = 2$ *millimho* and that an inductance, *Le*, of *15 nh* is desired. If this inductance realization is to deliver a peak quality factor *(Qm)* of *100*

at frequency *(fm)* of *400 MHz*, (7.5.12) delivers a requisite shunt output resistance, R_O, of about *1.3 meg–ohms*. Such an output resistance is unrealistically large within the constraints imposed by low power transconductor design in state of the art deep submicron CMOS technology.

However, it may be attainable in silicon–germanium heterostructure bipolar junction transistor technology. A more reasonable resistance value is R_O = *100 kilo–ohms*. Then for *Le= 15nH* and $g_1 = g_2$ = *2 mhos, fm/Q_m = 53.05 MHz* For this ratio, Q_m = *15*, which is a quality factor considerably larger than that afforded by an on chip spiral. It follows that *fm = 796MHz* is achievable, provided *fm < fn*. With Q_m = *15* and R_O = *100 kohms,* (7.5.10) yields R_I = *2.25kilo ohms* which requires that the input port of the gyrator–based active inductor circuit be shunted by an appropriate resistance. Unfortunately, it is unlikely that this value of R_I guarantees maximal inductance flatness over the circuit passband. To this end, the damping factor in (7.4.8) corresponding to the required net effective shunt input resistance must be checked to see if design compromises are mandated.

7.6 Vin-Vout Characteristic of inductor using OTA :
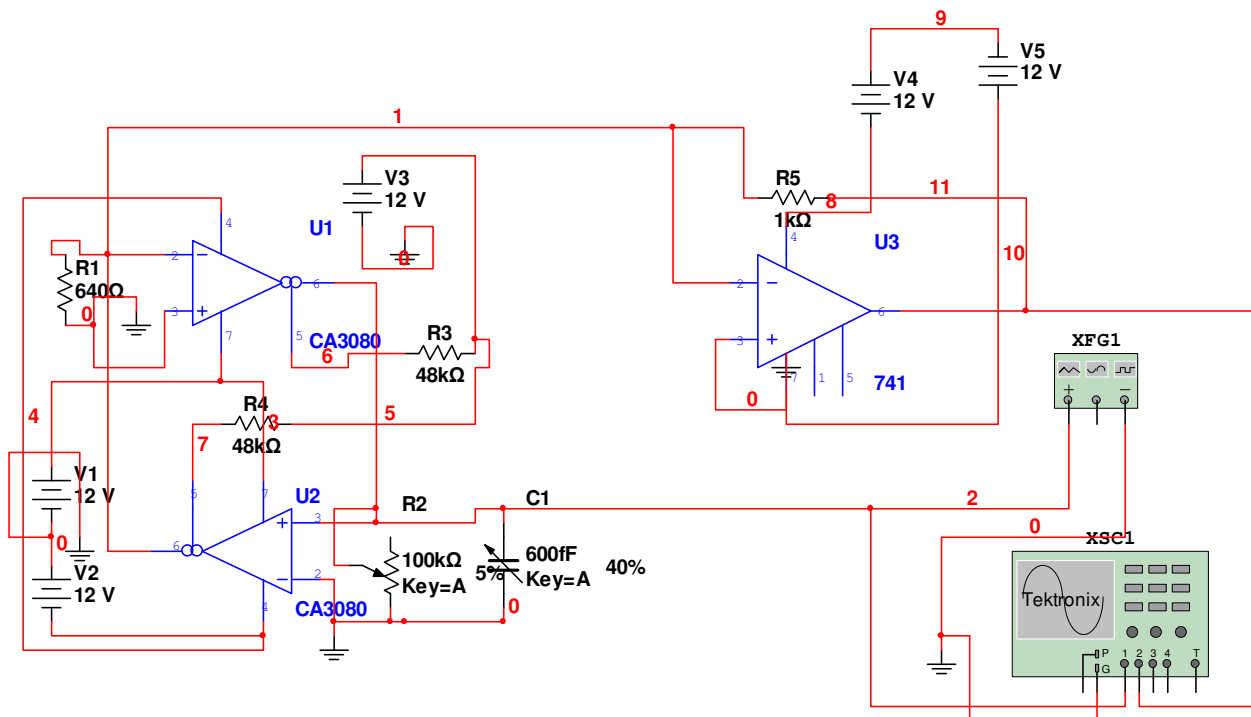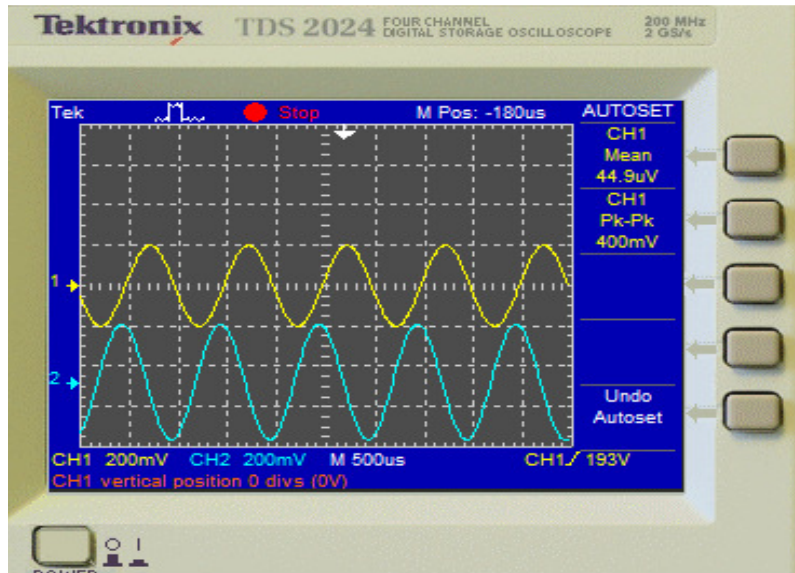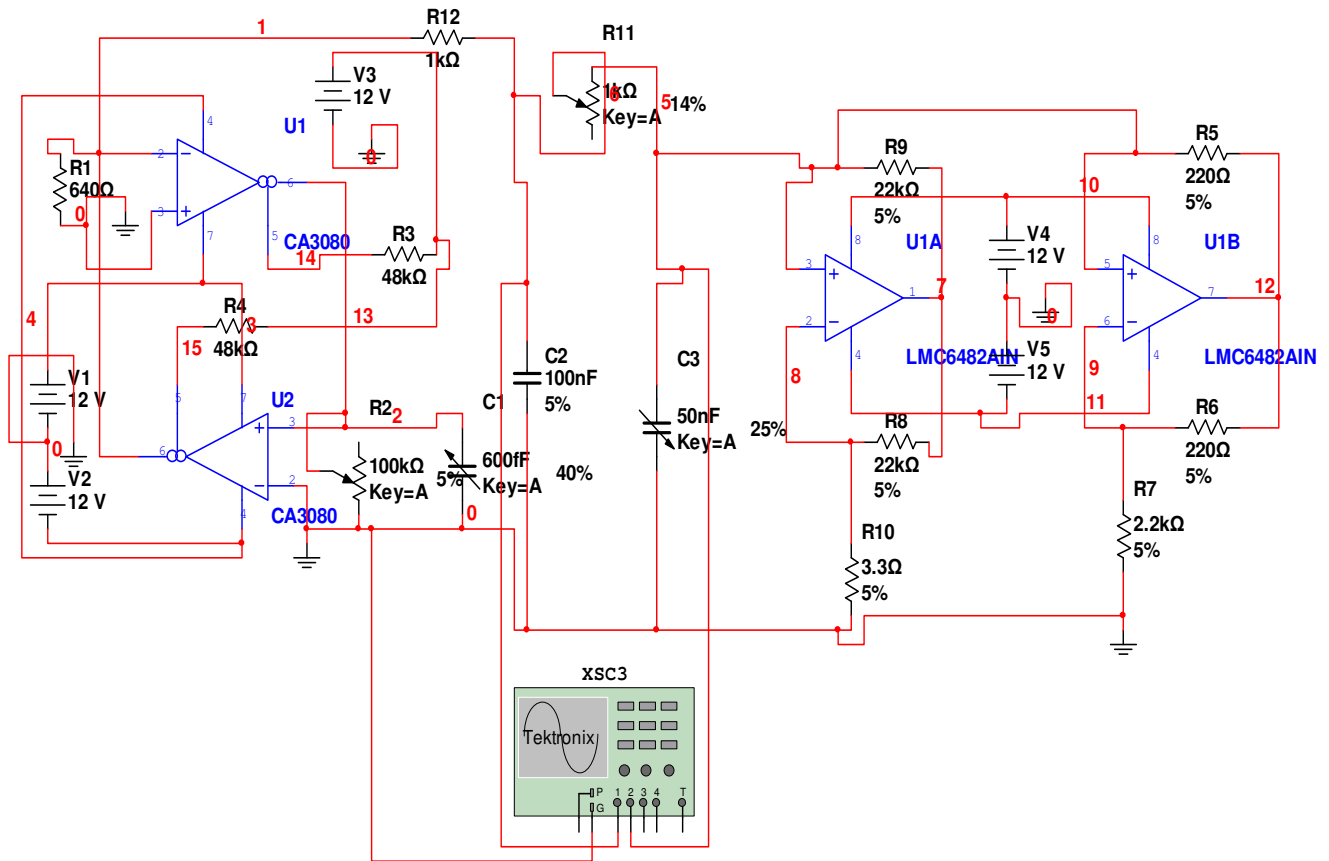
7.7 Vin–Vout Characteristics :

Fig.7.7: Vin–Vout Characteristics of inductor simulated by OTA

Here the input voltage v_{in} is represented by upper yellow wave and output voltage v_{out} is represented by below green wave in CRO.

Hence its prove that the v_{out} is leading than v_{in} due to inductive property.

7.8 Simulation and results of realization of Chua's circuit using OTA :

In this circuit inductor is replaced by OTA based gyrator circuit where CA 3080 OTA is used in the simulation of inductor two OTA have been used CA 3080 U1 and CA 3080 U2.

One input resistance R1 is used of 640 ohm that is connected to inverting terminal of U1 OTA and other is grounded. Another resistor R2 of 100 kΩ which is fix at 5 per. of its value and one capacitor C1 of 600 fF which is stable at 40 per. Of its value are connected in parallel and their one terminal connect to non inverting terminal of U2 OTA and another to ground.

Now by fixing the resistor R11 which has a value of 1 kΩ (with 1per. of tolerance) at 14 per. of its value and by varying the capacitor C3 which has a value of 50 nF (with 1per. of tolerance) at 30 per. of its value then we get a spiral Chua's attractor, capacitor C3 at 25 per. of its value then we get chaos and when we vary upto the 11% of the value of C3 then we find limit cycle.

7.9 V1 –V2 Characteristics :

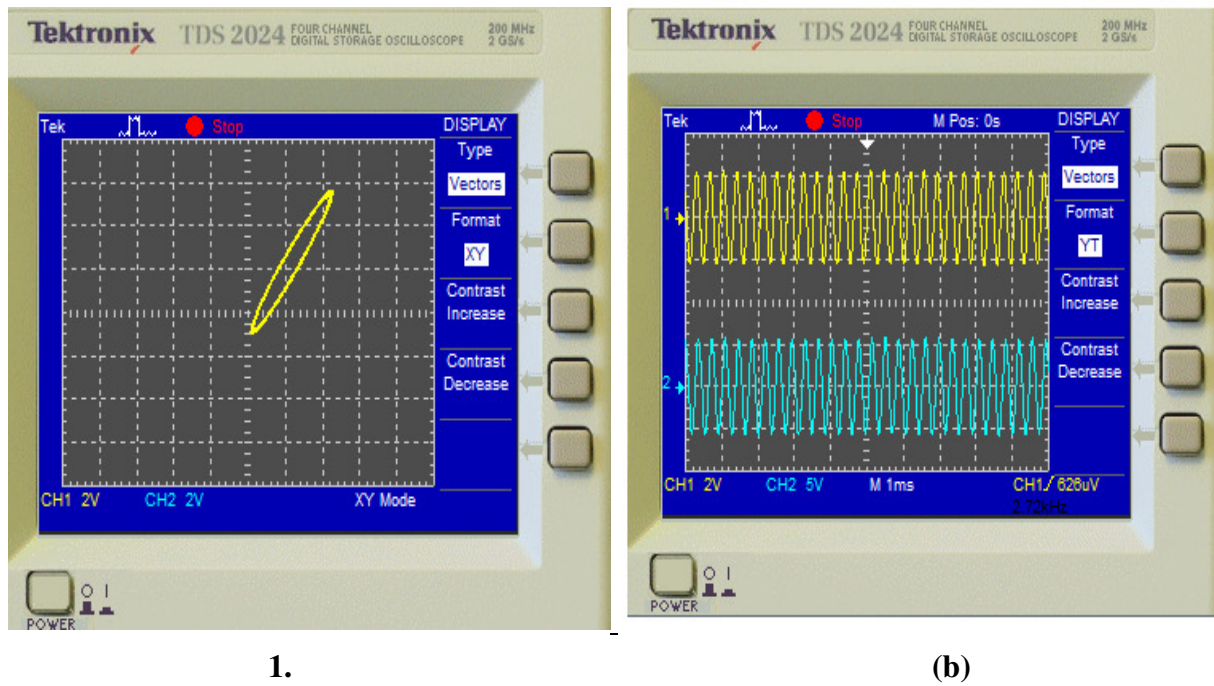1.   **(b)**

Fig.7.8 (a) Spiral Chua's attractor with C3 equal to 15 nf (b) Y(t) format of realization of Chua's circuit as in fig.7.8 (a)
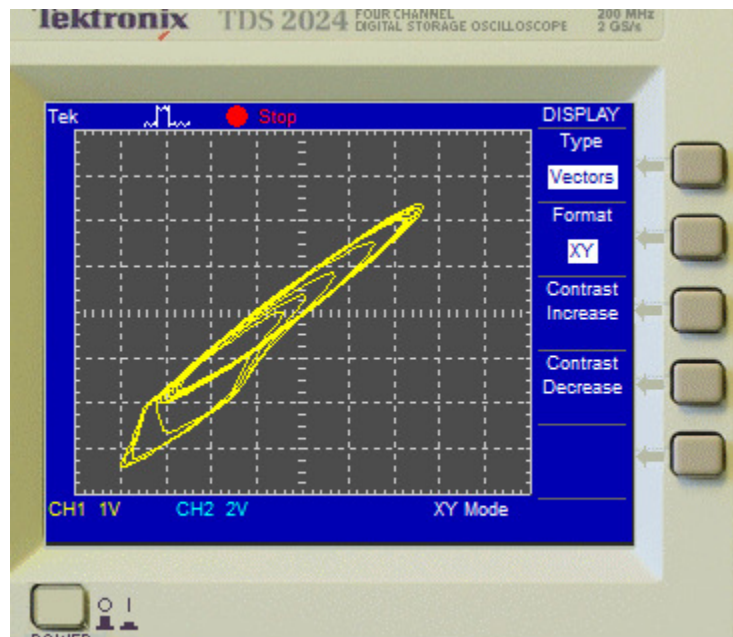

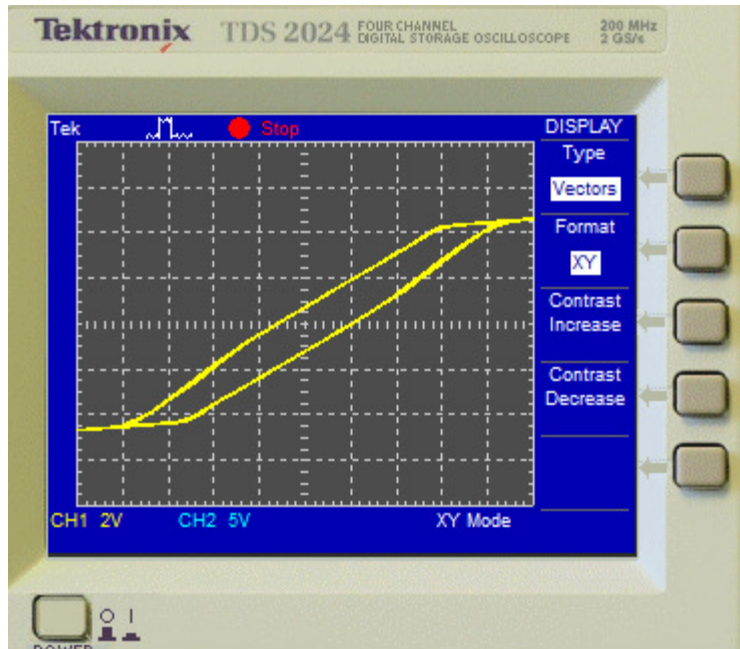**Fig.7.9: Double scroll Chua's attractor with C3 equal to 12.5 nf**

Fig.7.10: Limit cycle with C3 equal to 5.5 nf

CHAPTER 8

CONCLUSION AND FURTHER SCOPE

There are a lot of conclusions that can be drawn. It is shown that the output signals of V1 and V2 are different when the adjustable resistor is changed from one thousand to two ohm and turned round. There is also a difference in the quantity of stable points. When the resistor is changed from two thousand ohm downwards to one thousand ohm there are more stable points.

Chua's circuit is build from different components. Each component has a certain tolerance. But because it is a chaotic circuit' a little difference in the component' can lead to large differences in the out coming voltages. This is also by the different starting values.

We have proposed generic RC realizations of Chua's circuit. With these realizations, we have demonstrated that the core of this chaotic circuit is a sinusoidal oscillator. A large number of realizations of this circuit can be found simply by picking any sinusoidal oscillator from literature or by designing a new one.

Soft tuning of circuit parameters allows us to observe different structure of chaotic attractors. Physical realization would provide us with interesting tool for laboratory experiments. Realization could be made using only four IC. INIC is not necessary for the correct function of our circuit, but it is well suited for quickly swapping between consumption and distribution require for predjusted non-linearity.

Undoubtedly chaotic circuit will pay the significant role in future communication techniques. Such system that produces chaotic trajectories with several shapes can be very useful, mostly in coders, modulators and broadband signal generators.

The Chua circuit has been built in many laboratories as a physical source of pseudo random signals and in numerous experiments on chaotic studies. It has also been used extensively in many numerical simulations and exploited in avant-garde music compositions and in evolution of natural languages.

Arrays of Chua circuits have been used to generate two dimensional spiral waves and stationary patterns such as tuning and other exotic patterns. The dimensional attractors have been exploited for applications in image processing, neural networks, dynamic associative memories.

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