DESIGN AND ANALYSIS OF LOW POWER AND STABLE 7T CELL BASED SRAM

A thesis report submitted in partial fulfillment of the requirements for the award of degree of

Master of Technology

in

VLSI Design and Embedded Systems

Submitted by

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CERTIFICATE

This is to certify that the major project work thesis titled **"Design and analysis of low power and stable 7T cell based SRAM "**submitted by **Anand Kumar (Roll no.04/VLSI/09)** in partial fulfillment of the requirements for the award of degree of **Master of Technology in VLSI Design and Embedded Systems at Delhi Technological University** is an original work carried out under my supervision and has not been submitted for the award of any other degree to the best of my knowledge and belief.

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There are a number of people whose support and cooperation has enabled me to present this thesis in its current form and it is imperative that I express my gratitude at this juncture.

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And finally my pal Ajay Chopra, who, while busy with his own project, always lent an ear to many technicalities of my work and tried to make sense of what I sometimes couldn't.

Anand Kumar

Abstract

The design of a seven transistors (7T) SRAM cell is carried out in this project for enhancing the data stability and the read speed while simultaneously reducing the active and standby mode power consumption . With the 7T SRAM cell, the storage nodes are isolated from the bitlines during a read operation, thereby enhancing the data stability as compared to the standard six transistors (6T) SRAM circuits. The transistors of the cross-coupled inverters are not on the critical read delay path with the new technique. The design criteria of access and core mosfets for the read and write operation is analyzed in detail for significantly increasing write and read stability and active power consumption without causing a degradation in the read speed.

A performance comparison vis-a-vis the 6T cell for different parameters is carried out. With the designed 7T SRAM circuit, the read noise margin and the read speed are enhanced by up to 90% and 25%, respectively, as compared to the conventional 6T SRAM circuits.

Furthermore, the leakage power consumption of 7T SRAM circuit is reduced by up to 38%, as compared to the conventional 6T SRAM circuits in a 180nm CMOS technology.

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1. Introduction

1.1 Overview

Embedded SRAMs provide a direct means of bringing the benefits of transistor level density-scaling to the circuit and architecture levels and are therefore vital to this new model of IC scaling. Due to their regular structure and broad applicability to so many digital systems, SRAMs are carefully designed as one of the lead components during the development of new technology nodes, and they utilize highly specialized and aggressive layout rules that address sub-resolution fabrication limitations. This level of design attention has allowed SRAM bit-cells to follow density trends in-line with the transistors themselves.

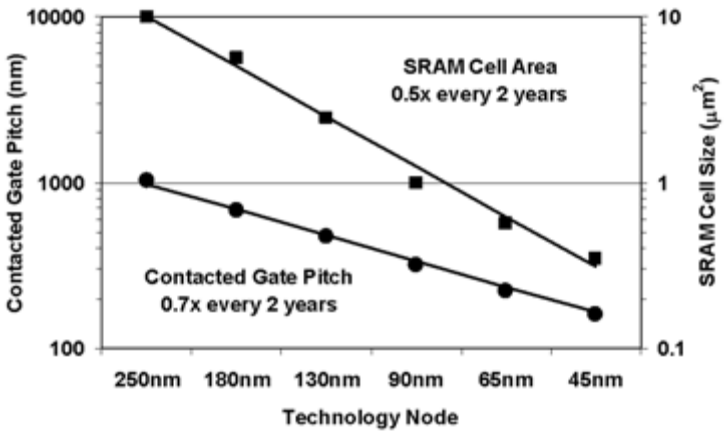


Figure.1.1[9]Density versus technology node

Accordingly, to benefit efficiently from transistor density-scaling, modern digital architectures increasingly emphasize the use and integration of more and more SRAMs. The resulting consequence for low-power devices is that SRAMs occupy a dominating portion of the total die area and the total power consumption.

An important evolution in the semiconductor industry is that, today, the application space for integrated circuits is extremely broad, extending far beyond desktop computing microprocessors to include ambient, remote, mobile, and implantable devices, to name a few. With regards to the

constituent digital circuits, all of these applications have vastly varying and highly stringent demands that require careful design within the associated trade-offs.

In order to adhere to intense scaling trends, SRAM design is also highly constrained, especially in the face of emerging limitations ranging from device-level variability to system-level power consumption. Since their impact on the overall system is so significant and since their design is so constrained, modern embedded SRAMs must be developed with the application in mind so that their own trade-offs can be carefully managed. Generally speaking, SRAMs are strongly subject to the power, performance, and density trade-offs.

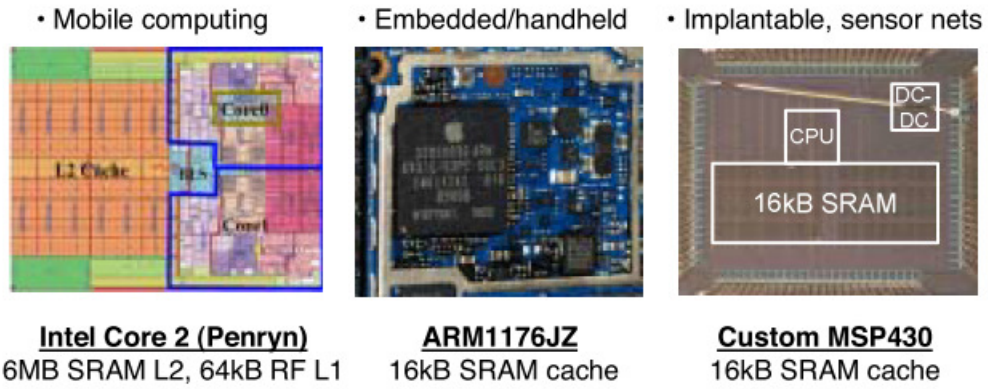


Figure 1.2 Example applications of embedded SRAMs[8]

The origins and effects of these trade-offs are discussed throughout the following chapters, but the overall implication is that improvement in one of the dimensions strongly stresses the others. Of course, all three dimensions are important to some degree in all applications; as a result, embedded SRAM design involves making judicious compromises in order to support the most important system-specific requirements.

1.2. Objective

The amount of embedded SRAM in modern micro-processors and systems-on-chips (SoCs) increases to meet the performance requirements in each new technology generation . Lower voltages and smaller devices cause a significant degradation in SRAM cell data stability with the

scaling of CMOS technology. In addition to the data stability issues, SRAM arrays are also an important source of leakage due to the enormous number of transistors employed in the embedded memory caches. The development of an SRAM cell that can provide higher data stability and lower leakage power is therefore highly desirable.

The aim is to construct a memory array using an alternative bitcell, the 7T , for purposes of increasing stability, speed, power savings and compare its performance vis- a- vis the 6T cell.

The tools employed are the **Cadence Schematic Composer, Spectre Simulator and Virtuoso.**

The technology being used is **180nm** and the process design kit being used is **gpdk180.**

The supply voltage is 1.8 V.

2. The incumbent – 6T memory cell

2.1 Construction

The conventional six-transistor (6T) SRAM is built up of two cross-coupled inverters and two access transistors, connecting the cell to the bitlines (Figure2.1). The inverters make up the storage element and the access transistors are used to communicate with the outside. The cell is symmetrical and has a relatively large area. No special process steps are needed and it is fully compatible with standard CMOS processes.

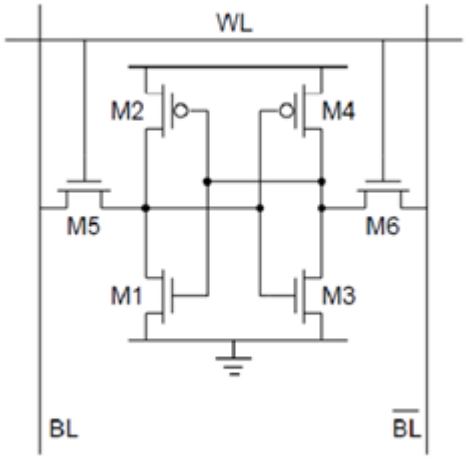


Figure2.1The standard 6T cell

2.2 The read operation

The 6T SRAM cell has a differential read operation. This means that both the stored value and its inverse are used in evaluation to determine the stored value. Before the onset of a read operation, the wordline is held low (grounded) and the two bitlines connected to the cell through transistors M5 and M6 (see figure 2.2) are precharged high (to VDD).Since the gates of M5 and M6 are held low, these access transistors are off and the cross-coupled latch is isolated from the bitlines.

If a “0” is stored on the left storage node, the gates of the latch to the right are low. That means that transistor M3 (see figure 2.2) is initially turned off. In the same way, M2 will also be off initially

since its gate is held high. This results in a simplified model, shown in figure, for reading a stored "0".

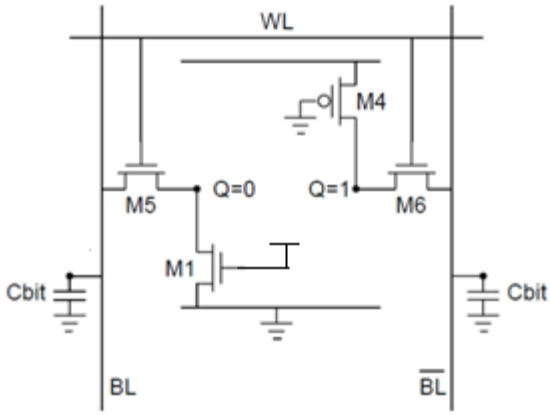


Figure 2.2Effective schematic during read

The capacitors, Cbit, (figure2.2) represent the capacitances on the bitlines, which are several magnitudes larger than the capacitances of the cell. The cell capacitance has here been represented only through the value held by each inverter (Q=0 and Q=1respectively). The next phase of the read operation scheme is to pull the wordline high and at the same time release the bitlines. This turns on the access transistors (M5 and M6) and connects the storage nodes to the bitlines. It is evident that the right storage node (the inverse node) has the same potential as BL and therefore no charge transfer will be take place on this side.

The left storage node, on the other hand, is charged to "0" (low) while BL is precharged to VCC. Since transistor M5 now has been turned on, a current is going from Cbit to the storage node. This current discharges BL while charging the left storage node. As mentioned earlier, the capacitance of BL (Cbit) is far greater than that of the storage node. This means that the charge sharing alone would lead to a rapid charging of the storage node, potentially destroying the stored value, while the bitline would remain virtually unchanged. However, M1 is also turned on which leads to a discharge current from the storage node down to ground. By making M1 stronger (wider) than M5, the current flowing from the storage node will be large enough to prevent the node from being charged high.

2.3 The sense amplifier

After some time of discharging the bitline, a specialized detection circuit called Sense Amplifier (see figure 2.3) is turned on.

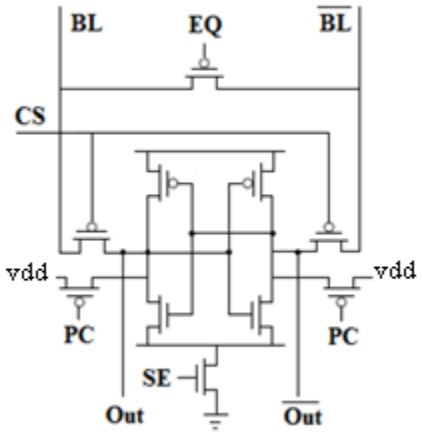


Figure2.3 The sense amplifier

It detects the difference between the potentials of BL and BL and gives the resulting output. Initially the sense amplifier is turned off (sense enable, SE, is low). At the same time as the bitlines of the 6T cell are being precharged high, so are the cross-coupled inverters of the sense amplifier. The bitlines are also equalized (EQ is low) so that any mismatch between the precharges of BL and BL is evened out.

When the wordline of the memory cell is asserted EQ and PC are lifted and the precharge of the sense amplifier is discontinued. The column selector CS is then lowered to connect the bitlines to the latch of the sense amplifier. In figure 2.4, for purpose of clarity, only one column selector transistor for each side of the sense amplifier is present. However, normally several bitlines are connected to the same sense amplifier, each one with its own column selector transistor. In this way, several bitlines can be connected to the same sense amplifier, and the column selectors are then used to determine which bitlines should be read.

After some time, when a voltage difference of about 50-100mV (for a 180nm process) has developed between the two inverters of the sense amplifier, the sensing is turned on. This is done by raising SE, and thereby connecting the sources of the NMOS transistors in the latch to gnd. Since

the internal nodes were precharged high the NMOS transistors are open and current is being drawn from the nodes. The side with the highest initial voltage will make the opposite NMOS (since it is connected to its gate) draw current faster. This will make the lower node fall faster and in turn shut of the NMOS drawing current from the higher node. An increased voltage difference will develop and eventually the nodes will flip to a stable state.

The Out node in figure is then connected to a buffer to restore the flank of the signal and to facilitate driving of larger loads. Also the Out node is usually connected to an inverter. This inverter is of the same size as the first inverter in the buffer. This is to make sure that the two sense amplifier nodes have the same load, and therefore will be totally symmetric. Note that it is essentially the “0” that is detected for the standard 6T SRAM, since the side with the stored “1” is left unchanged by the cell. The output is determined by which side the “0” is on; “0” on the normal storage node results in a “0” output while “0”on the inverse storage ode results in a “1” output. Therefore the performance is mainly dependent on the constellation M1-M5 or M3-M6 and their ability to draw current from the bitline.

2.4 The read constraint

When designing the transistor sizes for read stability, we must ensure that the stored values are not disturbed during the read cycle. The problem is that, as current flows through M5 and M1, it raises the output voltage at node Q which could turn on M3 and bring down the voltage at node Qbar. To avoid altering the state of the cell when reading, we must control the voltage at node Q by sizing M1 and M5 appropriately. We can accomplish this by making the conductance of M1 about 3 to 4 times that of M5 so that the drain voltage of M1 does not rise above VTn (mosfets threshold voltage) of M3 . This design must be carried out with due consideration to process variations and noise. In effect, the read stability requirement establishes the ratio between the two devices.

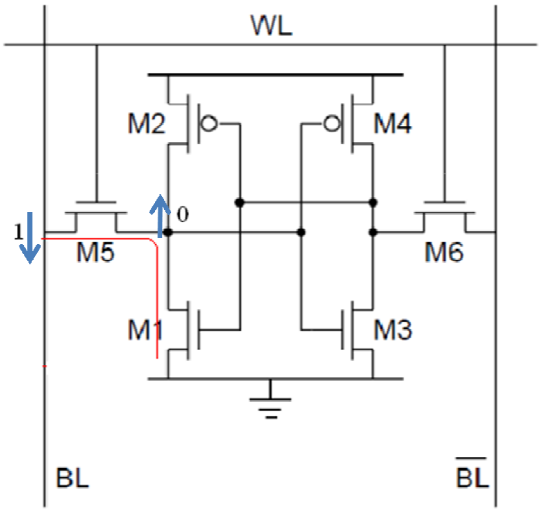


Figure2.4 The read stability constraints

2.5 The write constraint

The design of the SRAM cell for a proper write operation involves the transistor pair M4-M6.When the cell is first turned on for the write operation, they form a pseudo-NMOS inverter. Current flows through the two devices and lowers the voltage at node Qbar from its starting value of VDD. The design of device sizes is based on pulling node Qbar below inverter switching threshold to force the cell to switch via the regenerative action. Note that the bitline is pulled low before the wordline goes up. This is to reduce the overall delay since the bitline will take some time to discharge due to its high capacitance. The pull-up to pull-down ratio for the pseudo-NMOS inverter can be determined by writing the current equation for the two devices and setting the output to inverter threshold(VS). To be conservative, a value much lower than VS should be used to ensure proper operation in the presence of noise and process variations.

2.6 Static noise margins and read margins, defined

SNM is length of side of the largest embedded square on the butterfly curve.

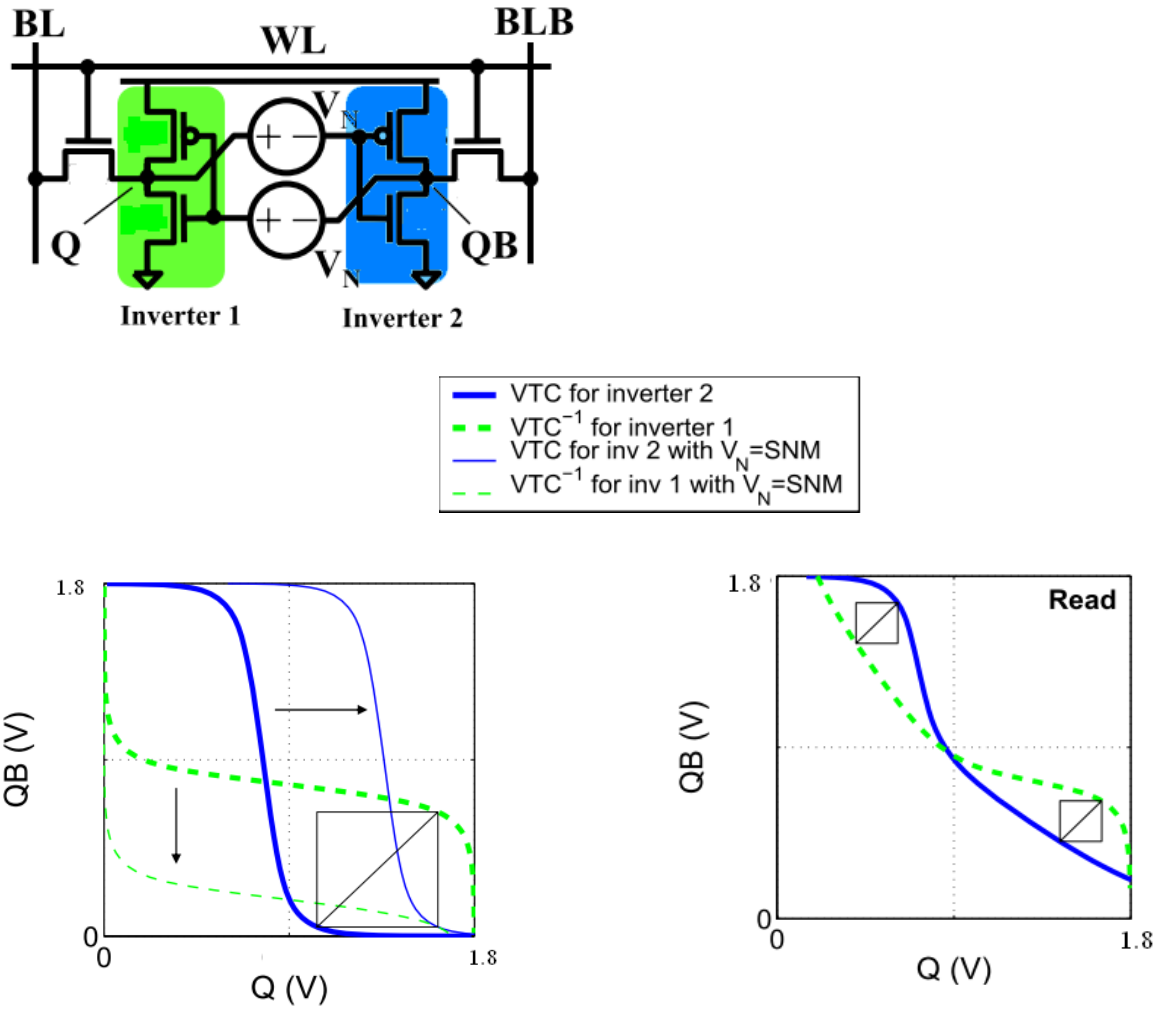


Figure2.5 SNM,Read SNM and their degradation

- Read SNM is the worst case.

2.7 The sized 6T cell

Figure2.6 The 6T with dimensions

We simulate them for various parameters: Write margins, Read margins, Read delay, Write delay, Leakage power etc. The observed values will then be compared against an improved bitcell design to be discussed next.

3. An alternative bitcell

3.1 The Motivation

The results obtained for the 6T memory cell indicate:

- Severe degradation of read stability-that is the robustness of the cell to noise during read process, for which sizing constraints demand strengthening of pull down nmos transistor with respect to the access transistor.
- Writability also demands that the access transistors be made stronger w.r.t to the pull up pmos transistor.

In general, anything that involves the data storing nodes to be a part of the access process will surely increase vulnerability of the node to noise and the chances of a data upset.

For the read process, if we could somehow decouple the data nodes from the bitlines and yet succeed in conveying the data information, it would greatly help towards increasing the read margins.

3.2 A case in the point-the 7T cell

This is a memory cell as proposed by Kursun et al (2008) [1]

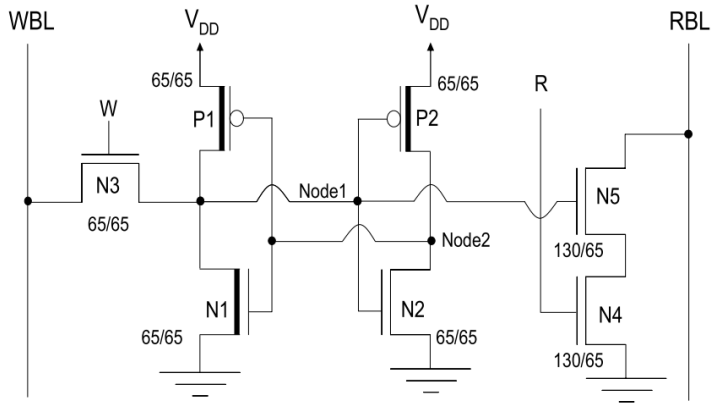


Figure3.1Originally proposed 7T cell

The key features of this cell:

- Bitline discharge during read process is dependent on the value stored at node1; logic 1 will enable discharge which can be consequently sensed, and logic 0 will cause not any bitline drop at all.

- The transistors of the cross coupled inverters are not on the read delay path and access transistors N4 and N5 can be sized according to delay requirements independent of the core mosfet(N1,P1,N2,P2) sizes.

- Increased read stability and increased read speed, reduced leakage and reduced write power are advantages claimed and will be subsequently explored.

1.3 The proposition

We plan to implement a similar cell, using the *gpdk180 process design kit*, albeit sans the use of high Vt transistors. Further, we compare the performance of the cell so designed, head to head with the 6T cell earlier described, in terms of data stability, delay, and power (in standby and active modes) as well as area.

3.4 The cell to be designed

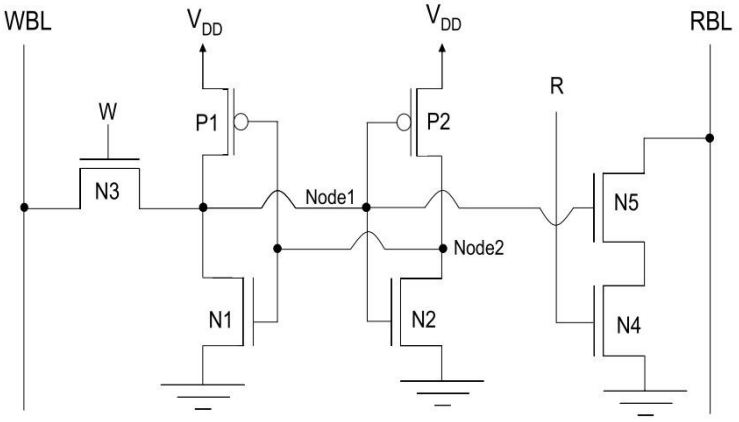


Figure 3.2The cell to be designed

- The circuit schematic of the proposed SRAM cell with transistors sized for a 180nm CMOS technology is shown in Fig3. 2.

- The cross-coupled inverters formed by the transistors N1, P1, N2, and P2 store a single bit of information. The write bitline WBL and the pass transistor N3 are used for transferring new data into the cell.

- Alternatively, the read bitline RBL and the transistor stack formed by N4 and N5 are used for reading data from the cell.

- Two separate control signals R and W are used for controlling the read and the write operations, respectively, with the proposed circuit as shown in Fig4. 2.

3.5 The read operation

- Prior to a read operation, the RBL is pre-charged to VDD .

- To start the read operation, the read signal R transitions to VDD while the write signal W is maintained at V GND . If a "1" is stored at Node1, RBL is discharged through the transistor stack formed by N4 and N5. Alternatively, if a "0" is stored at Node1 RBL is maintained at V DD .

- The storage nodes (Node1 and Node2) are completely isolated from the bitlines during a read operation. The data stability is thereby significantly enhanced as compared to the standard 6T SRAM cells.

- The RBL is conditionally discharged through the N4-N5 stack during a read operation. The transistors of the cross-coupled inverters are not on the read-delay-path. The transistor sizing of the cross-coupled inverters therefore does not affect the read speed of the proposed SRAM cell.

3.5.1 The sensing scheme employed

Because a single bitline is utilized during a read operation, we choose to employ a single ended sense amplifier as proposed by chen et al(2004):

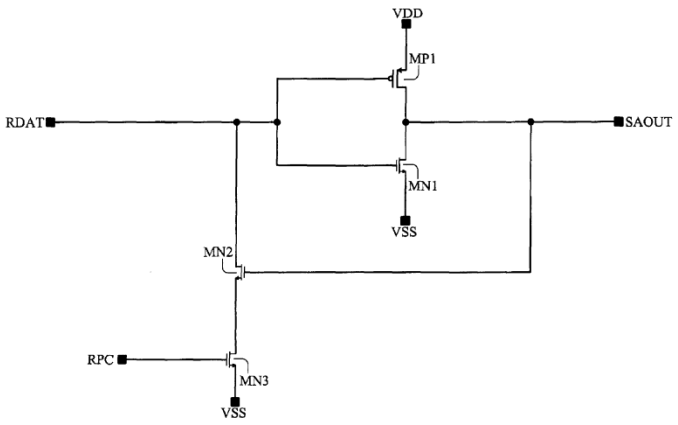


Figure3.3 Single ended sense amplifier

Its working may be briefly explained as follows:

- The falling voltage level is delivered through the RDAT line as an input to the inverter. When the voltage level falls below Vdd-|Vtp|, the pmos MP1 of the inverter turns on.

- When the voltage level falls below the inverter threshold a logic high at SAOUT in turn causes MN2 to turn on in turn providing an additional path for discharge and thus speeding up the same.MN3 is turned on as soon as the precharge activity is completed; this is signified by RPC going high.

3.5.2 Design criteria for read

- The access transistors attached to bitlines have to be sized keeping in mind that increased widths may offer the attraction of faster discharge but at the same time increase the node/bitline capacitance.

- We want the sense amp to step in as quickly as possible and provide an additional discharge path; the idea is to increase the inverter threshold so as to switch at the earliest while RDAT is falling.

- Since the pull down nmos transistors are of the core cell are in no way involved in the read process, we are spared the effort of strengthening them with respect to the access transistors, to maintain stability of the stored value. This will prove to a plus-point during write analysis as we shall find out.

3.5.3 The consolidated read assembly

Figure3.4 The complete read schematic of the 7T Sram cell

3.5.4 The read waveforms so obtained.

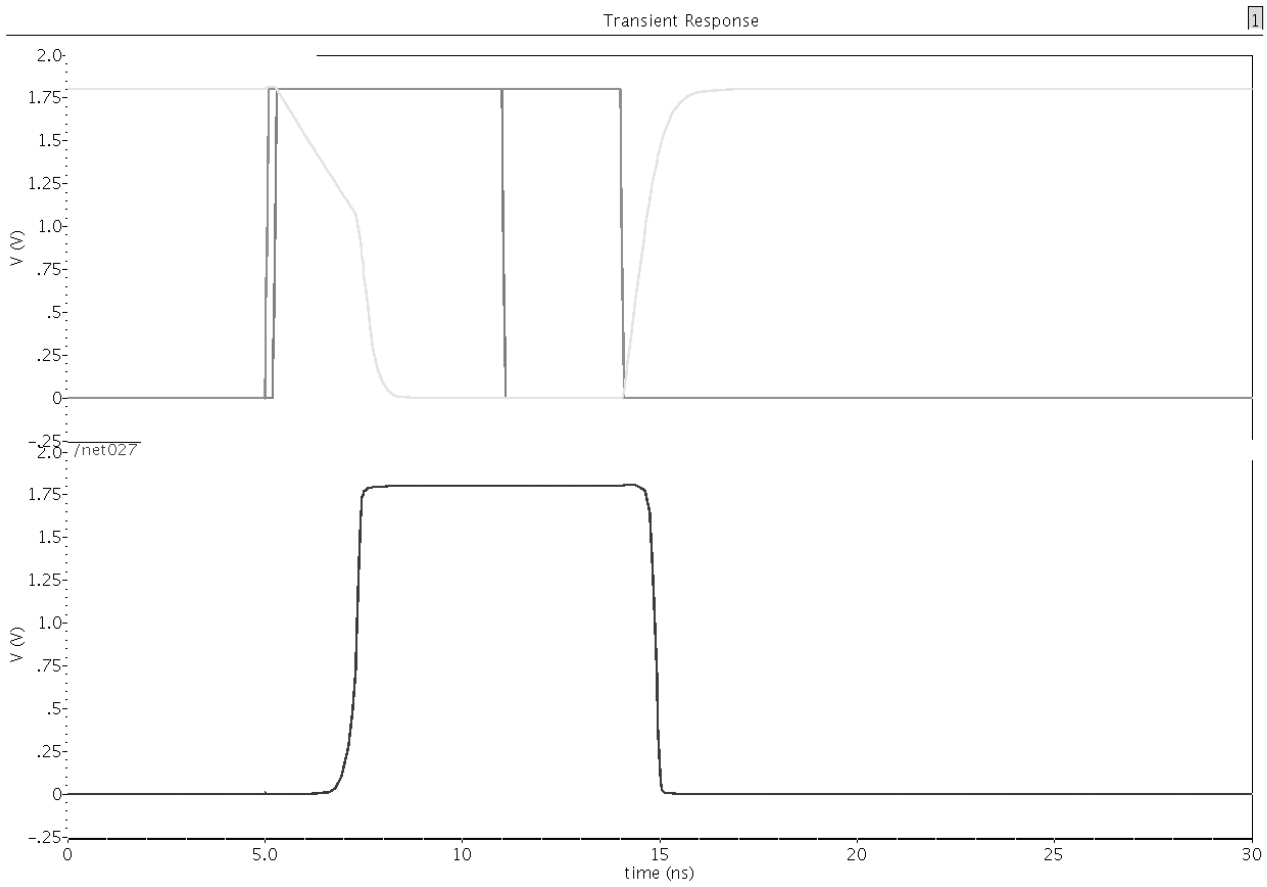


Figure 3.5 The read waveforms

3.6 The write operation

- Prior to a write operation the WBL is charged (discharged) to VDD (VGND) to get ready to force a “1” (“0”) onto Node1.

- To start the write operation, the write signal W transitions to VDD while the read signal R is maintained at VGND . The data is forced onto Node1 through bitline access transistor N3.

3.7 Analysis of single ended Writability

3.7.1 The conventional write process in the 6T cell

For a standard 6T SRAM cell, writing is done by lowering one of the bitlines to ground while asserting the wordline. To write a ’0’ BL is lowered, while writing a ’1’requires BL to be lowered.

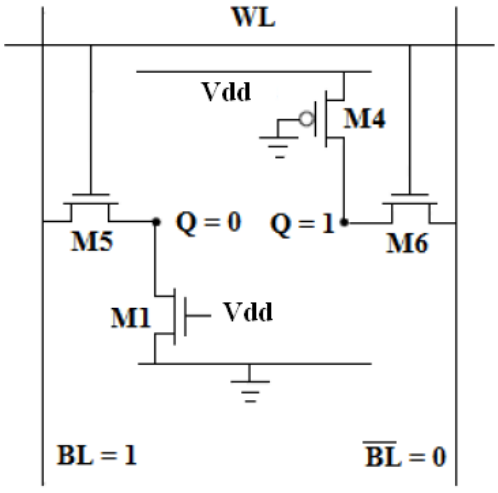


Figure3.6 The effective 6T write schematic

- Let’s assume that the cell has a ’0’ stored and for simplicity the schematic has been reduced in the same way as before. The bitlines no longer are released. Instead they are held at VDD

and GND respectively. It can be seen from the left side of the memory cell (M1-M5) that it is virtually identical to the read operation.

- During the discussion of read operation, it was concluded that transistor M1 had to be stronger than transistor M5 to prevent accidental writing. Now in the write case, this feature actually prevents a wanted write operation. Even when transistor M5 is turned on and current is flowing from BL to the storage node, the state of the node will not change. As soon as the node is raised transistor M1 will sink current to ground, and the node is prevented from reaching even close to the switching point. *So instead of writing a '1'to the node, a '0' will be written to the inverse node.*

- Looking at the right side of the cell, we have the configuration M4-M6. In this case BL is held at GND. When the wordline is raised M6 is turned on and current is drawn from the inverse storage node to BL. At the same time, however, M4 is turned on and, as soon as the potential at the inverse storage node starts to decrease, current will flow from VDD to the node.

- In this case M6 has to be stronger than M4 for the inverse node to change its state. The transistor M4 is a PMOS transistor and inherently weaker than the NMOS transistor M6 (the mobility is lower in PMOS than in NMOS).

- Therefore, making both of them minimum size, according to the process design rules, will assure that M6 is stronger and that writing is possible. *When the inverse node has been pulled low enough, the transistor M1 will no longer be open and the normal storage node will also flip, leaving the cell in a new stable state.*

3.7.2 The write process in the 7T cell

- The topology of the cell is such that writability has to occur through the lone access transistor provided for the purpose.

- Writability in the 6T cell was primarily about discharging one of the nodes to ground; the symmetrical structure of the 6T gave us the freedom to do so. Design criteria for this implied that we weaken the pmos pull up transistor w.r.t to the access transistor.

- However, in the 7T we have to contend with the other possibility of writing a one"1" to a node that stores a "0"; this in turn imposes other design constraints as we shall see.

3.7.3 Write margins, defined

Writing to an SRAM cell is, possible with a voltage higher than 0V on the discharged bitline (performing a write operation with an incomplete/partially discharged bitline). The write margin is the maximum incomplete bitline discharge voltage for which the successful transfer of new data into the 6T. The content of an SRAM cell with a higher write margin is easier to be modified.

For the 7T SRAM cells, two different write margins exist. The definition and measurement of the write margin when writing a "0" is similar to the 6T . Alternatively, when writing a "1" into the 7T SRAM cell, the write margin is the difference between V DD and the minimum bitline voltage required to achieve a successful transfer of a "1" into the cell.

3.7.4 Design for writability

Write 0: When we wish to write 0 to a node storing 1 we desire that the pmos pull up transistor be weak w.r.t the access transistor. This design criteria is very similar to that of the 6T because the process involved is the same-discharge.

Write 1: When we wish to write 1 to a node storing 0 we desire

a. That the pull down nmos N1 be weak as compared to the access transistor. This requirement is not a difficult one to meet since it does not pose a contradiction to the read stability, a

problem that the 6T poses and the 7T does away with, by reason of its decoupled node topology. We aim to size the pull down nmos to minimum dimensions.

b. Furthermore, since the access transistor transfers a degraded “1” (due to the Vt drop), the inverter formed by N2 and P2 is required to have a low switching threshold voltage that assists the transfer of a full “1’ onto Node1.

3.7.5 The sizing data and trends for write 0

The write 0 operation is in a 7T cell is similar to the 6T cell; the pmos pull up transistor that stores a “1” at a node must be weaker than the access transistor through which it is supposed to be discharged. To see how the writable “0”voltage depends on the pull up to access ratio we may tabulate observations as under:

We see that that it would be very much to our advantage if the access transistor is sized larger.Thus we choose to keep P1 sized minimum and proceed to analyze the sizing of N1,N2,P2 according to write “1” criteria as explained in the next section.

3.7.6 The sizing data and trends for write 1

The criteria stated in section 3.7.4 for write 1 point to the need of observing writability with respect to the threshold voltage of N2P2 versus access transistor size, given that we would choose a minimum sized transistor for P1, because write 0 demands so.

Figure3.7 Threshold voltage of N2P2 and accessN3 length impact on the writable WBL voltage.

Note that the threshold voltage of N2P2 is varied by keeping P2 minimum sized and N2 dimensions being varied.

Figure3.8 Threshold voltage of N2P2 and accessN3 length impact on the writable WBL voltage (2^{nd} angle)

3.7.8 The sized 7T SRAM cell

P1 is kept sized minimum at for write 0 stability.N1 only had a role in ensuring read stability; because the 7T relieves it of this responsibility we keep it sized minimum too.N2P2 sizes and access N3 sizes are chosen corresponding to a desired write 1 margin of 500mV, this corresponds to N3 as shown and N2P2 having a switching threshold of 670mV,as taken from the plots depicted in Figure 3.8.

4. Comparison of the results so obtained

4.1 Stability

4.1.1 Read stability

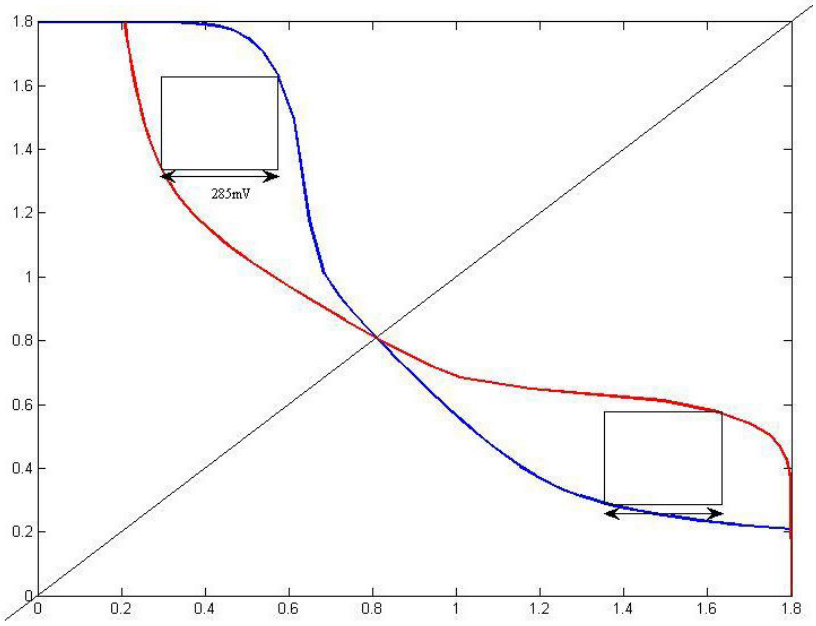


Figure4.1 Read SNM curves for 6T

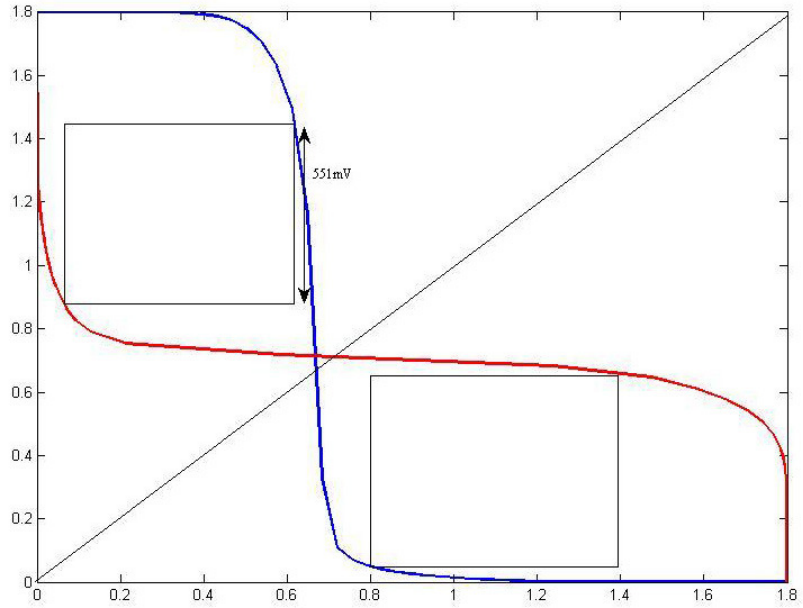


Figure4.2 Read SNM curves for the 7T

The measured read margins for the 6T : 285mV

The measured read margins for the 7T : 551mV

The measured results show that there is an **improvement in the read margin by about 90%** and this is clearly attributed to the decoupling of the data nodes from the bitlines during the read process.

4.1.2 Write stability

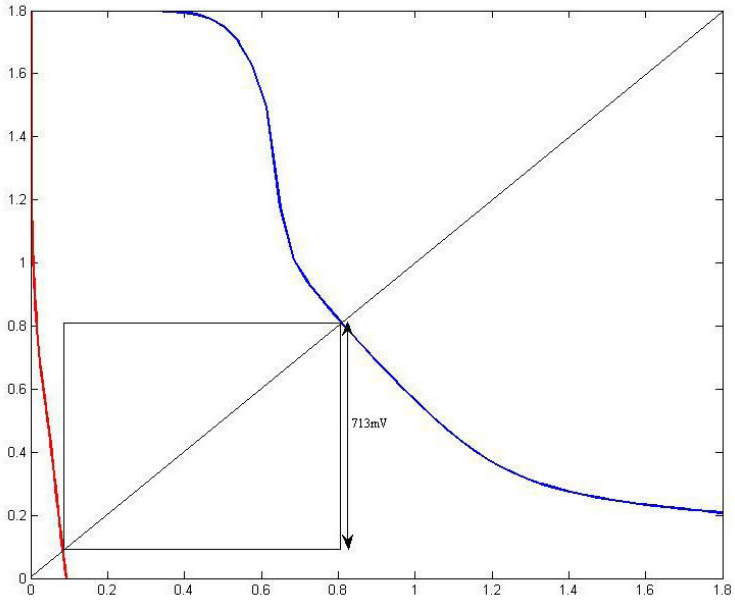


Figure4.3 Write margin (0) for the 6T

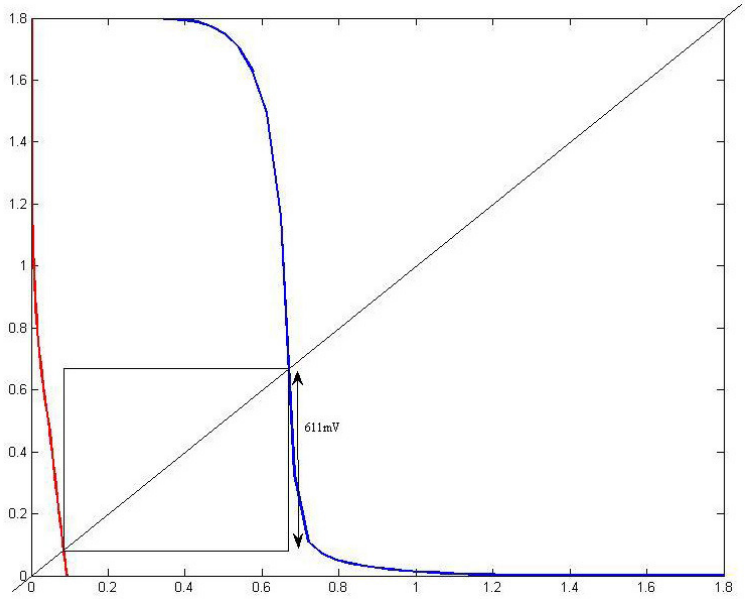


Figure 4.4 Write margin (0) for the 7T

The measured write margin (0) for the 6T : 713mV

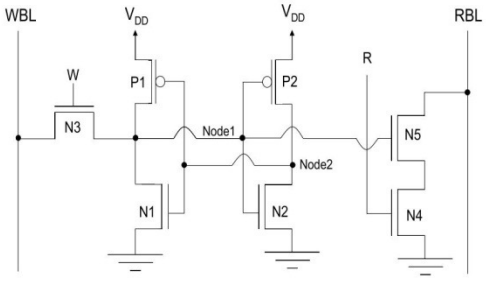
The measured write margin (0) for the 7T : 611mV

The measured results show that there is a **decrease in the write margin by 14.4%** and this is due to the fact that that write operation resulting in the discharge of the node storing 0 is a single ended activity with no charging activity at the other end/node. The steepened transfer characteristic in figure 4.4 verifies this by allowing a smaller square to be nested. However, 611mV in itself is quite adequate a margin to have.

4.2 Leakage power

The leakage power of the 6T cell is found out be7.21 picowatts per cell which will work out to be 73.8nW for a 1KB array.

The leakage power of the 7T cell is found out to be 4.47 picowatts per cell which represents a **reduction of 38% in the leakage power consumption.**



This can be attributed to the fact that leakage through N4 and N5 is

- Data dependent on the value stored at node 1.
- Stack effect of N4 and N5 makes it harder for a leakage path to ground.

4.3 Speed

4.3.1 Read delay

The read speed here will be defined as the time difference between the 50% of the activated read signal to the 50% of the sense amplifier output.

The read delay for the 7T has been found to be **2.1ns**

The read delay for the 6T has been found to be **2.621ns**

The 7T thus shows **an improvement of 25%** in the measured read delay

4.3.2Write delay

The write delay is measured as the time period from the 50% point of the low-to-high transition of the signal that controls the write driver until the storage node is discharged to VDD /2 (from an initial voltage of VDD).

The write delay for the 7T has been found to be **1.2ns**

The write delay for the 6T has been found to be **0.8ns**

The 7T thus shows **degradation in the write speed.** This is attributed to the fact that the write access transistor, having been upsized for purposes of write stability, has ended up increasing the writebitline (WBL) capacitance.

5. Conclusion

5.1 Summary

A seven transistors (7T) SRAM cell is designed in this project for enhancing the data stability ,both for read and write, improving the read speed while simultaneously reducing the active and standby mode power consumption . With the 7T SRAM cell, the storage nodes are isolated from the bitlines during a read operation, thereby enhancing the data stability as compared to the standard six transistors (6T) SRAM circuits. The design criteria of access and core mosfets for the read and write operation is analyzed in detail for significantly increasing write and read stability without causing a degradation in the read speed.

A performance comparison vis-a-vis the 6T cell for different parameters is carried out. With the designed 7T SRAM circuit, the read noise margin and the read speed are enhanced by up to 90% and 25%, respectively, as compared to the conventional 6T SRAM circuits.

Furthermore, the leakage power consumptions of 7T SRAM circuit are reduced by up to 38%, as compared to the conventional 6T SRAM circuits in a 180nm CMOS technology.

5.2 Further Direction

5.2.1Write assist techniques

5.2.1.1 Collapsing cell VDD

A primary challenge in the 7T lies in balancing a degraded WNM, due to difficulty writing '1' through the access transistor versus the increased size leading to decreased write speed. Nalam and Calhoun(2008)[3] show that by collapsing VDDCell or VDDC([4], [5]), we can solve this problem. As the timing waveforms in Fig. 5.1 show, collapsing VDDC weakens the cell feedback, enabling it to flip despite the weak '1' passed by N3. Collapsing VDDC reduces the Hold SNM of the half-selected cells (e.g. same V DDC , but WL=0), but it can be shown that the Hold SNM remains sufficiently high even when V DDC reduces enough to provide the 5T with adequate WNM.

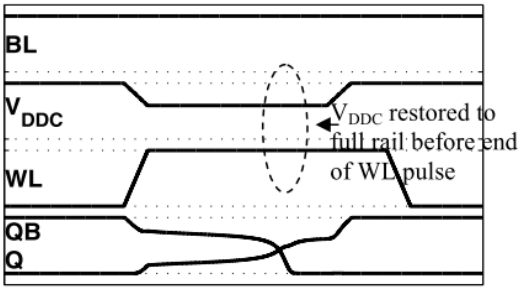


Figure 5.1 Timing for V DDC collapse write-assist.

5.2.1.2 Boosted wordline

Another technique which assists the bit cell to flip during a write event is boosting the word-line higher than the supply voltage (Figure 5.2). The boosting increases the VGS of the access transistor and hence increases its drive strength. The increased drive strength of the access transistor aids significantly in flipping the bit cell. The boost voltage can be routed as a separate power supply or it can be generated internally by a charge pump or by capacitive coupling .

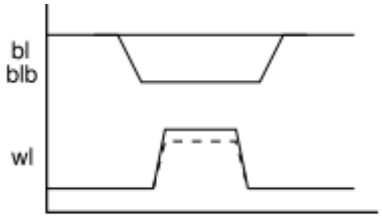


Figure 5.2 Boosted wordline

Wordline boosting can be used in combination with collapsing V DDC .It will be observed that boosting WL during write allows for a lower V DDC drop to achieve similar WNM.

5.2.2 Forward body biasing schemes.

Kousha,Ebrahimi et.al(2009)showed that implemented 7T SRAM could be further optimized for leakage through forward body biasing of the read stacked transistors. In order to reduce the leakage power consumption of the stacked read transistors (which forms a significant part of the total leakage power), these transistors are chosen to have high threshold voltages. Because of total separation of read and write circuits, these two transistors are not operating during the write phase the same as standby mode. So in these two phases their

threshold voltages are kept high to reduce the leakage power. And during read time using the proposed body biasing method, their threshold voltages are reduced to improve their performance.

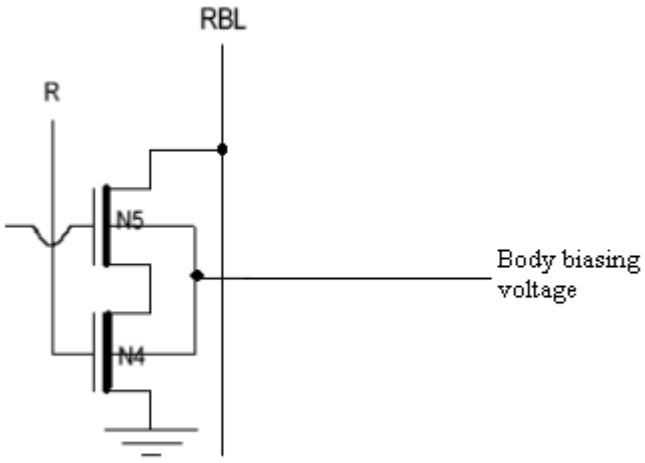


Figure 5.3 Application of body bias to access transistors to reduce leakage.

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