A
Dissertation
on

REALIZATION OF P, PD, PI AND PID CONTROLLERS USING OTRA

submitted in partial fulfillment of the requirements

for the award of degree of

Master of Technology

in

VLSI Design and Embedded System

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CERTIFICATE

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This is to certify that the report entitled **"*Realization of P, PD, PI and PID Controllers using OTRA (Operational Transresistance Amplifier)*"** submitted by Saurabh Chitransi, Roll. No. 17/VLSI/09, in partial fulfillment for the award of degree of Master of Technology in VLSI Design & Embedded System at **Delhi Technological University, Delhi**, is a bonafide record of student's own work carried out by him under my supervision and guidance in the academic session 2009-11. The matter embodied in dissertation has not been submitted for the award of any other degree or certificate in this or any other university or institute.

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ACKNOWLEDGEMENT

It has been rightly said, “we are build on the shoulders of others” for everything we have achieved the credit goes to our faculty members.

I would like to express my immense gratitude to my advisor, **Asst. Prof. Rajeshwari Pandey**, for her enthusiasm, encouragement, patience, & timely support. It is my privilege to have worked under her supervision. Her invaluable guidance & helpful discussion at every stage of this project helped me in timely materialization & successful completion of this project.

My special thanks to Dr. Neeta Pandey for her support and guidance to understand the SPICE and to operate on OrCad PSpice tool.

I am thankful to my friends Chandra Shekhar, Piyush Gupta, and Praveen Kumar for valuable discussions.

I am grateful to my parents and my younger brothers Shivam and Pushkar for their moral support. They have been always around to cheer me up, in the odd times of this work. I am also thankful to my classmates for their unconditional support and motivation during this work.

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ABSTRACT

Control engineering deals with understanding of plant under operation, and obtaining a desired output response in presence of system constraints. There has been an ever increasing demand of controllers in process industry for improving manufacturing processes and energy efficiency.

The evolution of submicron technologies has resulted in the requirement to use low power supply voltages which makes it difficult to design voltage mode circuits with high linearity and wide range. Also as signal processing extends to higher frequencies, the traditional design methods based on voltage operational amps are no longer adequate. However generally analog controllers are designed using operational amplifiers. To overcome these problems circuits operating in current mode, which have the inherent property of higher bandwidth, larger dynamic range and better linearity, are preferred. Various analog building blocks operating in the current mode such as various generations of current conveyor, CDBA, OTA, OTRA etc are available in literature. OTRA being a current mode device inherits all the advantages of current mode techniques, in addition it is free from parasitic input capacitances and resistances.

In this thesis OTRA based controllers i.e. P, PD, PI and PID with independent tuning of proportional K_p, derivative K_d and integral K_i constants are presented. These configurations can be made fully integrated by implementing the resistors using matched transistors operating in linear region. To observe the effect of controller on second order system a second order low pass filter is designed and simulated. In order to verify the functionality of proposed controller circuits, a closed loop control system using the proposed controllers and second order LPF is designed and simulated using SPICE.

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INTRODUCTION

1.1 Motivation

Control engineering deals with understanding of plant under operation, and obtaining a desired output response in presence of system constraints. Controllers have applications in various sectors of industry, such as quality control of manufactured products, automated assembly lines, machine-tool control, space technology and weapon systems, computer control, transportation systems, power systems, robotics, Micro-Electro-Mechanical Systems (MEMS), nanotechnology etc [1]. There has been an ever increasing demand of controllers in process industry for improving manufacturing processes and energy efficiency [2]. Especially energy efficiency is the focus and controllers have a significant role to play. Hence there has been a significant endeavor to obtain effective controller designs.

Proportional-integral-derivative (PID) controllers are one of the most important control elements used in the process control industry. Generally operational amplifiers are used to design classical analog controllers. However the operational amplifiers, being voltage mode circuit, have their own limitation of constant gain bandwidth product and low slew rate. Current mode building blocks such as Current Conveyor, OTA, CDBA, CDTA, OTRA etc. have larger bandwidth, dynamic range, and also greater linearity than their voltage-mode counterparts, op-amps [3].These active blocks therefore would be a better substitute of OPAMP for designing the analog controllers.

Operational Transresistance Amplifier (OTRA) is a high gain current input, voltage output amplifier [4]. OTRA being a current mode building block inherits the advantages of current mode processing as well as it is free from parasitic input capacitances and resistances as its input terminals are virtually grounded and hence, non-ideality problem is less in circuits implemented using OTRA. In literature, OTRA based controllers have not been reported so far.

In low power analog applications, the effect of noise is prominent. To reduce the effect of noise on the circuits, designers of analogue ICs usually build their circuitry as differential rather than single-ended structure.

In view of above, Differential Operational Transresistance Amplifier-based controllers are introduced in this dissertation. To verify the theoretical analysis of these controllers second order closed loop system using second order Low Pass Filter and the controllers are designed and simulated using SPICE.

1.2 Literature Review

OTRA is the basic building block of a number of applications both in current and voltage and mixed modes. The first CMOS circuit of OTRA was introduced in 1992 by J. J. Chen, H. W. Tsao & C. C. Chen [4]. Reference [5] 1995 shows that the input terminals of OTRA being virtually grounded, the circuits designed using OTRA were insensitive to stray capacitances [5]. In 1999 Salama and Ahmed M. Soliman introduced a simple CMOS realization of OTRA based on cascaded connection of modified differential current conveyor (MDCC) and a common source amplifier [6]. In [7] they proposed a new circuit based on same cascaded connection of modified differential current conveyor (MDCC) and a common source amplifier as in [6] but with improved performance and less number of transistors. The Circuit proposed in [8] is based on same input stage of OTRA proposed in [7] and a differential gain stage is used instead of the single common source amplifier and a compensation circuit is used to compensate difference between the two drain voltages of input transistors. The circuit proposed in [9] is another modification of circuit presented in [7] where differential gain stage is used instead of the single common source amplifier. Several other CMOS realizations of OTRA are also available in literature [10-12]. Circuit presented in [10] consists of a differential current controlled current source (DCCCS) followed by a voltage buffer whereas circuit reported in [11] is made of R_m cell, feedback network and output driver. A low voltage regulated cascode current mirror with a low voltage regulated cascode load forms core of the circuit proposed in [12]. OTRA is commercially available from several manufacturers under the name current differencing or Norton amplifier, [13-15].

Various applications of OTRA also exist in literature. Filters using OTRA are proposed in [5-6, 16-21] and oscillators & multi vibrators are presented in [21-27] whereas Schmitt trigger is presented in [28]. Realizations of immittance using OTRA are reported in [29-31].

Further literature survey reveals that a number of circuits have been reported relating to proportional (P), proportional integral (PI), proportional derivative (PD), and proportional integral & derivative (PID) controllers in [32–38]. Circuits presented in [32, 33] are based on OpAmps and have their own limitation of finite gain bandwidth. [34] Presents OTA based controllers and [35] presents CDBA based controllers whereas CCII based controllers are proposed in [36-38]. However, no such OTRA based controllers have been reported in literature so far.

1.3 Objective and Scope of the Project

The objective of the project is to design circuits of classical controllers i.e. P, PI, PD and PID using Operational Transresistance Amplifier, analyze their effect on Second Order Control System and design & simulate their MOS-C equivalent circuits for minimizing the chip area and for making these circuits electronically tunable.

These controllers are best suited for the systems where knowledge of the underlying process is absent. These OTRA based designs are best suited for the Low Power and High Speed applications like MEMS (Micro-electromechanical systems) and Low Power Medical Devices apart from its traditional field of application i.e. Process Industry.

1.4 Organization of thesis

The thesis is organized as follows:

Chapter 2: It describes the basics of OTRA, and differential OTRA. It further describes their internal circuit structures. Terminal characteristics of these circuits have been verified through PSPICE simulations.

Chapter 3: This chapter describes the time domain analysis of standard second order system and time domain design specifications. A second order Low Pass Filter circuit using differential OTRA is proposed and it simulation results are also included.

Chapter 4: In this chapter detailed description of basic controllers i.e. P, PD, PI and PID and their effect on second order closed loop is given. Differential OTRA based PD, PI, and PID controllers are proposed and analyzed in this chapter. MOS-C equivalent of P, PD, PI and PID controllers are also discussed.

Chapter 5: This chapter analyzes the simulation results of the circuits proposed in this dissertation.

Chapter 6: In this section conclusion of the thesis work and future scope of the work are presented.

Chapter-2

OPERATIONAL TRANS-RESISTANCE AMPLIFIER

This chapter describes the basics of OTRA as well as Differential OTRA. Here, CMOS realization of Differential OTRA [9] is discussed and its simulation results are presented. This simulated Differential OTRA is used for designing of controllers proposed in this work.

2.1 Basics of OTRA

Operational Trans-resistance Amplifier (OTRA) is a high gain current input, voltage output amplifier [4]. Symbol of OTRA is illustrated in Fig.2.1. OTRA is a three terminal device described by matrix equation:

$$\begin{bmatrix} V_p \\ V_n \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ R_m & -R_m & 0 & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ I_o \end{bmatrix} \quad (2.1)$$

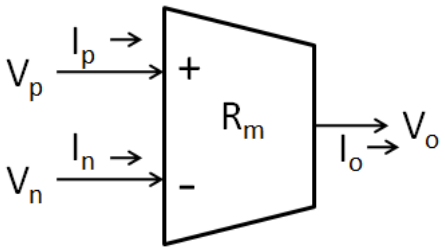


Fig. 2.1 Symbol of OTRA

From the above equation it is clear that both input and output terminals are characterized by low impedance, thereby eliminating response limitations incurred by capacitive time constants. The input terminals are virtually grounded leading to circuits that are insensitive to stray capacitances [5]. Ideally, the transresistance gain, R_m, approaches infinity, and external negative feedback must be used which forces the input currents, I_p and I_n, to be equal [6]. Thus OTRA must be used in a negative feedback configuration. Practically the Transresistance gain is finite and its effect should be considered. Also, the

frequency limitations associated with OTRA should be considered. Considering a single-pole model for the transresistance gain, R_m [6], then:

$$R_m(s) = \left(\frac{R_0}{1+{}^{s}/_{\omega_0}}\right) \tag{2.2}$$

For high frequency applications, the transresistance gain, $R_m(s)$, can be expressed as:

$$R_m(s) \approx \left(\frac{1}{sC_p}\right) \tag{2.3a}$$

where

$$C_p = \frac{1}{R_0 \omega_0} \tag{2.3b}$$

where, R_o is DC open loop transresistance gain and ω_o is transresistance cut off frequency. The small signal ac equivalent of the OTRA is shown in the Fig. 2.2.

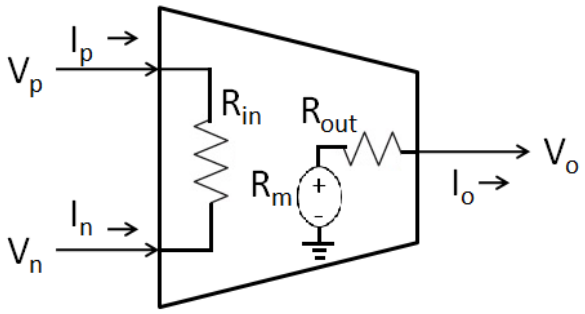


Fig. 2.2 Small Signal AC Equivalent of OTRA

2.2 Differential OTRA

Differential signal processing has higher dynamic range and power supply rejection compared to single-ended counterparts. These parameters are especially relevant in low power circuits. Other inherent advantages of differential circuits include immunity from common-mode noise signals and lower harmonic distortion.

Differential OTRA is a four terminal device characterized by the matrix equation [39]:

$$\begin{bmatrix} V_p \\ V_n \\ V_{o+} \\ V_{o-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ R_m & -R_m & 0 & 0 \\ -R_m & R_m & 0 & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ I_{o+} \\ I_{o-} \end{bmatrix} \tag{2.4}$$

Fig. 2.3 and 2.4 show the symbol and small signal ac equivalent of differential OTRA respectively [39].

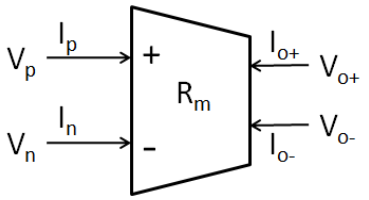


Fig. 2.3 Symbol of Differential OTRA [39]

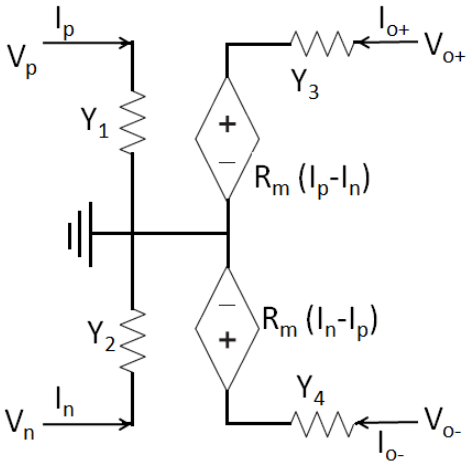


Fig. 2.4 Small Signal AC Equivalent of Differential OTRA [39].

2.3 CMOS Realization of Differential OTRA

CMOS realization of differential OTRA proposed in [9] is shown in Fig. 2.5. It is based on cascaded connection of modified differential current conveyor (MDCC) [40] and a differential gain stage.

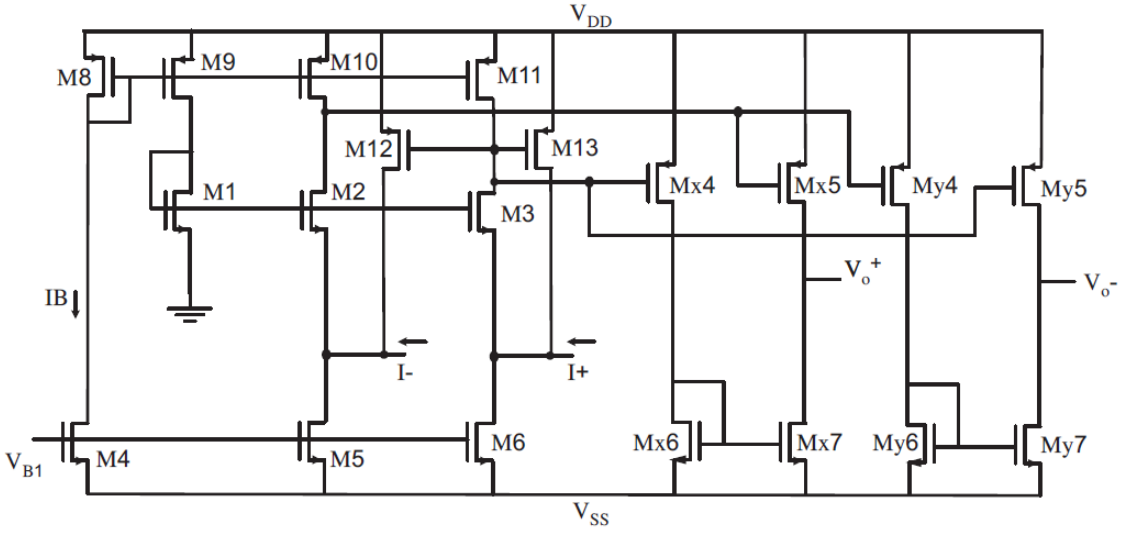


Fig. 2.5 CMOS Realization of Differential OTRA Proposed in [9]

Assuming that each of the groups of the transistors (M1-M3), (M5 and M6), (M9-M11) and (M12 and M13) are matched, and that all transistors operate in saturation region, the circuit operation can be explained as follows.

The current mirrors formed by (M8-M11) forces equal currents (IB) in the transistors M1, M2 and M3. This operation drives the gate to source voltages of M1, M2 and M3 to be equal and, consequently, forces the two input terminals to be virtually grounded.

Current mirrors formed by the transistor pairs (M10 and M11) and (M12 and M13) provide current differencing operation, whereas differential gain stage achieves the high gain stage. The transistors Mx4-Mx7 produce non-inverting output, while the transistors My4-My7 produce inverting output.

2.4 Simulation Results of Differential OTRA

For simulation CMOS implementation of differential OTRA proposed in [9] is used. The SPICE simulation is performed using 0.18µm, Level 7, CMOS process parameters provided by MOSIS (AGILENT) and supply voltages taken are ±1.5 V. Transistors aspect ratios are reported in Table 2.1.

Table 2.1 Transistors aspect ratios of the circuit shown in Fig.2.5.

Transistors	*W(µm)*	*L(µm)*
M1-M3	3.6	0.54
M4	5.4	0.18
M5, M6	5.4	0.36
M8	5.4	0.18
M9-M11	1.8	0.54
M12, M13	3.6	0.54
Mx4, Mx5, My4 and My5	0.18	0.18
Mx6, My7	1.8	0.18
My6, Mx7	0.18	0.18

Biasing voltage VB1 = -0.798013V. Simulation results are tabulated in Table 2.2 and shown in Figs. 2.6, 2.7 and 2.8.

Table 2.2 Simulation results of the circuit shown in Fig. 2.5

Parameters	*Results*	*Unit*
Input current dynamic range	-70 to 70	µA
Input resistances R1, R2	103.58	Ω
DC open loop transresistance	124.8	dBΩ
Gain bandwidth product	98.22	THz. Ω
Transresistance gain B.W. (-3dB)	56.52	MHz
Total power dissipation	2.12	mW
Capacitance C_p	1.61	fF

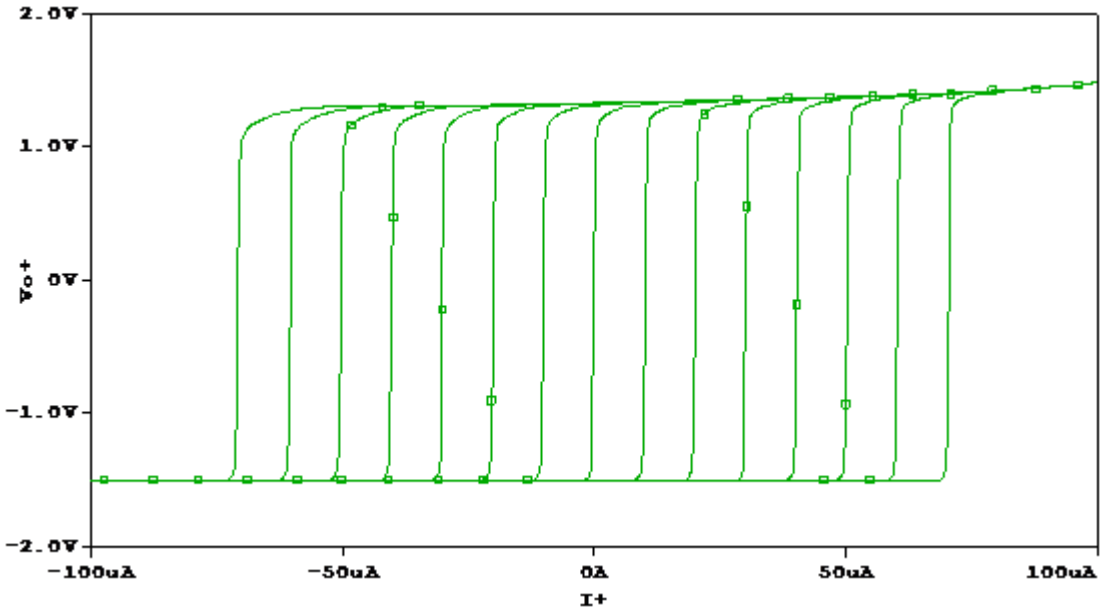


Fig. 2.6a Non-inverting DC Transfer Characteristics.

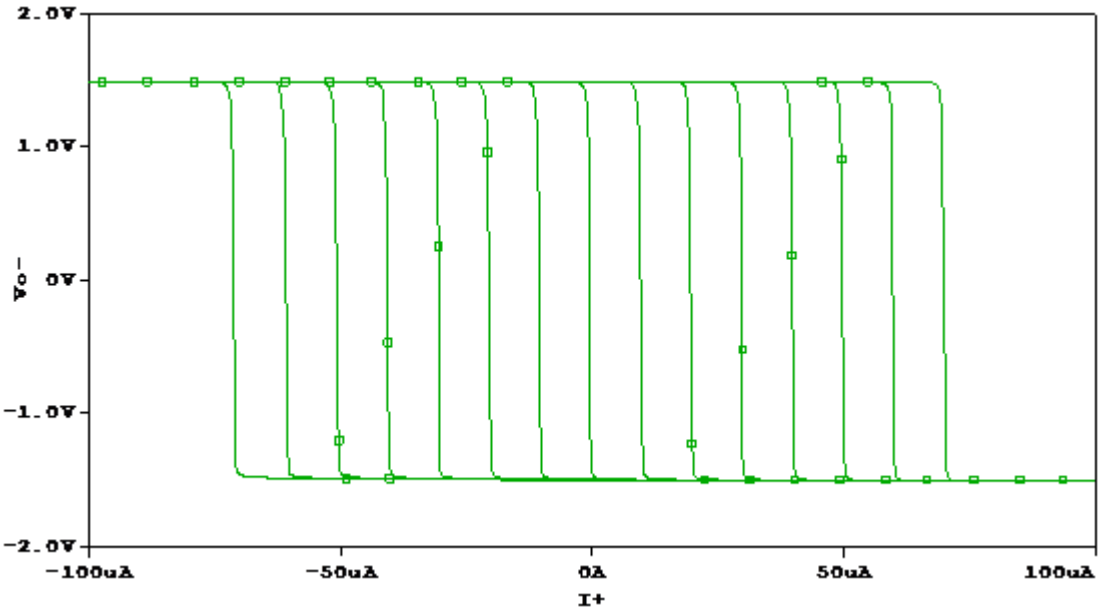


Fig. 2.6b Inverting DC Transfer Characteristics

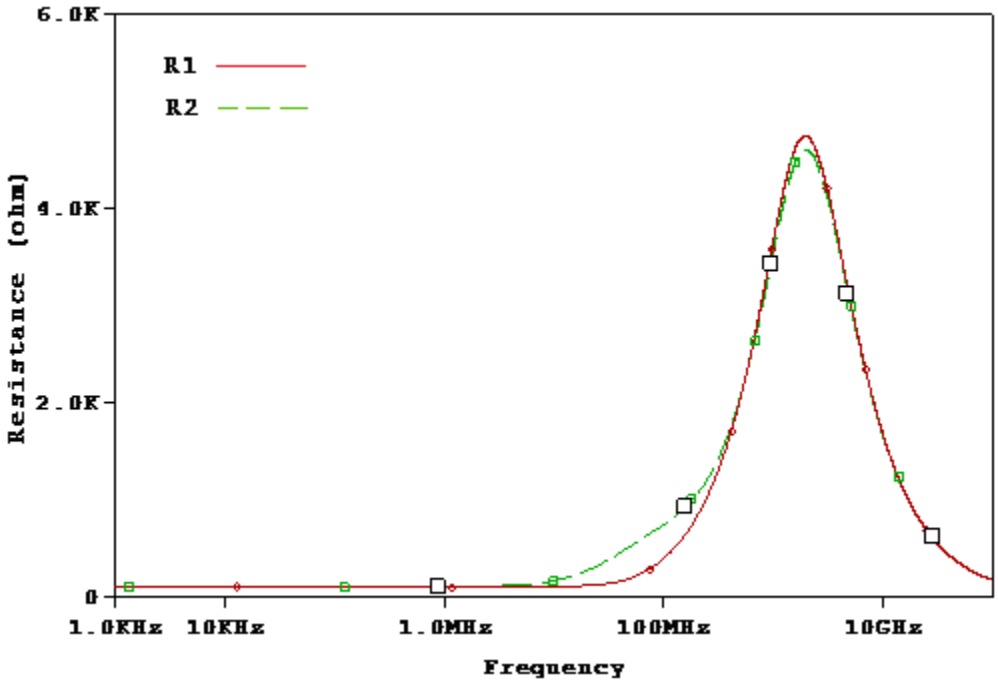


Fig. 2.7 Input Resistances of Differential OTRA

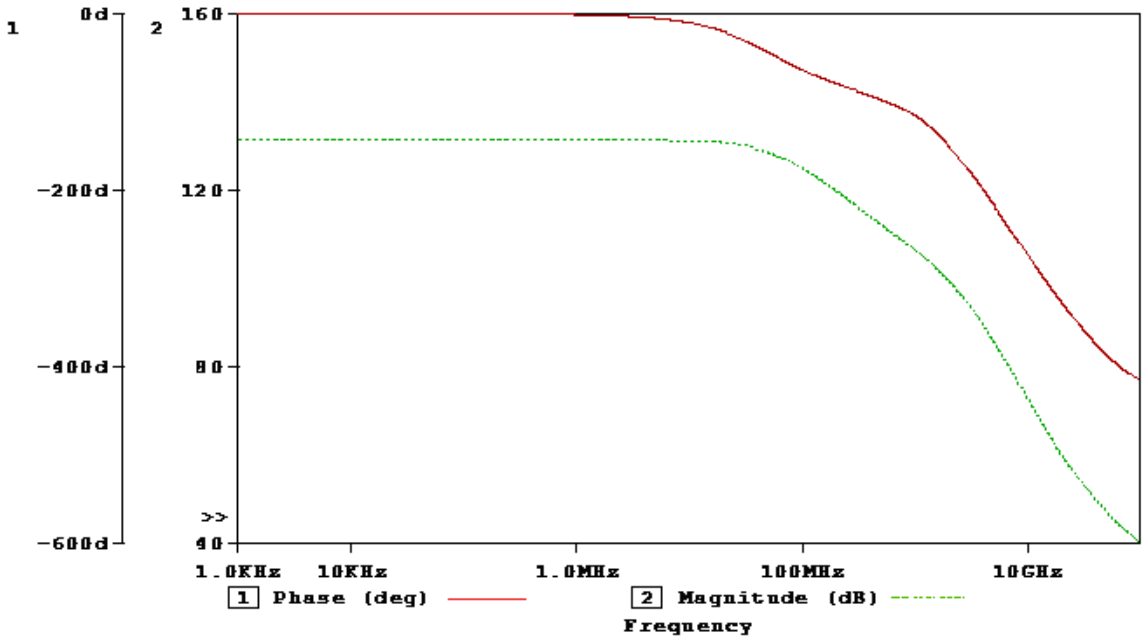


Fig. 2.8 Frequency Response of Differential OTRA

Chapter-3

Time Domain Analysis of Second Order System

As time is the independent variable in most of the control systems, time domain analysis is a usual practice for evaluating the system. In this analysis, a reference input signal is applied to the system under test, and performance of the system is evaluated by analyzing system response in time domain [1].

In this chapter, standard second order system and its unit step response is discussed for various conditions of damping ratio. Time domain specifications are defined, which will be useful for evaluation of Controller circuits. Also, a second order Low Pass Filter is proposed and its step response is analyzed and simulation results are depicted. This LPF will be helpful in observing the effect of controllers on second order system.

3.1 Standard Second Order System

Standard transfer function of the second order control system is given as:

$$T(s) = \frac{C(s)}{R(s)} = \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{3.1}$$

where, ω_n = natural frequency of oscillations

ξ = damping ratio or damping factor

Fig. 3.1 shows a standard form of a second order system in closed loop form.

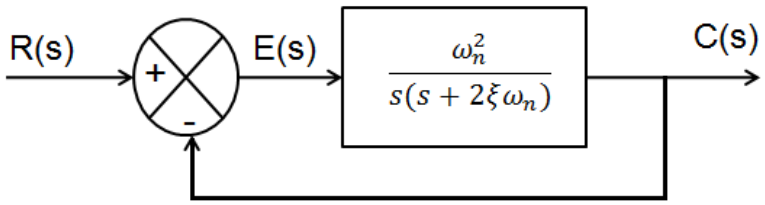


Fig. 3.1 Second Order System

The transient response of any system depends on the poles of transfer function T(s) [41]. The roots of denominator polynomial in s of *T(s)* are poles of transfer function. Thus denominator polynomial of T(s), given by:

$$D(s) = s^2 + 2\xi\omega_n s + \omega_n^2 \tag{3.2}$$

is known as the characteristic polynomial of the system and D(s) = 0 is known as characteristic equation of the system. The poles of T(s), or, the roots of characteristic equation

$$s^2 + 2\xi\omega_n s + \omega_n^2 = 0$$

$$s_{1,2} = -\xi\omega_n \pm \omega_n\sqrt{(\xi^2 - 1)}$$

If $\xi<1$

$$s_{1,2} = -\xi\omega_n \pm j\omega_n\sqrt{(1 - \xi^2)} = -\xi\omega_n \pm j\omega_d \tag{3.3}$$

where, ω_d is damped natural frequency of the system.

For

$\xi<1$, system is under damped

$\xi>1$, system is over damped and roots are real

$\xi = 1$, system is critically damped and roots are real & equal.

3.2 Unit Step Response of Second Order System

For unit step response, R(s) = 1/s, from eq. 3.1

$$C(s) = T(s).R(s) = \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2}.\frac{1}{s}$$

On solving it gives

$$C(t) = 1 - \frac{e^{\xi\omega_n t}}{\sqrt{1-\xi^2}}\sin(\omega_d t + \Phi) \tag{3.4}$$

where,

$$\Phi = \tan^{-1}\frac{\sqrt{1-\xi^2}}{\xi}$$

This response is plotted in Fig. 3.2. The response is oscillatory and as $t \rightarrow \infty$, it approaches unity.

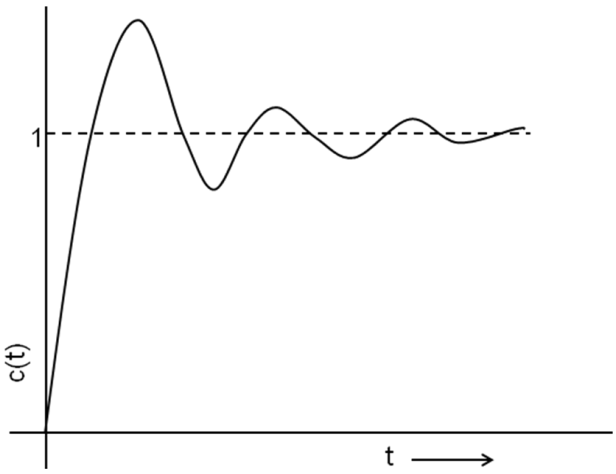


Fig. 3.2 Step Response of An Underdamped Second Order System

If ξ = 1, the two roots of the characteristic equations are $s_1 = s_2 = -\omega_n$ and response is given by

$$C(s) = T(s).R(s) = \frac{\omega_n^2}{(s+\omega_n)^2}.\frac{1}{s}$$

And

$$C(t) = 1 - e^{-\omega_n t} - t\omega_n e^{-\omega_n t} \qquad (3.5)$$

This is plotted in Fig. 3.3.

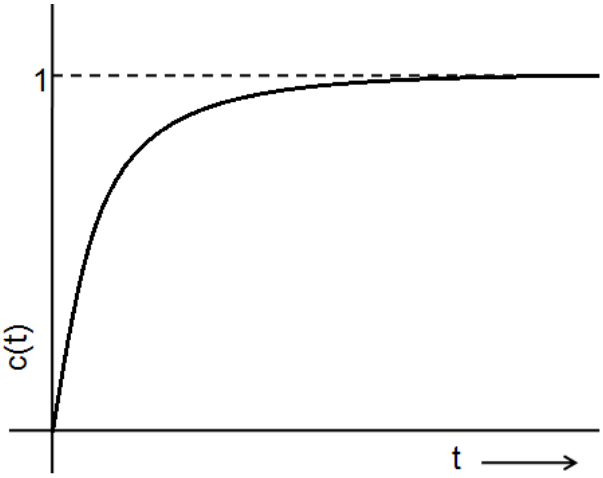


Fig.3.3 Response of A Critically Damped Second Order System

With increase in damping factor, ξ from a value less than to unity, oscillations decrease and just disappear [41]. If ξ increases beyond unity, roots of the characteristic equation become real and negative and hence, response approaches unity in an exponential way.

This response is known as over-damped response and is shown in Fig. 3.4.

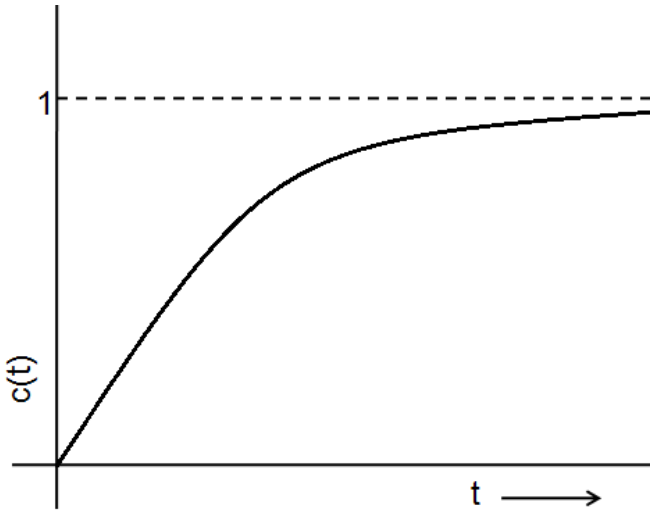


Fig. 3.4 Step Response of an Over-damped Second Order System

3.3 Time Domain specifications

Time domain system performance is measured in terms of following qualities [41].

1. Time it takes to respond to input.
2. Time it takes to reach desired output.
3. Error between desired and actual output.
4. Oscillations around desired output.

For designing any system, certain design specifications are given based on underdamped step response of second order system as shown in Fig. 3.5.

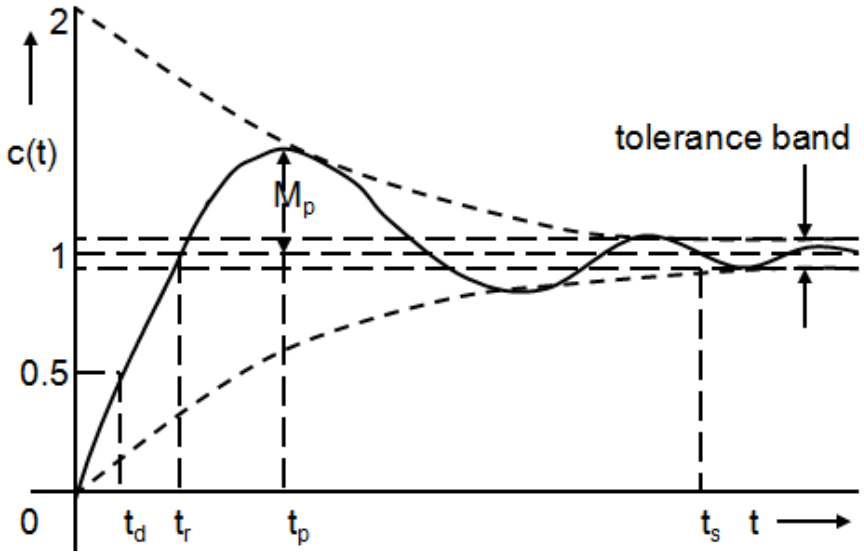


Fig. 3.5 Time Domain Specifications of a Second Order System

The design specifications are [1, 41-42]:

1. *Delay time, t_d:* It is the time taken by the output response to reach 50% of the steady state value for the first time. For second order system it is given by:

$$t_d = \frac{1+0.7\xi}{\omega_d} \tag{3.6}$$

2. *Rise time, t_r:* It is the time taken by the output response to rise from 10% to 90% of its final value and for a second order system is given by:

$$t_r = \frac{\prod - \Phi}{\omega_d} = \frac{\prod - \cos^{-1}\xi}{\omega_n\sqrt{1-\xi^2}} \tag{3.7}$$

3. *Peak time, t_p:* Time at which the output response attains its maximum value is called peak time. For second order system it is given by:

$$t_p = \frac{\prod}{\omega_d} = \frac{\prod}{\omega_n\sqrt{1-\xi^2}} \tag{3.8}$$

4. *Peak overshoot M_p:* It is defined as the difference between the peak value of response and the steady state value. It is usually expressed in percent of the steady state value. If the peak time is t_p, peak overshoot percentage is given by,

   Peak overshoot percentage, $M_p = \frac{c(t_p) - c(\infty)}{c(\infty)} \times 100$

   For second order system it is given by:

$$M_p = e^{-\prod\xi/\sqrt{1-\xi^2}} \times 100 \tag{3.9}$$

5. *Settling time t_s:* It is the taken by the output response to reach and remain within a specified tolerance limits (usually ± 2% or ± 5%) around the steady state value. For second order system it is given by:

$$t_s = \frac{4}{\xi\omega_n}, \quad \text{for } \pm 2\% \tag{3.10a}$$

$$t_s = \frac{3}{\xi\omega_n}, \quad \text{for } \pm 5\% \tag{3.10b}$$

6. *Steady state error e_{ss}:* It is the difference between desired and actual output as $t \to \infty$ or under steady state conditions.

$$e_{ss} = \lim_{t\to\infty}[r(t) - c(t)] = \lim_{s\to 0} sR(s)\frac{1}{1+G(s)H(s)} \tag{3.11}$$

3.4 Proposed Second Order Low Pass Filter

To verify the theoretical analysis of various controller circuits a second order Low pass filter is proposed and is shown in Fig. 3.6. It is designed using two differential OTRAs, two capacitors and five resistors. It is based on cascaded connection of the subtractor and the second order universal filter presented in [43]. From the Fig.3.6, the ratio V_o/V'_1 can be expressed as

$$V_1' = \frac{R_b}{R_a}(V_i - V_o) \tag{3.12a}$$

$$\frac{V_0(s)}{V_1'(s)} = \frac{G_1^{\,2}}{sC_2(G_1 + sC_1)} \tag{3.12b}$$

From equations 3.12a and 3.12b the transfer function of the LPF can be derived as

$$\frac{V_0(s)}{V_i(s)} = \frac{KG_1^{\,2}}{s^2C_1C_2 + sC_2G_1 + KG_1^2} \tag{3.13}$$

where, $K = \frac{R_b}{R_a}$

On comparing with the standard equation of second order system, eq. 3.1, it is seen,

$$\omega_n = G_1\sqrt{\frac{K}{C_1C_2}} \text{ and } \xi = \frac{1}{2\sqrt{K}} \tag{3.14}$$

Hence,

$$\omega_d = \frac{G_1}{2}\sqrt{\frac{4K-1}{C_1C_2}} \tag{3.15}$$

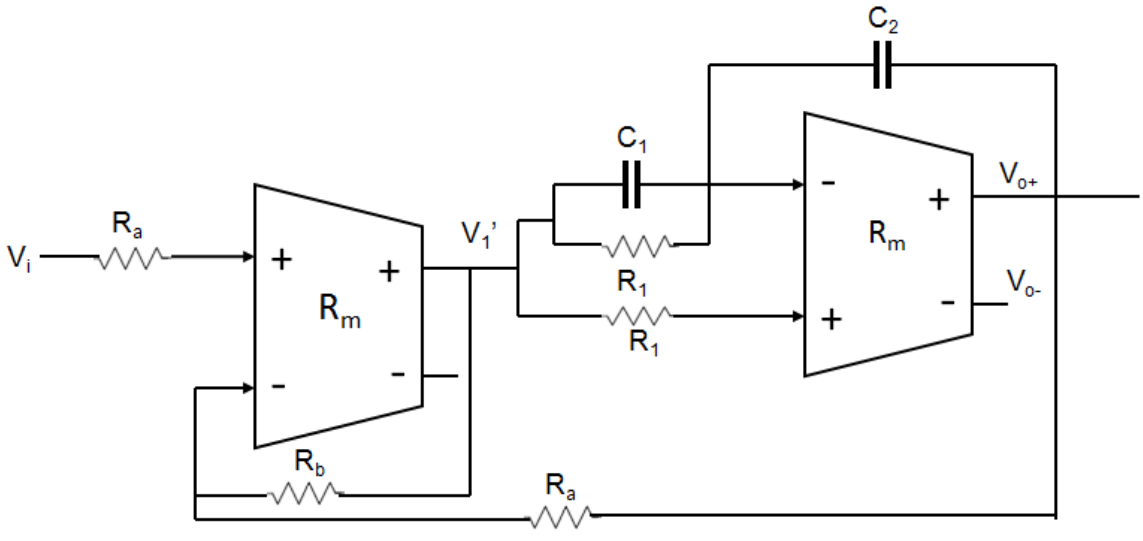


Fig. 3.6 Proposed Second Order Low Pass Filter

3.5 Simulation Results of Second Order LPF

For simulation of proposed second order low pass filter, differential OTRA simulated in 2nd chapter is used as an active component and values of passive element for the filters are selected as $R_a=R_b=20k\Omega$, $R_1=2k\Omega$, and $C_1= C_2=20pF$ which result in

$$\frac{V_0(s)}{V_i(s)} = \frac{6.25*10^{14}}{s^2+25*10^6 s+6.25*10^{14}} \quad (3.16)$$

$f_n = 3.98\ MHz,\ \xi = 0.5\ and\ f_d = 3.45\ MHz$

For time domain analysis a step signal of 50mV is applied and the simulated response is shown in Fig. 3.7 and the frequency response is shown in Fig. 3.8. Results are tabulated in table 3.1 and can be described as follow. Rise time of the system is 140ns and settling time is 303ns. Percentage of overshoot is 19.37% and cutoff bandwidth is 2.4MHz. Fig. 3.9 shows the effect of damping ratio, ξ on the step response of the second order LPF which follows the theoretical concept i.e. with the increase in damping ratio, ξ oscillations are decreasing.

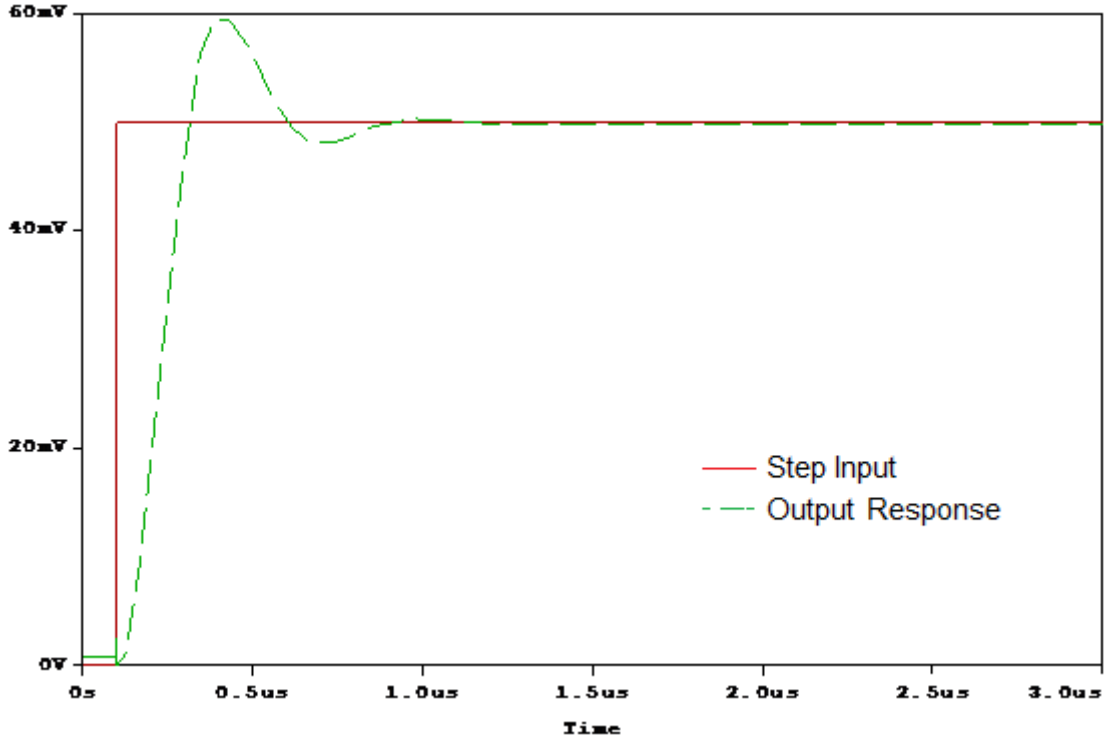


Fig. 3.7 Step Response of the Proposed Second Order LPF

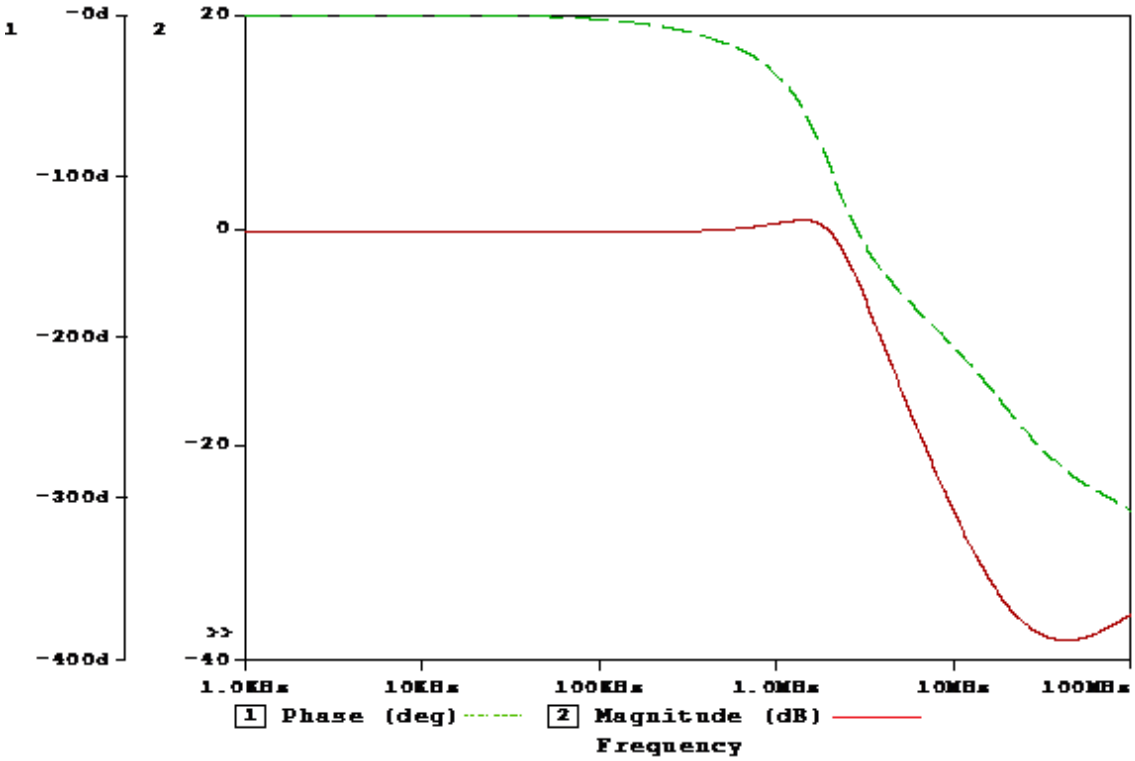


Fig. 3.8 Frequency Response of the Proposed Second Order LPF

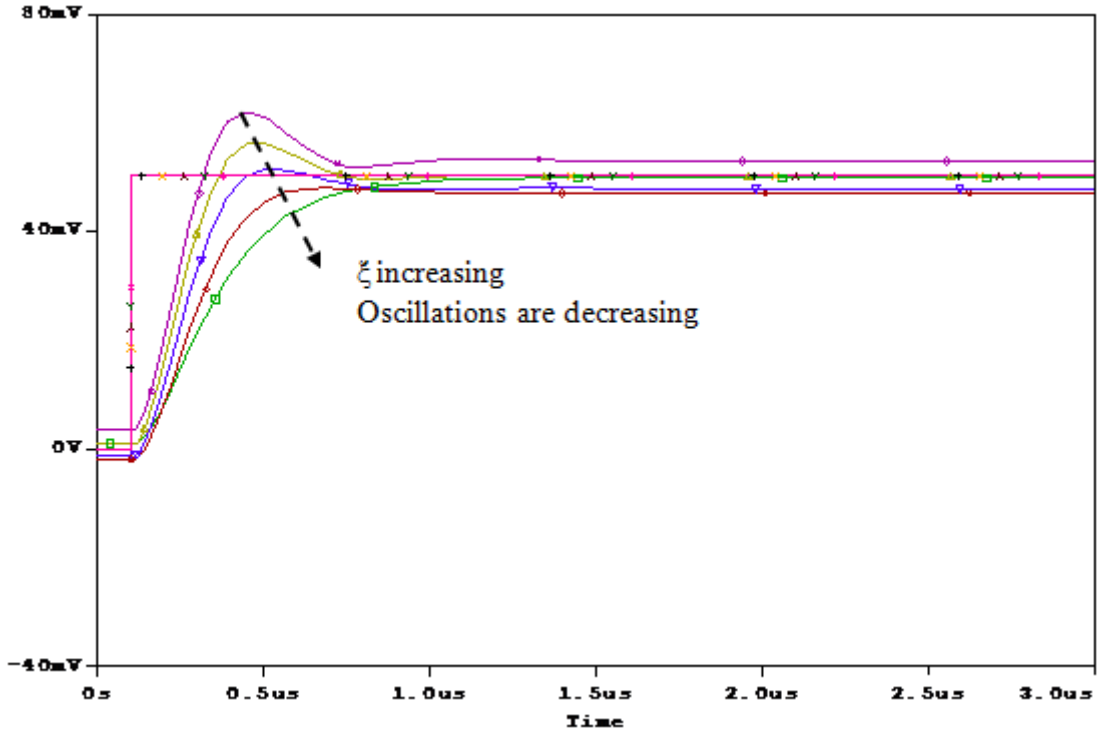


Fig. 3.9 Step Response of The Second Order LPF with varying ξ

Table 3.1 Simulation results of the Proposed Second Order LPF

Parameters	*Theoretical Values*	*Observed Values*
Overshoot (%)	16.30	19.37
Peak Voltage (V)	58.15m	59.49m
Rise time (seconds)	96.74n	140.17n
Settling Time (seconds)	240n	302.89n
Cutoff BW (-3dB) (Hz)	5.06M	2.41M

Chapter-4

PROPOSED CONTROLLERS

The performance of any control system can be improved by using different controllers in it. These controllers introduce poles and zeros for making the system response as desired. Major performance specifications are time response, steady state accuracy and stability. A **controller** is a device which monitors and modifies the operational conditions of a given dynamical system. The operational conditions are typically referred to as output variables of the system which can be modified by adjusting certain input variables.

In this chapter, classical controllers namely proportional (P), proportional-derivative (PD), Proportional Integrator (PI) and Proportional Integral and Derivative (PID), are discussed which is followed by their OTRA based realization. MOS-C implementations of all the controllers are also given which will help improve the chip area used in integration. Finally influence of controllers on performance of a second order system is also discussed.

4.1 Proportional Controller

4.1.1 Introduction

In proportional controller actuating signal, U(s) depends on the instantaneous value of the control error E(s) [42]. A proportional controller can control any stable plant, but it provides limited performance and nonzero steady state errors. This latter limitation is due to the fact that its frequency response is bounded for all frequencies. Fig. 4.1shows the block diagram of second order unity feedback control system using P-controller.

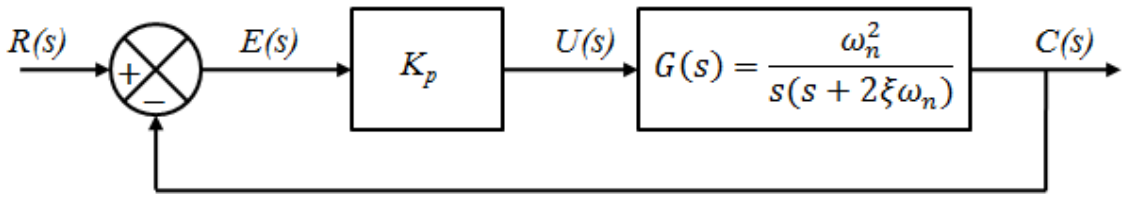


Fig. 4.1 Control System with P-controller

Mathematically,

$$U(s) = K_p E(s) \tag{4.1}$$

So, Transfer function

$$G_C(s) = K_p$$

where, K_p is constant of proportionality.

4.1.2 P-Controller with Second order system

From the Fig. 4.1 the transfer function of the complete system is,

$$T_p(s) = \frac{K_p \omega_n^2}{s^2 + 2\xi\omega_n s + K_p \omega_n^2} \tag{4.2}$$

On comparing it with standard second order equation, eq. 3.1

$$\omega_n' = \omega_n \sqrt{K_p}$$

$$\xi' = \frac{\xi}{\sqrt{K_p}}$$

From the above comparison, it is clear that natural frequency, ω_n increases while damping ratio, ξ decreases by $\sqrt{K_p}$, this results in following merits and demerits:

- Rise time reduces.
- Peak time reduces.
- Maximum peak overshoot increases.
- Does not affect settling time.
- Reduces steady state error.

4.1.3 OTRA based P-Controller

Proportional controller is shown in the Fig. 4.2. The circuit is basically a voltage controlled voltage source.

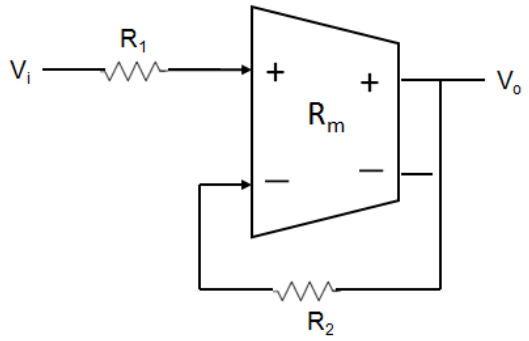


Fig. 4.2 OTRA based P-Controller

For Ideal case, $R_m = \infty$

$$I_p = I_n$$

So, Transfer function will be

$$K_p = \frac{V_0(s)}{V_i(s)} = \frac{R_2}{R_1} \qquad (4.3)$$

These parameters can be electronically tuned by implementing the linear passive resistors using MOS transistors operating in non-saturation region. The resistance value may be adjusted by appropriate choice of gate voltages. The resistors connected to the input terminals of OTRA can easily be implemented using MOS transistors with complete non-linearity cancellation [6]. Fig. 4.4 shows a typical MOS implementation of resistance connected between negative input and output terminals of OTRA.

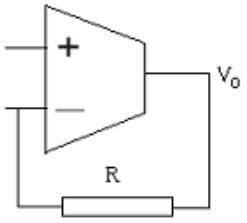
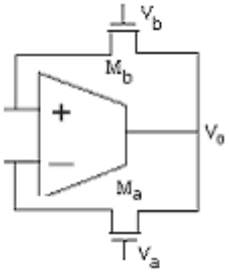
Resistor connected between V_n and V_0	Equivalent MOS-C implementation
	

Fig. 4.3 MOS implementation of a Linear resistance

The equivalent resistance value is given as

$$R = {}^{1}\!/_{\mu_n C_{OX}({}^{W}\!/_{L})\,(V_a - V_b)} \qquad (4.6)$$

where μ_n, C_{ox}, W and L are electron mobility, oxide capacitance per unit gate area, effective channel width, and effective channel length respectively which may be expressed as

$$\mu_n = \frac{\mu_0}{1+\theta(V_{GS}-V_T)}$$

$$Cox = {}^{\varepsilon_{ox}}\!/_{T_{ox}}$$

$$W = W_{drawn} - 2W_D$$

$$L = L_{drawn} - 2L_D$$

V_a and V_b are the gate voltages and other symbols have their usual meaning. Fig. 4.4 shows the MOS-C implementation of the circuit of Fig. 4.2.

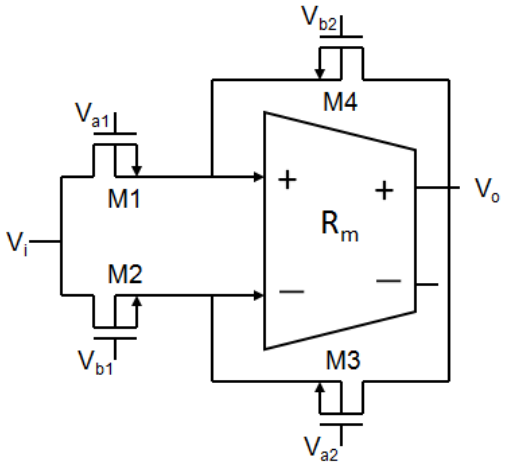


Fig. 4.4 MOS–C realization of P-Controller

4.1.4 Non-ideality Analysis

Taking the effect of the finite transresistance gain, R_m of OTRA into account K_p is given by:

$$K_p = \frac{R_2}{R_1} \epsilon\,(s) \qquad (4.4)$$

where,

$$\epsilon\,(s) = \frac{1}{1+{}^{R_2}/_{R_m}}$$

Using single pole model [2],

$$R_m = \frac{R_O}{1+{}^{s}/_{\omega_o}} \qquad (4.5a)$$

where, R_O is dc transresistance gain.

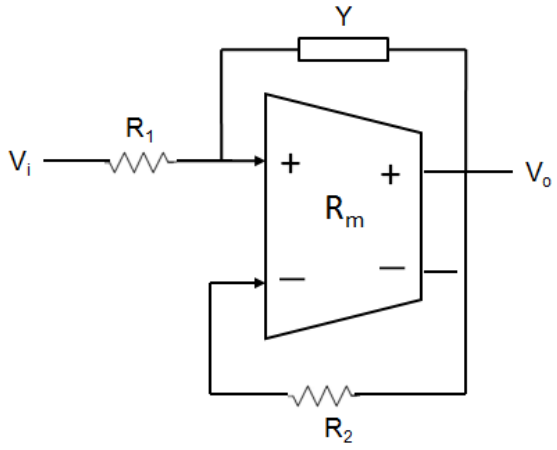


Fig.4.5 P-Controller with Compensation

For high frequency applications the trans-resistance gain, reduces to

$$R_m \approx \frac{1}{sC_p} \qquad (4.5b)$$

where,

$$C_p = \frac{1}{R_o \omega_o}$$

Now from Fig. 4.5

$$\in (s) = \frac{1}{1+R_2 (sC_p - Y)} \qquad (4.6)$$

by choosing: Y = s C_p , ∈(s) reduces to its ideal value of unity. Therefore, complete passive compensation of the P controller can be achieved by using a single capacitor connected between the output terminal and the non-inverting terminal.

4.2 PD Controller

4.2.1 Introduction

In PD controller the actuating signal U(s) is sum of proportional to the error signal E(s) and its rate of change. Therefore if the error is large or changing rapidly, the effect of the control will be an increase in the system response. It is a fast mode which ultimately disappears in the presence of constant errors. It is also known as predictive mode as it depends on the error trend. The main limitation of the derivative mode, viewed in isolation, is its tendency to yield large control signals in response to high frequency control errors, such as errors induced by set point changes or measurement noise [42]. Fig. 4.6 shows the block diagram of second order unity feedback control system using PD-controller.

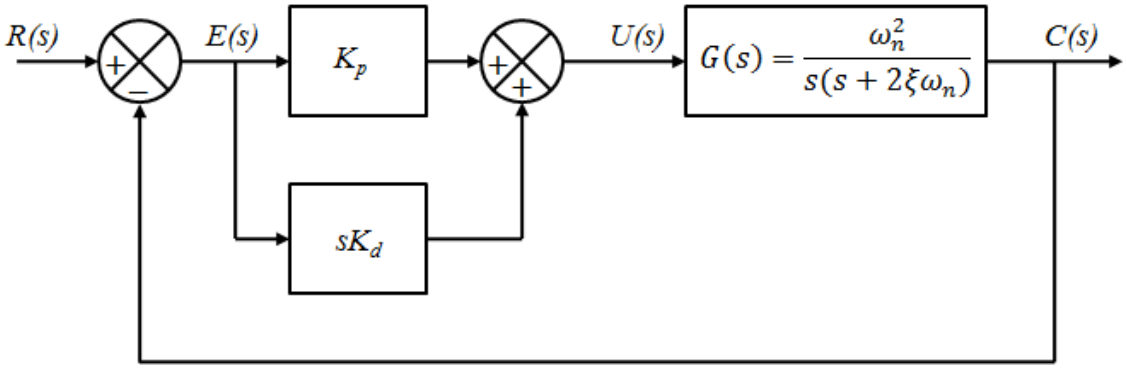


Fig. 4.6 Control System with PD-controller

The controller is a proportional-derivative (PD) type with the transfer function.

$$G_c(s) = K_p + K_d\, s \tag{4.7}$$

where, K_p and K_d are the proportional and derivative constants, respectively.

4.2.2 PD-Controller with Second order system

From the Fig. 4.6 the transfer function of the complete system can be calculated as,

$$T_{pd}(s) = \frac{(K_p + sK_d)\omega_n^2}{s^2 + (2\xi\omega_n + K_d\omega_n^2)s + K_p\omega_n^2} \tag{4.8}$$

On comparing it with standard second order equation, eq. 3.1

For $K_p = 1$,

$$\omega_n' = \omega_n$$

$$\xi' = \xi + \frac{K_d\omega_n}{2}$$

From the above results, it is clear that natural frequency, ω_n does not change while damping ratio, ξ increases, this result in following merits and demerits:

- Damping improves and peak overshoot reduces.
- Rise time reduces.
- Peak time reduces.
- Settling time reduces.
- Does not affect steady state error.

4.2.3 OTRA based Proposed PD-Controller

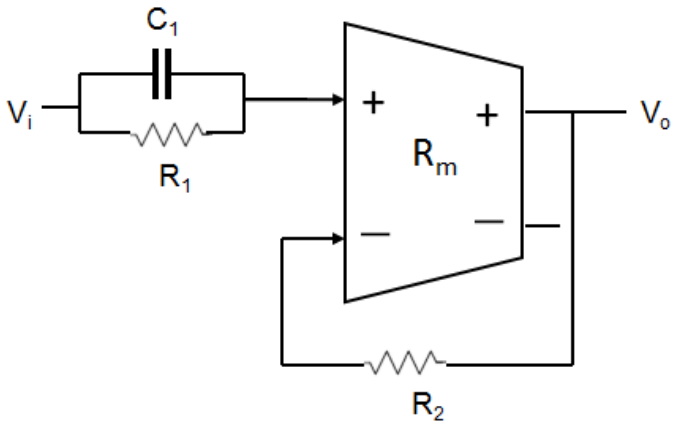


Fig. 4.7 OTRA based Proposed PD Controller

The proposed PD-Controller is shown in Fig. 4.7. Routine analysis of this controller, using terminal equations of OTRA and assuming OTRA to be ideal, i.e. $R_m = \infty$, results in

$$V_i\left(\frac{1}{R} + sC\right) = \frac{V_o^+}{R_f}$$

$$\frac{V_o^+}{V_i} = \frac{R_f}{R} + sCR_f \qquad (4.9)$$

comparison of equation 4.7 with equation 4.9 gives

$$K_P = \frac{R_f}{R}, \qquad K_D = CR_f \qquad (4.10)$$

From 4.10 it is clear that by varying R, K_p value can be adjusted independent of K_d and by simultaneous variation of R_f and R, K_d can be independently controlled. Fig. 4.8 shows the MOS-C implementation of the circuit of Fig. 4.7.

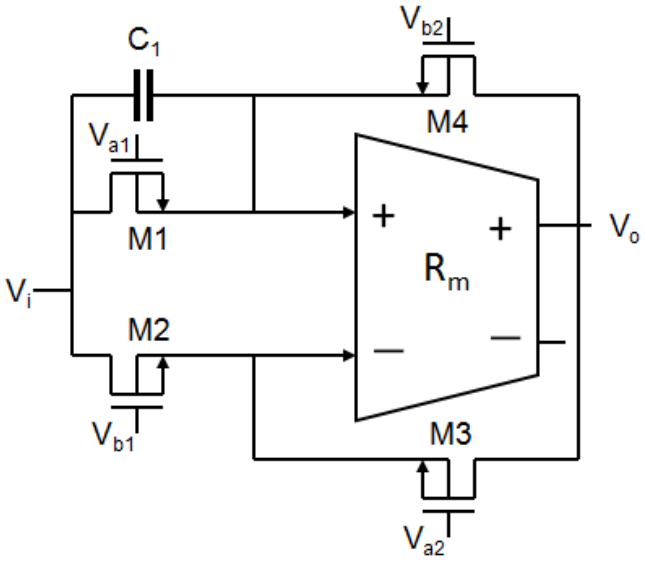


Fig. 4.8 MOS-C realization of Proposed PD Controller

4.2.4 Non-ideality Analysis

In this section the effect of finite trans-resistance gain (R_m) on PD controller is considered and for high frequency applications passive compensation is employed. Ideally, R_m is assumed to approach infinity. However, practically R_m is a frequency dependent finite value.

For low frequency applications the trans-resistance gain, reduces to

$$R_m \approx R_o$$

Taking this effect into account eq. 4.9 modifies to

$$\frac{V_o+}{V_i} = \left(R_o \parallel R_f\right)\left(\frac{1}{R} + sC\right) \qquad (4.11)$$

Since, $R_o >> R_f$

$R_o || R_f \approx R_f$

Hence eq. 4.11 reduces to eq. 4.9. The effect of R_o can thus be eliminated by choosing $R_f << R_o$.

For high frequency applications the trans-resistance gain, reduces to

$$R_m(s) \approx \left(\frac{1}{sC_p}\right)$$

Taking this effect into account eq. 4.9 modifies to

$$\frac{V_o+}{V_i} = \frac{R_f}{R(1+sC_pR_f)} + sC\frac{R_f}{1+sC_pR_f} \qquad (4.12)$$

For high-frequency applications, compensation methods must be employed to account for the error introduced in eq. 4.9. Considering the circuit shown in Fig. 4.9, eq. 4.12 modifies to

$$\frac{V_o+}{V_i} = \frac{R_f}{R(1+R_f(sC_p-sY))} + \frac{sCR_f}{1+R_f(sC_p-sY)} \qquad (4.13)$$

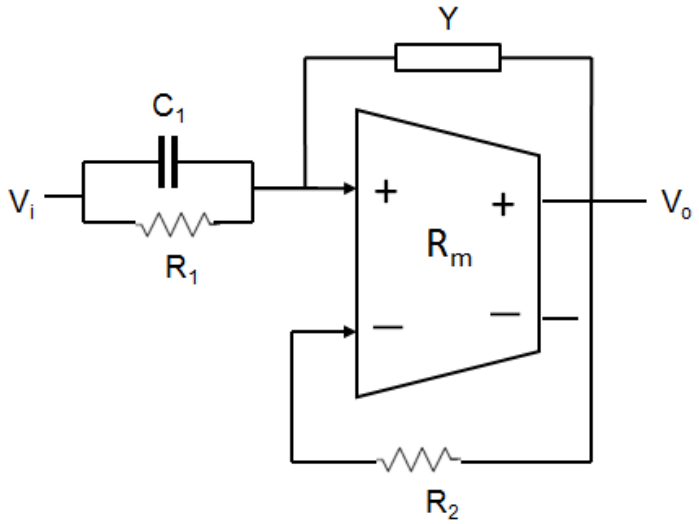


Fig. 4.9 Compensated PD Controller

By taking Y = sC_p, eq. 4.13 reduces to eq. 4.9. The effect of R_m can thus be eliminated by connecting a single capacitor between the non inverting terminal and the output as shown in Fig. 4.9. Thus passive compensation has achieved for both low as well as high frequency.

4.3 PI Controller

4.3.1 Introduction

In PI Controller, actuating signal drives the plant to be controlled with a weighted sum of the error signal and the integral of that value which implies that it is a slow reaction control mode. This characteristic is also evident in its low pass frequency response. The integral mode plays a fundamental role in achieving perfect plant inversion at $\omega = 0$. This forces the steady state error to zero in the presence of a step reference and disturbance. The integral mode, viewed in isolation, has two major shortcomings: its pole at the origin is detrimental to loop stability and it also gives rise to the undesirable effect (in the presence of actuator saturation) known as wind-up [42]. Fig. 4.10 shows the block diagram of second order unity feedback control system using PI controller.

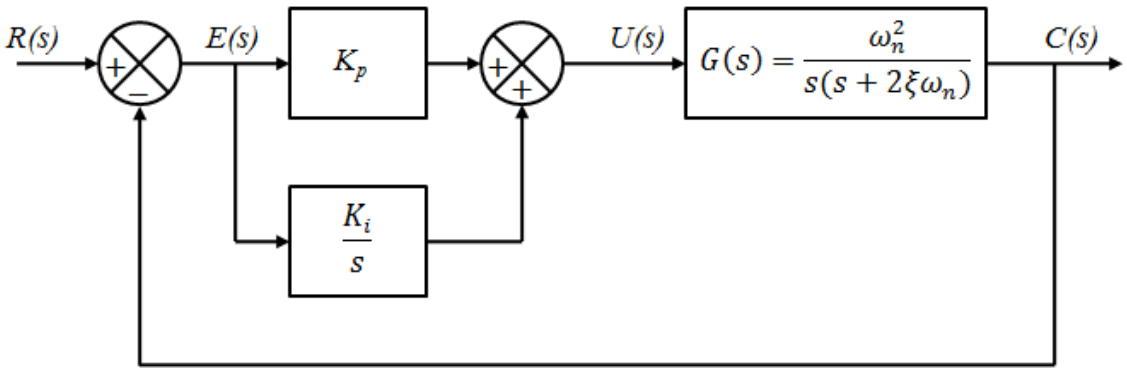


Fig. 4.10 Control System with PI-controller

The controller is a proportional-integrator (PI) type with the transfer function.

$$G_c(s) = K_p + \frac{K_i}{s} \qquad (4.14)$$

where, K_p and K_i are the proportional and integral constants, respectively.

4.3.2 PI-Controller with Second order system

From the Fig. 4.10 the transfer function of the complete system can be calculated as,

$$T_{pi}(s) = \frac{(K_i + sK_p)\omega_n^2}{s^3 + 2\xi\omega_n s^2 + K_p\omega_n^2 s + K_i\omega_n^2} \quad (4.15)$$

For $K_p = 1$, Error signal is given by

$$E(s) = R(s)\frac{s^2(s+2\xi\omega_n)}{s^3 + 2\xi\omega_n s^2 + \omega_n^2 s + K_i\omega_n^2} \quad (4.16)$$

And the steady state error is given by

For step input, $e_{ss} = 0$

For ramp input, $e_{ss} = 0$

For parabolic input, $e_{ss} = \frac{2\xi}{K_i\omega_n}$

Hence merits and demerits of PI-Controller can be described as

- It increases the type and order of the system.
- It improves steady state response by reducing the steady state error.
- Rise time increases

4.3.3 OTRA based Proposed PI-Controller

Proposed PI-Controller is shown in Fig. 4.11.

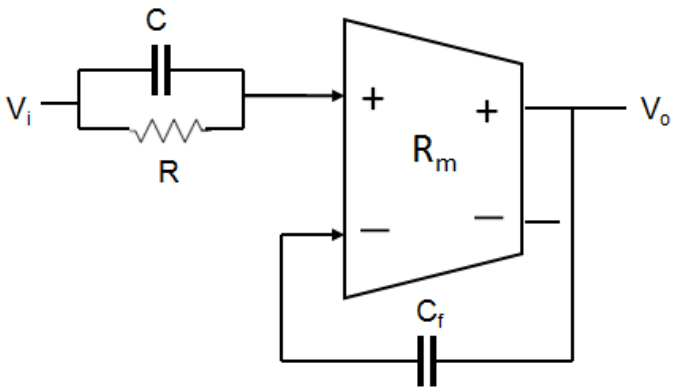


Fig. 4.11 OTRA based Proposed PI Controller

The routine analysis of this controller gives the following voltage transfer function

$$\frac{V_{o+}}{V_i} = \frac{C}{C_f} + \frac{1}{sC_fR} \quad (4.17)$$

On comparing equations 4.14 and 4.17

$$K_p = \frac{C}{C_f}, \qquad K_i = \frac{1}{C_fR} \quad (4.18)$$

From the above equation it is clear that by varying C, K_p value can be adjusted independent of K_i and by simultaneous variation of C_f and C, K_i can be independently controlled. Fig. 4.12 shows the MOS-C implementation of the circuit of Fig. 4.11.

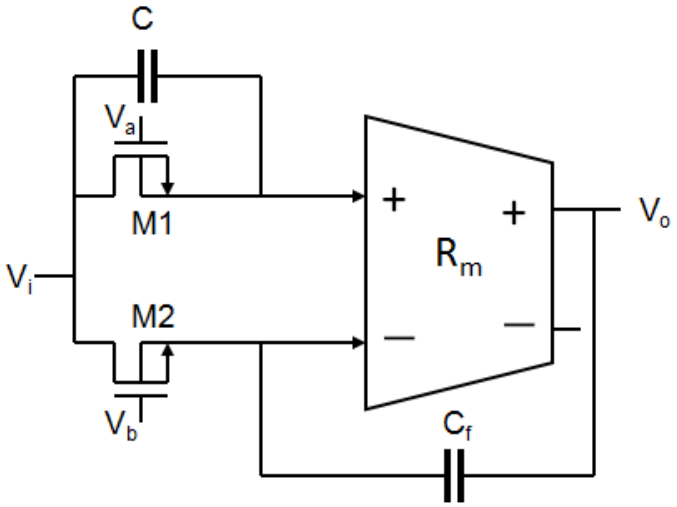


Fig. 4.12 MOS-C realization of Proposed PI Controller

4.3.4 Non-ideality analysis

Here, effect of finite trans-resistance gain (R_m) on PI controller is considered and passive compensation is employed.

Taking the effect of R_m into account, we get

$$\frac{V_o^+}{R_m} = V_i\left(\frac{1}{R} + sC\right) - sC_f V_o^+$$

Since

$$R_m = \frac{R_o}{1+sR_oC_o}$$

$$V_o^+\left(\frac{1}{R_o} + s(C_o + C_f)\right) = V_i\left(\frac{1}{R} + sC\right) \quad (4.19)$$

Since,

$$C_o \ll C_f$$

$$C_f + C_o \approx C_f$$

$$\therefore V_o^+\left(\frac{1}{R_o} + sC_f\right) = V_i\left(\frac{1}{R} + sC\right) \quad (4.20)$$

Now, for eliminating the effect of R_o, circuit is modified as shown in Fig. 4.13

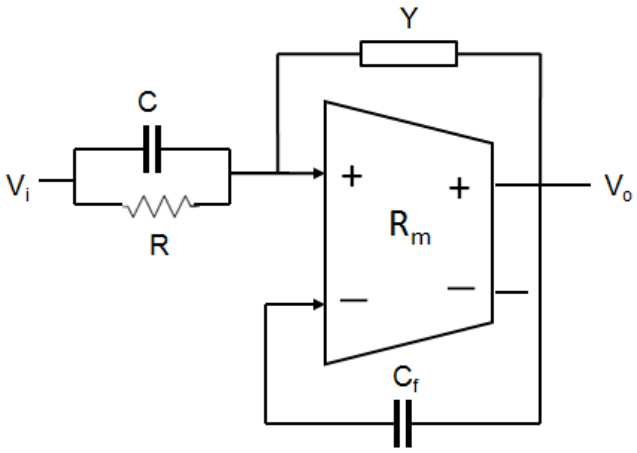


Fig. 4.13 Compensated PI Controller

Considering the circuit shown in Fig. 4.13, eq. 4.20 modifies to

$$V_o + \left(\frac{1}{R_o} + sC_f - Y\right) = V_i\left(\frac{1}{R} + sC\right) \tag{4.21}$$

By taking Y = $1/R_o$, eq. 4.21 reduces to eq. 4.17. Hence the effect of finite R_m is completely eliminated.

4.4 PID Controller

4.4.1 Introduction

The PD controller improves damping of the system, but the steady-state response is not affected. The PI controller improves the relative stability and the steady-state error at the same time, but the rise time is increased [1]. So, none of them alone is capable of achieving the complete improvement in performance of a system. This leads to the motivation of using a PID controller so that the best features of each of the PI and PD controllers are utilized. Fig. 4.14 shows the block diagram of second order unity feedback control system using PID controller.

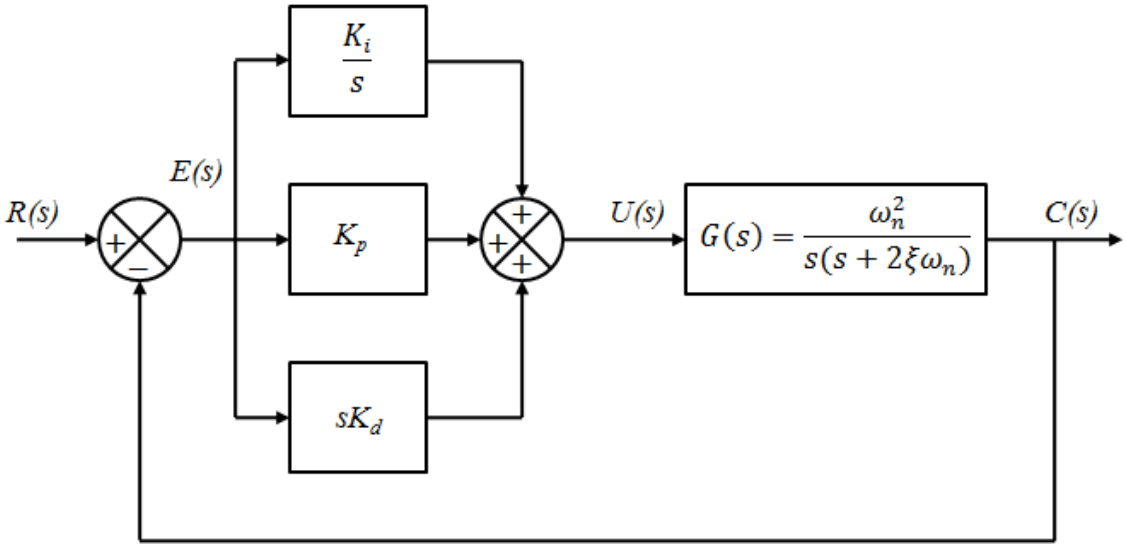


Fig. 4.14 Control System with PID-controller

Transfer function of PID Controller is given by

$$G_c(s) = K_p + K_d\, s + \frac{K_i}{s} \qquad (4.22)$$

where, K_p, K_d and K_i are the proportional, derivative and integral constants, respectively.

Advantages of PID controller:

- High speed.
- High accuracy.
- High stability.
- No offset problem.

4.4.2 OTRA based Proposed PID-Controller

Proposed PID-Controller is shown in Fig. 4.15.

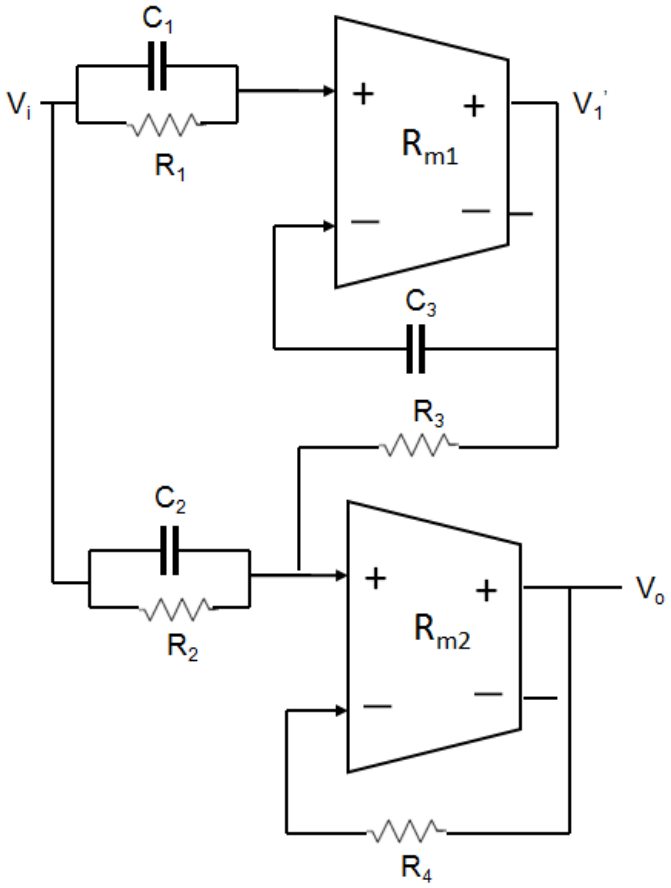


Fig. 4.15 OTRA based Proposed PID Controller

From Fig. 4.15 it is clear that PID is composed of PI and PD controllers. Here first OTRA works as PI controller while second is working as a PD controller as well as an adder. The analysis of the circuit reveals that

$$\frac{V_1'}{V_i} = \frac{C_1}{C_3} + \frac{1}{sC_3R_1} \tag{4.23}$$

$$V_o = V_i\left(\frac{R_4}{R_2} + sC_2R_4\right) + V_1'\frac{R_4}{R_3} \tag{4.24}$$

From eq. 4.23 & 4.24

$$\frac{V_0}{V_i} = \left(\frac{R_4}{R_2} + sC_2R_4\right) + \frac{R_4}{R_3}\left(\frac{C_1}{C_3} + \frac{1}{sC_3R_1}\right) \tag{4.25}$$

On comparing it with 4.22

$$K_p = \frac{R_4}{R_3} \times \frac{C_1}{C_3} + \frac{R_4}{R_2}, \quad K_d = C_2R_4 \quad \& \quad K_i = \frac{R_4}{R_3} \times \frac{1}{C_3R_1} \tag{4.26a}$$

Component choice of $R_4 = R_3$, $R_2 = \infty$, results in

$$K_p = \frac{C_1}{C_3}, \quad K_d = C_2R_4 \quad \& \quad K_i = \frac{1}{C_3R_1} \tag{4.26b}$$

For $R_4 = R_3$, $C_1 = 0$, we get

$$K_p = \frac{R_4}{R_2}, \quad K_d = C_2R_4 \quad \& \quad K_i = \frac{1}{C_3R_1} \tag{4.26c}$$

From the above equations it is clear that by varying R_2 or C_1 or both K_p can be adjusted independently, by variation of C_2 or simultaneous variation of R_4 & R_2 K_d can be varied independently, and K_i can be independently controlled by varying R_1 or simultaneously varying C_1 & C_3. Fig. 4.16 shows the MOS-C implementation of the circuit of Fig. 4.15.

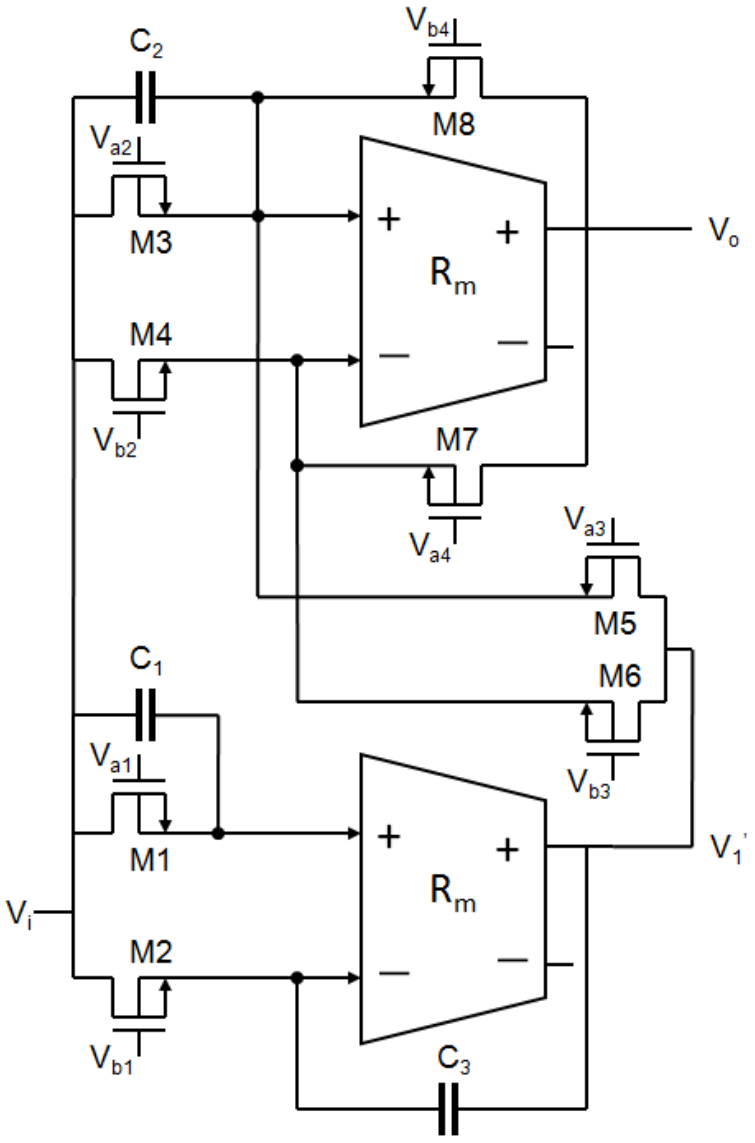


Fig. 4.16 MOS-C realization of Proposed PID Controller

Chapter-5

SIMULATION RESULTS

In order to verify the results of theoretical propositions, all controller circuits namely P, PD, PI and PID are simulated using PSICE program. 180nm, Level 7, CMOS process parameters provided by MOSIS (AGILENT) are used for simulation and supply voltages taken are ±1.5V. Further, to verify the influence of proposed circuits on second order system, a closed loop control system using proposed controllers and second order LPF is designed and simulated. The differential OTRA proposed in [9] is used as an active building block for all the controller circuits.

5.1 Simulation Results of P Controller

For the OTRA based P controller shown in Fig. 4.2, the values of the passive components are chosen as R_1=10K and R_2=20K. For time domain analysis, a 3mV, 2.5 MHz sinusoidal input voltage is applied. Both ideal and simulated results are presented in Fig. 5.1. Frequency domain characteristics are depicted in Fig. 5.2.

For MOS-C implemented P controller shown in Fig. 4.4 aspect ratios of the transistors used for implementing the resistances are listed in Table.5.1.

Table 5.1 Aspect ratios for MOS-C implementation of P Controller

Transistor	*W(µm)/L(µm)*
M1,M2	0.18µ/.54µ
M3,M4	0.18µ/1.08µ

Gate voltages are set as V_{a1}= V_{a2} = 1.2V and Vb1=0.59V, Vb2 =0.64V which result in resistance values as R_1 ≈10KΩ and R_2 ≈20KΩ. Fig. 5.3 shows the transient response and Fig. 5.4 shows frequency domain characteristics of MOS-C implementation of P controller.

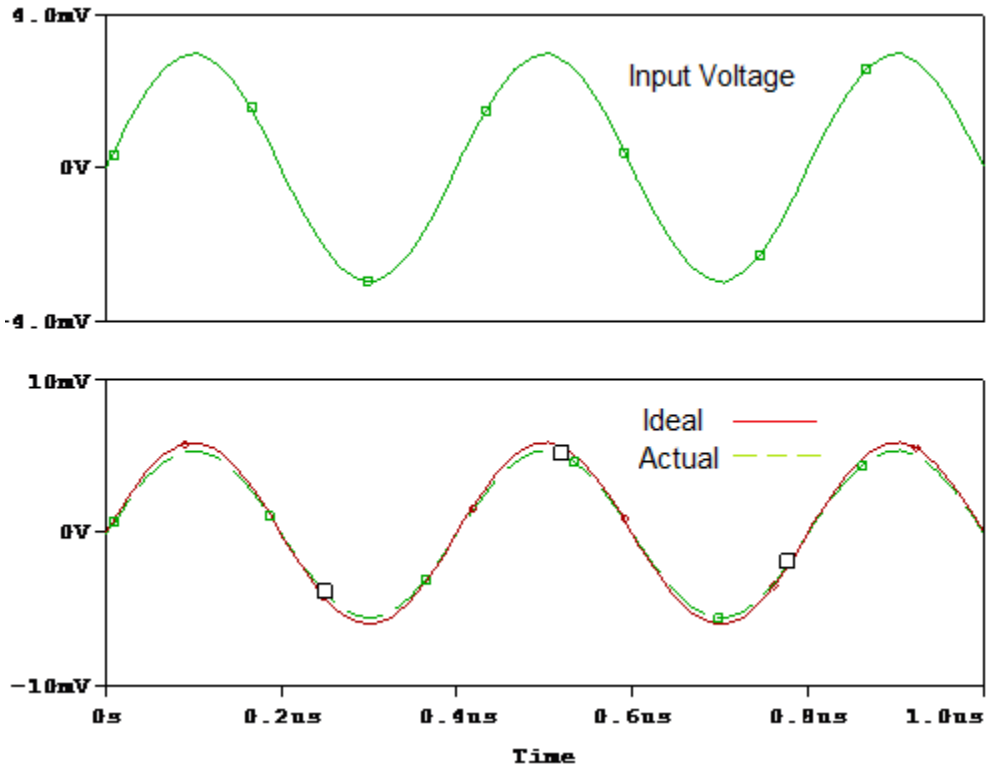


Fig. 5.1 Transient response of the P Controller

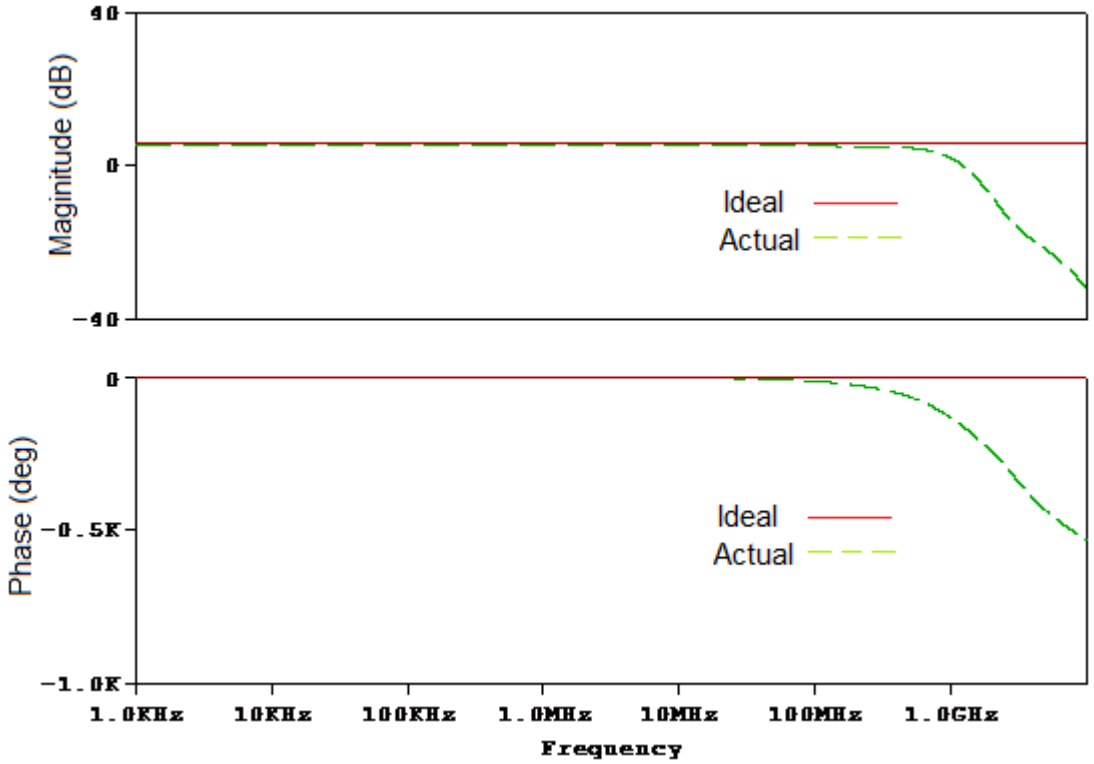


Fig. 5.2 Frequency and phase Response of P controller

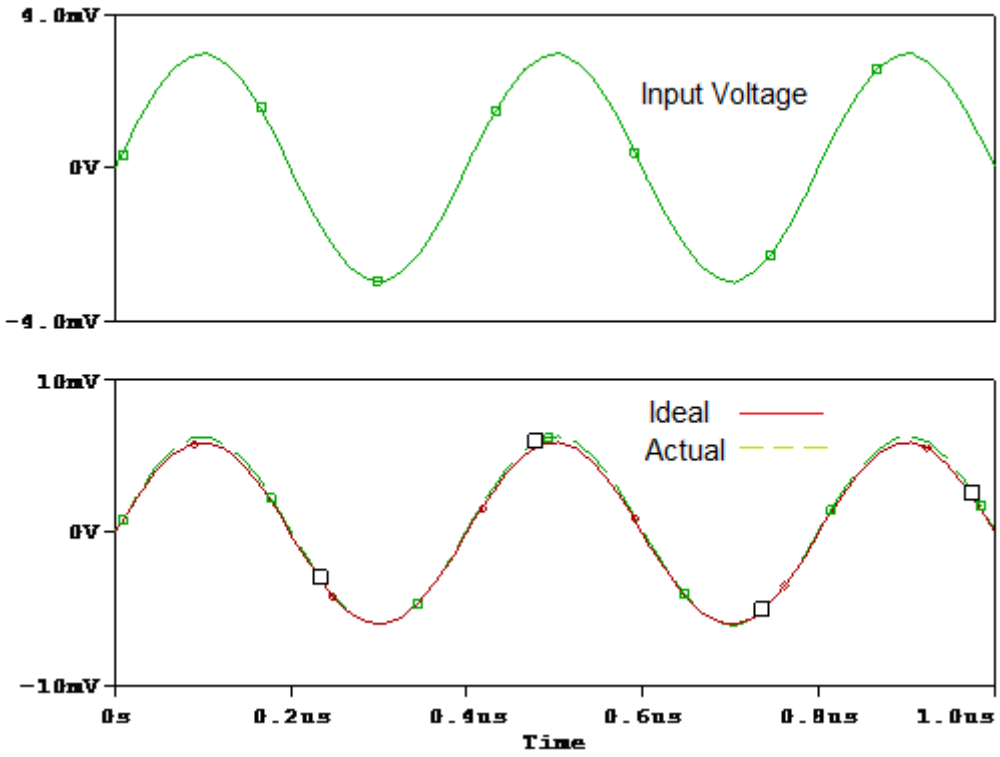


Fig. 5.3 Transient response of MOS-C implementation of P Controller

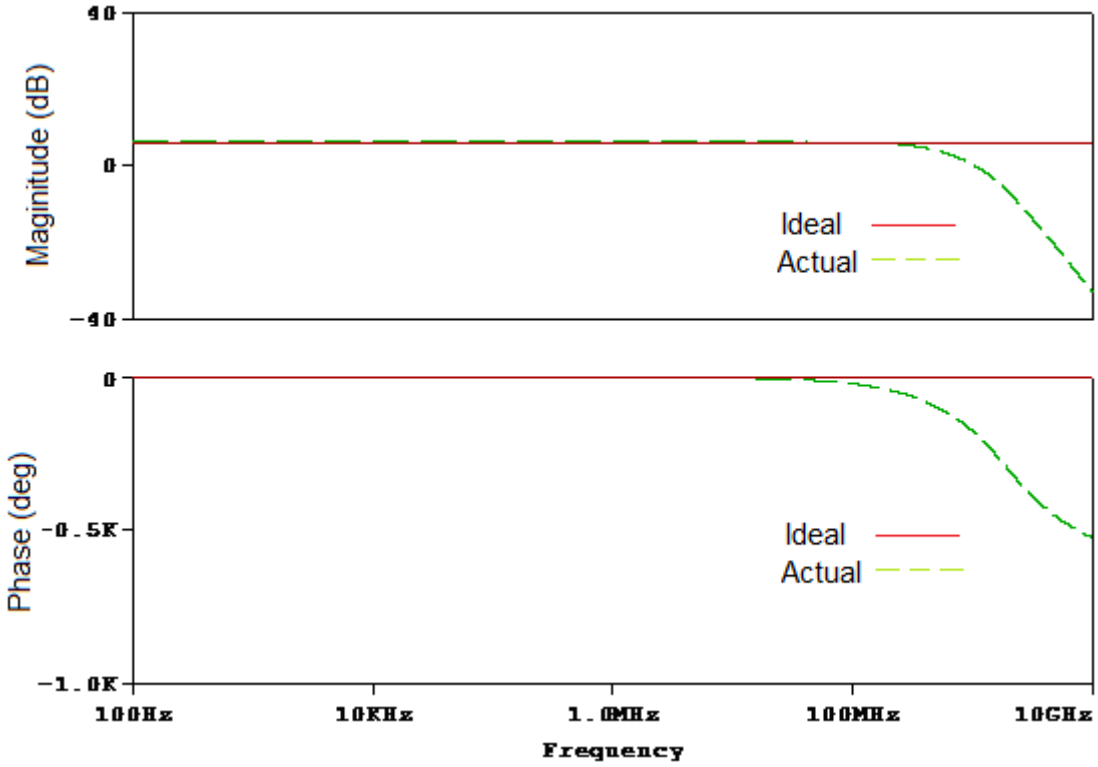


Fig. 5.4 Frequency and phase Response of MOS-C implementation of P controller

Fig. 5.5 shows a closed loop control system realized using the proposed P controller and a second order low-pass filter (LPF). Fig. 5.6a shows the step response of the LPF without P controller for a step input of 50mV whereas Fig.5.6b depicts the effect of P controller on step response of the closed loop system. Fig. 5.7 shows the effect of varying K_p on second order system and it is observed that with increase in K_p, rise time decreases while peak overshoot increases.

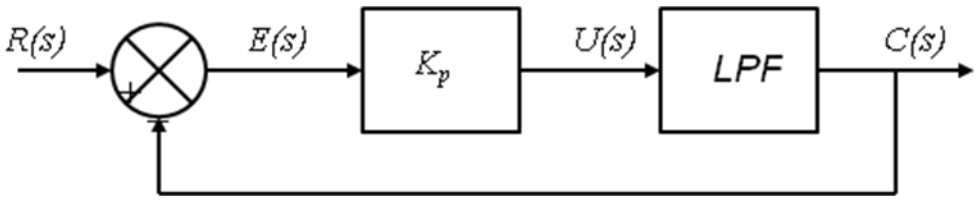


Fig. 5.5 Closed Loop Control System using P controller

Performance comparison of second order system with and without P controller is shown in Table. 5.2. It is clearly visible from table 5.2 that the response of the system has been improved with smaller rise time of 108.75ns, but Peak overshoot percentage is increased to 30.14%.

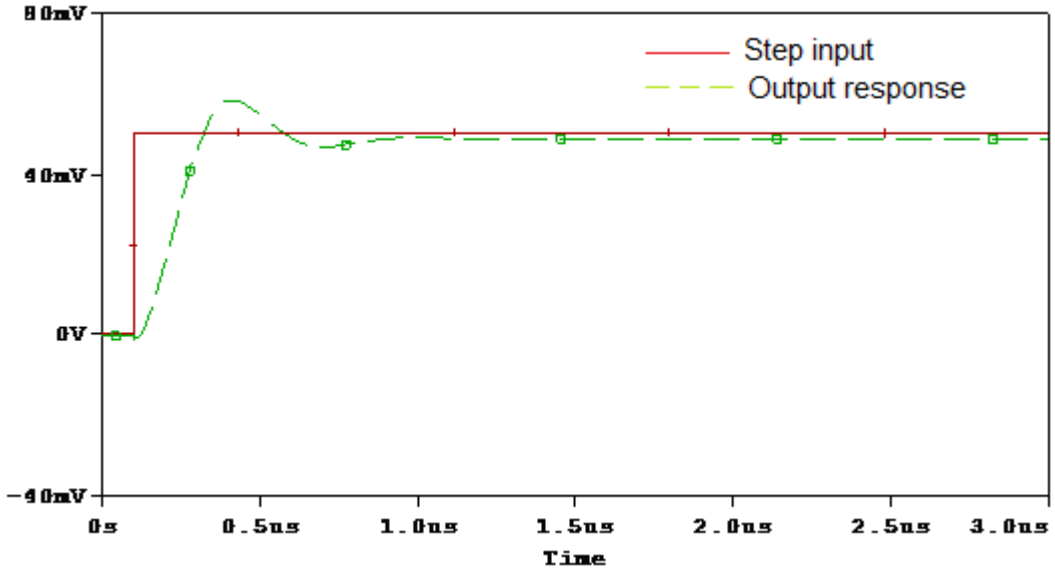


Fig. 5.6a Step Response of a second order system without P controller

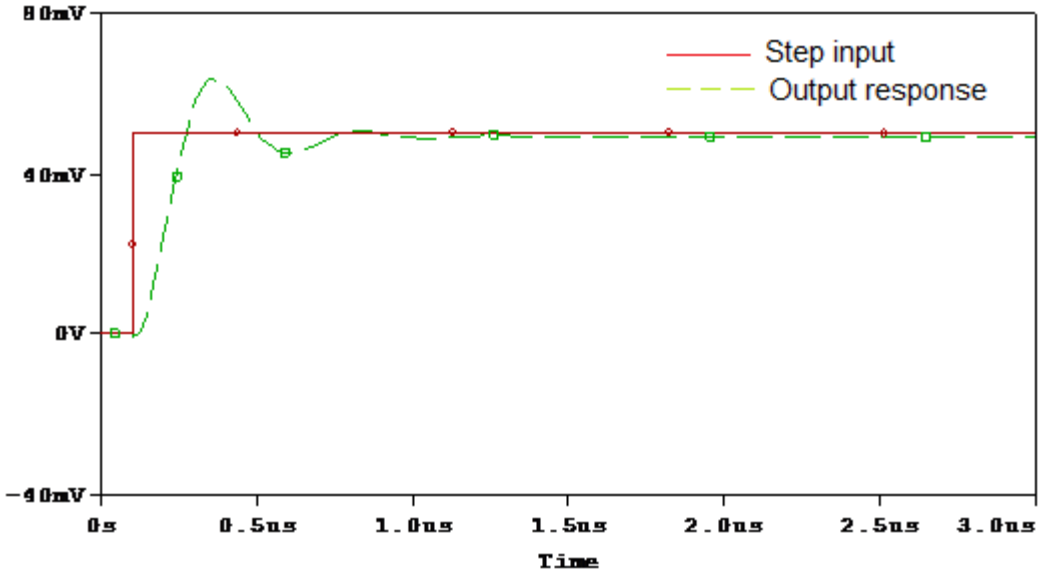


Fig. 5.6b Step Response of a second order system with P controller

Table 5.2 Performance Comparison of closed loop system with and without P controller

Parameter	*Without P Controller*	*With P Controller*
Overshoot	19.56%	30.14%
Peak output	58.26mV	62.64mV
Rise time	140.43ns	108.75ns
Settling time	303.12ns	675.11ns

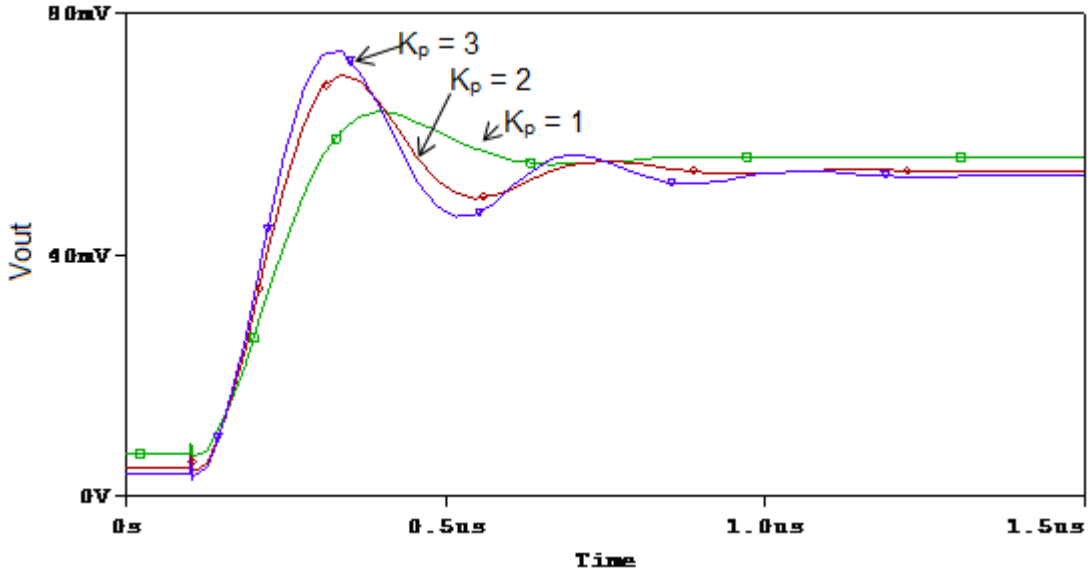


Fig. 5.7 Step Response of a second order system with P controller with varying K_p

5.2 Simulation Results of PD Controller

For OTRA based proposed PD controller shown in Fig. 4.7, the values of passive elements are chosen as R_1 = 10KΩ, R_2 = 20KΩ and C_1 = 20pF. For time domain analysis, a 3mV peak triangular input voltage is applied and both ideal and simulated results are presented in Fig. 5.8. Frequency domain characteristics are depicted in Fig. 5.9.

For MOS-C implemented PD controller shown in Fig. 4.8 the aspect ratios of the transistors used for implementing the resistances are listed in Table.5.3.

Table 5.3 Aspect ratios for MOS-C implementation of PD Controller

Transistor	*W(μM)/L(μM)*
M1,M2	0.18μ/.54μ
M3,M4	0.18μ/1.08μ

Gate voltages are set as V_{a1}= V_{a2} = 1.2V and Vb1=0.59V, Vb2 =0.64V which result in resistance values as R_1 ≈10KΩ, R_2 ≈20KΩ and the chosen value of capacitance is C_1 = 20pF. Fig. 5.10 and Fig. 5.11 show the transient response and frequency domain characteristics of MOS-C implementation of PD controller respectively.

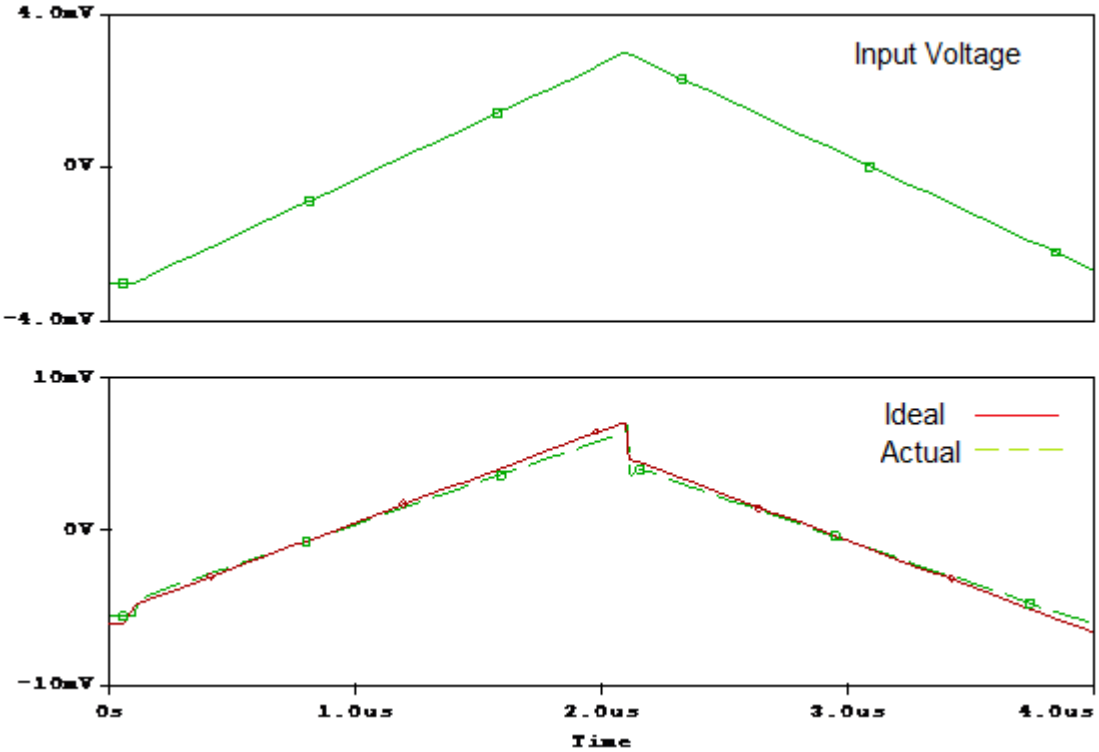


Fig. 5.8 Transient response of the PD Controller

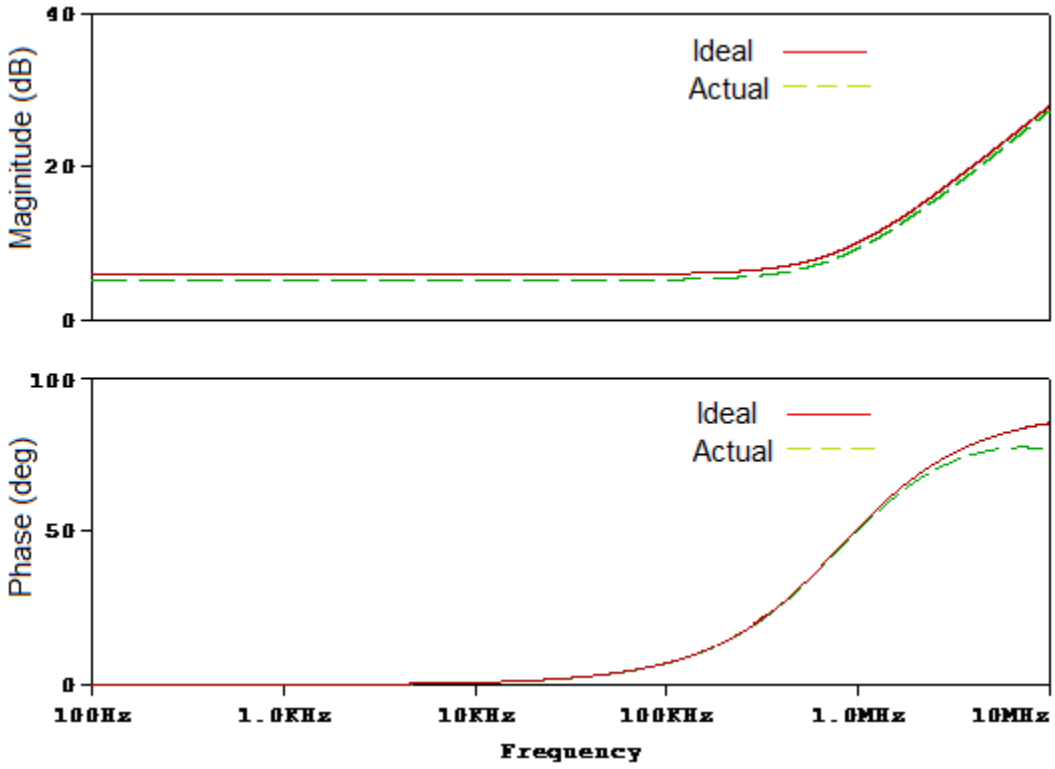


Fig. 5.9 Frequency and phase Response of PD controller

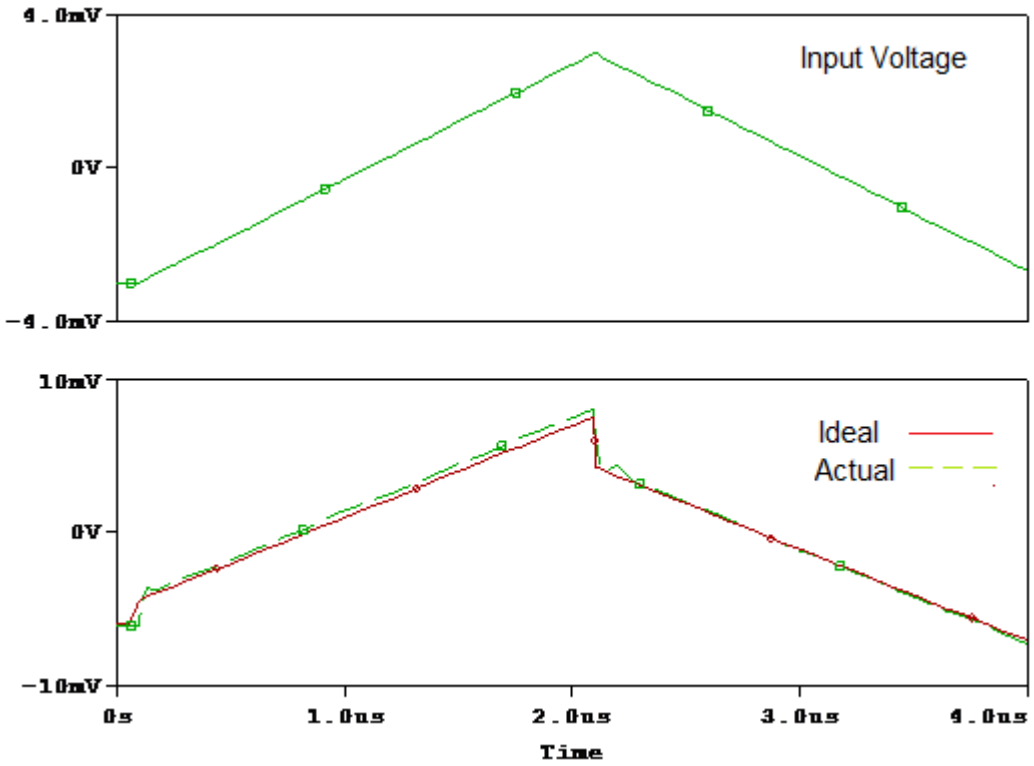


Fig. 5.10 Transient response of the MOS-C implemented PD Controller

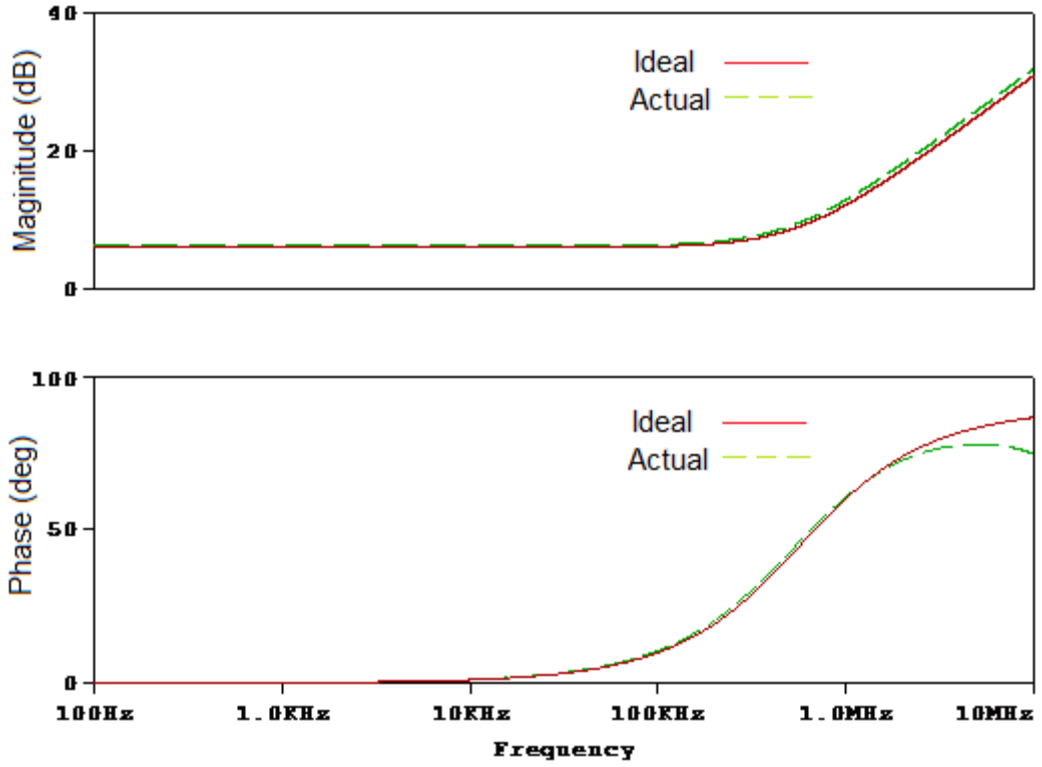


Fig. 5.11 Frequency and phase Response of the MOS-C implemented PD Controller

From the above results it is clear, that resistive components of PD controller can easily be replaced by MOS transistors working in linear region. Fig. 5.12 shows a closed loop control system realized using the proposed PD controller and a second order low-pass filter (LPF). Fig. 5.13a shows step response of the LPF without PD controller for a step input of 50mV whereas Fig.5.13b depicts the effect of PD controller on step response of the closed loop system.

Performance comparison of second order system with and without PD controller is shown in Table. 5.4. It is clearly visible from the table 5.4 that the response of the system has been improved with reduced overshoot percentage to 12.89% and smaller rise time of 124.27ns. Fig. 5.13c shows the step response with the variation in K_d and it shows that with increase in K_d, peak overshoot decreases.

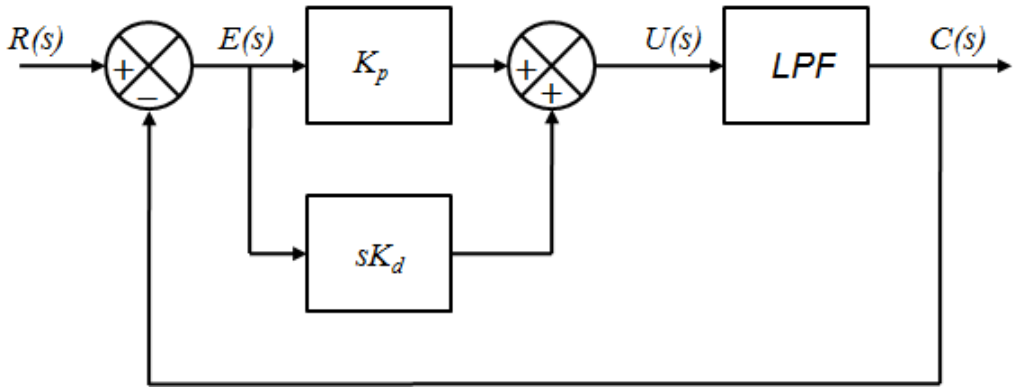


Fig. 5.12 Closed Loop Control System using PD controller

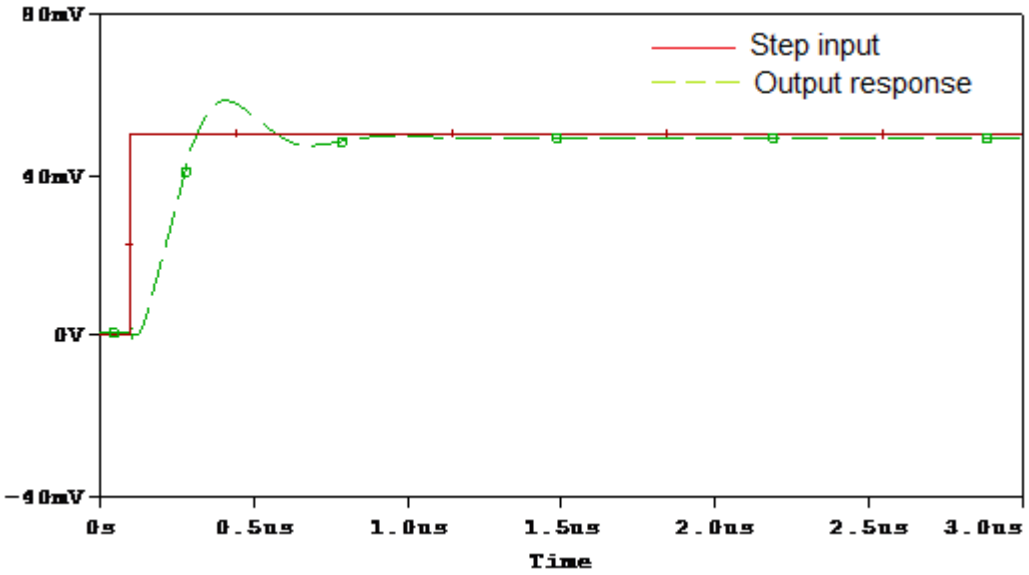


Fig. 5.13a Step Response of a second order system without PD controller

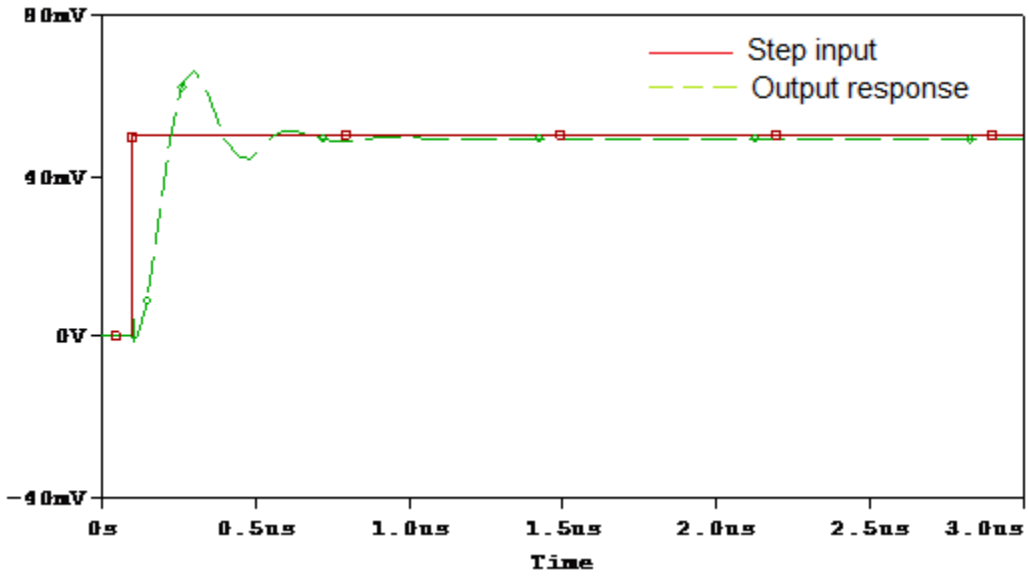


Fig. 5.13b Step Response of a second order system with PD controller

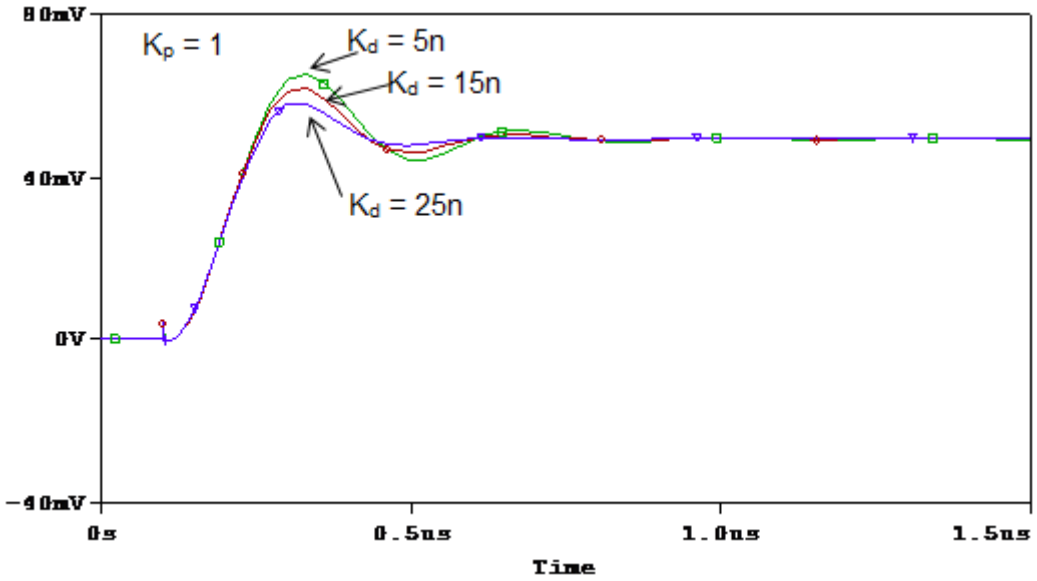


Fig. 5.13c Response of a second order system with PD controller with varying K_d

Table 5.4 Performance Comparison of closed loop system with and without PD controller

Parameter	*Without PD Controller*	*With PD Controller*
Overshoot	19.56%	12.89%
Peak output	58.26m	56.53mV
Rise time	140.43ns	124.27ns
Settling time	303.12ns	278.97ns

5.3 Simulation Results of PI Controller

For the OTRA based proposed PI controller shown in Fig. 4.11, the values of passive element are chosen as R_1= 10KΩ, R_2 = 20KΩ and C_1 = 20pF. For time domain analysis, a 3mV step input voltage with 20ns rise time is applied and both ideal and simulated results are presented in Fig. 5.14. Frequency domain characteristics are depicted in Fig. 5.15.

For MOS-C implemented PI controller shown in Fig. 4.12 the aspect ratios of the transistors used for implementing the resistances are listed in Table.5.5.

Table 5.5 Aspect ratios for MOS-C implementation of PI Controller

Transistor	*W(μM)/L(μM)*
M1,M2	0.18μ/1.08μ

Gate voltages are set as V_{a1}= 1V and Vb1=0.5V which result in resistance value as R_1 ≈50KΩ and the chosen values of capacitances are C_1 = 4pF and C_f = 2pF. Fig. 5.16 and Fig. 5.17 show the transient response and frequency domain characteristics of MOS-C implementation of PI controller respectively.

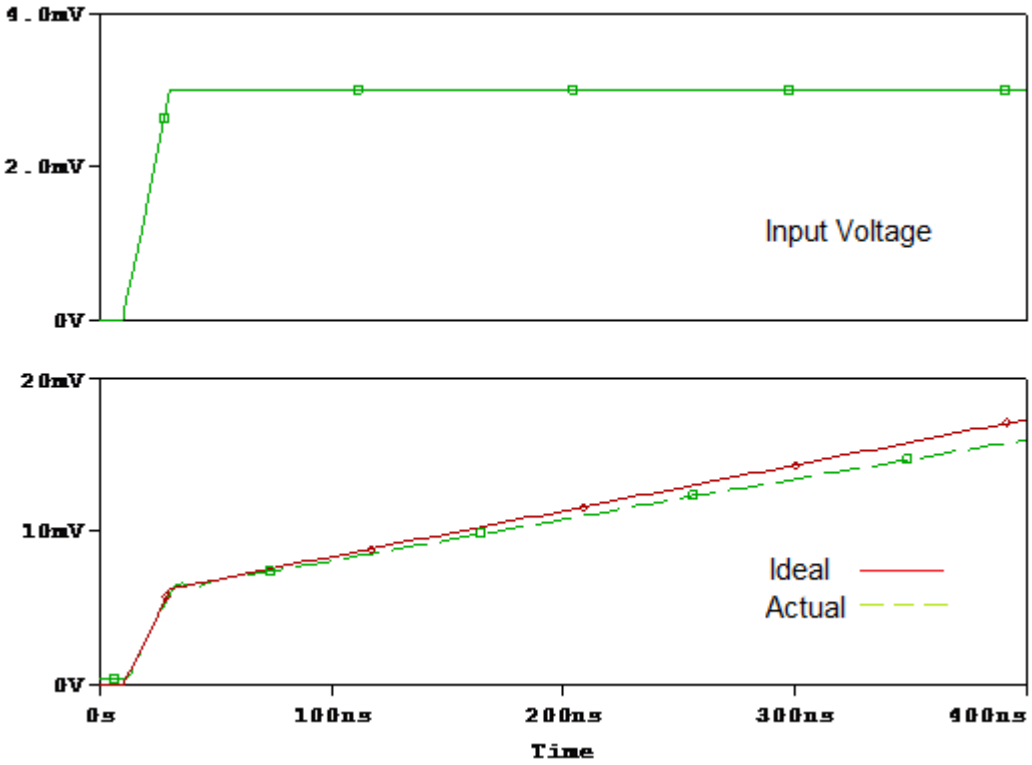


Fig. 5.14 Transient response of the PI Controller

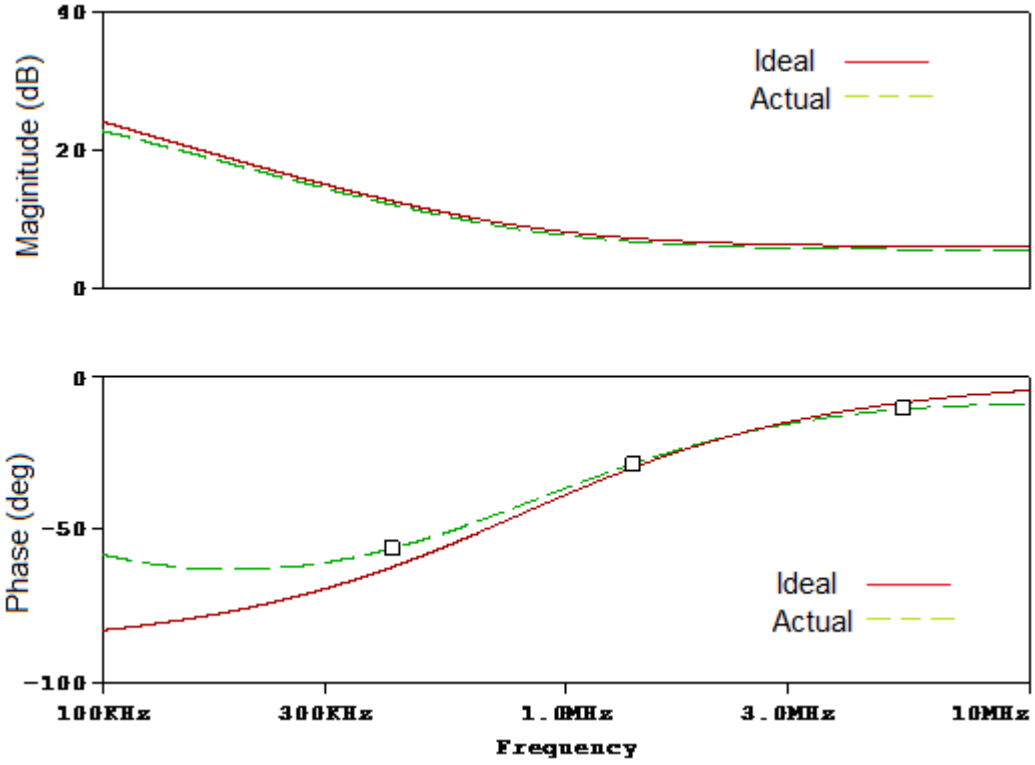


Fig. 5.15 Frequency and phase Response of PI Controller

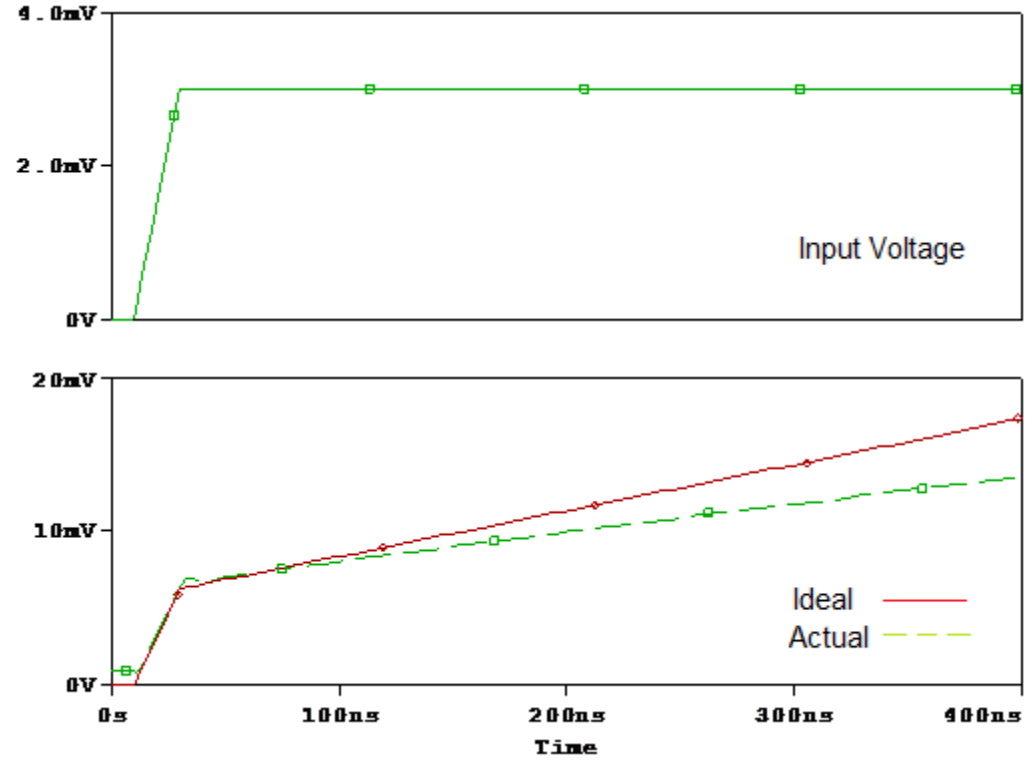


Fig. 5.16 Transient response of the MOS-C implemented PI Controller

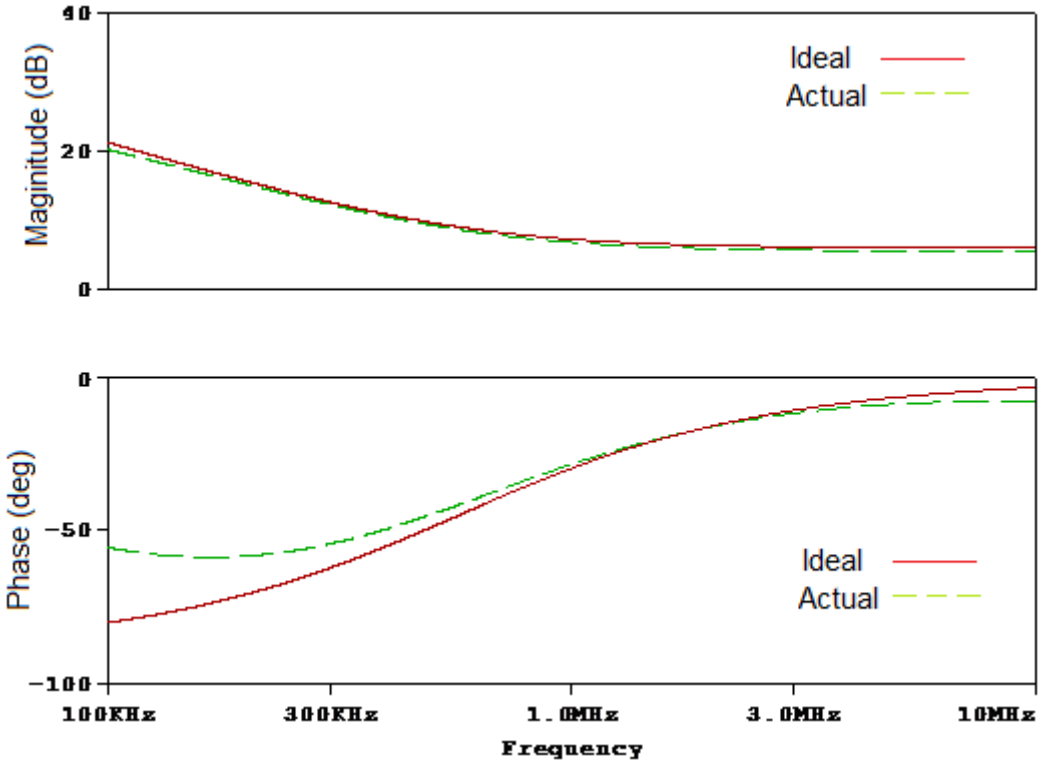


Fig. 5.17 Frequency and phase Response of the MOS-C implemented PI Controller

Fig. 5.18 shows a closed loop control system realized using the proposed PI controller and a second order low-pass filter (LPF). Fig. 5.19 depicts the effect of PI controller on step response of the closed loop system.

Performance comparison of second order system with and without PI controller is shown in Table. 5.6. From the table 5.6, the response of the system has been improved having smaller settling time of 266ns as well as smaller maximum peak amplitude of 57.8mV. Fig. 5.19b shows the step response with the variation in K_i.

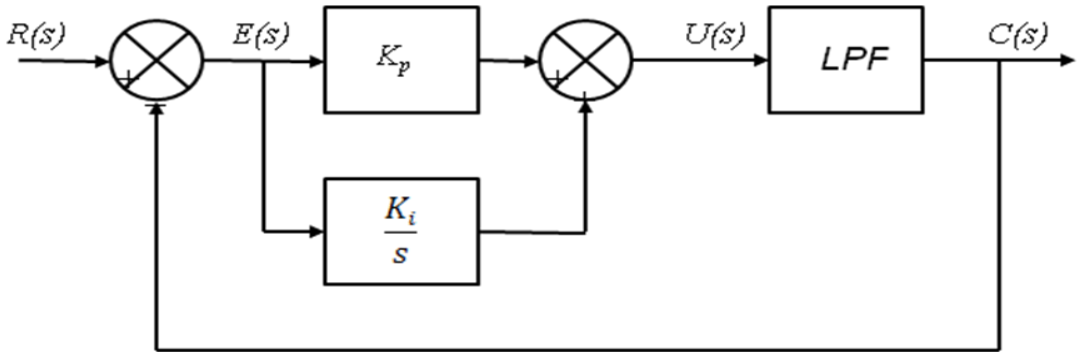


Fig. 5.18 Closed Loop Control System using PD controller

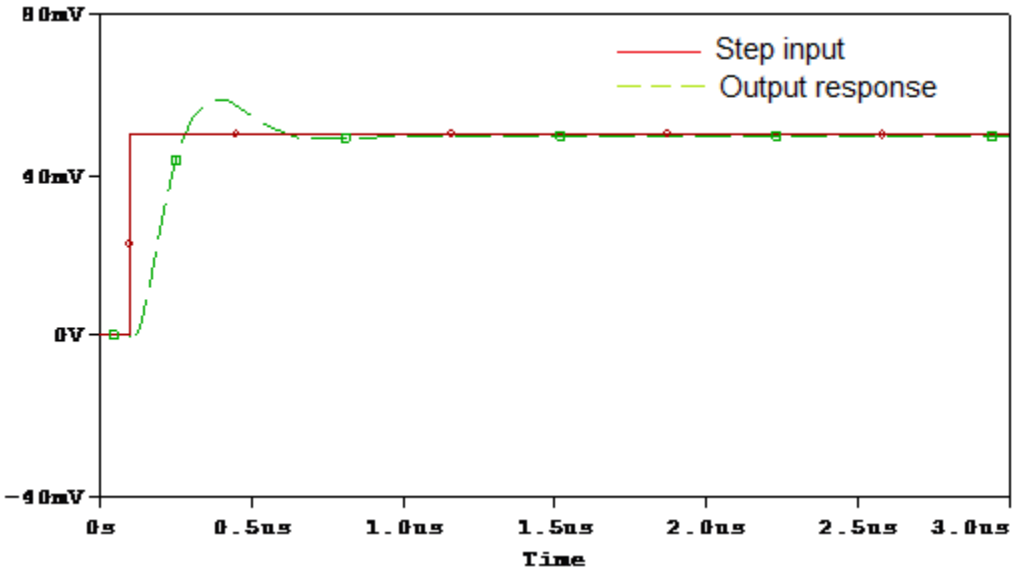


Fig. 5.19a Step Response of a second order system with PI controller

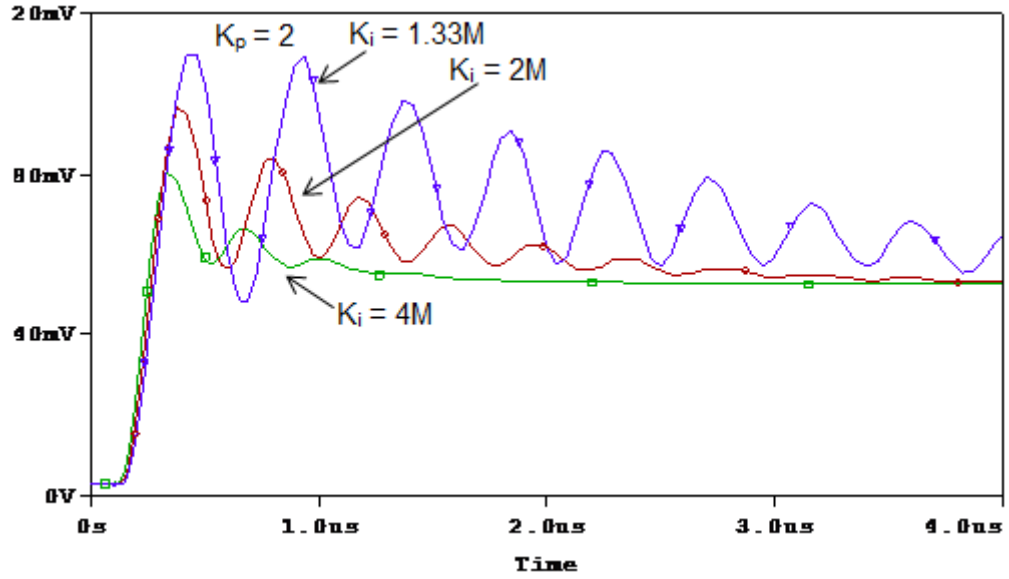


Fig. 5.19b Response of a second order system with PI controller with varying K_i

Table 5.6 Performance Comparison of closed loop system with and without PI controller

Parameter	*Without PI Controller*	*With PI Controller*
Overshoot	19.56%	18.76%
Peak output	58.26mV	57.83mV
Rise time	140.43ns	112.28ns
Settling time	303.12ns	266.11ns

5.4 Simulation Results of PID Controller

To simulate, differential OTRA based proposed PID controller shown in Fig. 4.15 values of passive elements are $R_1 = R_2 = R_3 = R_4 = 50K$, $C_1 = C_3 = 10pF$ and $C_2 = 0.05pF$. For time domain analysis, a 3mV step signal with 10ns rise time is applied and both ideal and simulated results are presented in Fig. 5.20.

For MOS-C implemented PID controller shown in Fig. 4.16 the aspect ratios of the transistors used for implementing the resistances are listed in Table.5.7. Gate voltages are set as $V_{a1} = V_{a2} = V_{a3} = V_{a4} = 1V$ and $Vb1 = V_{b2} = V_{b3} = V_{b4} = 0.5V$ which result in resistance values as $R_1 = R_2 = R_3 = R_4 \approx 50K$ and the chosen value of capacitances are $C_1 = C_3 = 10pF$ and $C_2 = 0.05pF$. Fig. 5.21 shows the transient response of MOS-C implementation of PID controller.

Table 5.7 Aspect ratios for MOS-C implementation of PID Controller

Transistor	*W(μM)/L(μM)*
M1,M2	0.18μ/1.8μ
M3,M4	0.18μ/1.8μ
M5,M6	0.18μ/1.8μ
M7,M8	0.18μ/1.8μ

For verification of functionality of the proposed PID controller a closed loop control, system consisting of the proposed PID controller and a second order low-pass filter (LPF), as shown in Fig. 5.22 is realized. For simulation a step signal of 50mV is used. Fig. 5.23 depicts the effect of PID controller on step response of the closed loop system.

Performance comparison of second order system with and without PID controller is shown in Table. 5.8 which reveals that there is an overall improvement in the performance of the system with decreased overshoot, faster response with improved rise and settling time and smaller maximum peak amplitude.

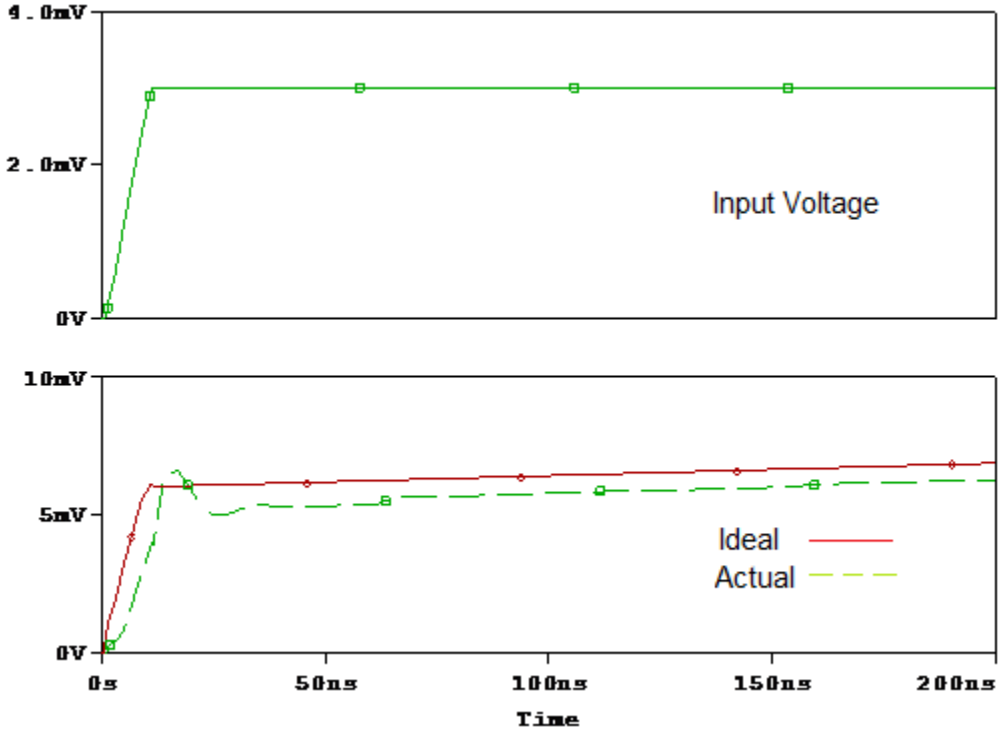


Fig. 5.20 Transient response of the PID Controller

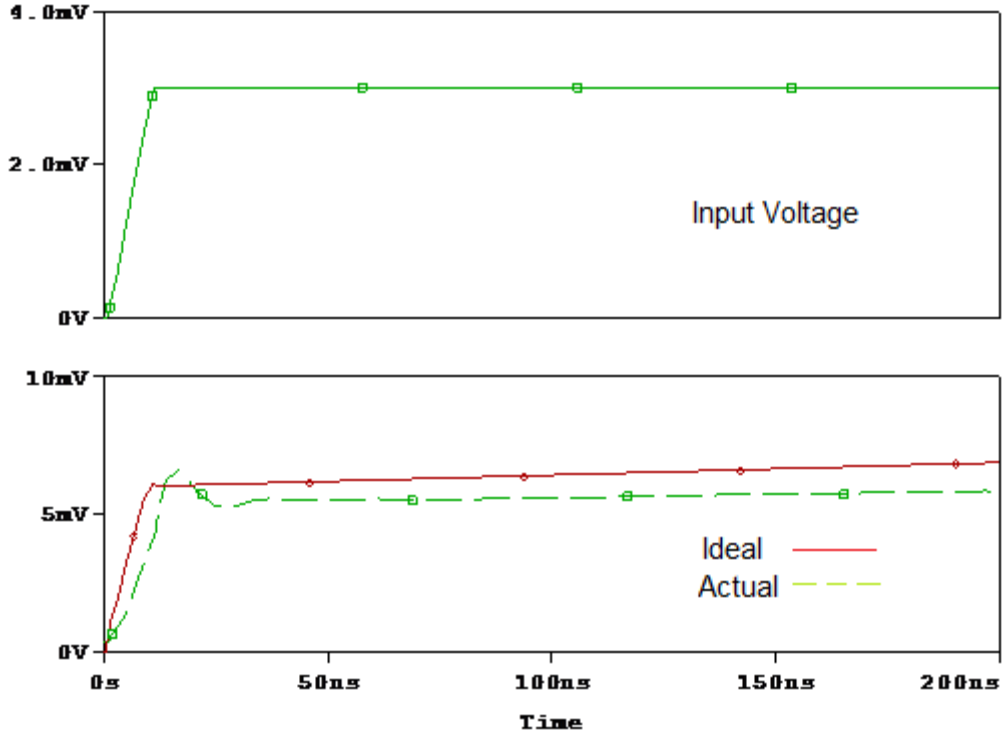


Fig. 5.21 Transient response of the MOS-C implemented PID Controller

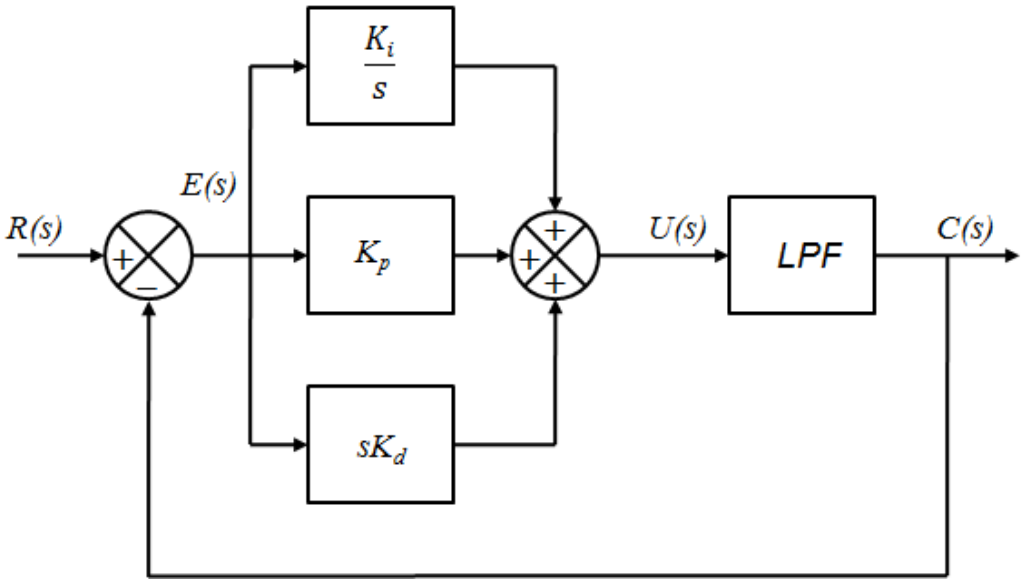


Fig. 5.22 Closed Loop Control System using PID controller

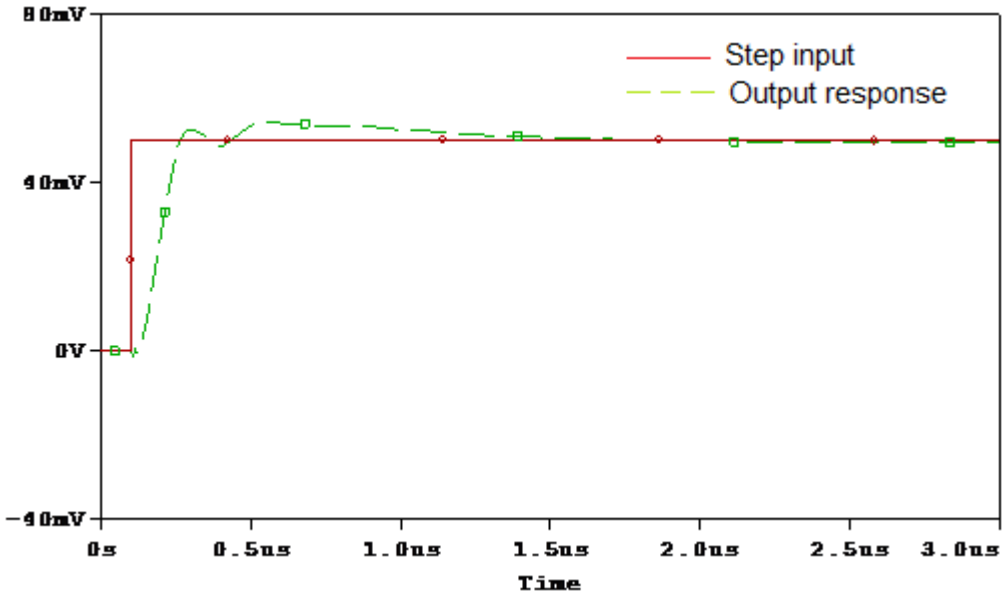


Fig. 5.23 Step Response of a second order system with PID controller

Table 5.8 Performance Comparison of closed loop system with and without PID controller

Parameter	*Without PID Controller*	*With PID Controller*
Overshoot	19.56%	8.16%
Peak output	58.26mV	52.59mV
Rise time	140.43ns	99.75ns
Settling time	303.12ns	252.27ns

5.5 Performance Comparison of Controllers

Table 5.9 shows the performance comparison of controllers. This table clearly indicates with the help of controllers the performance of system is improved in a desired manner.

The effect of P controller is to make the system to respond faster i.e. improve rise time at the cost of overshoot but this is the simplest controller and can be easily designed.

The PD controller improves all the parameter, prominently overshoot and very small improvement in settling time is observed.

PI controller influences mainly the settling time as compared to all other parameter.

PID includes best features of all individual controllers and results in improvement of all the performance measure parameters.

Table 5.9 Performance Comparison of closed loop system with and without controllers

Parameter	*LPF*	*With P Controller*	*With PD Controller*	*With PI Controller*	*With PID Controller*
Overshoot	19.56%	30.14%	12.89%	18.76%	8.16%
Peak output	58.26mV	62.64mV	56.53mV	57.83mV	52.59mV
Rise time	140.43ns	108.75ns	124.27ns	112.28ns	99.75ns
Settling time	303.12ns	675.11ns	278.97ns	266.11ns	252.27ns

Chapter-6

CONCLUSION AND FUTURE SCOPE

6.1 Conclusion

Differential Operational transresistance (OTRA) based proportional (P), proportional-derivative (PD), proportional integral (PI) and proportional integral derivative (PID) controllers have been presented which possess the feature of independent tuning of proportional (K_p), derivative (K_d) and integral (K_i) constants.

Their MOS-C equivalent circuits were also designed. This is done by implementing the resistors using MOS transistors operating in linear region. Simulation results of these controllers are in close agreement with theoretical values. Implementing the resistors using MOS transistors results in lesser chip area consumption and therefore these controller designs are suitable for full integration.

As an application, a second order closed loop system was designed and simulated using SPICE program. The simulated results are in line with the proposed theory. The performance analysis reveals that P controller improves rise time at the cost of other performance parameter, PD controller enhances overshoot percentage specially, PI controller refines settling time while PID as a combination of P, I & D, enhances transient as well as steady state time response of the system.

6.2 Future Scope

Time domain analysis of differential OTRA based controllers is presented in this thesis, but other analysis like stability analysis, noise analysis, effect of parameter variation, effect of power supply variation etc. are yet to be explored to make these controllers a market product.

Various methods of parameter tuning like Ziegler–Nichols, Cohen-Coon, Skogestad, Process Reaction curve etc. can be further used.

In this work, step response of second order system with and without controller is analyzed for series (cascade) configuration of system. This analysis can be carried out for other system configurations like feedback, state-feedback, series-feedback, forward with series and feed-forward in which controllers are introduced for improving the system performance.

Further these controllers can be designed and simulated for multi input multi output (MIMO) system.

These OTRA based designs are best suited for the Low Power and High Speed applications so these can be used in MEMS (Micro-electromechanical systems) and Low Power Medical Devices.

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Appendix

Simulations have been performed using SPICE at 180nm technology and the model files provided by MOSIS (AGILENT) used have the following parameters:

.MODEL NMOS NMOS (LEVEL = 7

+ TNOM = 27	TOX = 4.1E-9	
+XJ = 1E-7	NCH = 2.3549E17	VTH0 = 0.3750766
+K1 = 0.5842025	K2 = 1.245202E-3	K3 = 1E-3
+K3B = 0.0295587	W0 = 1E-7	NLX = 1.597846E-7
+DVT0W = 0	DVT1W = 0	DVT2W = 0
+DVT0 = 1.3022984	DVT1 = 0.4021873	DVT2 = 7.631374E-3
+U0 = 296.8451012	UA = -1.179955E-9	UB = 2.32616E-18
+UC = 7.593301E-11	VSAT = 1.747147E5	A0 = 2
+AGS = 0.452647	B0 = 5.506962E-8	B1 = 2.640458E-6
+KETA = -6.860244E-3	A1 = 7.885522E-4	A2 = 0.3119338
+RDSW = 105	PRWG = 0.4826	PRWB = -0.2
+WR = 1	WINT = 4.410779E-9	LINT = 2.045919E-8
+XL = 0	XW = -1E-8	DWG = -2.610453E-9
+DWB = -4.344942E-9	VOFF = -0.0948017	NFACTOR = 2.1860065
+CIT = 0	CDSC = 2.4E-4	CDSCD = 0
+CDSCB = 0	ETA0 = 1.991317E-3	ETAB = 6.028975E-5
+DSUB = 0.0217897	PCLM = 1.7062594	PDIBLC1 = 0.2320546
+PDIBLC2 = 1.670588E-3	PDIBLCB = -0.1	DROUT = 0.8388608
+PSCBE1 = 1.904263E10	PSCBE2 = 1.546939E-8	PVAG = 0
+DELTA = 0.01	RSH = 7.1	MOBMOD = 1
+PRT = 0	UTE = -1.5	KT1 = -0.11
+KT1L = 0	KT2 = 0.022	UA1 = 4.31E-9
+UB1 = -7.61E-18	UC1 = -5.6E-11	AT = 3.3E4

```
+WL      = 0                WLN     = 1                WW      = 0
+WWN     = 1                WWL     = 0                LL      = 0
+LLN     = 1                LW      = 0                LWN     = 1
+LWL     = 0                CAPMOD  = 2                XPART   = 0.5
+CGDO    = 6.7E-10          CGSO    = 6.7E-10          CGBO    = 1E-12
+CJ      = 9.550345E-4      PB      = 0.8              MJ      = 0.3762949
+CJSW    = 2.083251E-10     PBSW    = 0.8              MJSW    = 0.1269477
+CJSWG   = 3.3E-10          PBSWG   = 0.8              MJSWG   = 0.1269477
+CF      = 0                PVTH0   = -2.369258E-3     PRDSW   = -1.2091688
+PK2     = 1.845281E-3      WKETA   = -2.040084E-3     LKETA   = -1.266704E-3
+PU0     = 1.0932981        PUA     = -2.56934E-11     PUB     = 0
+PVSAT   = 2E3              PETA0   = 1E-4             PKETA   = -3.350276E-3    )

.MODEL PMOS PMOS (                    LEVEL   = 7

+ TNOM    = 27              TOX     = 4.1E-9
+XJ   = 1E-7                NCH     = 4.1589E17        VTH0    = -0.3936726
+K1   = 0.5750728           K2      = 0.0235926        K3      = 0.1590089
+K3B= 4.2687016             W0      = 1E-6             NLX     = 1.033999E-7
+DVT0W   = 0                DVT1W   = 0                DVT2W   = 0
+DVT0 = 0.5560978           DVT1    = 0.2490116        DVT2    = 0.1
+U0= 112.5106786            UA      = 1.45072E-9       UB      = 1.195045E-21
+UC      = -1E-10           VSAT    = 1.168535E5       A0      = 1.7211984
+AGS     = 0.3806925        B0      = 4.296252E-7      B1      = 1.288698E-6
+KETA    = 0.0201833        A1      = 0.2328472        A2      = 0.3
+RDSW    = 198.7483291      PRWG    = 0.5              PRWB    = -0.4971827
+WR      = 1                WINT    = 0                LINT    = 2.943206E-8
+XL      = 0                XW      = -1E-8            DWG     = -1.949253E-8
+DWB     = -2.824041E-9     VOFF    = -0.0979832       NFACTOR = 1.9624066
+CIT     = 0                CDSC    = 2.4E-4           CDSCD   = 0
+CDSCB   = 0                ETA0    = 7.282772E-4      ETAB    = -3.818572E-4
```

+DSUB = 1.518344E-3 PCLM = 1.4728931 PDIBLC1 = 2.138043E-3
+PDIBLC2 = -9.966066E-6 PDIBLCB = -1E-3 DROUT = 4.276128E-4
+PSCBE1 = 4.850167E10 PSCBE2 = 5E-10 PVAG = 0
+DELTA = 0.01 RSH = 8.2 MOBMOD = 1
+PRT = 0 UTE = -1.5 KT1 = -0.11
+KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9
+UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4
+WL = 0 WLN = 1 WW = 0
+WWN = 1 WWL = 0 LL = 0
+LLN = 1 LW = 0 LWN = 1
+LWL = 0 CAPMOD = 2 XPART = 0.5
+CGDO = 7.47E-10 CGSO = 7.47E-10 CGBO = 1E-12
+CJ = 1.180017E-3 PB = 0.8560642 MJ = 0.4146818
+CJSW = 2.046463E-10 PBSW = 0.9123142 MJSW = 0.316175
+CJSWG = 4.22E-10 PBSWG = 0.9123142 MJSWG = 0.316175
+CF = 0 PVTH0 = 8.456598E-4 PRDSW = 8.4838247
+PK2 = 1.338191E-3 WKETA = 0.0246885 LKETA = -2.016897E-3
+PU0 = -1.5089586 PUA = -5.51646E-11 PUB = 1E-21
+PVSAT = 50 PETA0 = 1E-4 PKETA = -3.316832E-3)