A

Dissertation

on

"Development of CMOS Based Current Differencing Buffered Trans Conductance Amplifier And its Applications"

Submitted in partial fulfillment of the requirement

For the award of Degree of

MASTER OF TECHNOLOGY

(VLSI Design and Embedded Systems)

Submitted by

Ajay Chopra

(Roll No. 2K09/vls/01)

Under the Guidance of

Rajeshwari Pandey

(Assistant Professor)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION

DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)

BAWANA ROAD, DELHI

June-2011

CERTIFICATE

DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)

BAWANA ROAD, DELHI – 110042

Date:_____

This is to certify that the thesis entitled "**Development of CMOS current Differencing Buffered Trans conductance Amplifier and its Applications**" has been completed by **Mr. Ajay Chopra** submitted in partial fulfillment of the requirement for the award of degree of **Master in Technology** in **VLSI Design and Embedded Systems** is a record of his work carried out by him under my supervision. The matter embodied in this thesis has not been submitted for the award of any degree or diploma.

(Rajeshwari Pandey)

PROJECT GUIDE

(Dept. of Electronics and Communication Engineering)

DELHI TECHNOLOGICAL UNIVERSITY

BAWANA ROAD, DELHI – 110042

ACKNOWLEDGEMENT

With profound respect and gratitude, I take the opportunity to convey my thanks to our very respectable **Prof. Rajeev Kapoor (HOD), Prof. Asok Bhattacharya, Mrs. Rajeshwari Pandey,** my faculty guide for the project, and **Dr. Neeta Pandey** for their constant encouragement and guidance. There help and guidance have been instrumental in successful completion of this project. I would like to express my gratitude towards all the faculty members as well as the Technical staff of the department for their co-operation and support provided by them during the course of this project .

(Ajay Chopra)

Master of Technology

(VLSI Design and Embedded System)

Dept. of Electronics and Communication Engineering

DELHI TECHNOLOGICAL UNIVERSITY

BAWANA ROAD, DELHI – 110042

ABSTARCT

The major goal of this work is to present a new CMOS realization for the current differencing buffered Trans Conductance amplifier (CDBTA). A design technique based on flipped voltage follower current sources is preferred to obtain a high performance CDBTA. The proposed circuit can operate with the minimum supply voltages of ±0.6 V. It also consumes less power .The proposed CDBTA has good voltage and current gain accuracies. The performance of the CDBTA is verified using SPICE. For the simulations, UMC 0.18 µ CMOS process is used. To verify the functionality of the proposed analog building block and to demonstrate its utility two applications namely a notch filter and a general impedance converter configuration are also proposed. The SPICE simulations results of these applications are in remarkable agreement with the theoretical results.

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CHAPTER-1

Introduction

Designers have been trying to integrate versatile circuit blocks into their circuitry. In an effort to reduce cost and space and improve performance, designers are integrating more and more circuit blocks, both analog and digital, onto a single chip. In order to reduce power dissipation, it is advantageous, at least for digital circuit blocks, to implement these "mixed-signal" chips in a standard CMOS process. In a further effort to reduce power dissipation in digital circuit blocks, it is advantageous to reduce the supply voltage V_{dd}. For a standard CMOS inverter, power dissipation may be expressed as:

$$P_{avg} = C * V_{dd} * f$$

In an effort to increase the intrinsic gain of CMOS devices, the trend in the MOSFET design industry is to shrink the gate oxide thickness, T_{ox}. Unfortunately, as T_{ox} is reduced, the MOSFET device's tolerance for high voltage levels at the gate is also reduced. This means that, for reliability purposes, it is advantageous to reduce the maximum voltage supply V_{dd}. This trend in reducing the supply voltage means that analog designers face challenges such as reduced input common mode range, output swing and linearity. Part of the problem is that V_{T0} does not scale in a linear fashion with the reduction in minimum device length. Unfortunately for the designer, V_{T0} does not tend to decrease at the same rate as V_{dd}. Some fabs do offer low V_{T0} processes specially suited for analog blocks. However, they tend to cost more than standard CMOS processes. It is therefore desirable to use low voltage design techniques, in order to be able to implement analog circuit blocks using standard CMOS process.

In a never-ending effort to reduce power consumption and gate oxide thickness, the integrated circuit industry is constantly developing smaller power supplies. Today's analog circuit designer is faced with the challenges of making analog circuit blocks with sub 1V supplies with little or no reduction in performance. Furthermore, in an effort to reduce costs and integrate analog and digital circuits onto a single chip, the analog designer must often face the above challenges using plain CMOS processes.

With the advent of the portable electronic and mobile communication system low-voltage and low-power mixed mode circuit design has gained importance. For the operation of such systems like hearing aids, implantable cardiac pacemakers, cell-phones and hand held multimedia terminals etc. battery is the main source of power. They require low power dissipation so as to have reasonable battery life and weight. Battery adds volume and weight as so there is search for the alternatives and the alternatives are solar power, fuel cells etc. But the problem is with the voltage levels of these sources. The voltage of a single solar cell is about 0.5 V and integrated circuits require much higher voltages for their operation. Obtaining higher voltages on chip by voltage multiplication which is nothing but DC-DC conversion is noisy and not compatible with the analog circuits. It can be done either using inductors or without using inductors. Also in analog design the issue of Power Supply Rejection Ratio should be taken care of.

As the feature size of CMOS processes reduces, the supply voltage has to be reduced for the reduction of power dissipation per cell. Supply voltage reduction guarantee the reliability of devices as the lower electrical fields inside layers of a MOSFET produces less risk to the thinner oxides, which results from device scaling. However, the reduction in supply voltage leads to degraded circuit performance in terms of available bandwidth and voltage swing[1]. Scaling down the threshold voltage of the MOSFETs reduces the performance loss (degraded bandwidth, low voltage swing etc.) somewhat but it has its own disadvantages i.e. the increase in the static power dissipation.

The performance of digital circuits is improved by scaling but the analog cells, benefit marginally because minimum size transistors cannot be used due to noise and offset requirements. In today's design techniques the aim is to achieve high speed, and high integration on chip with a large dynamic range. One of the factors, which affect these parameters, is power dissipation in the circuit. There are three major sources of power dissipation. Dynamic power consumption caused by charging and discharging of (usually parasitic) capacitance; Static power consumption due to non-zero current of MOSFETs in OFF state in digital circuits or the biasing current in the analog circuits; Short-circuit power consumption due to the current flowing during the lapse of time when both PMOS and NMOS transistors are in the ON state. For the low

voltage high performance analog circuit design current mode design technique, which offer voltage independent high bandwidth analog circuit, is a good alternative.

Originally current mode term was coined by Barrie Gilbert when he was working on the Trans linear loops. In current mode design the designer is more concerned with current levels for the operation of the circuits. The voltage levels at various nodes are immaterial. Some authors[1] write that signals are represented by current in current mode circuits and by voltages in voltage mode circuits.

All conventional analog circuits are voltage mode circuits (VMCs) where the circuit performance is determined in terms of voltage levels at various nodes including the input and the output nodes example operational amplifier. But all these circuits suffer from the following disadvantages:

1. Output voltage cannot change instantly when there is a sudden change in the input.
2. Voltage due to stray and other circuit capacitances.
3. Bandwidth of the op amp based circuits is usually low because of finite unity gain Bandwidth

Due to these disadvantages current mode circuits are gaining importance in recent time, with number of circuits that are being developed using current mode approach like current conveyors[2], current feedback amplifier[3], OTA[4], OTRA[5], CDBA[6], CDTA[7] etc. In Chapter 3, a new low voltage CMOS based Current differencing buffered/trans conductance amplifier is proposed which has both the low and high impedance voltage output and current output terminals respectively which will provide flexibility in different circuit design applications.

CHAPTER 2

Literature Survey

2.1 Literature Survey On CDBA

Current differencing buffered amplifiers (CDBA) are important building blocks of many analog signal processing applications. The realization of Current differencing buffered amplifier has attracted the attention of researcher in the area of analog signal processing since long. IC Op-Amps were the main building blocks for the realization of analog signal processing filters during the decades of seventies and eighties. The current feedback operational amplifier (CFOA) which is commercially available as AD844 was developed by analog devices as a high speed Op-Amp which did not suffer from slew rate limitations and gain bandwidth (GB) conflict for medium and low frequency applications. Though the CFOA was intended to be substitute for traditional VOA, it is actually a 4 terminal device whereas traditional VOA is a 3 terminal device. Acar and Ozoguz [8] proposed a multi terminal active component with two inputs and two outputs, namely Current differencing buffered amplifier. It is derived from current feedback operational amplifier. It can operate in both current and voltage mode provides flexibility and enables a variety of circuit designs.

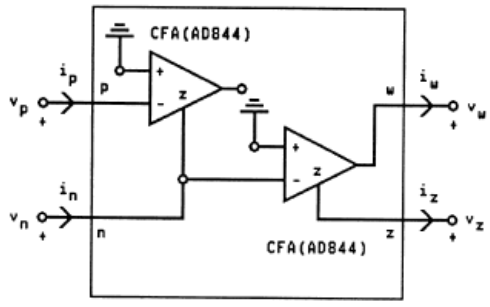

Fig 2. 1 CFOA used to realize the CDBA

The Current conveyor (CCII) proposed by Smith and Sedra [9] has been used by many researchers to design different circuits with different properties Tarim and Kuntman [10] proposed a high performance current differencing buffered amplifier by using two second generation current conveyors (CCII) and a voltage buffer. The CDBA offered contains only

MOS transistors and is designed to be implemented in CMOS technology. The CCII chosen for this purpose is given in Fig 2.2 and is reported to behave almost like an ideal CCII for continous-time applications . The high impedances at y and z terminals as well as the high accuracy of the current transfer ratio i_z / i_x are obtained by using improved active feedback cascode current mirrors.

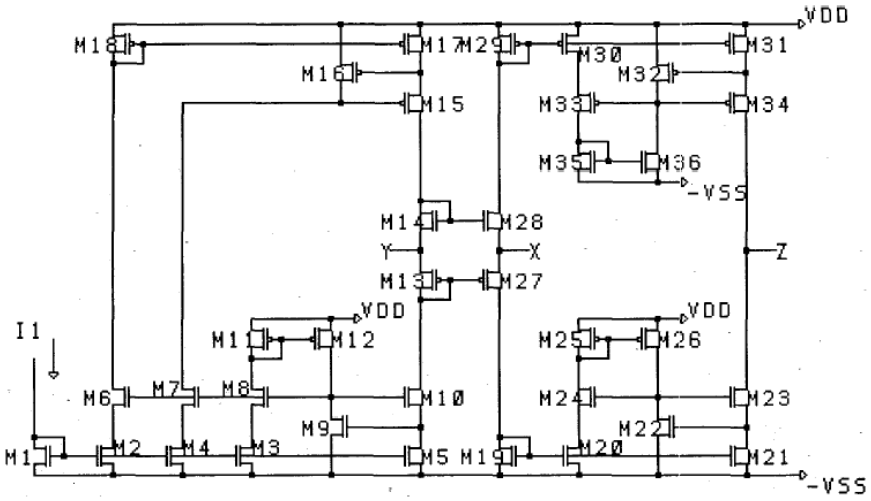

Fig 2. 2 The CCII circuit used to realize the CDBA

The high performance voltage buffer given in Fig 2.3 used to construct the CDBA circuit, which offers a very low gain error and low output impedance. Sawangarom, Tangsrirat and Surakampontom [11] proposed the NPN based current differencing buffered amplifier. It was shown that the CDBA based on NPN transistor can operate with a minimum power supply of 2 volts.

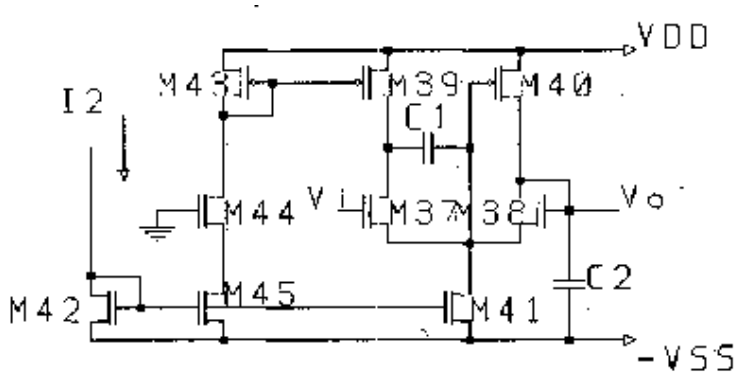

Fig 2. 3 The voltage buffer used to realize the CDBA

In order to avoid the limitation of high frequency operation effecting from PNP transistors, the CDBA was designed so that signals pass through only NPN transistors. NPN based CDBA consist of two blocks, current differencing circuit and voltage follower. The current differencing circuit is obtained by using two unity gain current amplifier Q_1-Q_5 and Q_7-Q_{11} and the current mirror Q_{12}-Q_{15} reflects the current to output port and transistors Q_{16}-Q_{20} form voltage buffer. The configuration is given in Fig 2.4

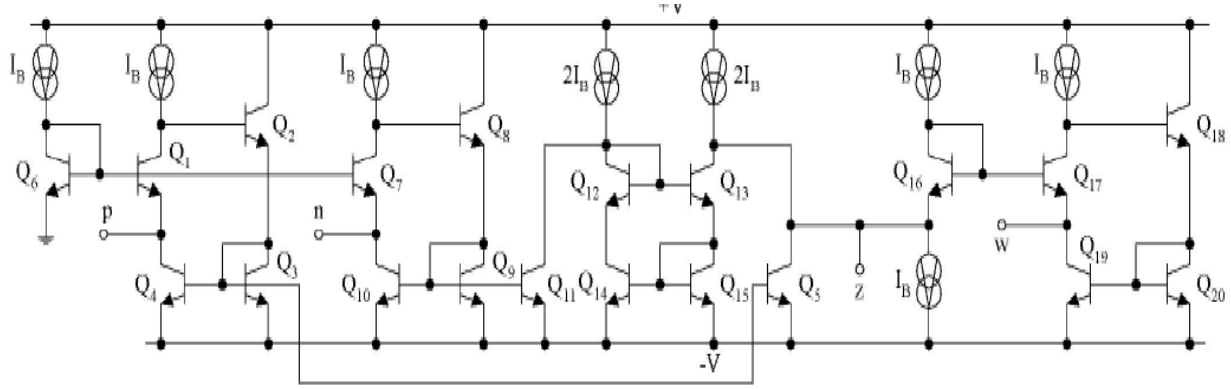

Fig 2. 4 NPN transistor based CDBA

W.Tangsrirat, K. Klahan, K. Kaewdang and W. Surakampontorn [12] proposed a low voltage wide band NMOS based CDBA, which has a low resistance at both the current-input terminals (p, n)and at the output-voltage terminal (w). It was shown that the CDBA based on NMOS transistor was superior in terms of supply voltage and frequency range. It can operate at minimum supply voltage of ±1.25 volts. The realization of NMOS based CDBA was based on the modification of low impedance current conveyor (CCII+) to function as a current differencing circuit and a voltage buffer circuit. Group of transistors (M_1 – M_5) and (M_1’ – M_5’) form to unity gain current amplifier and transistors (M_7 – M_{10}) form a positive current mirror. Transistor (M_{11} – M_{15}) forms the buffered voltage amplifier circuit. The circuit is given in Fig 2.5

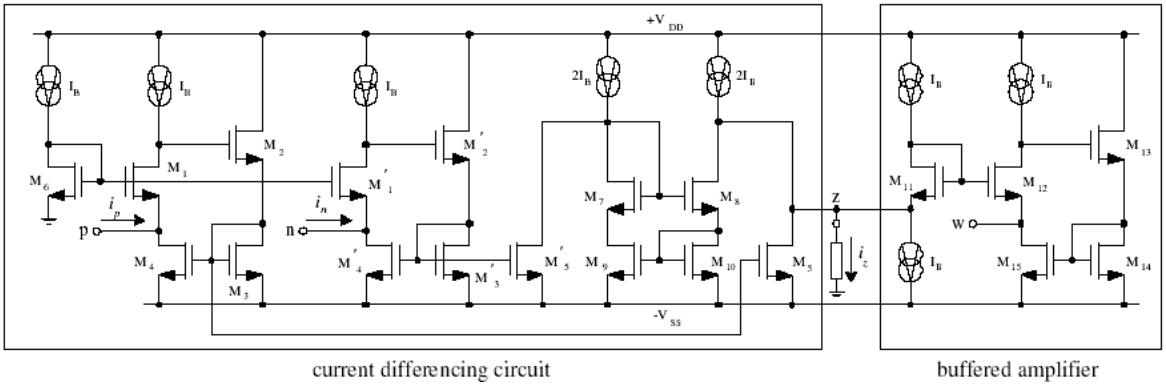

Fig 2. 5 NMOS based CDBA

The existing CDBAs do not use low-voltage power supplies and have quite high input terminal resistances, high power consumption, most of them suffer from limited output voltage swing. Therefore Cem Cakir, Shahram Minaei, and Oguzhan Cicekoglu [13] proposed a low voltage low power CDBA which overcome these drawbacks. Supply voltages of this circuit are chosen as ±0.75 V. The current subtractor circuit is formed by the transistors M_1 to M_{12}. This circuit exploits the flipped voltage follower current sources (FVFCS). A FVFCS is characterized by very low supply requirements and low impedance at input terminals [14]. The buffered circuit is formed by the transistors M_{13} to M_{26}. The configuration is given in Fig 2.6

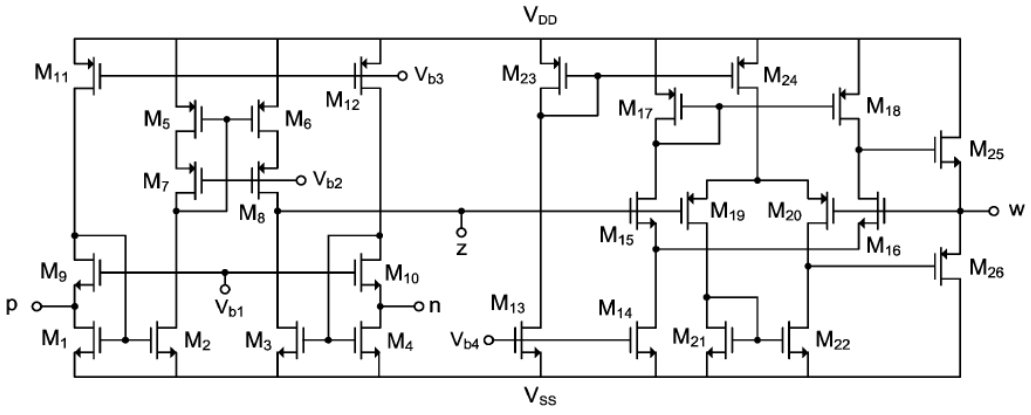

Fig 2. 6 Low voltage, low power and high swing current differencing buffered amplifier

Cem CAKIR and Oguzhan CICEKOGLU [6] in 2008 proposed a low power high performance CDBA. This circuit can be operated with the power supplies down to ±0.75V and it also consumes less power than its counterparts. The current subtractor circuit consists of the transistors M_1 to M_{10}. This circuit is based on the flipped voltage follower current sources (FVFCS) which give rise to very low input resistances at the input ports [15]. Output stage of this CDBA offers low output impedance and a moderate output swing. This circuit is a class AB voltage buffer which is based on the differential FVF (DFVF) topology [14]. It uses two complementary DFVF cells, M_{12}-M_{16} and M_{11}-M_{15}, with current sources, M_{13} and M_{14}. The configuration of this CDBA is given in Fig 2.7

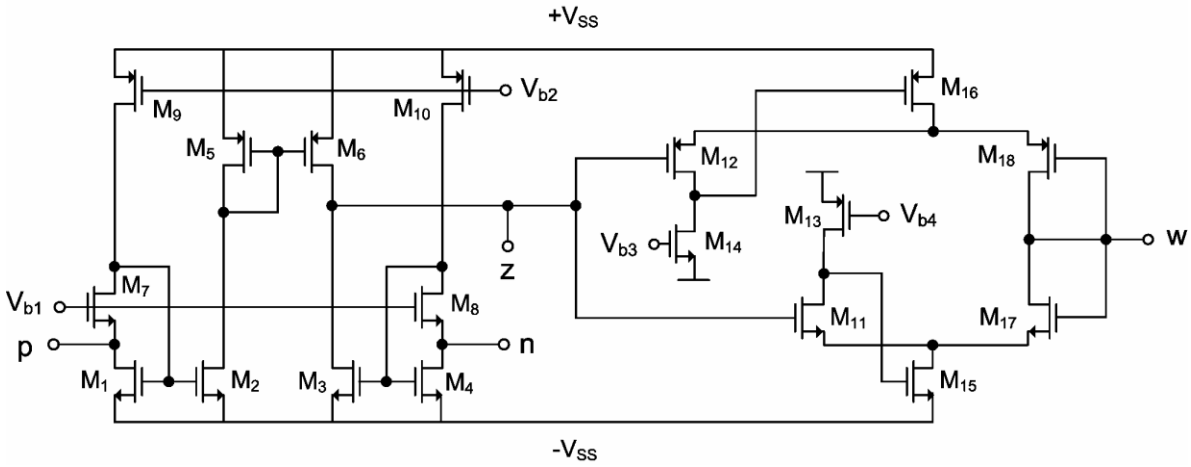

Fig 2. 7 Low-Voltage High-Performance CMOS Current Differencing Buffered Amplifier

Cem Cakir, Shahram Minaei, and Oguzhan Cicekoglu [16] in 2009 proposed a low voltage low power CMOS CDBA. The circuit can operate with the minimum supply voltage of ±0.6 volts. The terminal resistance of CMOS based CDBA's are quite high on the order of several hundred ohms and there voltage and current transfer ratios are smaller than one. Most of the existing CDBA's are operated at high supply voltages and they have much power consumptions, all these disadvantages are overcome by using this CDBA. Low voltage CDBA circuit, which is based on the use of the current differencing circuit (M_1–M_8) and the voltage buffer (M_9–M_{14}). The configuration of this CDBA is given in Fig 2.8

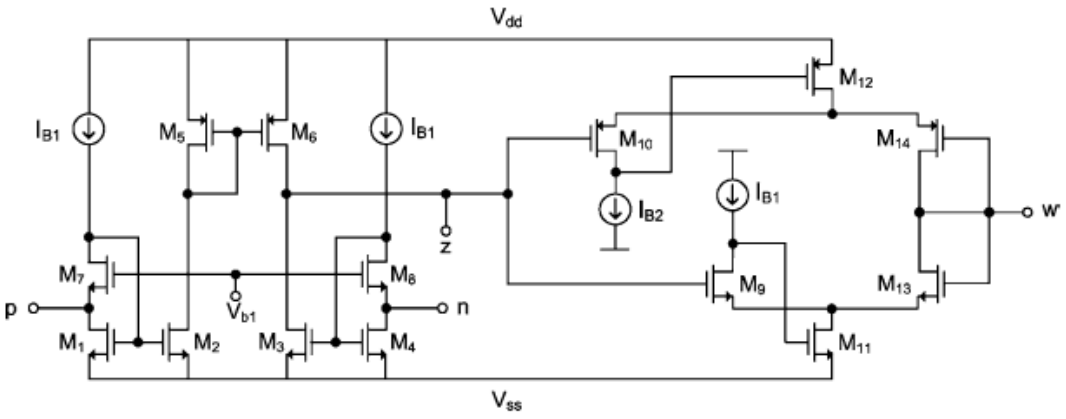

Fig 2. 8 Low voltage low power CMOS current differencing buffered amplifier

2.2 Literature Survey Of CDTA

Current differencing trans-conductance amplifier (CDTA), recently reported current-mode active building block, appears to be very useful for current-mode signal processing. Its advantages have been already shown in the literature [17-20]. Using the CDTA element, it is possible to obtain circuit solutions with less number of passive elements than its counterparts and it also leads to compact circuit structures requiring a few active building blocks in some applications [21]

The CDTA element with its schematic symbol in Fig 2.9 has a pair of low-impedance current inputs p and n, and an auxiliary terminal z, whose outgoing current is the difference of input currents.

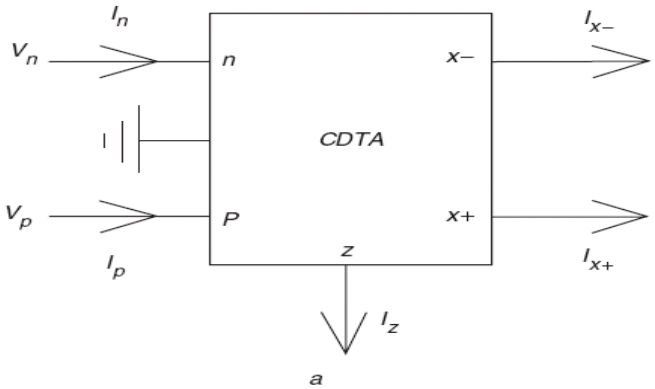

Fig 2. 9 CDTA block

Here, output terminal currents are equal in magnitude, but they flow in opposite directions, and the product of trans conductance (gm) and the voltage at the z terminal gives their magnitudes.

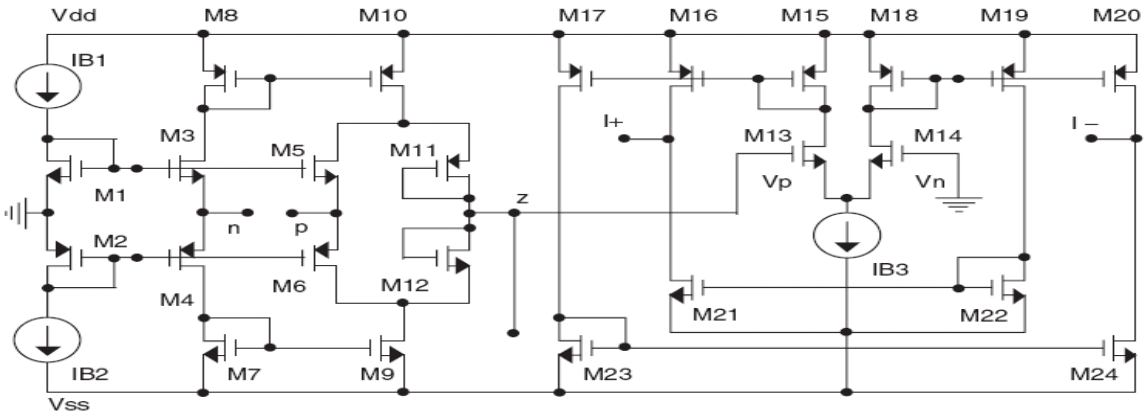

Fig 2. 10 CMOS based CDTA block

A possible CMOS-based CDTA circuit (A.U.Keskin and D. Biolek realization) suitable for the monolithic IC fabrication is displayed in Fig. 2.10. In this circuit, transistors from M_1 to M_{12} perform the current differencing operation while transistors from M_{13} toM_{24} convert the voltage at the z-terminal to output currents at the two outputs of the DO-OTA section[22]. Atilla Uygur1, Hakan Kuntman proposed a new circuit for the CDTA as shown below:

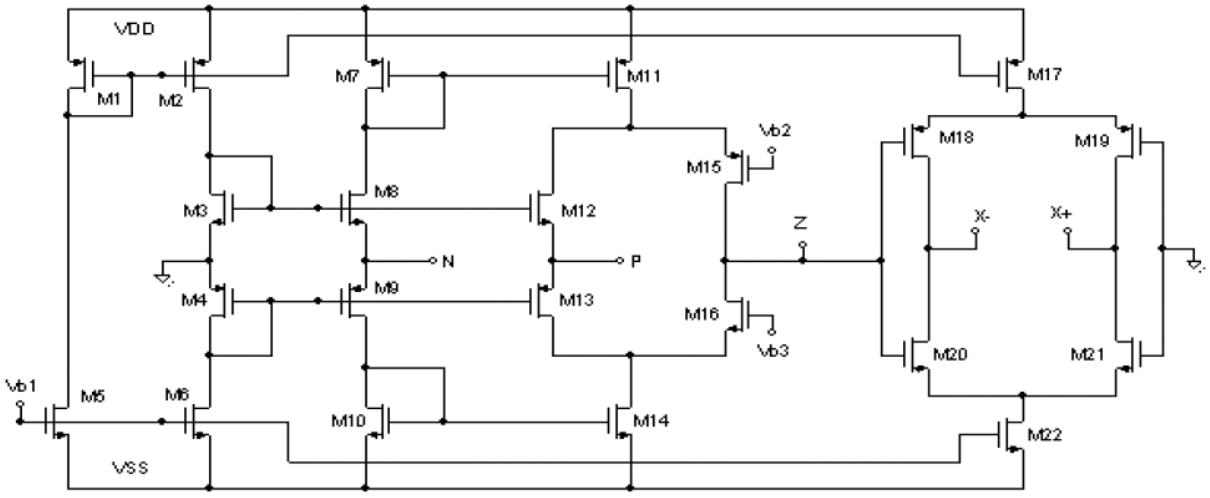

Fig 2. 11 CMOS based CDTA by Atilla Uygurl

Here M1-M16 form the current Differencing part and the M17-M22 forms the Trans conductance part[23].

Fırat KACAR1, Hulusi Hakan KUNTMAN2[23] proposed CMOS realization of the CDTA element is shown in Figure 2.12. Transistors M_1 to M_{24} form the input differential current-controlled current source (DCCCS) stage, which is used for transforming the differential input current to the intermediate voltage, or the voltage at the z terminal. Transistors M_{25} to M_{60} form the high-performance dual-output trans conductor stage[24].

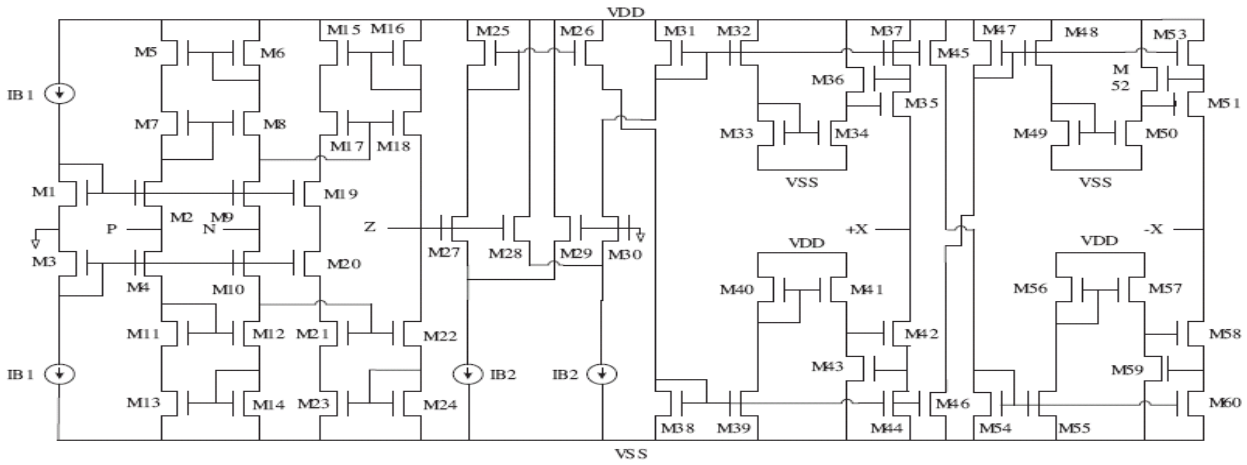

Fig 2. 12 A new, improved CMOS realization of CDTA

A. Uygur, H. Kuntman proposed Low -Voltage Current Differencing Transconductance Amplifier in a Novel All-pass Configuration CMOS realization of the CDTA element is in Fig. 2.13. The transistors M1 to M10 form the input stage of the CDTA element. In the current mirrors of the input stage, flipped voltage followers (FVF) are used.

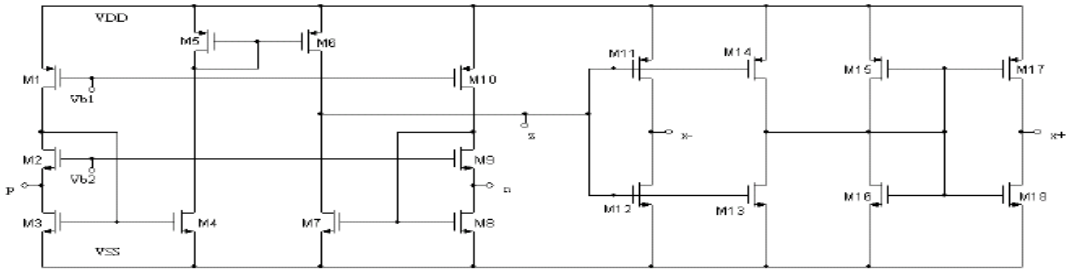

Fig 2. 13 Proposed Low -Voltage Current Differencing Transconductance Amplifier in a Novel All-pass Configuration

Feedback in FVF results in very low input resistances at the input terminals. Input resistance of the p and n terminals can be given using the output resistance of FVF. In the circuit, to construct the current mirrors, outputs of FVF are used as inputs of CDTA. M_2, M_3 and M_8, M_9 are FVF transistors [25]. This CDTA worked on the ±0.75 volts, this was less as compared to other proposed earlier.

CHAPTER 3

Low Voltage Low Power CMOS Current Differencing Buffered /Trans-Conductance Amplifier

3.1 Introduction

The major goal of this work is to present a new CMOS realization for current differencing buffered/ Transconductance amplifier (CDBTA). A design technique based on the flipped voltage follower currents source [14]-[15] is preferred to obtain a high performance CDBTA. The proposed circuit can operate with the minimum supply voltage of ±0.6 V. It also consumes less power. Moreover the proposed CDBTA has good voltage and current gain accuracies.

Low voltage circuit design has gained importance with the advent of the portable electronics and mobile communication systems. In recent years there has been much effort to decrease the supply voltage and to minimize the power consumption of the circuits. Current mode circuits are useful for the low voltage operation and therefore, they have been receiving a great deal of interest as an alternative to voltage mode circuits especially for analog signal processing applications.

In addition to the low voltage operations popularity of current mode circuits can be attributed to some other features as dynamic range, low power consumption and higher speed. Most of them mainly stem from the fact that there circuits have low impedance levels. Many active elements which are able to function in current mode such as current conveyor, current operational amplifier (COA)[3], operational trans resistance amplifier (OTRA) [5]and current differencing buffered amplifier (CDBA)[6] have been introduced as a response to these demands .The Current differencing buffered/transconductance amplifier operate in both current mode and voltage mode, which provides flexibility in circuit designing.

Moreover, it is free from many parasitic capacitances and appropriate for high frequency operation. The following section presents a brief circuit description of CDBTA. A high performance CDBTA based on flipped voltage follower technique is discussed.

3.2 Circuit Description

The block diagram and equivalent circuit of CDBTA are shown in Fig 3.1 CDBTA consists of 3 fundamental building blocks, which are namely

(i) Current differencing part
(ii) Voltage buffered part
(iii) Trans-conductance part

The current and voltage characteristics of CDBTA can be described by the following equations.

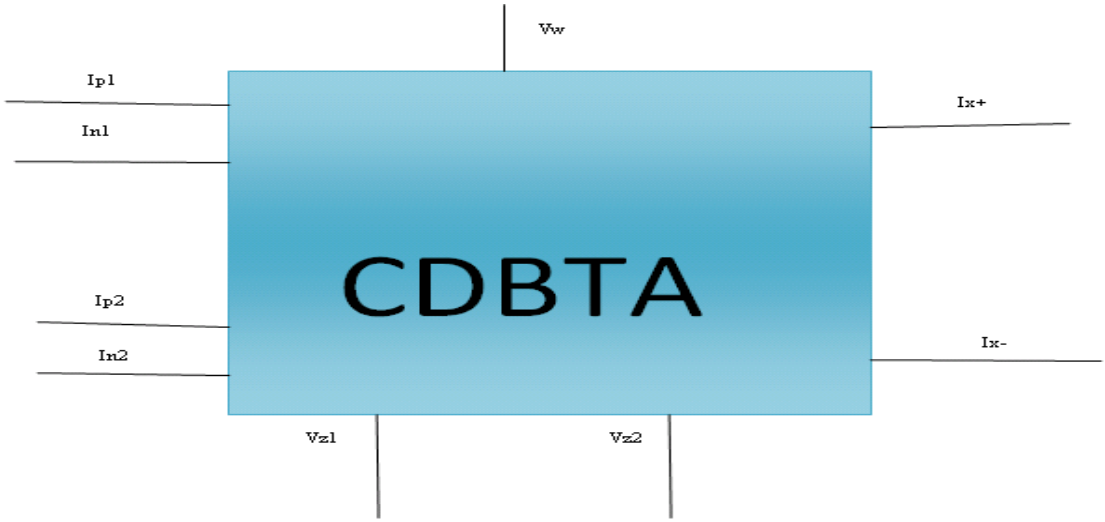

Fig 3. 1 Block Diagram for Current differencing Buffered /Trans-conductance Amplifier

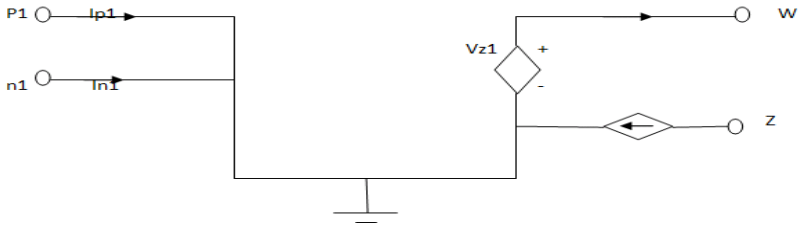

Fig 3. 2 Current Differencing Buffered part

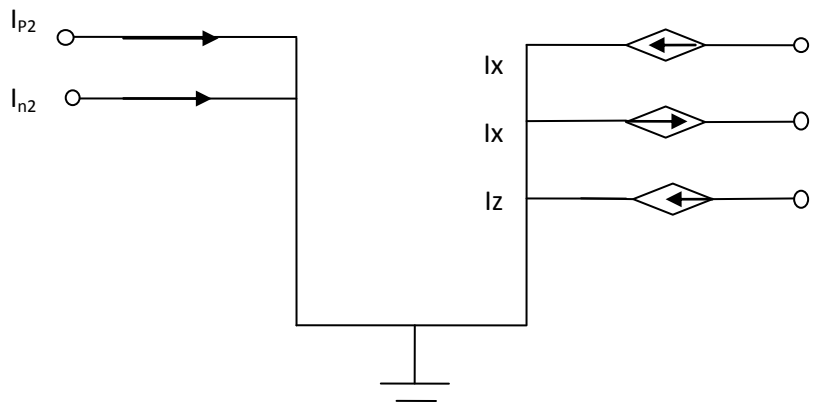

Fig 3. 3 Current Differencing Trans-conductance part

$$I_{z1} = \alpha_1 I_{p1} - \alpha_1 I_{n1} \quad (1)$$

$$I_{z2} = \alpha_2 I_{p2} - \alpha_1 I_{n2} \quad (2)$$

$$V_W = \beta_y V_{z1} \quad (3)$$

$$V_{p1} = V_{p2} = V_{n1} = V_{n2} = 0 \quad (4)$$

$$I_+ = g_m V_{z2} \quad (5)$$

$$I_+ = -g_m V_{z2} \quad (6)$$

Where α_1 , α_2 are current gain, β_v is voltage gain, they should be unity in ideal case

They can be expressed as $\alpha_{p1}=1-€_{p1}$ $\alpha_{p2}=1-€_{p2}$ $\alpha_{n1}=1-€_{n1}$ $\alpha_{n2}=1-€_{n2}$ denote the current tracking errors and $\beta v=1-€v$ denotes voltages tracking error.It is clear that $P_{1,2}$ and $N_{1,2}$ are current mode input terminal which have ideally zero impendence.

With $€_{p1}$, $€_{n1}$, $€_{p2}$, $€_{n2}$ <<1

$€_{p1}$,$€_{n,1}$ $€_{p2}$,$€_{n2}$ denote the current tracking errors and $€_v$ denotes the voltage tracking error.

The current of z_1, z_2 is equal to the difference of the two input currents I_p and I_n. Therefore it is defined as the current output which has ideally infinite impendence. Moreover, the voltage terminal w follows that of terminal z. Hence the terminal w is the voltage output that should have zero impedance.

3.3 Low Voltage CDBTA

Figure 3.4 shows the complete schematics of low voltage CDBTA circuit which is based on the use of current differencing circuit(M_1-M_8),(M_{15}-M_{22}),Voltage buffer (M_9-M_{14}) and tarns conductance (M_{23}-M_{30}).

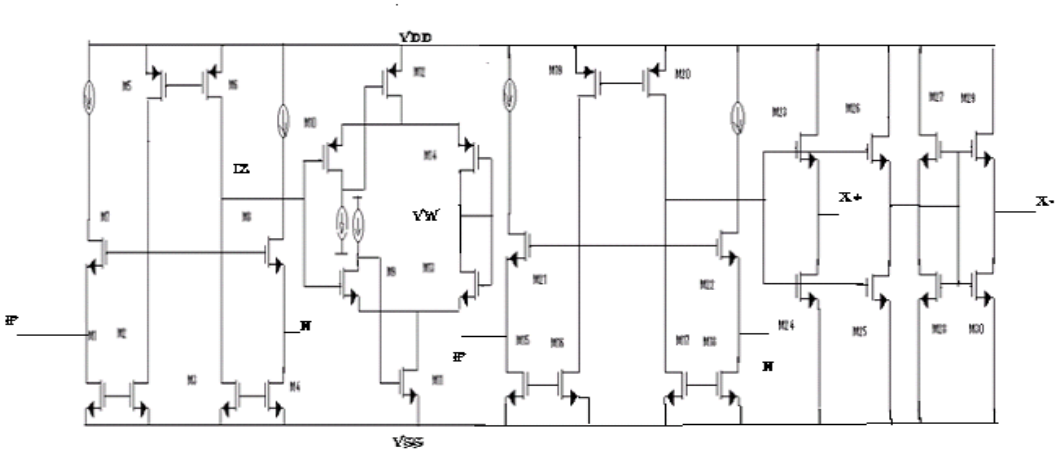

Fig 3. 4 Current Differencing Buffered /Trans conductance amplifier

The input resistance of FVFCS [14] looking at the node X in Fig 3.5 can be expressed as:

$$Rx = \frac{\frac{1}{gm2}*(1+rb/ro2)//r01}{gm1(rb||gm2*r01*r02)} \quad (7)$$

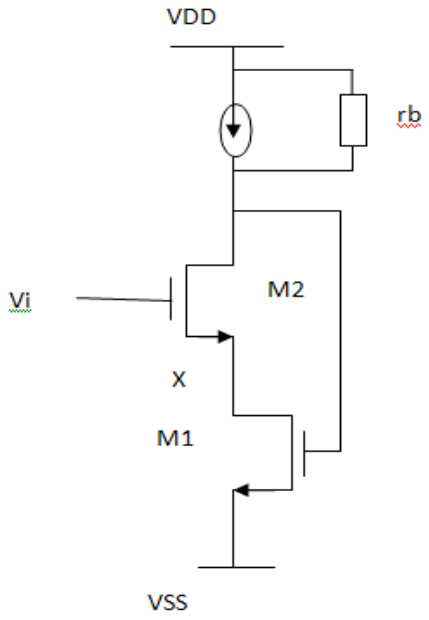

Fig 3. 5 Circuit for Finding Input Impedance

Where r_b is the output resistance of current source ,r_o is the output resistance and g_m is the trans conductance of the transistors. For a simple current source with $r_b = r_{o2}$ resistance at the node X in equation is changed to

$$Rx = \frac{2}{g_{m1}g_{m2}r_{o2}} \tag{8}$$

The current subtractor circuit is illustrated in Fig.3.6 which consists of the transistors M_1 to M_8 similarly for M_{15}-M_{22}. Current of the terminals-z follows the difference of the currents of terminal-p and terminal-n. Hence, we name terminal-z as current output. The current of the terminal-z can be expressed as follows:

$$I_Z = I_{B1} + I_p - (I_{B1} + I_n) = I_p - I_n \tag{9}$$

The current source, I_{B1} forces equal currents of 56 µA in the transistors (M_1–M_4). Thus, the gate to source voltages of these transistors will be equal, which forces the voltages of the two input terminals to be zero.

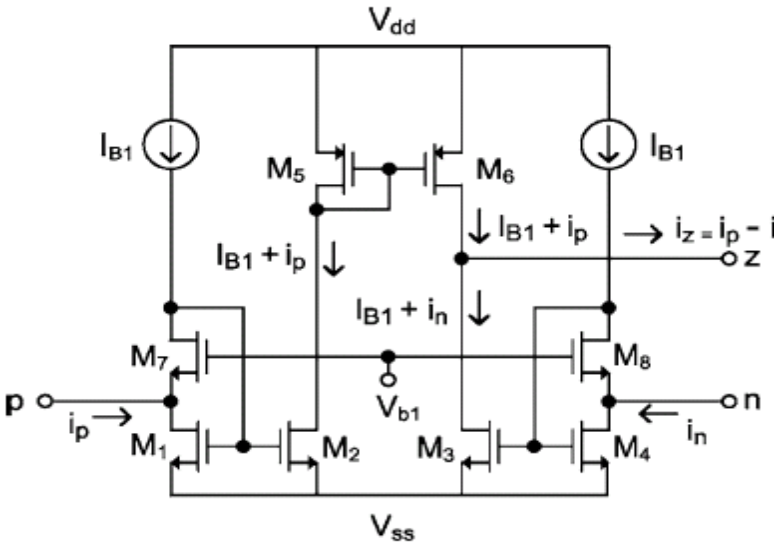

Fig 3. 6 Current Differencing circuit

3.4 Simulations Results

For the simulation UMC 0.18µm CMOS Technology is used. The aspect ratio of the transistors are shown in table 1. The current I_{b1},I_{b2} are selected as 56 µA and 84µA respectively. The proposed circuit is supplied by voltage of ±0.6v.

Table 1 Aspect ratio of MOS Transistors

MOSFET	W(µm)	L(µm)
M1-M4	3.6	1.8
M4-M8	180	1.8
M9	43	0.36
M10	240	0.36
M11	72	0.36
M12	240	0.36
M13	72	0.36
M14	240	0.36
M15	3.6	1.8
M16	3.6	1.8
M17	3.6	1.8
M18	3.6	1.8

M19	180	1.8
M20	180	1.8
M21	180	1.8
M22	180	1.8
M23	10	0.7
M24	44	1.4
M25	44	1.4
M26	10	0.7
M27	10	0.7
M28	4	1.4
M29	10	0.7
M30	4	1.4

Fig 3.7 shows input resistance for both buffered/trans conductance section of the circuit. Input resistance can be determineg by performing Ac analysis. Input resistance so determined is 35 Ω.

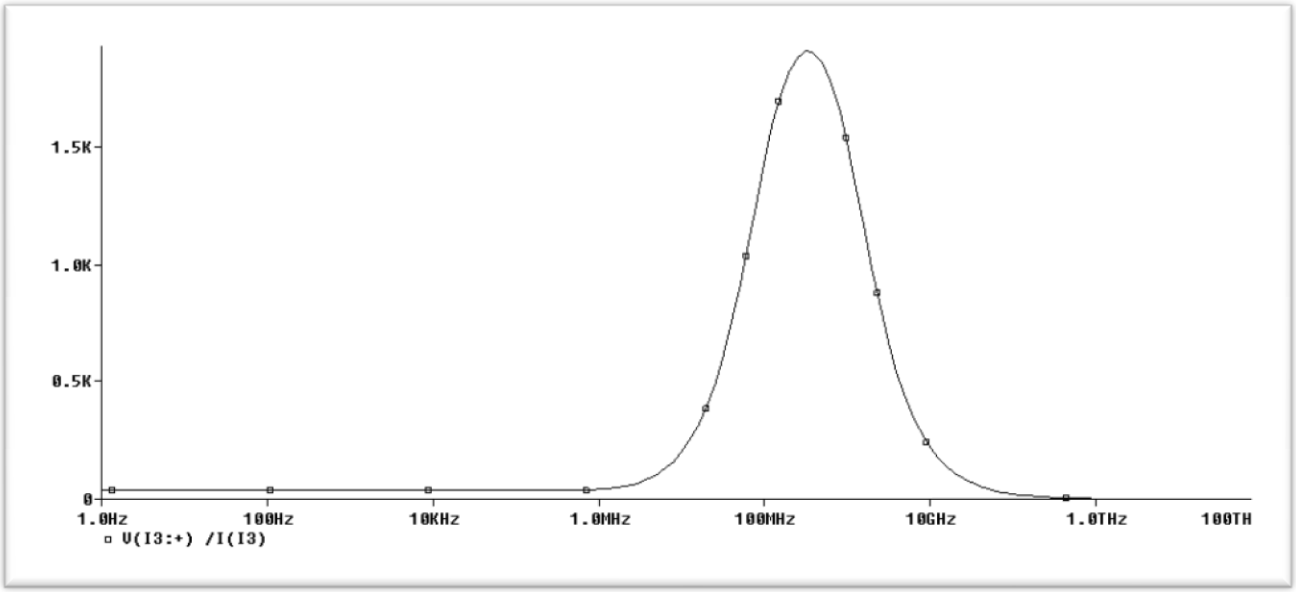

Fig 3. 7 Input resistances for both current differencing sections.

Fig 3.8 shows the resistance of the z terminal and is quite high of the order of 250 kΩ.

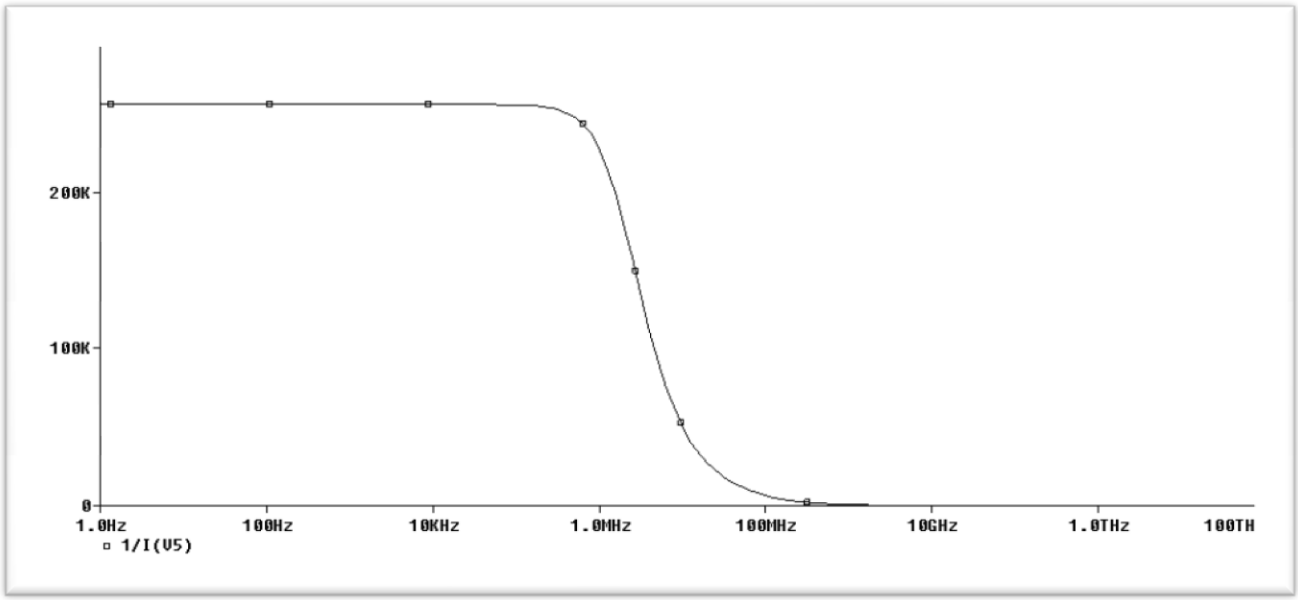

Fig 3. 8 Z Terminal Resistance

Fig 3.7 shows the output impedance of the current terminal of trans conductance part which is 16kΩ.

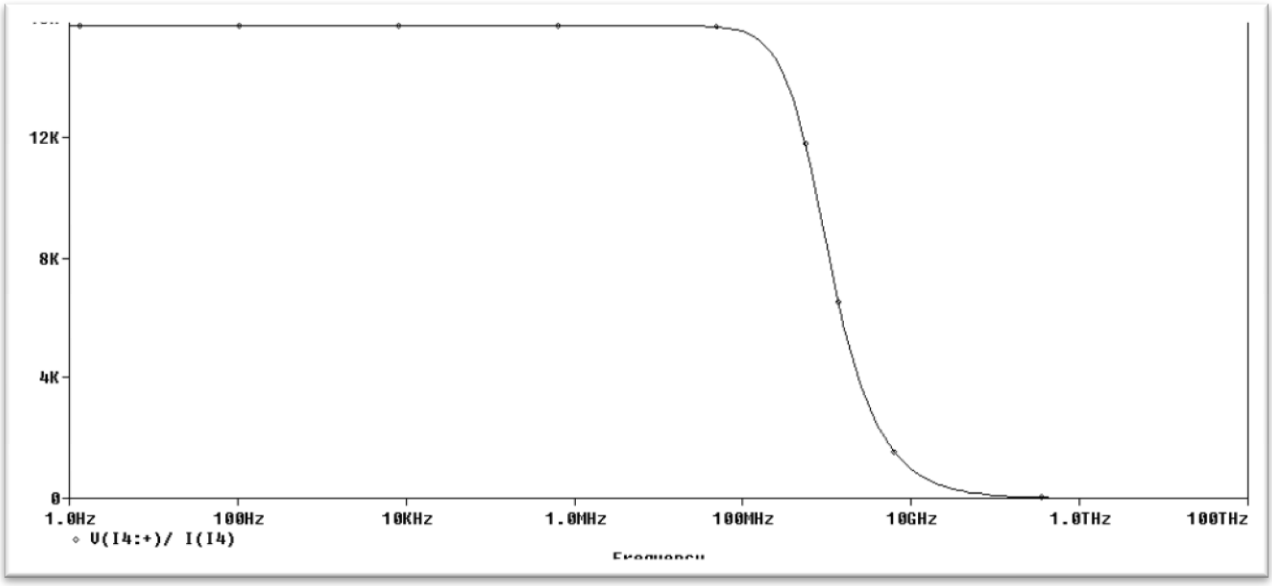

Fig 3. 9 Output resistances for Transconductance part.

Fig 3.10 shows output current of Z terminal by varying the current of I_{n1} from -60µA to 60µA.

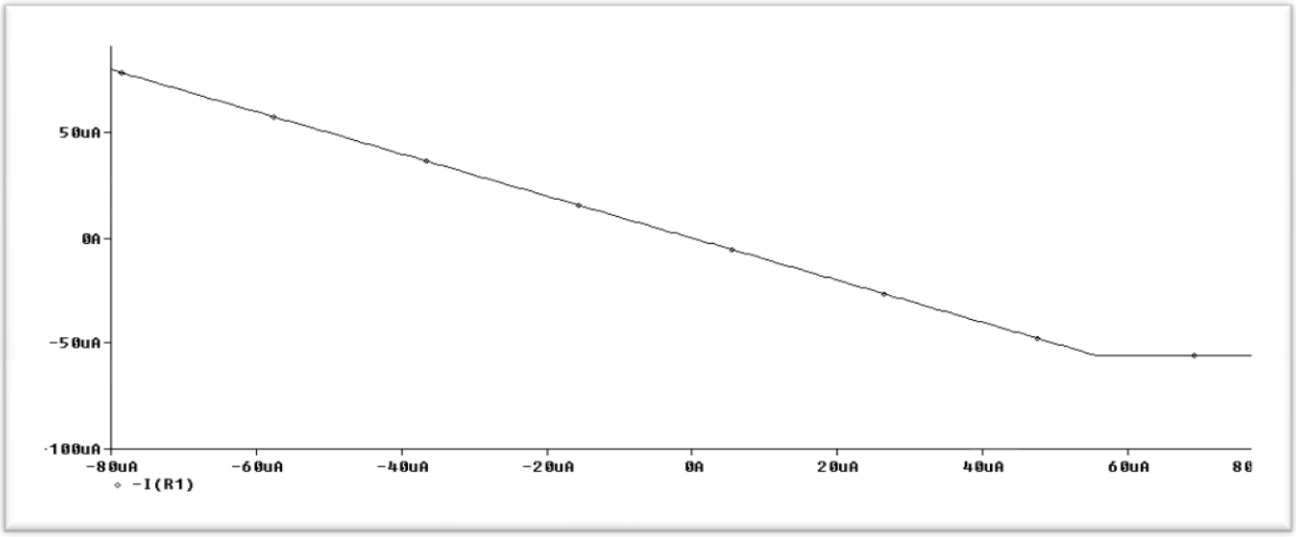

Fig 3. 10 z terminal current Vs In1

Fig 3.11 shows the variation of In1 current from -60µA to 60µA using DC analysis and plotting the output V_{Z1} along with the V_w i.e. the buffered voltage .

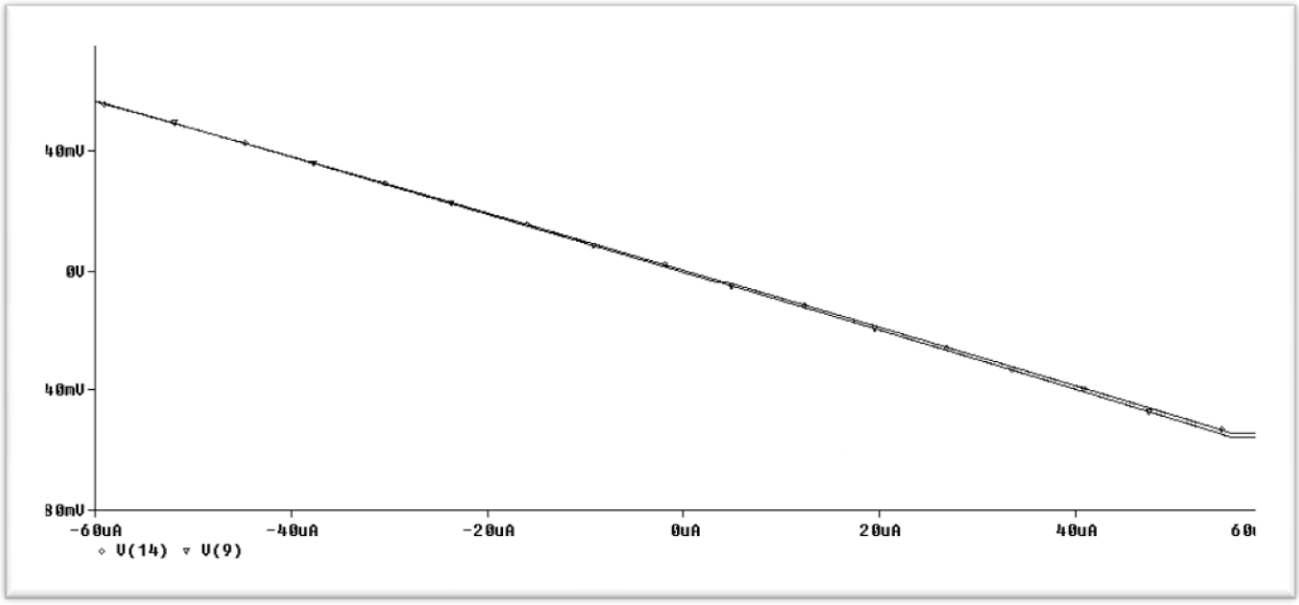

Fig 3. 11 Plot of Output voltage Vz and V_W Vs In

Fig 3.12, shows the output V_Z and the V_w for a variation of In1 from -60µA to 60µA .

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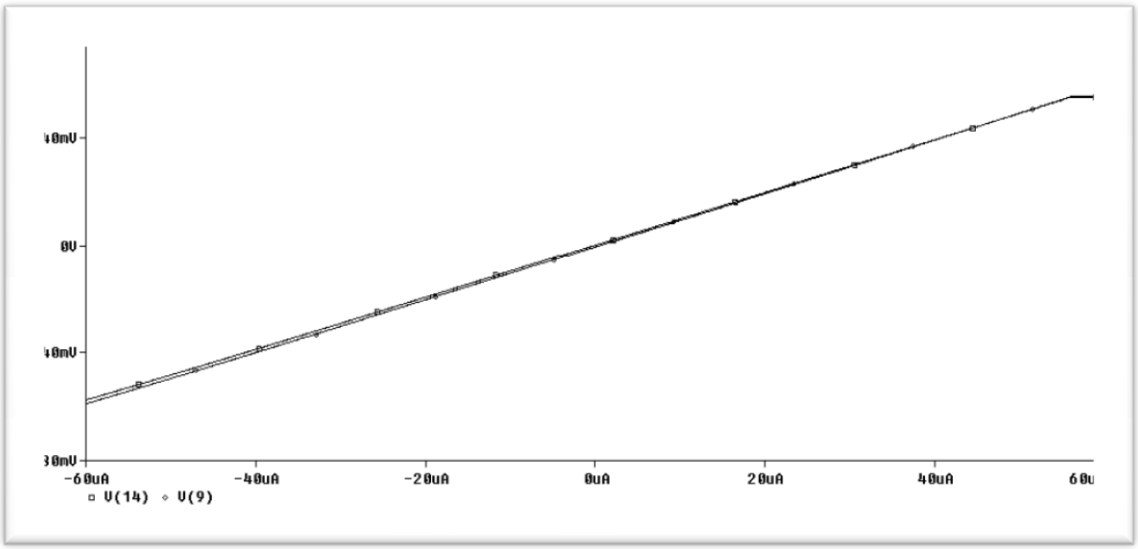


Fig 3. 12 Plot of Output voltage Vz1 and V_W obtained by varying Ip1 current

Fig3.13 shows the plot of I_{x+} and I_{x-} with respect to variation in I_{p2} current. I_{p2} results in the output current across the Z terminal and hence the voltage V_{z2} ,which is applied to the trans conductance stage. V_{z2} multiplied with the g_m produces output current I_{x+} and I_{x-}..

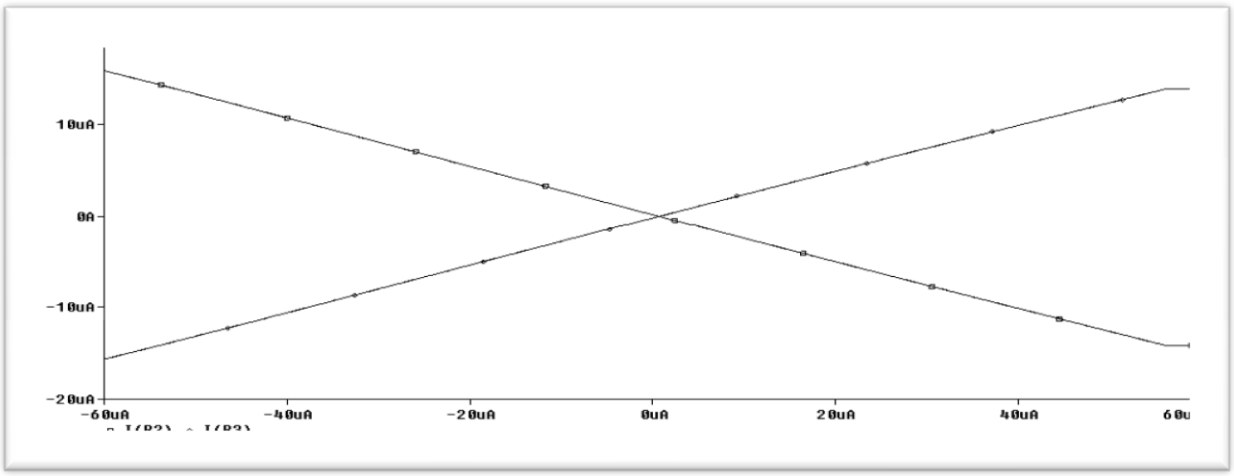


Fig 3. 13 Plot of Ix+ and Ix- current

Fig3.14 shows the plot for gm ,which is calculated by varying the input voltage and accordingly measuring the derivative of the current which gives the g_m. The value of gm which is obtained is 200uA/V.

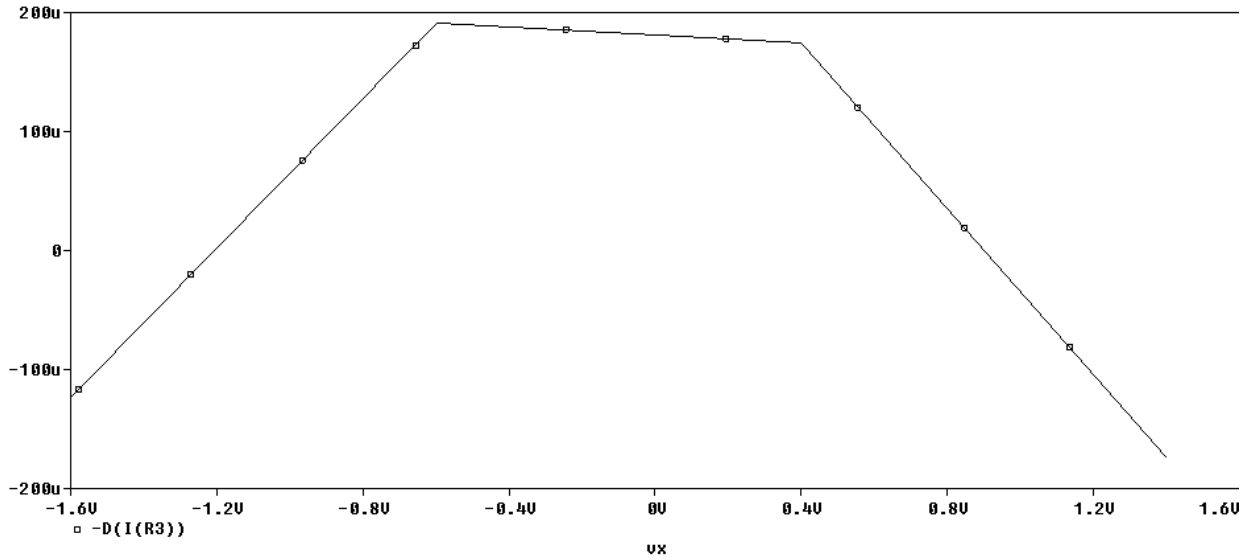


Fig 3. 14 Calculated gm for I+ and I- outputs

Fig3.15 shows the Impedance at the V_w terminal which comes out to be 350Ω.

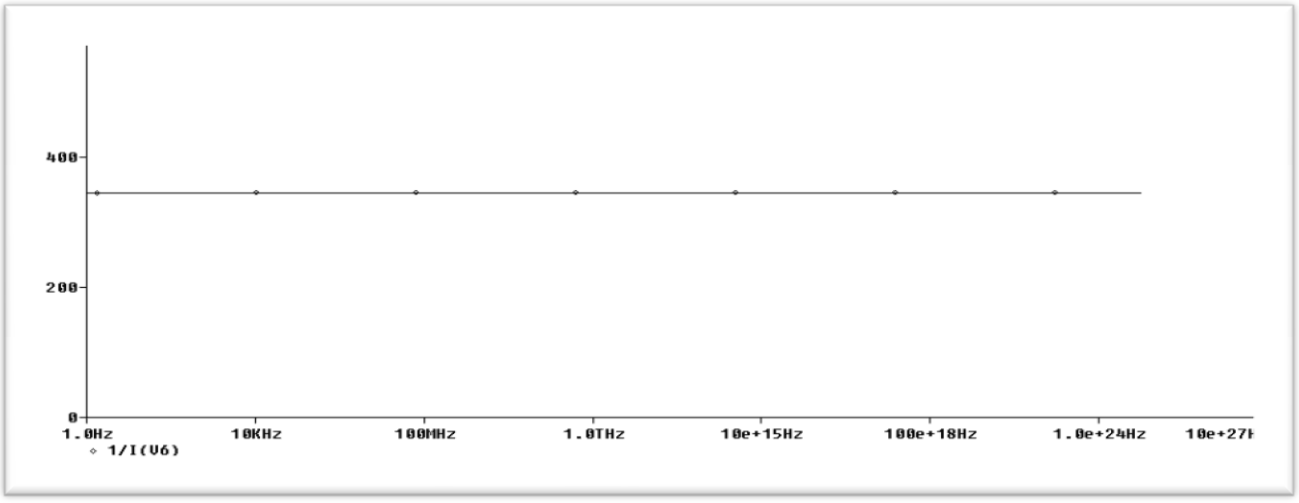


Fig 3. 15 Impedance at the V_W terminal

CHAPTER 4

Applications of CDBTA

4.1 Notch Filter

As an application example, a current-mode second-order notch filter circuit is implemented[6]. The current transfer function of the circuit is given as follows:

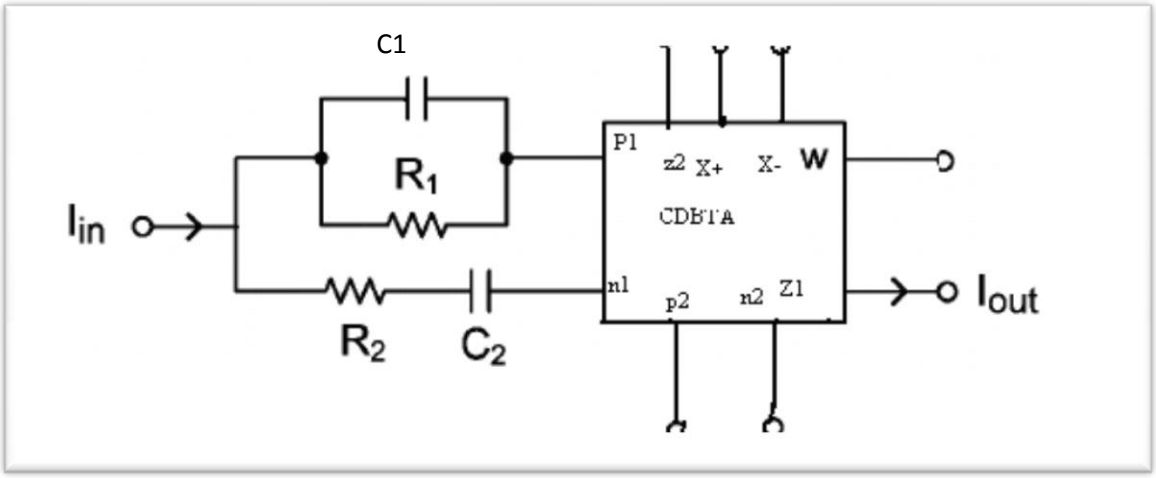
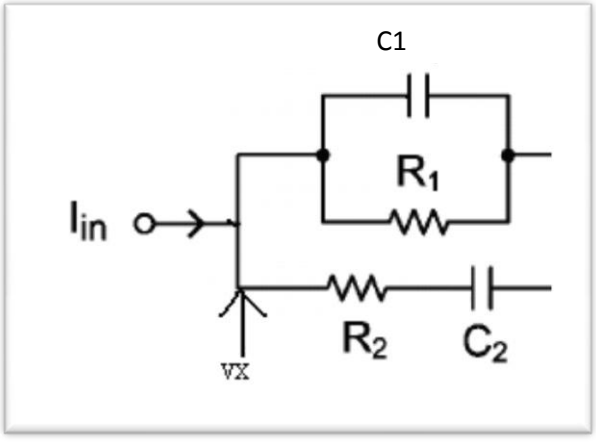


Fig 4. 1 Notch filter using CBDTA



Now calculating the value of Vx at the node

$$V_x = I_{in} \times (R_p || R_s)$$

Where

$R_p = \frac{R_1}{sR_1C_L+1}$ and $R_s = R_2 + \frac{1}{sC_2}$

Substituting $R_p||R_s$ in above equation

$$V_x = \frac{R_1(sR_2C_2+1)}{s^2C_1C_2R_1R_2+s(R_1C_1+R_2C_2+R_1C_2)+1} I_x \quad (9)$$

Now calculate the output current which is $I_{out} = I_p - I_n$

$$I_p = V_x/R_p$$

$$I_n = V_x/R_s$$

$$I_{out} = \frac{(s^2C_1C_2R_1R_2+s(R_1C_1+R_2C_2-R_1C_2)+1)}{R_1(sR_2C_2+1)} V_x \quad (10)$$

$I_{out}=(S^2*C_1*C_2*R_1*R_2+S*(R_2*C+R_1*C_2+R_1*C_1)+1)/(S^2*C_1*C_2*R_1*R_2+S*(R_{1*}C_1+R_2*C_2+R_1*C_2)+1)I_{in}$

$$I_{out} = \frac{(s^2C_1C_2R_1R_2+s(R_1C_1+R_2C_2-R_1C_2)+1)}{s^2C_1C_2R_1R_2+s(R_1C_1+R_2C_2+R_1C_2)+1} Iin \quad (11)$$

Therefore matching condition for the realization of the second-order notch filter will be $R_1C_2 = R1C1+R2C2$. The natural frequency, w_o and quality factor, Q for the filter can be expressed as:

$$\omega_o = \sqrt{\frac{1}{C_1C_2R_1R_2}} \quad (12)$$

$$Q = \sqrt{\frac{C_1C_2R_1R_2}{R_1C_1+R_2C_2+R_1C_2}} \quad (13)$$

To verify the theoretical analysis, this filter is simulated by using UMC 0.18 µm CMOS process parameters.

Fig 4.2 shows simulation result for notch filter. By taking the matching condition into consideration, external component values are chosen as R_1=50 k Ω, R_2=25 k Ω, C_1=25 pF and C_2=50 pF. The center frequency of the circuit is found as f_c=127 kHz which is in close agreement with the theoretical one.

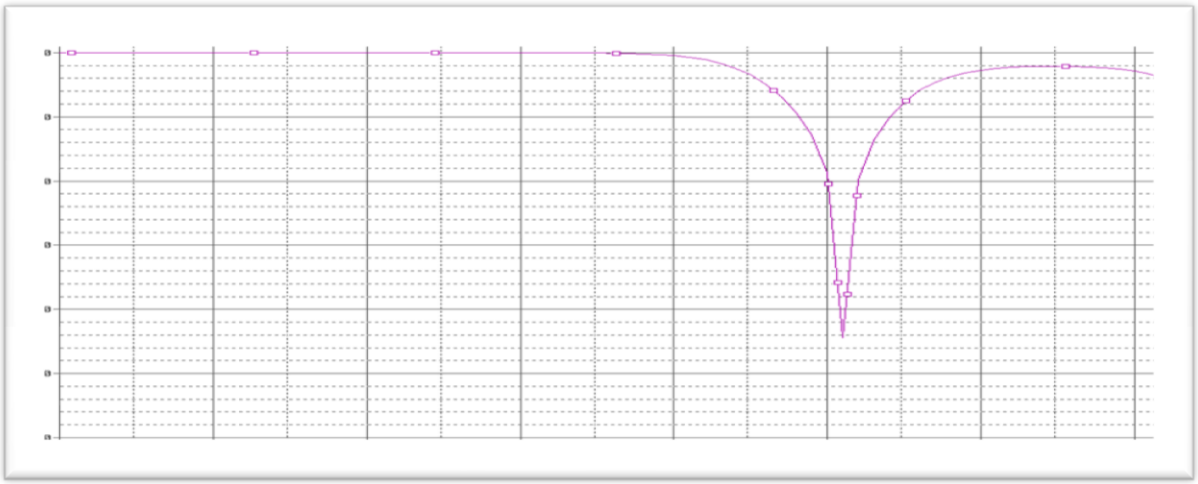


Fig 4. 2 Frequency Response of Notch Filter

4.2 A Four Quadrant Multiplier Using CDBTA

Four quadrant analog multiplier (FQAM) circuits perform real time multiplication of two bipolar signals V_x , V_y , and by preserving the correct polarity relationship, produce an output $V_o = kV_xV_y$, k being a scale factor. They find wide applications in communication. In this section the use of CDBTA is proposed in the realization of a FQAM with single-ended voltage output. It is shown that the CDBTA simplifies the design of such multipliers

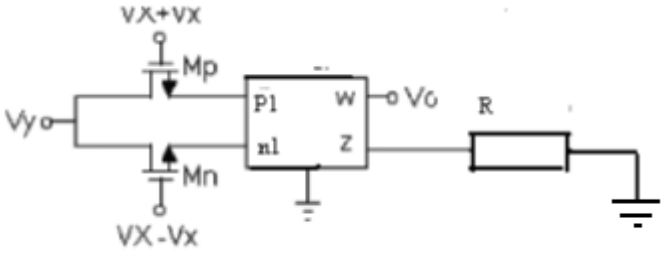


Fig 4. 3 Multiplier circuit using CDBTA

In the configuration shown in Fig.4.3, the MOSFETs, M_p, M_n are working in the linear region

V_x and V_y are time varying voltage signals, while V_X and V_Y are the bias voltages, and CDBTA inputs keep the sources of the two MOSFETs, M_p and M_n, virtually grounded. Here, the output currents are obtained from current equation in linear region

Where, $V_{GS} = V_X + V_x$ and $V_{DS} = V_y$,

$KM_p = KM_n = K$,

$$I_p = K(V_X + V_x - V_T - V_y/2)V_y \quad (14)$$

$$I_n = K(V_X - V_x - V_T - V_y/2)V_y \quad (15)$$

The difference of these currents provides

$$I_z = I_p - I_n = 2KV_xV_y \quad (16)$$

If we apply external resistance, then there will be an output voltage V_z which represents the multiplication of two input voltages. A 10 kHz voltage signal, V_y , with 1.2 V_{p-p} amplitude is multiplied by 1 kHz, V_x of the same amplitude . Fig4.4 shows resulting multiplication (modulation) signal at the output.

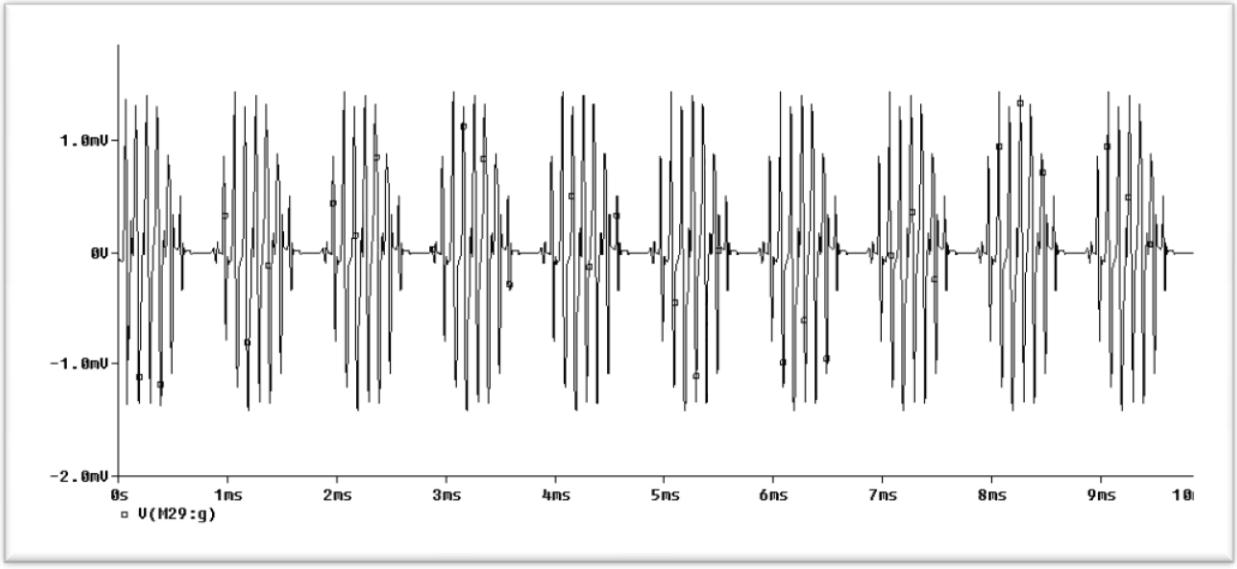


Fig 4. 4 Multiplier output

4.3 General Impedance Converter Using CBDTA

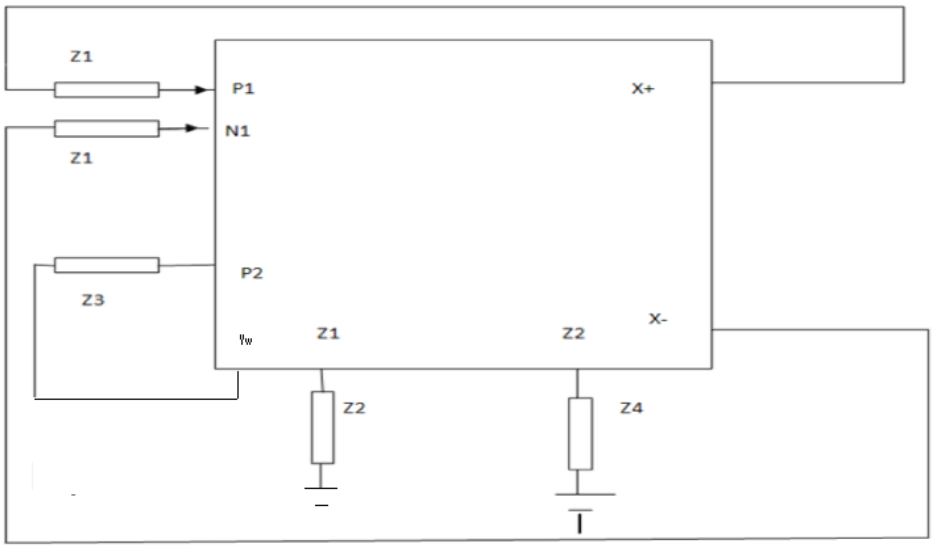


Fig 4. 5 General Impedance Converter

Active inductor simulation has been an important research topic in active network synthesis as realization of a spiral inductor in an integrated circuit has some drawbacks in the usage of space, weight, cost and tunability. These simulators find application in areas such as oscillator design, filter design, phase shifters and parasitic element cancellation.

A variety of inductance simulator using different high-performance active building blocks such as, Operational Transconductance Amplifiers (OTAs) current feedback op-amps, and four-terminal floating nullors (FTFNs), current conveyors , current differencing buffered amplifier (CDBAs) , operational transresistance amplifier, etc. are available in literature.

In this section a novel floating GIC using Current Differencing Buffered Trans conductance Amplifiers (CDBTA), is presented which can be used to implement the active inductor Capacitor and frequency dependent negative resistance(FDNR), with appropriate component choice.

From Fig 4.5 the input impedance can be derived. Routine analysis of the circuit results in following equations

$$I_{z1} = I_{p1} - I_{n1} = \frac{(V_1 - V_2)}{Z_1} \tag{17}$$

$$V_z = I_Z Z_2 = \frac{(V_1 - V_2)Z_2}{Z_1}$$

$V_w = V_z$ (18)

$$I_{p2} = \frac{V_w}{Z_3} = \frac{(V_1 - V_2)Z_2}{Z_1 Z_3} \quad (19)$$

$$V_{z2} = I_{p2} Z_4 = \frac{(V_1 - V_2)Z_2 Z_4}{Z_1 Z_3} \quad (20)$$

$$I_+ = g_m V_{z2} = \frac{(V_1 - V_2)Z_2 Z_4 g_m}{Z_1 Z_3} \quad (21)$$

$$I_- = -g_m V_{z2} = \frac{-(V_1 - V_2)Z_2 Z_4 g_m}{Z_1 Z_3} \quad (22)$$

Which gives

$$\frac{(V_1 - V_2)}{I_+} = \frac{Z_1 Z_3}{Z_2 Z_4 g_m} \quad (23)$$

$$Z_{in} = \frac{Z_1 Z_3}{Z_2 Z_4 g_m} \quad (24)$$

Proper choice of components in Z_{in} helps in implementing floating inductor, capacitor or FDNR

(i) Inductor : $Z_1 = R_1$, $Z_2 = R_2$, $Z_3 = R_3$, $Z_4 = 1/sC_4$

$$Z_{in} = \frac{R_1 R_3}{R_2 (1/sC_4) g_m} \quad (25)$$

$$Z_{in} = sL_{eq}$$

(ii) Capacitor: $Z_1 = R_1$, $Z_2 = R_2$, $Z_3 = 1/sC_3$, $Z_4 = R_4$

$$Z_{in} = \frac{R_1 (1/sC_3)}{R_2 R_4 g_m} \quad (26)$$

$$Z_{in} = 1/sC_{eq}$$

(iii) FDNR: $Z_1 = 1/sC_1$, $Z_2 = R_2$, $Z_3 = 1/sC_3$, $Z_4 = R_4$

$$Z_{in} = \frac{(1/sC_1)(1/sC_3)}{R_2 R_4 g_m} \quad (27)$$

This represents a type-D floating FDNR with the general form $1/Ds^2$, where $D = C_1 C_3 R_2 R_4 g_m$

For verification the functionality of the proposed GIC, it is used in an RLC circuit.

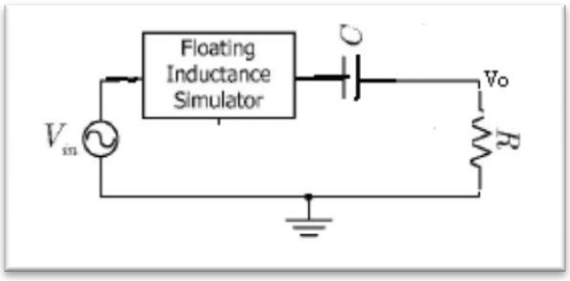


Fig 4. 6 RLC circuit with GIC

For floating inductor selecting $Z_1 = Z_2 = Z_3 = 1k\Omega$, $Z_4 = 1/s(1nf)$ and $g_m = 200\mu\, A/V$, results in inductance value of L_{eq} = 5mH.

Therefore, $f = \frac{1}{(2*3.14*\sqrt{10^{-9}*5*10^{-3}})} = 71.21kHz$

C=1nf and R=1k for above circuit

Theoretically calculated frequency and the observed frequency as shown in Fig 4.7 for Band pass filter are found in close agreement.

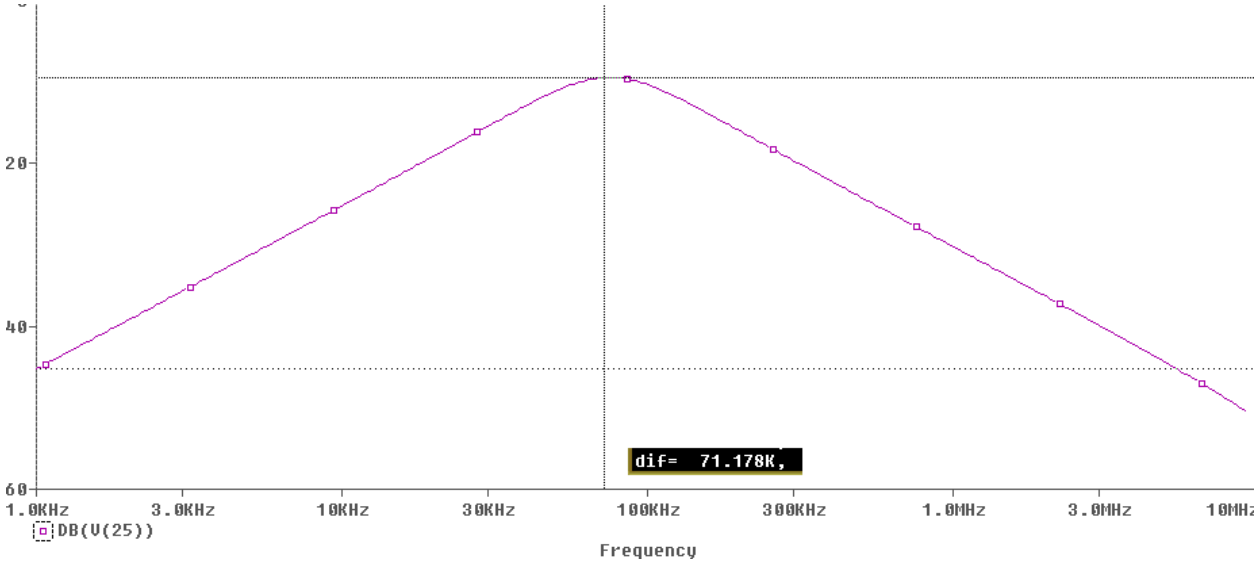


Fig 4. 7 Bandpass Output response for RLC circuit

CONCLUSION

In this Thesis a novel CMOS current differencing buffered Trans conductance amplifier (CDBTA) is proposed, which is suitable for low voltage operation. Proposed circuit operates with the power supplies of ±0.6 V. It has both voltage and current output which makes it versatile for many application. The Table below summarizes impedances at different terminals.

Parameter	Schematics(Values)
Input n1,2-terminal resistance(Ω)	35
Input p1,2 terminal resistance(Ω)	35
Terminal-z resistance(K Ω)	250
Terminal-w resistance (Ω)	350
Terminal-X+ resistance (KΩ)	16
Terminal-X- resistance (KΩ)	16
Gm(UA/V)	200

UMC 0.18 Um Spice parameters are used for SPICE simulations. Few applications of CDBTA namely notch filter, multiplier and general impedance converter are designed and simulated and the results of these circuits are found to be in close agreement with theoretical results.

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APPENDIX- I

PSPICE

PSpice, now developed towards more complex industry requirements, is integrated in the complete systems design flow from OrCAD and Cadence Allegro. It also supports many additional features, which were not available in the original Berkeley code like Advanced Analysis with automatic optimization of a circuit, encryption, a Model Editor, support of parameterized models, has several internal solvers, auto-convergence and checkpoint restart, magnetic part editor and Tabrizi core model for non-linear cores.

Pspice Products Included In Orcad

- PSpice
- PSpice A/D — a mixed-signal simulator, that provides a complete simulation environment for designs that contain both analog and digital electronic parts.
- PSpice Advanced Analysis incorporates five capabilities — sensitivity analysis, Monte Carlo (yield) analysis, Parametric Plotter and the already mentioned Optimization and Smoke analysis.

File Types Used And Created By Pspice

The basic input file for PSpice is a text (ASCII) file that has the file type "CIR." In the beginning, this will be created by hand as the primary method of getting the circuit we want modeled into the PSpice program. Later, when we use the schematic capture program, it will create the *.CIR file for us, along with several auxiliary file types. The output file always generated by PSpice is a text (ASCII) file that has the file type "OUT . This output file is created even if run is unsuccessful due to input errors. The cause for failure is reported in the *.OUT file, so this is a good place to start looking when you need to debug your simulation model. You examine the *.OUT file with the TextEdit or Notepad programs. When everything works properly, the output results are found in this file if a DC analysis is performed. If running a transient analysis or a frequency sweep analysis, there will be too much data for the *.OUT file.

In these cases, we add a command to the *.CIR file that tells PSpice to save the numerical data in a *.DAT file.The aforementioned *.DAT file is by default a binary (i.e., non-ASCII) file that requires a MicroSim application called PROBE to see the data. PROBE is installed with PSpice from the CD-ROM. The default storage format can be changed to ASCII if needed. This is not recommended because it requires more disk space to store the data in ASCII code. A companion file to the *.DAT file is the *.PRB file which holds initializing information for the PROBE program. Another common method used by experienced PSpice users is the use of *.INC (include) files. These enable to store frequently used subcircuits that have not yet been added to a library. One can access these *.INC files with a single command line in the *.CIR file very conveniently. Other files used with PSpice are *.LIB files where the details of complex parts are saved. Additional file types includes *.SCH (the schematic data, itself), *.ALS (alias files) and *.NET (network connection files).

Some Facts And Rules About Pspice

- PSpice is not case sensitive. This means that names such as *Vbus*, *VBUS*, *vbus* and even *vBuS* are equivalent in the program.
- All element names must be unique. Therefore, you can't have two resistors that are both named "Rbias," for example.
- The first line in the data file is used as a title. It is printed at the top of each page of output. You should use this line to store your name, the assignment, the class and any other information appropriate for a title page. PSpice will ignore this line as circuit data. Do not place any actual circuit information in the first line.
- There must be a node designated "0." (Zero) This is the reference node against which all voltages are calculated.
- Each node must have at least two elements attached to it.
- The last line in any data file must be ".END" (a period followed by the word "end.")
- All lines that are not blank (except for the title line) must have a character in column 1, the leftmost position on the line.
    - Use "*" (an asterisk) in column 1 in order to create a comment line.

- Use "+" (plus sign) in column 1 in order to continue the previous line (for better readability of very long lines).
- Use "." (period) in column 1 followed by the rest of the "dot command" to pass special instructions to the program.
- Use the designated letter for a part in column 1 followed by the rest of the name for that part (no spaces in the part name).

- Use "whitespace" (spaces or tabs) to separate data fields on a line.
- Use ";" (semicolon) to terminate data on a line if you wish to add commentary information on that same line.

PSpice is a computer program used mostly by engineers and scientists. Accordingly, it was created with the ability to recognize the typical metric units for numbers. Unfortunately, PSpice cannot recognize Greek fonts or even upper vs. lower case. Thus our usual understanding and use of the standard metric prefixes has to be modified. For example, in everyday usage, "M" indicates "mega" (10^6) and "m" stands for milli (10^{-3}). Clearly, this would be ambiguous in PSpice, since it is not case sensitive. Thus, in PSpice, a factor of 10^6 is indicated by "MEG" or "meg." "M" or "m" is reserved for 10^{-3}. Another quirk of PSpice is the designation for 10^{-6}. In most publications, the Greek letter, μ, is used for this multiple. Since there can be no Greek fonts (or any other special font designations) in PSpice, the early developers of PSpice borrowed a trick from those who used typewriters. Before the IBM Selectric typewriter was introduced, most writers of technical papers had to improvise for Greek letters. Since the Latin letter "u" (at least in lower case) sort of resembled the lower case Greek μ, it was widely used as a substitute for μ. Hence, either "U" or "u" stands for 10^{-6} in PSpice.

METRIC PREFIX DESIGNATIONS USED IN PSPICE:

Number		Prefix	*Common Name*
10^{12}	-	"T" or "t"	*tera*
10^{9}	-	"G" or "g"	*giga*
10^{6}	-	"MEG" or "meg"	*mega*
10^{3}	-	"K" or "k"	*kilo*
10^{-3}	-	"M" or "m"	*milli*
10^{-6}	-	"U" or "u"	*micro*

10^{-9} - "N" or "n" *nano*

10^{-12} - "P" or "p" *pico*

10^{-15} - "F" or "f" *femto*

An alternative to this type of notation, which is in fact, the default for PSpice output data, is "textual scientific notation." This notation is written by typing an "E" followed by a signed or unsigned integer indicating the power of ten.

APPENDIX-II

Model :180nm

MOSIS PARAMETRIC TEST RESULTS

RUN: T42P (MM_NON-EPI) VENDOR: TSMC
TECHNOLOGY: SCN018 FEATURE SIZE: 0.18 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: DSCN6M018_TSMC

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	0.27/0.18			
Vth		0.51	-0.53	volts
SHORT	20.0/0.18			
Idss		581	-282	uA/um
Vth		0.52	-0.53	volts
Vpt		4.6	-5.4	volts
WIDE	20.0/0.18			
Ids0		19.5	-8.0	pA/um
LARGE	50/50			
Vth		0.43	-0.41	volts
Vjbkd		3.1	-4.2	volts
Ijlk		<50.0	<50.0	pA
K' (Uo*Cox/2)		171.3	-35.9	uA/V^2
Low-field Mobility		406.79	85.25	cm^2/V*s

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameters XL and XW in your SPICE model card.

Design Technology	XL (um)	XW (um)
SCN6M_DEEP (lambda=0.09)	0.00	-0.01

thick oxide 0.00 -0.01
SCN6M_SUBM (lambda=0.10) -0.02 0.00
Thick oxide -0.02 0.00

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>6.6	<-6.6	volts

PROCESS PARAMETERS	N+	P+	POLY	N+BLK	PLY+BLK	M1	M2	UNITS
Sheet Resistance			6.4	7.3	7.5	61.0	318.2	0.08	0.08	ohms/sq
Contact Resistance				9.5	10.1	8.7			4.73	ohms
Gate Oxide Thickness					41					angstrom

PROCESS PARAMETERS	M3	POLY_HRI	M4	M5	M6	N_W	UNITS
Sheet Resistance	0.08	1004.0	0.07	0.07	0.03	924	ohms/sq
Contact Resistance	9.10		13.49	17.38	19.58		ohms

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	0.76	volts
Vinv	1.5	0.79	volts
Vol (100 uA)	2.0	0.08	volts
Voh (100 uA)	2.0	1.64	volts
Vinv	2.0	0.83	volts
Gain	2.0	-21.78	
Ring Oscillator Freq.			
D1024_THK (31-stg,3.3V)		320.91	MHz
DIV1024 (31-stg,1.8V)		388.85	MHz
Ring Oscillator Power			
D1024_THK (31-stg,3.3V)		0.07	uW/MHz/gate
DIV1024 (31-stg,1.8V)		0.02	uW/MHz/gate

COMMENTS: DEEP_SUBMICRON

T42P SPICE BSIM3 VERSION 3.1 PARAMETERS

SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

* DATE: Apr 27/04
* LOT: T42P WAF: 8003
* Temperature_parameters=Default
.MODEL CMOSN NMOS (LEVEL = 49

```
+VERSION = 3.1          TNOM    = 27          TOX     = 4.1E-9
+XJ      = 1E-7         NCH     = 2.3549E17   VTH0    = 0.3672292
+K1      = 0.5893162    K2      = 3.053194E-3 K3      = 1E-3
+K3B     = 1.8246765    W0      = 1E-7        NLX     = 1.771394E-7
+DVT0W   = 0            DVT1W   = 0           DVT2W   = 0
+DVT0    = 1.2540673    DVT1    = 0.3671218   DVT2    = 0.0374285
+U0      = 262.3448599  UA      = -1.473692E-9 UB     = 2.452512E-18
+UC      = 6.566514E-11 VSAT    = 1.025312E5  A0      = 2
+AGS     = 0.4532362    B0      = 3.222688E-7 B1      = 5E-6
+KETA    = -0.0109204   A1      = 0           A2      = 0.9744209
+RDSW    = 105          PRWG    = 0.5         PRWB    = -0.2
+WR      = 1            WINT    = 1.660932E-9 LINT    = 1.520122E-8
+XL      = 0            XW      = -1E-8       DWG     = -2.794177E-9
+DWB     = 7.839758E-9  VOFF    = -0.091184   NFACTOR = 2.2684002
+CIT     = 0            CDSC    = 2.4E-4      CDSCD   = 0
+CDSCB   = 0            ETA0    = 3.031184E-3 ETAB    = 9.427488E-6
+DSUB    = 0.0153239    PCLM    = 0.704686    PDIBLC1 = 0.2435533
+PDIBLC2 = 2.76003E-3   PDIBLCB = -0.1        DROUT   = 0.8035265
+PSCBE1  = 4.372065E10  PSCBE2  = 2.518414E-9 PVAG    = 0.0749313
+DELTA   = 0.01         RSH     = 6.4         MOBMOD  = 1
+PRT     = 0            UTE     = -1.5        KT1     = -0.11
+KT1L    = 0            KT2     = 0.022       UA1     = 4.31E-9
+UB1     = -7.61E-18    UC1     = -5.6E-11    AT      = 3.3E4
+WL      = 0            WLN     = 1           WW      = 0
+WWN     = 1            WWL     = 0           LL      = 0
+LLN     = 1            LW      = 0           LWN     = 1
+LWL     = 0            CAPMOD  = 2           XPART   = 0.5
+CGDO    = 8.79E-10     CGSO    = 8.79E-10    CGBO    = 1E-12
+CJ      = 9.605878E-4  PB      = 0.8         MJ      = 0.3831903
+CJSW    = 2.643918E-10 PBSW    = 0.8         MJSW    = 0.1407086
+CJSWG   = 3.3E-10      PBSWG   = 0.8         MJSWG   = 0.1407086
+CF      = 0            PVTH0   = -6.317463E-6 PRDSW  = -2.8440536
+PK2     = 9.250773E-4  WKETA   = 1.074587E-3 LKETA   = -7.453047E-3
+PU0     = 4.3638022    PUA     = -1.50117E-12 PUB     = 0
+PVSAT   = 1.356677E3   PETA0   = 1.003159E-4 PKETA   = -2.902589E-3  )
*
.MODEL CMOSP PMOS (                LEVEL   = 49
+VERSION = 3.1          TNOM    = 27          TOX     = 4.1E-9
+XJ      = 1E-7         NCH     = 4.1589E17   VTH0    = -0.38888
+K1      = 0.5636481    K2      = 0.0308017   K3      = 0
+K3B     = 7.400372     W0      = 1E-6        NLX     = 1.385693E-7
+DVT0W   = 0            DVT1W   = 0           DVT2W   = 0
+DVT0    = 0.5846878    DVT1    = 0.2165736   DVT2    = 0.1
+U0      = 113.6325808  UA      = 1.459877E-9 UB      = 1.18636E-21
+UC      = -1E-10       VSAT    = 2E5         A0      = 1.7849198
```

```
+AGS     = 0.3754547      B0      = 3.172437E-7    B1      = 7.280105E-7
+KETA    = 0.0156934      A1      = 0.3222966      A2      = 0.3
+RDSW    = 196.7345438    PRWG    = 0.5            PRWB    = -0.1589203
+WR      = 1              WINT    = 0              LINT    = 2.702835E-8
+XL      = 0              XW      = -1E-8          DWG     = -2.627805E-8
+DWB     = 1.03876E-9     VOFF    = -0.0927458     NFACTOR = 2
+CIT     = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0              ETA0    = 0.145648       ETAB    = -0.0543017
+DSUB    = 0.9610783      PCLM    = 2.0812378      PDIBLC1 = 7.131255E-4
+PDIBLC2 = 0.0185628      PDIBLCB = -9.170788E-4   DROUT   = 0
+PSCBE1  = 3.206374E9     PSCBE2  = 9.279285E-10   PVAG    = 15
+DELTA   = 0.01           RSH     = 7.3            MOBMOD  = 1
+PRT     = 0              UTE     = -1.5           KT1     = -0.11
+KT1L    = 0              KT2     = 0.022          UA1     = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11       AT      = 3.3E4
+WL      = 0              WLN     = 1              WW      = 0
+WWN     = 1              WWL     = 0              LL      = 0
+LLN     = 1              LW      = 0              LWN     = 1
+LWL     = 0              CAPMOD  = 2              XPART   = 0.5
+CGDO    = 6.41E-10       CGSO    = 6.41E-10       CGBO    = 1E-12
+CJ      = 1.136354E-3    PB      = 0.8459606      MJ      = 0.4088875
+CJSW    = 2.255183E-10   PBSW    = 0.832695       MJSW    = 0.3342249
+CJSWG   = 4.22E-10       PBSWG   = 0.832695       MJSWG   = 0.3342249
+CF      = 0              PVTH0   = 4.532819E-3    PRDSW   = 7.6587079
+PK2     = 3.513392E-3    WKETA   = 0.0251295      LKETA   = -2.32504E-3
+PU0     = -2.4738884     PUA     = -8.40745E-11   PUB     = 1E-21
+PVSAT   = -50            PETA0   = 1E-4           PKETA   = -2.114056E-3    )
*
```