‘NANOSTRUCTURED SILICON SOLAR CELL’

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IN PARTIAL FULFILLMENT OF THE REQUIREMENTS

FOR THE MASTER OF TECHNOLOGY IN NANOSCIENCE AND TECHNOLOGY

BY

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UNDER THE SUPERVISION OF

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Certificate

This is to certify that Mr. Saurabh Jain has done a 1 year Research cum Project Work on the topic entitled 'NANOSTRUCTURED SILICON SOLAR CELL' under my supervision. The present research work is being submitted to Department of Applied Physics, Delhi Technological University (Formerly Delhi College of Engineering), in partial fulfilment of the requirement for the award of the degree of Master of Technology in Nanoscience and Technology, embodies faithful record of research work carried out by Mr. Saurabh Jain. He has worked under my guidance and that this work has not been submitted, in part of full, for any other degree of Delhi Technological University or any other university.

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Saurabh Jain

CHAPTER 1: INTRODUCTION

Considering the growing evidence that CO_2 emissions from fossil fuels are a major contributor to anthropogenic global climate change, a source of carbon-neutral energy will be needed at the scale of our current global energy consumption. We propose to use solar energy due to its abundance and wide availability, but there are significant challenges to producing cost-competitive solar energy solutions. One of strategy to reduce the cost of current solar cells by using materials with high aspect ratios. This principle has been shown to improve the efficiency of low-quality and therefore inexpensive materials in simulations, but there are significant challenges and drawbacks associated with using highly structured materials. Some of these include the expected increase in surface and junction recombination, as well as the expected decrease in open circuit voltage due to reduced carrier flux per unit of junction area.

1.1 Background Information

Recently there has been a great deal of interest in the fabrication of semiconductor nanomaterials and nanostructures. These are structures or objects with dimensions on the nanoscale. One of the main reasons for this interest is that nanomaterials tend to have properties that differ from those of the bulk material. These properties, such as the large surface area of nanomaterials, can be exploited for various applications. Silicon-based nanostructures are attracting interest as the techniques used to produce them are largely compatible with existing semiconductor fabrication processes. Silicon nanostructures also have properties that differ from those of bulk silicon, such as a band-gap that is tunable by the size of the structure, which are of interest when producing semiconductor devices.

One silicon nanostructure is nano-crystalline silicon, which consists of array of nanometre-sized crystallites embedded in a silicon material. This material can be used in thin film solar cells [1] (Yue et al., 2006), the properties of which differ from crystalline and amorphous silicon based solar cells. The use of nanostructures in solar cells has several advantages over crystalline devices and amorphous thin films devices, including lower production costs, increased conversion efficiency and improved stability. Nanocrystalline silicon solar cells are predominantly produced as thin film devices ~500 nm thick, not including the substrate upon which they are grown. The production of these thin film devices uses much less material than crystalline-based devices allowing lower

production costs than those for crystalline silicon solar cells [2] (Green, 2004). Nanocrystalline silicon based solar cells, although having lower conversion efficiencies than crystalline solar cells; potentially have a higher efficiency than their amorphous counterparts.

Creating higher efficiency solar cells is the focus of much research effort. By producing higher efficiency solar cells, or producing efficient solar cells cheaply, the use of solar cells as an alternative energy source becomes more favourable. In an era of rising oil prices and great concern about the environmental impact of coal, oil-fired or nuclear power plants, the hunt is on for clean alternative energy sources. The use of silicon nanostructures would potentially allow for the reduced production and material costs associated with thin film photovoltaics while maintaining the higher efficiency and stability that are characteristic of crystalline solar cells.

A silicon nanowire is an elongated single crystal of silicon with a diameter of tens, to a few hundreds of nanometers and with a length of several micrometres. Silicon nanowires have been the focus of much recent interest due to their unique properties which often differ significantly from bulk silicon. The electronic band-gap of silicon nanowire is tunable with the adjustment of the nanowire diameter. The band-gap is known to increase as the diameter of the nanowire is decreased. It has been shown that array of silicon nanowires when applied to strong light yield high degree absorbance of applied light. Both of these properties would be of interest when producing solar cells [3] (Ma et al., 2003).

Controlling the band-gap allows the ability to tune the spectrum of light absorbed by the device. As a solar cell generates power by absorbing light, the demonstrated band-gap tuning and high absorbance bodes well for the use of silicon nanowires in solar cells. Both of these properties would be of interest when producing solar cells.

Recent results show that silicon nanowires can be used as anti-reflective coatings on crystalline solar cells [4], [19] (Peng et al., 2005). Peng and co-workers' (2005) have used a top down fabrication technique to prepare silicon nanowires on silicon wafer using silver nitrate ($AgNO_3$) and hydrogen fluoride (HF). There has been some mention of silicon nanowire photovoltaics within the literature where nanowires are used as anti-reflective coatings [4], [19] (Peng et al., 2005). However, to date there has been little work done on incorporating silicon nanowires into thin film devices. Silicon nanowires have been produced by chemical vapour deposition and plasma enhanced chemical vapour

deposition which is often used with catalysts like gold which is hindered for the silicon photovoltaics technology. Thus it would be of great interest to produce solar cells incorporating silicon nanowires into their design to take advantage of the properties of these silicon nanowires to improve the efficiency of the solar cell, without overly increasing cost of production.

1.2 Motivation: --Global Climate Change

The primary motivational force behind this work is the apparent onset of anthropogenic global climate change. Evidence is mounting that human actions have created circumstances in which the energy flux of the Earth is slightly out of balance, causing a rise in the global average temperature, and climate models predict that this temperature change may bring with it a host of sweeping changes in the weather patterns and coastlines of the world. The increased levels of CO_2 and other greenhouse gases in the atmosphere are key contributors to global climate change, and the chief source of CO_2 emissions is the burning of fossil fuels for energy. As a result, finding carbon-neutral alternatives to fossil fuels is an important and active area of research across the sciences, and the focus of this work has been on the understanding and development of silicon nanowire based devices for solar energy generation.

There are a number of possible choices to replace fossil fuels, but light from the sun is one of the most abundant sources of carbon-neutral energy available. Indeed, the fossil fuels currently used are essentially concentrated energy from the sun stored as chemical bonds. To understand the scale of the available solar energy resource, consider that the solar constant, the energy of incoming sunlight per unit area, is 1.37 kW- m^{-2}. The cross-sectional area of the Earth is about 1.27×1014 m^2 on average, giving a total incident power from the sun of about 174,000 TW. This is the flux outside the atmosphere of the Earth, so it must be corrected for the total amount of energy that is reflected, which is known as the Earth's albedo and is about 30% on average. This gives a total absorbed power from the sun of about 122,000 TW. This is a vast resource compared to the total global power consumption of only 15 TW currently. Taking this analysis one step further, we can calculate the total land area necessary to generate all of the world's power from the sun. Assuming 10% efficient energy conversion, and given that land mass accounts for only 29.2% of the total surface of the Earth, we find that 0.4% of the Earth's land area would be needed to be covered in solar energy conversion devices in order to power the

planet. In contrast, using all of the arable land to grow crops for biomass would only yield a power equivalent of ~8 TW, about half of what is currently being consumed, and there would also be fierce competition between land use for energy crops and for food crops. Thus, solar energy is clearly an attractive avenue for providing significant carbon-neutral energy. Solar energy spectrum for AM 0 and AM 1.5 is as shown in figure 1.1 below.

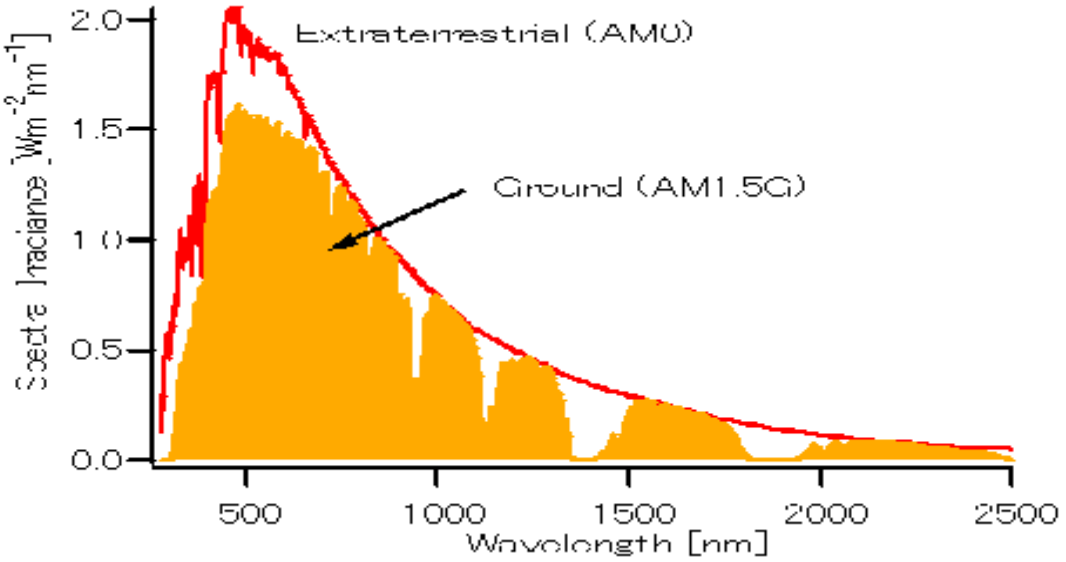


Figure 1.1*: *Solar spectrum for AM 0 and AM 1.5

1.3 High Aspect Ratio Structures for Solar Energy

In order to take advantage of the vast solar energy resource in a meaningful way, it will be necessary to develop and manufacture solar energy conversion devices that are cost competitive with fossil fuels and nuclear fission. Although the price of conventional crystalline and multi-crystalline silicon solar cells continues to drop due to advances in manufacturing and due to economies of scale, a significant breakthrough in solar energy capture and conversion could lead to a step change in the cost of solar electricity. Furthermore, many groups are vigorously working toward the ultimate goal of a nanostructured fuel-producing device that could be manufactured cheaply at large scale. Photon capture and conversion will be an essential component of either photovoltaic or nanostructured photovoltaic energy conversion devices. For these reasons, this work focuses primarily on the nanostructured properties of high-aspect-ratio silicon structures with the goal of understanding the utility of these types of structures for low-cost solar energy capture and conversion. See Figure 1.2.

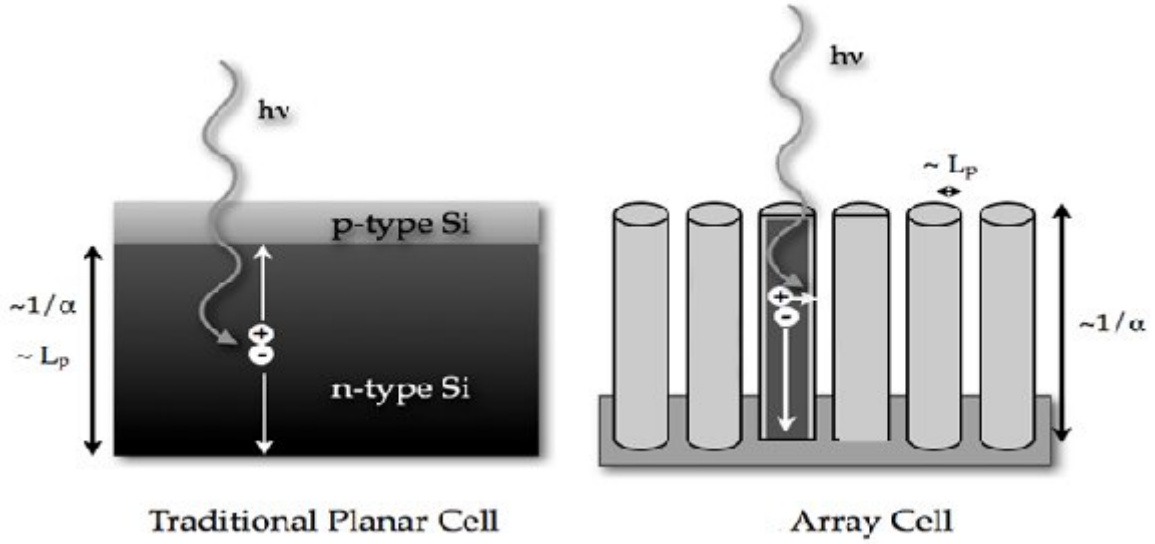


Figure 1. 2: *Schematic diagram of a traditional planar solar cell and the proposed wire array geometry. In the planar cell, the absorption length (~1/α) must be comparable to the minority carrier diffusion length (Lp). In the array cell, the absorption length (~1/α) independent to the minority carrier diffusion length (Lp).*

1.4 SILICON AND SILICON NANOWIRES

Question can be raised why only silicon is the preferred material for the solar cell development. Number of reasons for this are: ---

1. Silicon is one of the most abundant elements in the Earth's crust (25.7%) second only to oxygen.

2. Silicon is usually found in the form of oxides and silicates, such as sand and quartz. Arguably one of the more important and versatile elements, silicon can be used to produce everything from bricks to computer chips.

3. Strong technical backup from the micro-electronics industry.

4. Stable nature and non-toxic in nature.

5. Less complex process to produce solar cell.

1.4.1 Crystalline Silicon

Crystalline silicon (c-Si) forms the basis of many of today's integrated circuits as it is a readily available semiconductor which is relatively easy to process and dope to form semiconductor devices. Crystalline silicon has a type of face centered cubic structure and

is dark grey in colour with a slight bluish tinge. When cleaned and etched or polished, crystalline silicon is highly reflective. A photo of a sample of crystalline silicon is shown in Figure 1.3. Devices made from crystalline silicon include many integrated circuits, diodes and solar cells. High purity crystalline silicon is typically produced using the Czochralski process.

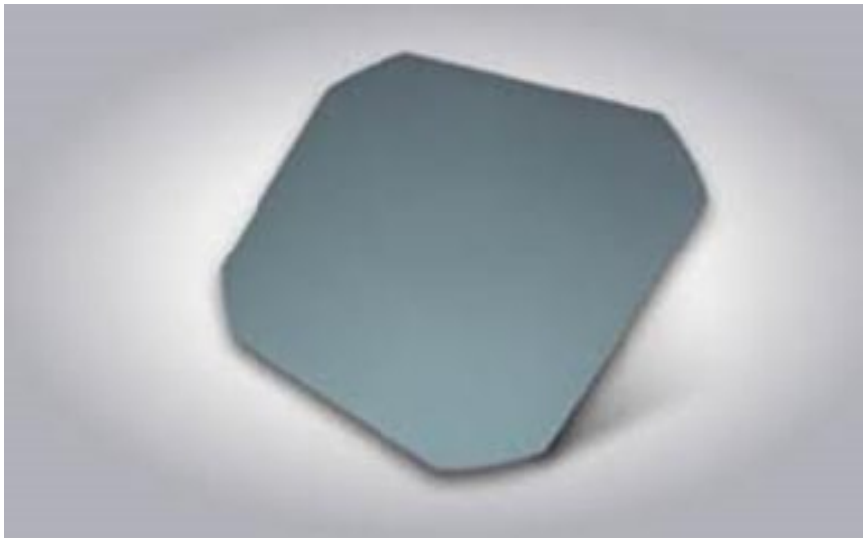


Figure 1.3: *Photograph of crystalline silicon wafers*

Silicon crystals/ingots are typically cut to produce wafers with different surface orientations such as (111), (100) and (110). The nomenclature (xyz) refers to the orientation of the crystal plane defined in terms of the axes (a1, a2, a3). This is illustrated in Figure 4 which shows a unit cell of the face-centered-cubic crystal structure with the different crystal planes. The nomenclature [xyz] refers to a direction as described by a vector where x, y and z are the components of the vector in terms of the axes (a1, a2, a3). An example [111] vector is shown in Figure1.4. Figure1.4 also shows the arrangement of the atoms in a face-centered-cubic unit cell, the basic unit of a crystal lattice. Silicon itself has a face-centered diamond cubic crystal structure.

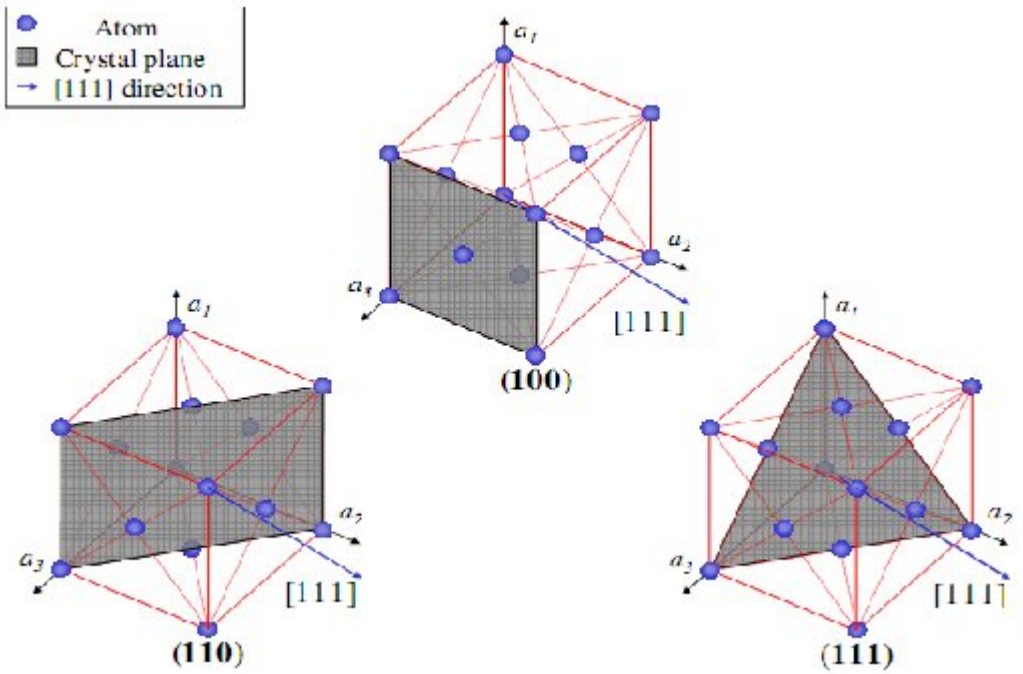


Figure 1.4: *Face centered cubic crystal unit cell showing crystal planes and the [111] direction. ([5] From Kittel*)

1.4.2 Amorphous silicon

Amorphous silicon (a-Si) is a glass-like material that structurally does not have long range structural order and is randomly oriented. Due to the random orientation of the material, the absorption coefficient of light in amorphous silicon tends to be higher than that of crystalline silicon [5] (from kittel).

One of the main uses of a-Si silicon is in the solar cell industry for the fabrication of cost effective thin film solar cells. Amorphous materials are glass-like, randomly structured materials which gives amorphous solar cells some fairly unique properties and problems. An illustration of this glass like structure, hydrogenated amorphous silicon, is shown in Figure 1.5. Amorphous silicon by itself has many dangling bonds which trap charge carriers thereby reducing the efficiency of the cell. By creating hydrogenated amorphous silicon (a-Si:H), a hydrogen and silicon alloy, many of the traps can be eliminated [6] (Wilson, 1980). This allows it to be used in photovoltaic applications with useful efficiencies. In Figure 1.5 the dangling bonds have hydrogen atoms attached so as to passivate them and eliminate the traps.

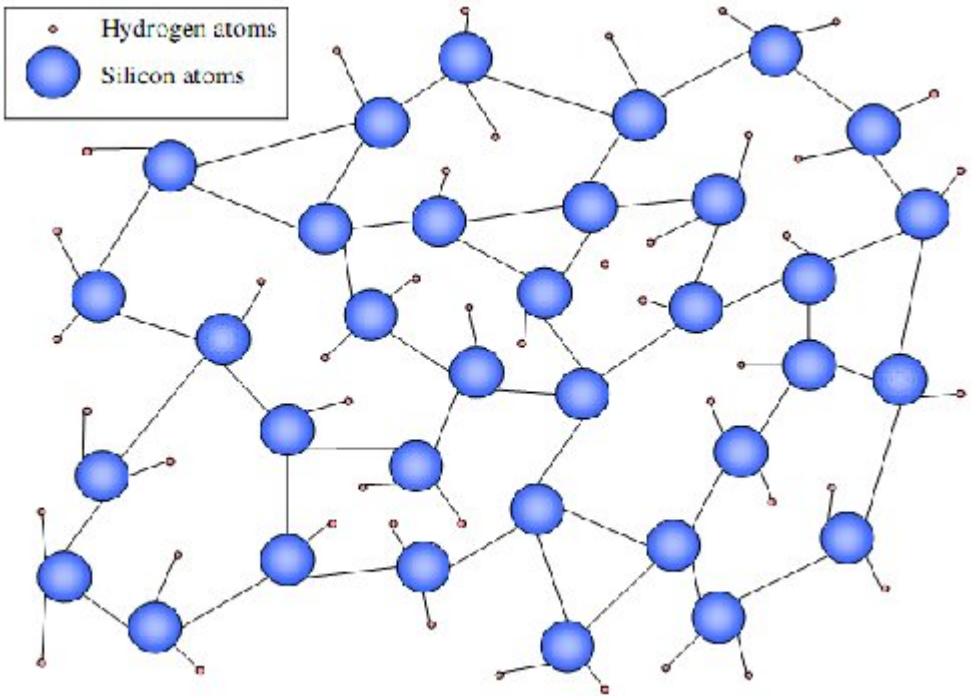


***Figure 1.5**: Representation of the structure of hydrogenated amorphous silicon [6](Wilson, 1980)*

1.4.3 Polycrystalline Silicon

Typically, polycrystalline silicon is defined as having a grain size (crystallite diameter) of between 10-30µm and a crystalline fraction of close to 100%. Polycrystalline silicon can be doped and used to fabricate solar cells, amongst other devices [7] (Cabarrocas, 2004).

1.4.4 Microcrystalline Silicon

Microcrystalline silicon is commonly defined as having a grain size between 10-20 nm and a crystalline fraction of between 10 and 100%.Microcrystalline silicon is an attractive material for electronic device applications due to its high carrier mobility and hence, high electrical conductivity. This variant of silicon is commonly used in the photovoltaic industry to produce single junction solar cells [7] (Cabarrocas, 2004).

1.4.5 Nanocrystalline Silicon

Nanocrystalline silicon (nc-Si) is similar to microcrystalline silicon. Nanocrystalline silicon is commonly defined as having a grain size between 2 and- 5nm and a crystalline fraction of between 10 and 80%. This form of silicon is an interesting material as it has

good optical and electronic properties [7] (Cabarrocas, 2004). It can be also be used to produce cheaper solar cells [8] (Yue et al., 2006).

1.4.5.1 Quantum wire/Nanowires

There has been much recent interest in silicon-based quantum wires (nanowires). Crystalline silicon nanowires are a new form of semiconductor material, the properties of which differ from those of bulk silicon. A nanowire is a quasi-one-dimensional structure that has a nanoscale diameter, a length often in the micron range and a high aspect ratio. The aspect ratio refers to the ratio of the length to the diameter. Nanowires have diameters ranging between a few nanometers to the few hundreds of nanometers and lengths ranging up to a few millimeters. A nanowire usually has an approximately circular cross section. Nanowires can be bonded to, or embedded in, the surface of a substrate throughout their entire length. Or they can be freestanding, being attached to a substrate by only one end. Silicon nanowires can be fabricated using a range of different techniques and growth mechanisms, allowing their diverse potential applications.

1.5 The Presence of the Term 'Silicon Nanowires' in the Literature

Many papers in the literature dealing with silicon nanowires and other semiconductor nanostructures begin with an introductory sentence similar to: 'Lately there has been a great deal of interest in silicon nanowires, silicon nanostructures and nanoscale semiconductors'. There are a number of variations but all express the same sentiment that (a) there has been an increase in interest in silicon nanowires and (b) that there is a large amount of recent interest. Silicon nanowires have been referred to as 'silicon filaments' or 'filamentary crystals' as far back as 1964 by Wagner and Ellis [9] (Wagner et al., 1964).

1.6 Growth Mechanism of silicon nanowire

Many different growth mechanisms have been used to grow silicon nanowires. Each growth mechanism has its own defining characteristics to create nanowire.

1.6.1 Vapour-Liquid-Solid (VLS) Growth Mechanism

The most commonly used mechanism invoked to describe the growth of silicon nanowires is the Vapour Liquid Solid (VLS) mechanism. This was first proposed by Wagner and Ellis in 1964 to describe the growth of silicon filaments (Wagner and Ellis, 1964). The VLS mechanism uses a vapour phase reactant ($SiCl_4$, SiI_2 or SiH_4), a liquid

catalyst and a solid substrate to produce small diameter filaments or crystals of silicon [10] (Wagner and Ellis, 1964). The silicon comes from the disproportionation of SiI_2 or the hydrogen reduction of SiH_4.The VLS mechanism can be used to produce silicon nanowires.See figure1.6

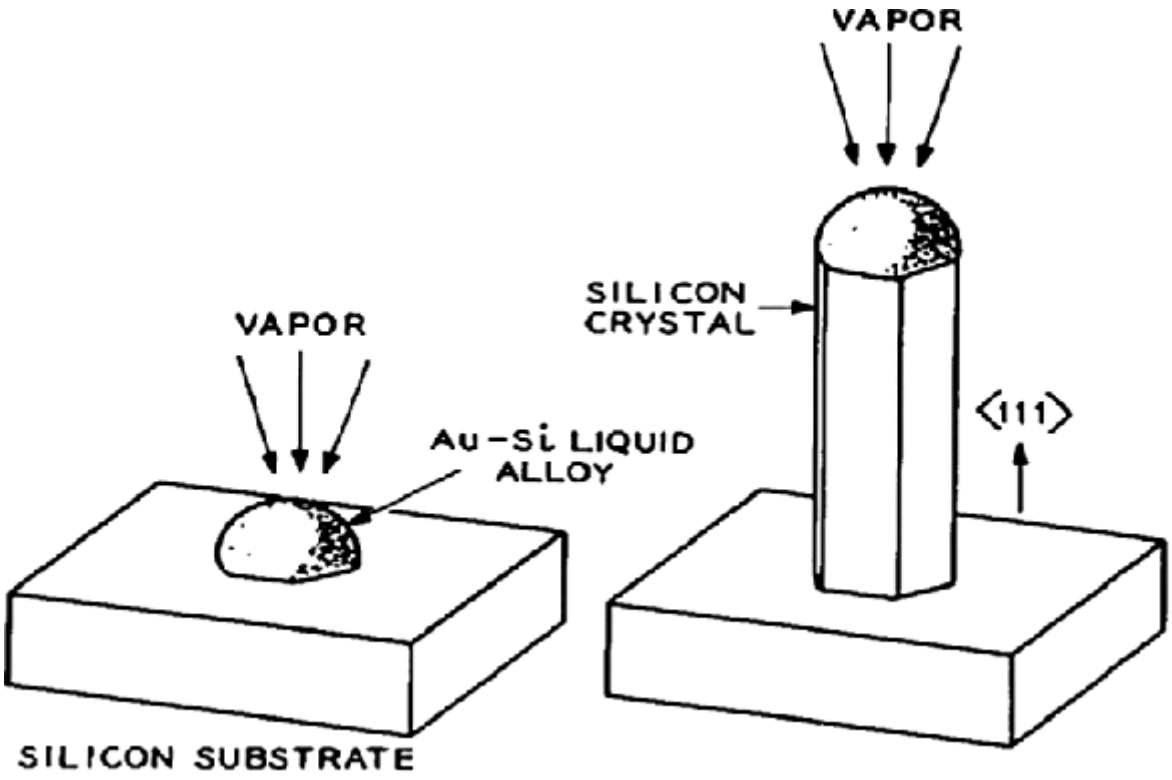


***Figure 1.6**: Schematic diagram of silicon nanowires growth by VLS method* [11] *(McIlroy et al., 2004).*

The VLS mechanism uses a liquid catalyst that absorbs material from the surrounding vapour, often $SiCl_4$, SiI_2 or SiH4. Thin films of metallic catalysts are often used to grow silicon nanowires. A thin layer of metal catalyst is deposited onto a substrate under vacuum and is then placed in a deposition chamber which is also under vacuum. The substrate is heated until the metal catalyst melts. In the case of gold on a silicon substrate, a eutectic with silicon forms at 363°C. The liquid catalyst forms small droplets, or islands, on the surface of the substrate. The size of the island determines the size of the resulting nanowire. The gas source of silicon is then introduced and is thermally decomposed and absorbed by the liquid metal. When the catalyst becomes supersaturated with silicon, crystalline silicon is deposited underneath the metal droplet [11] (McIlroy et al., 2004).

The catalyst plays an important role in the growth of nanowires or filaments via the VLS mechanism. The choice of catalyst depends on the type of nanowire that is to be produced as the material to be used must be soluble in the catalyst. It

is also desirable that the catalyst produces a liquid alloy or eutectic droplet with a relatively low melting point. A liquid catalyst droplet acts as a preferred site for the deposition of material from the vapour phase reactants. To lower the melting point of the catalyst further, droplets or clusters with small diameters can be used as it is known that the melting point of droplets with a diameter below 200nm is lower than that of the bulk material. In the case of lead, for example, the melting point is decreased by about 200K for particles of a radius of 3nm. So where the catalyst particle size is below 200nm, the eutectic point of the nanoparticles and silicon will be reduced, allowing for lower temperature growth of silicon nanowires via the VLS mechanism. Silicon nanowires can be grown via thermal CVD at temperatures as low as 320°C using gold as a catalyst which is well below the eutectic point of gold and silicon [12] (Westwater and co-workers, 1998).

The morphology of the nanowire is also determined in part by the catalyst. The diameter of the catalyst droplet determines the size of the resulting nanowire. It has been shown using Au nanoclusters, which are nanoparticles of Au that the diameter of the grown nanowires increases proportionally with cluster diameter [13] (Cui et al., 2001).

1.6.2 The Solid Liquid Solid (SLS) Mechanism

SLS mechanism is analogous to the VLS mechanism. Only difference is the use of a solid phase source of silicon rather than a vapour phase source. SLS mechanism can be used to produce silicon nanowires using a gold catalyst. In this technique nanowires produced involved the heating a gold coated silicon (c-Si (111)) substrate in a quartz-tube furnace under a flowing H_2 atmosphere at 200 Torr for different time.

The SLS mechanism has three steps:-

1. Firstly Au-Si droplets form on the substrate when the substrate temperature is raised to the growth temperature. This forms a solid-liquid interface between the silicon substrate and the liquid catalyst droplet.
2. In the second phase, the H_2 flowing over the surface of the droplets collides with and exchanges energy with the Si atoms on the surface of the droplets. The continual collision of the H_2 with the droplets induces supersaturation at the surface of the droplets. Silicon atoms then precipitate out to nucleate the nanowires, forming a second solid-liquid interface between the liquid droplet and the nucleated nanowire.

3. The third and final phase of the SLS mechanism is the axial growth of the silicon nanowire. The compositional gradient between the two solid-liquid interfaces maintains the diffusion of Si atoms from the substrate to the growing nanowire, via the liquid catalyst droplet, allowing the growth of the silicon nanowire to continue.

1.6.3 Other Growth Mechanisms

Oxide Assisted Growth, in this mechanism silicon nanowires are produced by thermal evaporation using an oxygen-assisted growth mechanism [14] (Pan, Lim and co-worker, 2005).

Sulphide Assisted Growth (SAG), silicon nanowires could be grown when sulphur powder is used as a catalyst in a low-vacuum CVD system [15] (Niu, Sha and Yang, 2004).

Stress Driven Growth, silicon nanowires also can be grown on a silicon substrate in a furnace without the presence of a silicon vapour or a metal catalyst. Nanowire growth would only occur if a native oxide layer was present on the silicon substrates and only after crack formation at the high temperatures used, as the nanowires were found to nucleate from the cracked regions. The different thermal expansion coefficients of SiO_x and crystalline silicon led to the creation of the cracks and a stress gradient in the sample. Prokes and Arnold (2005) proposed that this leads to the transport of silicon atoms from the stressed regions to the stress free regions resulting in the nucleation of nanowires out of the cracks [16].

1.7 Properties of Silicon Nanowires

One of the major points of interest in investigating nanostructured and nanoscale materials is how the properties of these materials differ from that of bulk silicon.

Several groups have performed Raman Spectroscopy (RS) on silicon nanowires and compared the results to bulk silicon. One of the main items of

interest is the diameter dependent downshift of the crystalline silicon peak that occurs in the Raman spectra for silicon nanowires. Silicon nanowires have been shown to have a Raman spectrum which exhibits a downshift in wavenumber of the transverse optical (TO) crystalline silicon peak in comparison to bulk crystalline silicon. This shift has been shown to be diameter dependent; there is a larger shift for smaller diameter nanowires while for larger diameters the value approaches that of bulk silicon [17] (Yu et al., 1998). This downshift has been attributed to the quantum confinement effect.

SiNWs arrays drastically suppress light reflection over a wide spectral bandwidth. The reflectance is less than 1.4% over the range of 300–600 nm for SiNWs fabricated on single-crystal Si wafers. This remarkably low reflectance of the SiNWs array is attributed to several distinct advantages associated with the wire geometry:

(1) The ultrahigh surface areas of high-density SiNWs;

(2) The sub-wavelength light-trapping effects of SiNWs arrays; and

(3) The collective light scattering interactions among SiNWs, which trap light and make it, travel many turns over distances much longer than the array thickness.

Therefore, SiNWs solar cells can have extremely low reflectance without any antireflection coatings [4] (Peng.et al., 2005).

The band-gap or energy-gap is an important property of silicon nanowires that has been shown to be dependent upon the diameter of the nanowire. The energy gap increases with decreasing diameter from 1.1eV for 7nm to 3.5eV for 1.3nm. The energy gap was found by using Scanning Tunnelling Spectroscopy (STS) measurements. The increase in band-gap is an indication of a quantum confinement effect within the silicon nanowires at low diameters [3] (Ma et al., 2003).

The properties of silicon nanowires as reported in the literature are strongly size dependant. For small diameters, properties such as the band-gap change greatly from that of bulk silicon. Larger diameter nanowires have properties that tend to approximate those of bulk silicon.

1.8 Photovoltaics (PV)

The word Photovoltaic is a combination of the Greek word for Light and the name of the physicist Allesandro Volta. It identifies the direct conversion of sunlight into energy by means of solar cells. The conversion process is based on the photoelectric effect discovered by Alexander Bequerel in 1839. The photoelectric effect describes the release of positive and negative charge carriers in a solid state when light strikes its surface. There are a number of different ways to produce solar cells and a range of materials from which they can be produced. Silicon is a commonly used semiconductor material for producing solid state solar cells. Solar cells produced using silicon have different properties when they are made using different types of silicon.

- PV benefits from a number of attractive features:
  - Abundance of free fuel in the form of sunlight
  - No moving parts – low maintenance
  - Totally noiseless, pollution free, benign source of energy
- However, it also suffers from a few limitations:
  - Low energy density
  - Requires storage in batteries
  - Produces D.C. electricity that needs to be converted to A.C. for many applications.

1.9 How Does a PN junction Solar Cell Work?

Solar cells are composed of various semiconducting materials. Semiconductors are materials, which become electrically conductive when supplied with light or heat, but which operate as insulators at low temperatures.

To produce a solar cell, the semiconductor is contaminated or "doped". "Doping" is the intentional introduction of chemical elements, with which one can obtain a surplus of either positive charge carriers (p-conducting semiconductor layer) or negative charge carriers (n-conducting semiconductor layer) from the semiconductor material. If two differently contaminated semiconductor layers are combined, then a so-called p-n-junction results on the boundary of the layers.

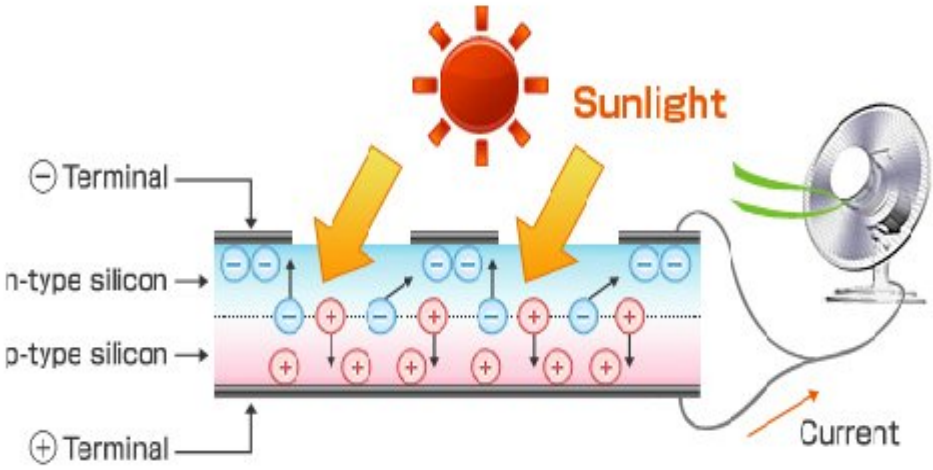


***Figure 1.7**: Schematic diagram showing operation of basic p-n junction solar cell*

At this junction, an interior electric field is built up which leads to the separation of the charge carriers that are released by light. Through metal contacts, an electric charge can be tapped. If the outer circuit is closed, meaning a consumer is connected, then direct current flows. A transparent anti-reflection film protects the cell and decreases reflective loss on the cell surface. In the present study, an attempt is made to use the silicon nanowires array as anti-reflection surface in silicon solar cells. The main objectives of the work are as below:-

1. To develop the SiNWs on the silicon wafers with the electroless chemical deposition technique using Silver (Ag) as a catalyst.
2. To fabricate the silicon solar cell with the front surface as SiNW array.
3. To optimize the parameters of the SiNWs array solar cells, hence lowering the cost of solar cells and use them as antireflective coating.
4. To optimize the conditions for the growth of SiNWs.

1.10 Different Cell Types

One can distinguish three cell types according to the type of crystal. This can be been seen in the table 1.1.

Material	*Lab efficiency (%)*	*Production efficiency (%)*
Monocrystalline Silicon	approx. 24	14 to17
Polycrystalline Silicon	approx. 18	13 to15
Amorphous Silicon	approx. 13	5 to7

Table 1.1: *Comparison of efficiencies of different types of silicon solar cells on the bases of material used.*

1.11 Natural Limits of Efficiency

In addition to optimizing the production processes, work is also being done to increase the level of efficiency, in order to lower the costs of solar cells. However, different loss mechanisms are setting limits on these plans. Basically, the different semiconductor materials or combinations are suited only for specific spectral ranges. Therefore a specific portion of the radiant energy cannot be used, because the light quanta (photons) do not have enough energy to "activate" the charge carriers. On the other hand, a certain amount of surplus photon energy is transformed into heat rather than into electrical energy. In addition to that, there are optical losses, such as the shadowing of the cell surface through contact with the glass surface or reflection of incoming rays on the cell surface. Other loss mechanisms are electrical resistance losses in the semiconductor and the connecting cable.

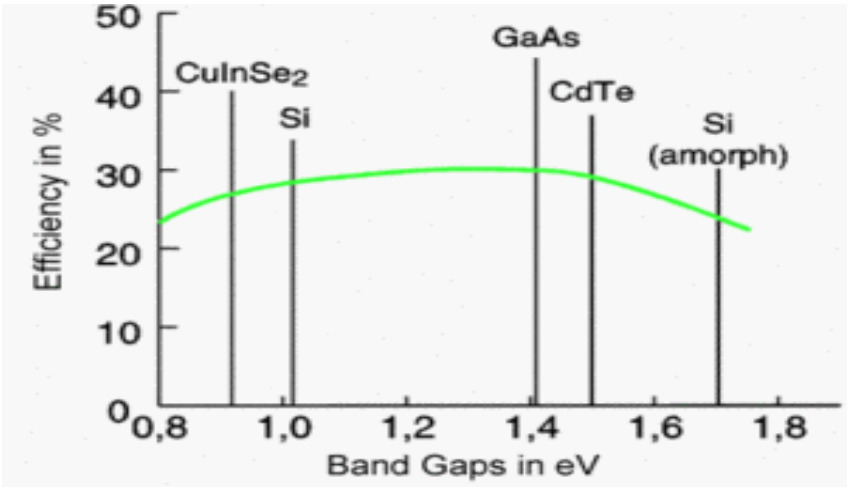


Figure 1.8: *Limitation of efficiency with respect to band gap*

Single loss mechanisms (photons with too little energy are not absorbed, surplus photon energy is transformed into heat) cannot be further improved because of inherent physical limits imposed by the materials themselves. This leads to a theoretical maximum level of efficiency, i.e. approximately 29% for crystal silicon.

1.12 Characteristic Current Voltage Curve for solar cell and its important parameters

Typical voltage-current characteristics, known as the IV curve, of a diode without illumination is shown in black in Figure 1.9. The applied potential is in the forward bias direction. The curve shows the turn-on and the build-up of the forward bias current in the diode. Without illumination, no current flows through the diode unless there is external potential applied. With incident sunlight, the IV curve shifts to fourth quadrant and indicates that there is external current flow from the solar cell to a passive load i.e. power is being drawn from the device.

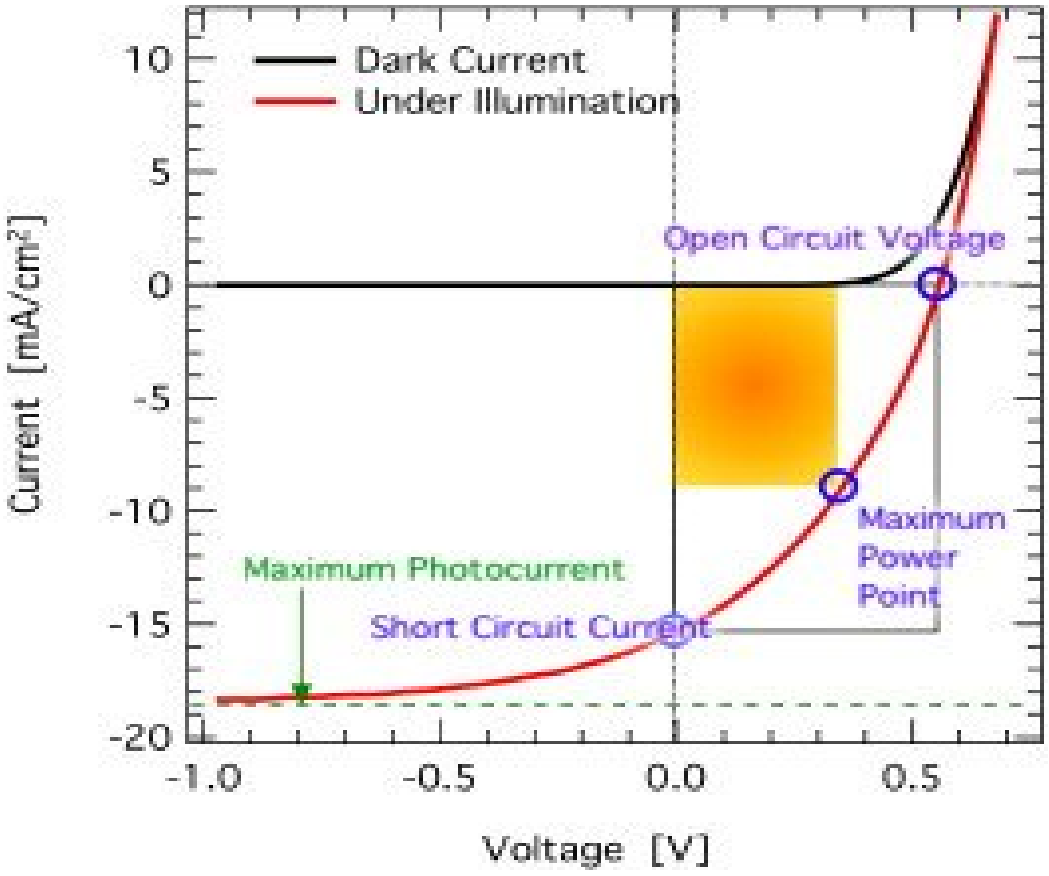


***Figure 1.9**: Typical voltage-current characteristics*

Short circuit current, I_{sc}, flows with zero external resistance (V= 0) and is the maximum current delivered by the solar cell at any illumination level.

Open circuit voltage, V_{oc}, is the potential that develops across the terminals of the solar cell when the external load resistance is very large (ideally open).

The power delivered to the load is of course zero at both extremes and reaches a maximum (P_{max}) at a finite load resistance value. P_{max} is shown as the area of the shaded rectangle in figure 1.9.

Fill Factor, FF, which is defined as the ratio of P_{max} to the area of the rectangle formed by V_{oc} and I_{sc}.

$$FF = \frac{P_{\max}}{(Voc)(Isc)}.$$

Efficiency,η, the efficiency of a solar cell is the ratio of the electrical power it delivers to the load, to the optical power incident on the cell (P_{in}). Maximum efficiency is when power delivered to the load is P_{max}. Using expression of Fill Factor, maximum efficiency may be written as:

$$\eta_{\max} = \frac{P_{\max}}{P_{in}} = \frac{(Voc)(Isc)(FF)}{P_{in}}$$

Quantum efficiency, QE, The "quantum efficiency" (Q.E.) is the ratio of the number of carriers collected by the solar cell to the number of photons of a given energy incident on the solar cell. The quantum efficiency may be given either as a function of wavelength or as energy. If all photons of a certain wavelength are absorbed and the resulting minority carriers are collected, then the quantum efficiency at that particular wavelength is unity .The quantum efficiency for photons with energy below the band gap is zero. A quantum efficiency curve for an ideal solar cell is shown in figure 1.10. While quantum efficiency ideally has the square shape shown in same figure 1.10, the quantum efficiency for most

solar cells is reduced due to recombination effects. The same mechanisms which affect the collection probability also affect the quantum efficiency.

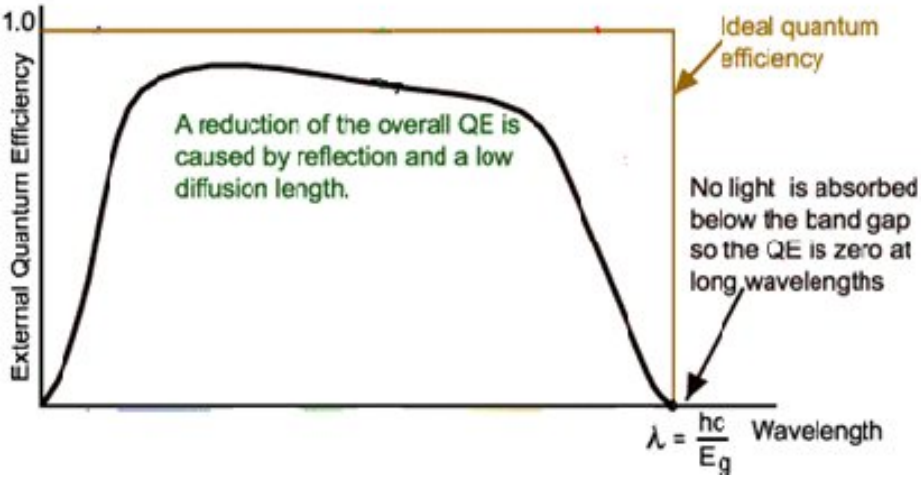


***Figure 1.10**: Quantum Efficiency for the solar cell[18]*

Two types of quantum efficiency (QE) of a solar cell are often considered:

• External Quantum Efficiency (EQE) is the ratio of the number of charge carriers collected by the solar cell to the number of photons of a given energy shining on the solar cell from outside (incident photons i.e. without correction of photons lost due to reflection).

• Internal Quantum Efficiency (IQE) is the ratio of the number of charge carriers collected by the solar cell to the number of photons of a given energy that shine on the solar cell from outside and are absorbed by the cell (after correction of reflection loss).

The "external" quantum efficiency of a silicon solar cell includes the effect of optical losses such as transmission and reflection.

Spectral Response of solar cell, the spectral response is the ratio of the current generated by the solar cell to the power incident on the solar cell. A spectral response curve is shown in the figure 1.11.

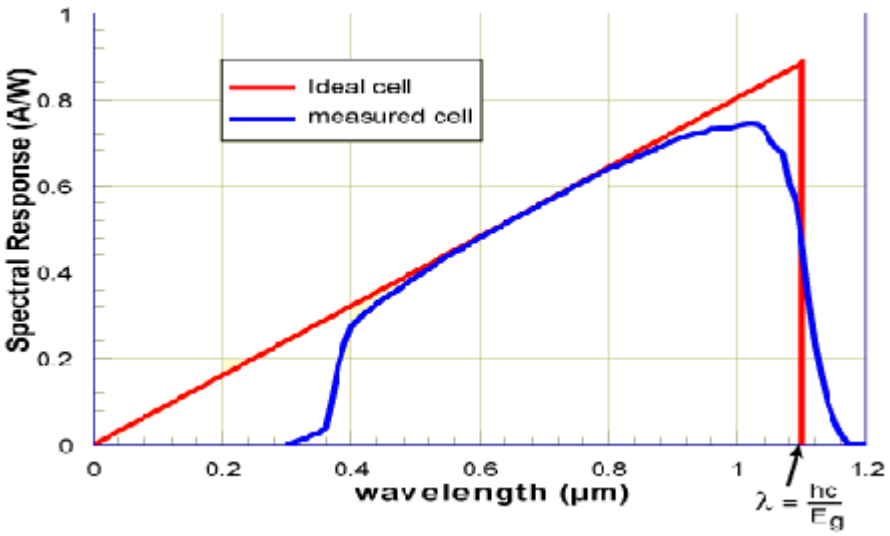


***Figure 1.11**: Spectral Response for the solar cell [18]*

The spectral response is conceptually similar to the quantum efficiency. The ideal spectral response is limited at long wavelengths by the inability of the semiconductor to absorb photons with energies below the band gap. This limit is the same as that encountered in quantum efficiency curves. However, unlike the square shape of QE curves, the spectral response decreases at small photon wavelengths. At these wavelengths, each photon has a large energy, and hence the ratio of photons to power is reduced. Any energy above the band gap energy is not utilised by the solar cell and instead goes to heating the solar cell.

1.13 Equivalent circuit model of the solar cell

Figure 1.12 shows the simplified equivalent circuit model of a solar cell. The value of the series resistance Rs, is typically much lower than the parallel resistance Rp (sometimes referred to as the shunt resistance Rsh). For the ideal solar cell, Rs would be zero, and Rp would be infinite.

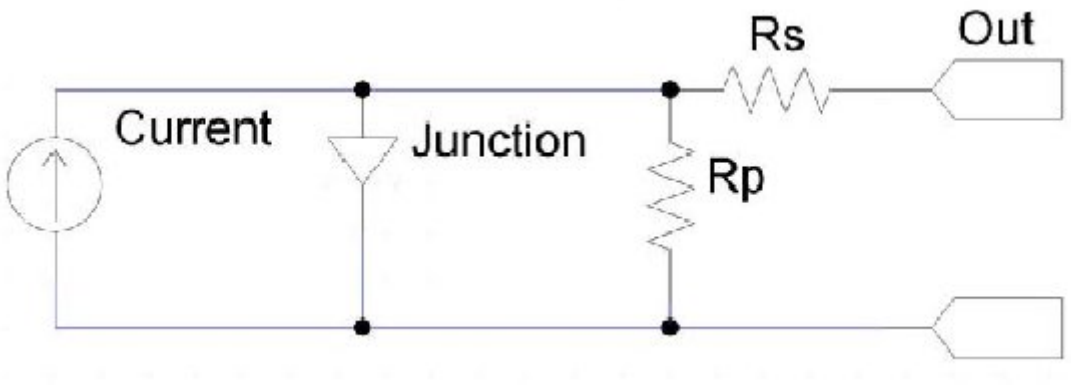


Figure 1.12: *A simplified equivalent circuit model of the solar cell*

1.14 PN Junction Silicon Solar cell

The basic structure of a typical systematics p-n junction of silicon solar cell is shown in figure 1.13.

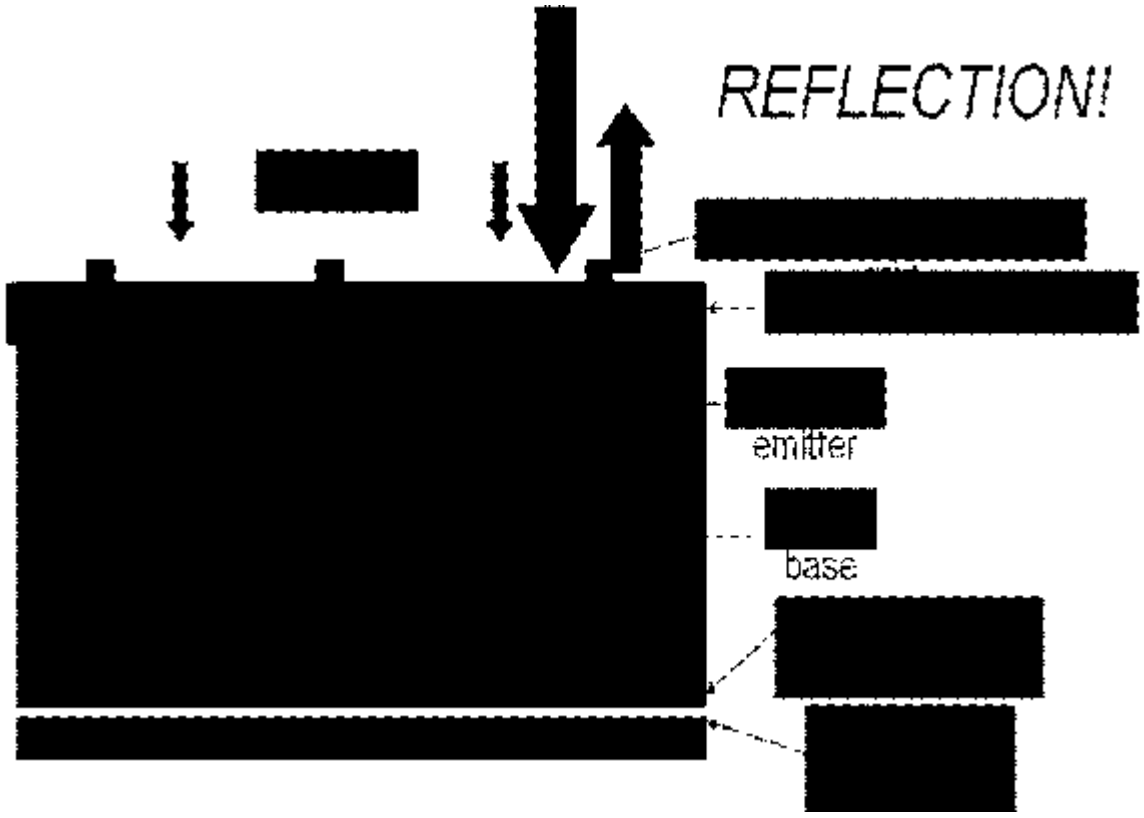


Figure 1.13: Typical systematics p-n junction of silicon solar cell

Chapter 2: Experimental Systems and techniques

2.1 Current Voltage (IV) Characteristics

The Current Voltage (IV) characteristic, also known as a JV characteristic when referring to current density, is a commonly used tool for analyzing the electrical characteristics of a semiconductor device. IV characteristics simply show the current flow through a device as the voltage applied to it is varied. Information such as resistance and conductance can be gleaned using this technique. The characteristics of non-ohmic devices can also be examined.

This technique is often used to analyze solar cells. It gives information on the basic electrical properties of a solar cell including the fill-factor, series-resistance, shunt-resistance, short circuit current and open-circuit voltage, from which other factors such as the efficiency of the cell can be calculated.

The IV characteristics of the nanowire based solar cell fabricated in this project were measured using an existing characterization system (model: Bunkoh-Keiki Co., CEP-25HS-50 SR) under AM 1.5 spectral irradiance (100 mW/cm^2 at 25^{o}C) at NPL, New delhi. IV characteristics show the current flowing through a device as the voltage applied to it is varied, allowing information about the device to be gathered, as described in Chapter 1.

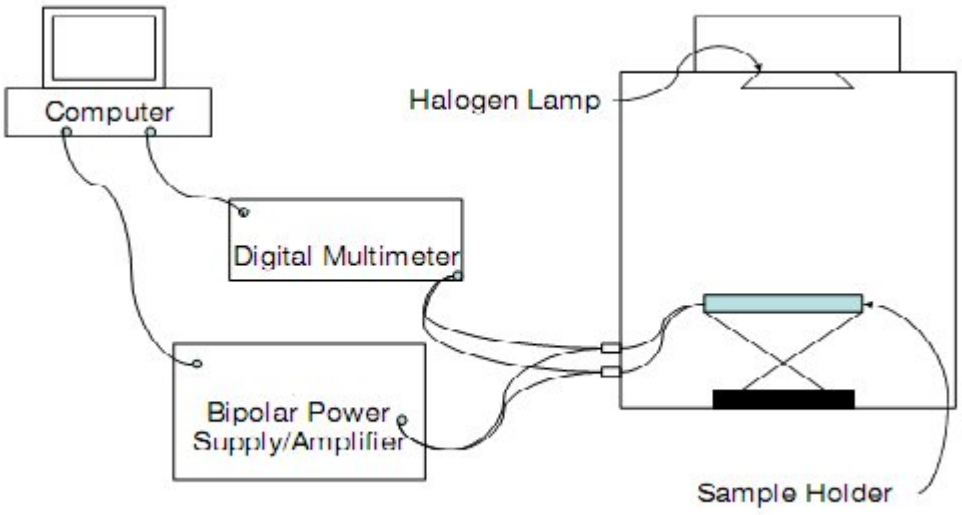


Figure 2.1: *Schematic of the Current-Voltage characterization system.*

The IV system was run in two modes. In the dark mode, the sample was isolated from any illumination. The data recorded by the computer could then be used to find the resistance of the material and the presence of any photo- conductance. A schematic diagram of the system can be seen in Figure 2.1.

As shown in figure 2.2 the samples were placed in a light-proof box to ensure they were exposed to the correct lighting conditions. For the photovoltaic devices produced the efficiency, fill factor, and current density were measured using ***Solar cell Spectral Response System*** (model Bunkoh-Keiki Co., Model: CEP-25HS-50 SR).

Figure 2.2*: Solar cell spectral response system at NPL, New Delhi*

2.2 Scanning Electron Microscopy

One of the major difficulties with nanotechnology and nanoscale materials arises in actually observing the material. How can the structure be observed if it is smaller than the wavelength of visible light? Electron microscopes are an answer to this question. There are two main types of electron microscopes, Scanning Electron Microscopes (SEM) and Transmission

Electron Microscopes (TEM) and each has its own properties. While conventional light microscopes have a resolution in the order of ~200nm, the SEM has a resolution of ~1nm and TEM a resolution of ~0.1nm. Due to this vastly improved resolution, electron microscopes are commonly used to directly observe the morphology of nanostructured materials. Hence, Scanning electron microscopy is a popular and versatile characterization technique for a number of reasons.

Scanning electron microscopes function by firing a finely focused electron beam at a sample and then collecting information from the sample. The various signals emitted, and the results of electron beam interaction with the sample, are shown in Figure 2.3. The signals which are used to produce images are usually secondary electrons (SE) and back scattered electrons (BSE) for SEM.

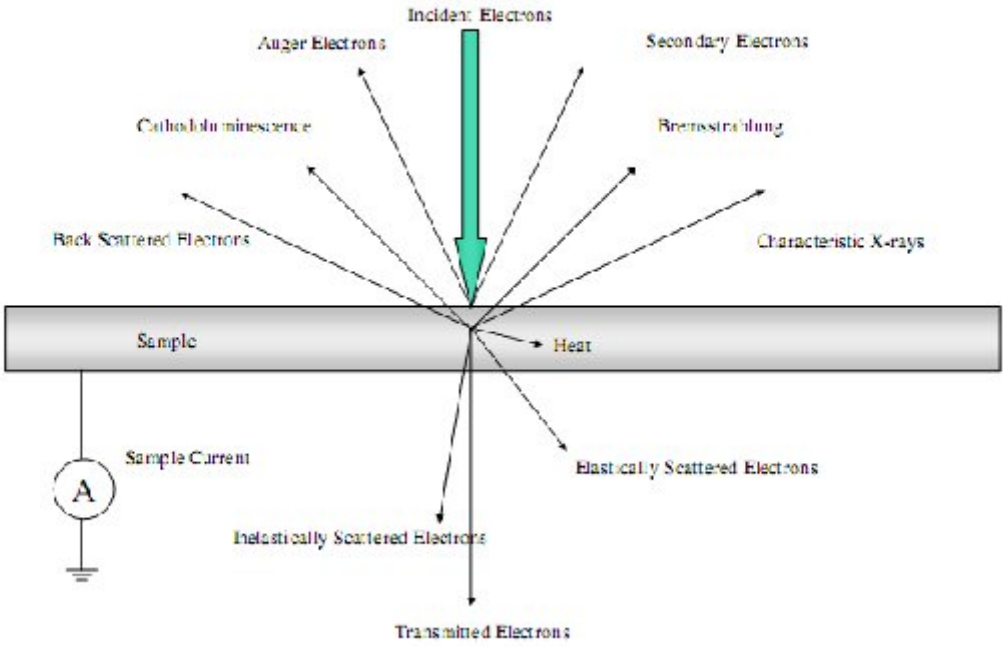


Figure 2.3: *Principal result of electron beam interaction with the sample*

The primary mode of operation for the SEM is collecting the secondary electrons. These are loosely bound outer shell electrons that are provided with enough energy by the incident electron beam to be ejected from the material. When collected, these electrons provide topographical information about the sample. A second mode of operation involves back scattered electrons. Back scattered electrons originate in the incident electron beam. The electrons are fired at the sample and after many elastic scattering events some return to the surface and leave the sample. These can be collected to provide compositional information as the number of back scattered electrons is highly proportional to the atomic number of the material.

The elements of an electron microscope are the electron source, a series of electromagnetic lenses, apertures, signal collectors and an image capture system. A simplified schematic is shown in Figure 2.4. The electrons are fired at the sample from an electron gun which can be one of several types depending on the instrument used. The most common electron gun used on older instruments is the tungsten filament which is relatively cheap but has a shorter lifetime than many other electron sources.

The accelerating voltage also helps to determine the resolution of the SEM. The resolution in the electron microscope is limited by the wave nature of electrons. The resolution and wavelength used are related through Abbe's equation

$$d = \frac{0.61\lambda}{n \sin \alpha}$$

where d is the resolution, λ is the wavelength, n is the refractive index of the medium through which the electrons are travelling and α is the numerical aperture.

The wavelength of the electron is related to the accelerating voltage:

$$\lambda = \frac{h}{\sqrt{2mqV}}$$

where h is Planck's constant, m the mass of the electron, q the charge of the electron and V the accelerating voltage. From this it can be seen that a high accelerating voltage will produce electrons with a smaller wavelength and hence a finer resolution.

The electromagnetic lens system is used to de-magnify, direct and focus the e-beam onto the sample. A series of scan and deflection coils are used to raster the e-beam across the sample to form an image. The final aperture controls the depth of field of the micrograph. A smaller aperture allows a greater depth of field but reduces the current at the sample by physically blocking a portion of the e-beam. Another variable that alters the depth of field and image resolution is the working distance, or the distance between the sample and the final lens pole piece. With an increased working distance the image resolution decreases but the depth of field is improved. For smaller working distances the opposite holds. At times a larger working distance may need to be used to allow rotation of the sample within the specimen chamber. A larger working distance is used to avoid potentially damaging the back-scattered- electron detector when mounted on the final lens pole piece.

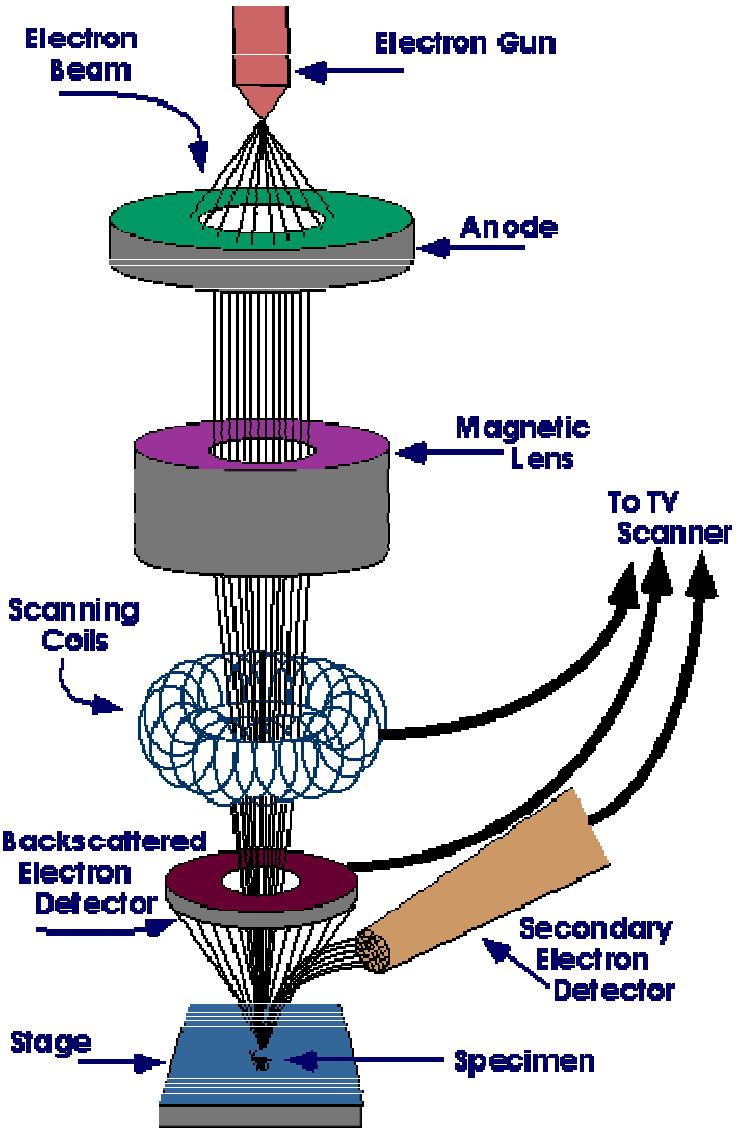


Figure 2.4: *Simplified schematic of an SEM*

The signals emitted from the sample are collected by several different types of collectors. For collecting secondary electrons an Everhart-Thornley detector is commonly used. The electrons are drawn to the detector by a metal grid with a positive bias on it. Back scattered electrons are often collected using a solid state detector (p-n junction) which is positioned around the pole piece of the objective lens. The signals from these detectors traditionally were used to display the image on a Cathode Ray Tube (CRT). In recent practice these signals have been captured by a computer which then manages the display and storage of the micrographs as image files. The micrographs can then be analyzed using analytical software to extract information, such as the size of morphological features, and printed out as required. In present work SEM

(Model: LEO 440 VP and Zeiss, EVO MA10) operating at 15 kV was used to examine the morphology of the nanostructured silicon surfaces.

2.3 Metal Coating systems

Two metal coating units are used during this project. One is thermal evaporation system, shown in Figure 2.5, was used for coating aluminium (Al) film at the rear surface of the silicon nanowire wafers required for back surface field (BSF) for solar cells and another metal deposition unit used is electron beam evaporation unit, as shown in figure 2.6, was used to deposit titanium and silver metal contacts of on the front and rear side of the silicon nanowire solar cells.

Figure 2.5: *Thermal evaporation unit at NPL, New Delhi*

For thermal evaporation unit, the required metal such as aluminium was placed in a tungsten filament basket which was attached to two electrodes within the system. Samples were placed on a framework above the filament. For the solar cells front metal grid pattern, a metal (Cu) mask, mask consisting of a series of equal-sized pattern is used for a metal coating. For deposition, the system was evacuated to a pressure in the order of 10^{-6} Torr. Once the required pressure was achieved, the filament was heated resistively by passing high current using a low tension through the filament and therefore heating the metal (Al) to the evaporation temperature of Al. Al film of thickness ~ 2 μm was deposited.

Thereafter, current was slowly reduced and switched off and system was kept in high vacuum condition to allow the samples and filament to cool down to ambient temperature. Finally, vacuum system was switched off and vacuum chamber was vent by air to take out the samples.

Figure 2.6 *Electron beam evaporation system at NPL, New Delhi*

The process of metal deposition using electron beam evaporation system is similar to that of thermal evaporation of Al except that source of heating the metal was by e-beam rather than resistive heating by passing current through the filament. The metals such as silver (Ag) and titanium (Ti) were placed in two crucibles made of graphite. After creating high vacuum of the order ~ 2.0 x 10^{-6} Torr, e-beam was focused at the centre of the respective crucible and heating of the metal takes place. The intensity of the e-beam was increased by increasing the e-gun current resulting into the melting and finally evaporation of the material. A shutter is located between the filament and the samples. Once the evaporation of the metal starts the shutter was then opened and the metal was deposited on the samples. The shutter is used to avoid the contamination, impurities (present in the evaporant) of the metal films adsorbed in the evaporant material which gets desorbed during heating to the evaporation temperature. Thickness of the film could be monitored in-situ by a quartz crystal based thickness monitor. After depositing the required film thickness of Ti, e-beam was switched off and crucible was allowed to cool for some time and then the crucible containing Ag was selected and process was repeated

to deposit the Ag film. In this way Ti/Ag layer was deposited (layer by layer) for front and rear metal contacts on the solar cells. Front surface contacts are usually made of grid pattern to allow light to fall on the cell surface. The metal covered area on the front surface should not be more than 10% of the cell surface. The back surface contact is simply a metal layer fully covering the back surface. Finally, the system was allowed to cool to room temperature, chamber was vent and sample was taken out for contact sintering.

2.4 Sintering Unit (Rapid Thermal Processing)

Sintering is a method for making objects from powder, by heating the material in a sintering furnace below its melting point (solid state sintering) until its particles adhere to each other. For the formation of back surface field (BSF) and metal contact sintering, Rapid thermal processing (RTP) unit (Model; Annelsys ASOne, France) was used. The optical photograph of the RTP system is shown in Figure 2.7 which is shown below.

Figure 2.7*: Rapid thermal processing unit for firing contacts sintering and BSF formation*.

The RTP system heating is done with set of 18 halogen lamps through a quartz window. RTP refers to a semiconductor manufacturing process which heats silicon wafers to high temperatures (850^{O} C and above) on a timescale of several seconds or less. Unlike

conventional furnace sintering/annealing process, RTP is rapid, causing very low thermal budget, well controlled temperature profile etc. The present system can reach a maximum temperature up to 1200 ˚C and can accommodate a single wafer of 6 inch diameter or several wafers of smaller dimensions at a time. The BSF formation was carried out in Ar ambient at a temperature of 850 ˚C for a soaking period of 2 minutes and heating was achieved at a ramp rate of 25-30˚C per sec. Metal contacts (Ti/Ag) sintering for both rear and front contacts, was carried out at an optimized soaking temperature of 650 ˚C for 2 minutes in nitrogen ambient. The required temperature was achieved at ramp rate of 20 ˚C.

2.5 Diffusion furnace

Diffusion furnaces are used to create a high temperature environment which is required for the diffusion of impurities in the silicon wafers. A process tube is kept inside the furnace. The furnace consists of heating coils which on giving current heats up and produces high temperature inside the furnace. Three heating coils, one at the middle, and two near edges of the tube, are secured together to form a continuous coil, with the middle heating coil enabling optimal temperature at the middle of the furnace. These three coils give three heating zones and the temperature of these three coils can be calibrated so as to give a constant temperature inside the furnace. As shown in the figure 2.8.

Formation of emitter (or p-n junction) that is n type diffusion on the front of p-silicon wafer is done in a conventional horizontal tube furnace. Quartz tube was used as process tube. P_2O_5 solid disc was used as phosphorus source shown in figure 2.9. Diffusion is done at temperature of $900^{O}C$ for time of about 40 minutes.

Figure 2.8: *Diffusion furnaces, NPL, New Delhi*

The diffusion with P_2O_5 takes place in the following way:-

The P_2O_5 forms a glass on silicon wafer and is then reduced to phosphorous by silicon

$$\mathbf{2P_2O_5 + 5Si \longrightarrow 4P + 5SiO_2}$$

and the phosphorous is released and diffuses into silicon. Procedural description of diffusion process will be given in next chapter.

Solar cells processing involving chemical cleaning, high temperature diffusion of phosphorus etc… were performed in semi clean envorinment and extreme care were taken to avoid any metal impurities like Fe, C oxygen etc. which are very harmful to the solar cell performance**.**

Figure 2.9*: P_2O_5 disc dopant source*

Chapter 3 Experimental Methodology

In this chapter, details of the experimental work, methodology and silicon nanostructures preparation, their characterization and finally integration in solar cell fabrication will be described. The typical silicon solar cell fabrication process includes the following process steps/sequence: The schematic of complete process sequence of a basic silicon solar cell fabrication is presented in Figure 4.1 and Process sequence of silicon nanowires preparation followed by solar cell fabrication on it is shown in Figure 4.2.

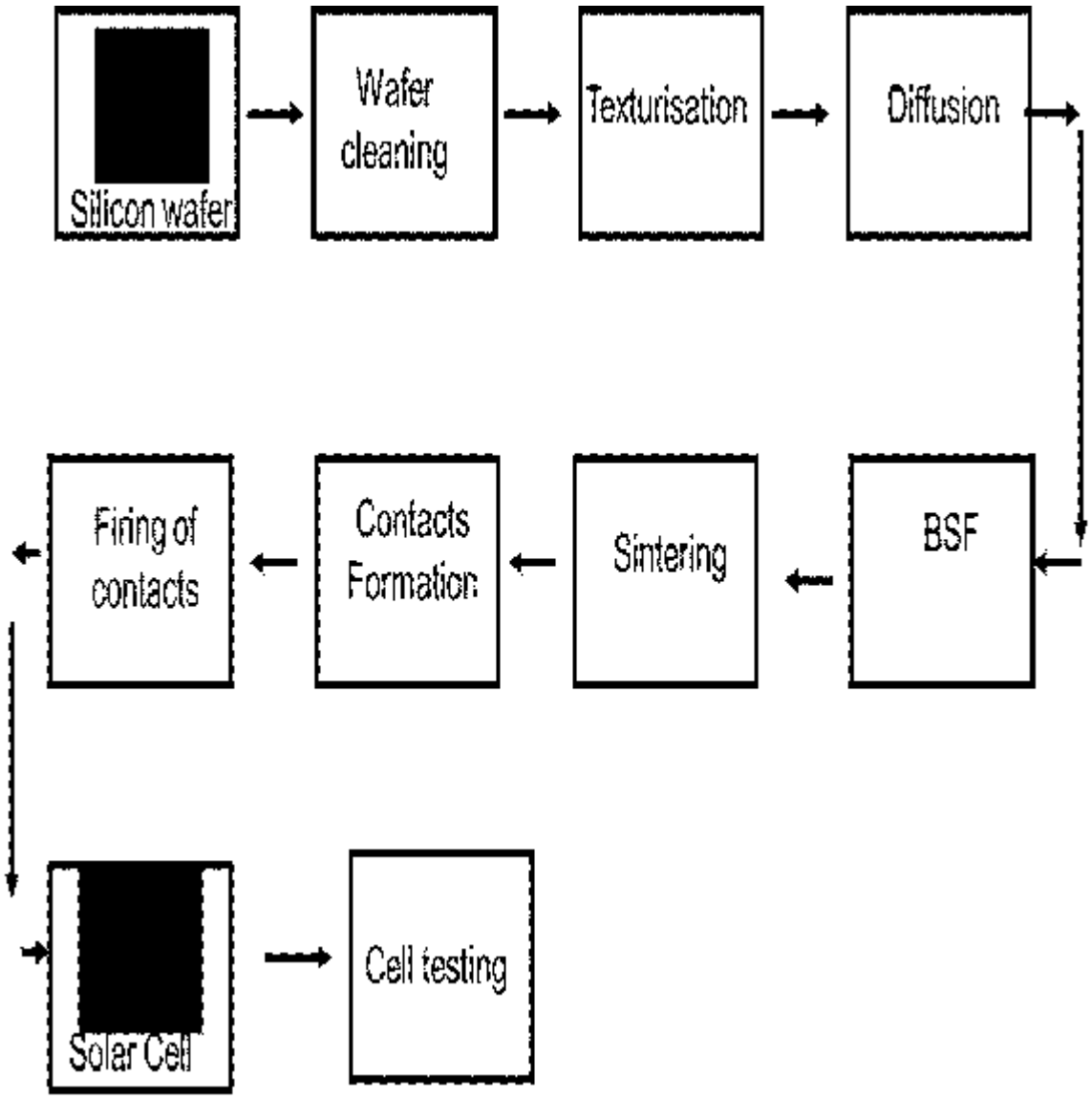


Figure 3.1: *Schematic of complete process sequence of typical solar cells fabrication.*

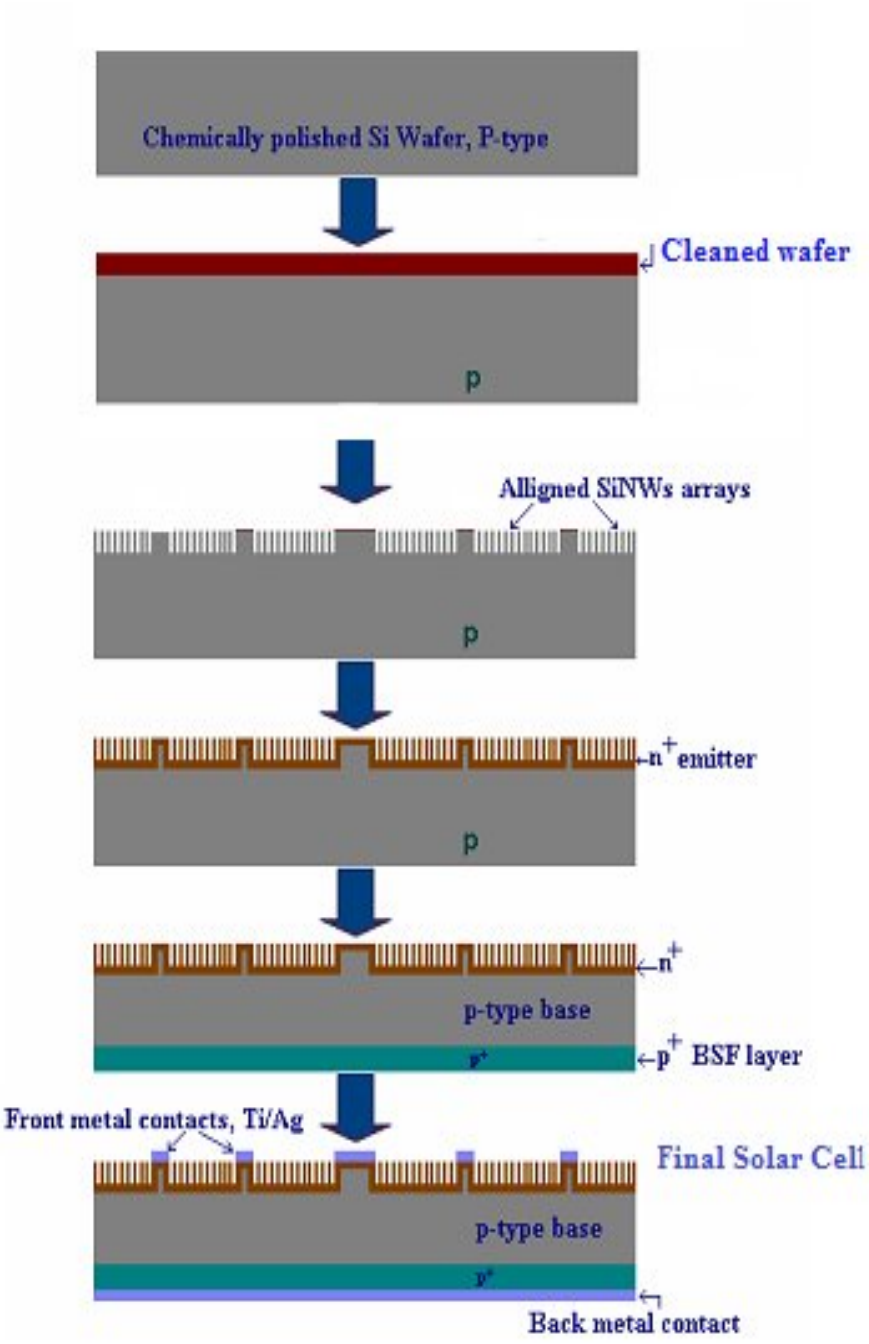


Figure 3.2: *Process sequence of silicon nanowires preparation followed by solar cell fabrication on it*

Each Process will be discussed briefly: ----

3.1 Silicon Wafer details ---

Boron doped p-type (100) orientation silicon wafers (resistivity ~ 1±0.2 Ω-cm) thickness ~ 300 μm and diameter ~ 50 mm were used in the present study.

3.2 Chemical Polishing

The wafers were as-cut which contains lots of damages on the surface (defects generated during wafer cutting of silicon ingot process due to saw or other tools used). The as-cut wafers have lots of defects and are not useful for solar cells fabrication. Therefore the very first step of solar cell fabrication is to remove saw-damages via chemical etching of wafers in suitable chemical. Wafer is polished manually with chemical namely acetic acid, HF and nitric acid with 1:1:5 ratio respectively. Wafers were polished in Teflon beakers for about 3 minutes each to get the desired results for this project. In this process about 10-15 μm silicon is etched from both sides. To get uniform etching wafers are continuously stirred during etching. After etching in $HF+CH_3COOH+HNO_3$ (1:1:5 vol.), the wafers were rinsed copiously with DI water followed by drying with nitrogen or air. Acetic acid is used to moderate the rate of reaction.

3.3 Cleaning of silicon Wafer

Cleaning of silicon wafer is done by two processes or solutions. First is *Piranha Solution* and second is using *RCA (Radio Corporation of America) process*. Piranha solution is used before the silicon nanowire growth whereas RCA process is used prior to the high temperature diffusion process.

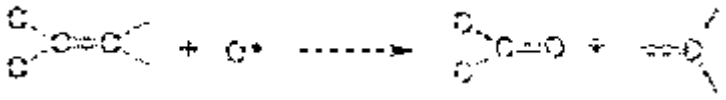
Piranha Solution: It consists of sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2) in 4:1 ratio by volume, and is used to clean organic residues from the substrates. Because the mixture is a strong oxidizer, it will remove organic contaminations, and it will also hydroxylate most surfaces (add OH groups), making them extremely hydrophilic (water compatible) surface.

Mechanism of cleaning in Piranha solution: ----

H_2SO_4 boosts conversion of H_2O_2 from a relatively mild oxidizing agent into one sufficiently aggressive to dissolve elemental carbon, a material that is notoriously resistant to room temperature aqueous reactions. This transformation can be viewed as the energetically favourable dehydration of H_2O_2 to form hydronium ions, bisulphate ions, and, transiently, atomic oxygen as below:-

$$H_2SO_4 + H_2O_2 \rightarrow H_3O^+ + HSO_4^- + O$$

It is this extremely reactive atomic oxygen species that allows piranha solution to dissolve elemental carbon. Carbon allotropes are difficult to attack chemically because of the highly stable and typically graphite-like hybridized bonds that surface carbon atoms tend to form with each other. The most likely route by which piranha solution disrupts these stable carbon-to-carbon surface bonds is for atomic oxygen first to attach directly to a surface carbon to form a carbonyl group:



RCA Cleaning Process: The RCA cleaning is a standard set of wafer cleaning steps which needs to be performed before high temp processing steps (oxidation, diffusion, CVD) of silicon wafers in semiconductor manufacturing. RCA cleaning includes RCA-1 and RCA-2 cleaning procedures. RCA-1 is done for the removal of organic contaminants, while RCA-2 for the removal of oxides and RCA-3 for metallic contaminants.

Werner Kern developed the basic procedure in 1965 while working for RCA, the Radio Corporation of America. It includes the following:

1. Removal of the organic contaminants (Organic Clean)

2. Removal of thin oxide layer (Oxide Strip)

3. Removal of ionic contamination (Ionic Clean)

Procedure is described below:-

The wafers are prepared by soaking them in DI water.

The first step (called SC-1, where SC stands for Standard Clean) is performed with a 1:1:5 solution of NH_4OH (ammonium hydroxide) + H_2O_2 (hydrogen peroxide) + H_2O (DI water) at 75-80 °C typically for 10 minutes. This treatment results in the formation of a thin silicon dioxide layer (about 10 Angstrom) on the silicon surface, along with a certain degree of metallic contamination (notably Fe) that shall be removed in subsequent steps. This is followed by transferring the wafers into a DI water bath.

The second step is a short immersion in a 1:50 solution of HF + H_2O at 25 °C, in order to remove the thin oxide layer and some fraction of ionic contaminants.

The third and last step (called SC-2) is performed with a 1:1:5 solutions of HCl + H_2O_2 + H_2O at ~80 °C. This treatment effectively removes the remaining traces of metallic (ionic) contaminants.

3.4 Texturisation (Silicon Nanowires Array Growth)

Growth of SiNWs arrays was carried out on piranha cleaned p-type, B-doped (100) silicon (1 Ω- cm) wafers in a Teflon beaker containing 5.0mol L^{-1} aqueous HF solution and 0.02mol L^{-1} and 0.05mol L^{-1} Ag_2O (Silver Oxide) at room temperature (30 ^{O} C).

The cleaned silicon wafers were inserted in the etching solution for different times. A thick layer of Ag layer deposited as immediately after the contact of silicon surface with solution. In this process, self-controlled galvanic reaction takes place in which both reduction and oxidation reactions takes place simultaneously at the interface of the metal (Ag) and semiconductor (silicon) surface. The deposited Ag act as active cathode and silicon surface in the contact with Ag as an anode. Holes are injected in the silicon valence band catalysed by Ag locally (Ag^{+}/Ag system). Therefore, silicon Si surface is oxidized locally which is immediately etched by HF. Therefore, a large number of nano-electrochemical cells are formed. This process continues with time. Very thick film of silver is deposited. The silicon wafer is fully wrapped with Ag layer. If the reaction is allowed to occur for longer duration, silicon nanowires structures are evolved due to selective etching of the wafers. The remaining (No-etched silicon wafers sections) silicon form the nanowires array structure. Silver film is removed from the conventional etchant namely ammonia hydroxide, hydrogen peroxide in the ratio of 3:1 respectively and i.e. NH_4OH:H_2O_2= 3:1.Then wafers were rinsed with DI water.

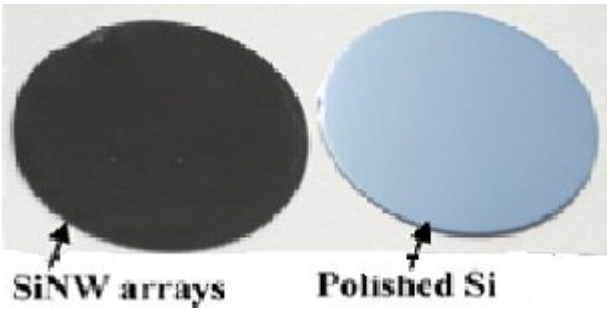


Figure 3.3 *Optical photograph of silicon nanowires array based wafer and polished wafer*

Calculation

E.g.1

To prepare 0.05 M Ag_2O in 100 ml of 25% HF solution (80 ml of DI water + 20 ml HF)

Molecular weight of Ag_2O is 231.78.

Volume of solution is 100ml

So, 0.05(grams/ litre) X 231.78 X 0.1 litre = 1.15 grams

E.g.2

To prepare 0.02 M Ag_2O in 100 ml of 25% HF solution (80 ml of DI water + 20 ml HF)

Molecular weight of Ag_2O is 231.78.

Volume of solution is 100ml

So, 0.02(grams/ litre) X 231.78 X 0.1 litre = 0.46 grams

3.5 Diffusion

Diffusion of impurities is typically done by placing semiconductor wafers in a carefully controlled high temperature quartz tube furnace and passing a gas mixture that contains the desired dopant through it. The temperature usually ranges between 800° and 1200° C for silicon. For diffusion in silicon, boron is the most popular dopant for introducing a p-type impurity, although aluminium is also widely used. Arsenic and phosphorous are extensively used as n-type dopants. In case of solar cells, n-type diffusion is preferred over p-type diffusion since minority carriers are responsible for conduction of current in a solar cell and the mobility of electrons is higher than that of holes. In solar cell and integrated circuit processing, a two-step diffusion process is used. They are:--

1) PREDEPOSITION

In this process a pre-deposition of diffused layer is formed under a constant surface concentration condition. Wafers are placed with dopant source (P_2O_5 disc

source in the present case) in the diffusion tube preheated at 900 °C. A thin layer of dopant atom is deposited on the surface of the wafers.

2) DRIVE – IN

The pre deposition step is followed by drive - in diffusion under a constant total dopant condition. Wafers are placed in the tube without the dopant source. In this step, the dopant atoms which are deposited on the surface of the wafers penetrate into the wafer and a p-n junction is formed.

Procedure is described below:-

The diffusion of phosphorus in p-type wafers was carried out in the following steps:

1. Clean the diffusion tube with 1:3::HF: HNO_3 solution carefully followed by rinsing with DI water copiously.
2. Put the tube into the furnace.
3. Start the nitrogen flow at the speed of 100 lph in the tube. This is done to remove the impurities from the tube. Nitrogen gas also acts as a carrier gas i.e. it carries forward the vapours of the dopant source.
4. Switch on the furnace and set the temperature to 900° C.
5. Allow the nitrogen to flow in the tube for 3 to 4 hours. Also the furnace will take around I hour to attain the temperature of 900° C.
6. Place the wafers and the activated dopant source disc on a quartz boat such that only side/surface to be made emitter (n-type) should face the dopant source (as shown below).

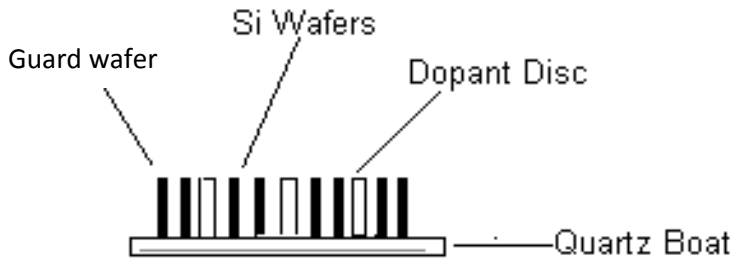


Figure 3.4: *Silicon wafer and dopant source arrangement in quartz boat for P-type diffusion*

7. Two guard wafers are also placed to prevent diffusion to occur on the back surface of the extreme wafers.
8. Insert the boat into the tube (PREDEPOSITION) step. Keep it inside the tube for 40 min. During this step there is a constant surface concentration of P after diffusion.
9. After 40 min take out the boat from the tube.
10. Remove the dopant source disc from the boat and insert the boat with wafers only in the tube for 20 min. This process is called DRIVE – IN step.
11. Switch of the heater of the furnace and allow it to cool down. Allow the nitrogen to flow in the tube till the temperature of the furnace reaches below 200, stop the nitrogen flow.

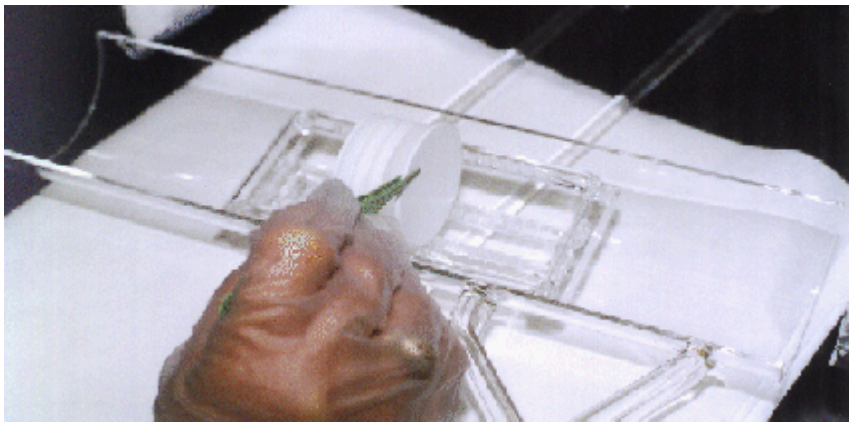


Figure 3.5: *Loading of source wafer*

Figure 3.6: *A view of the diffusion tube during the experiment*

3.6 Back surface field(BSF) Formation

A "***back surface field" (BSF)*** consists of a higher doped region at the rear surface of the solar cell. The interface between the high and low doped region behaves like a p-n junction and an electric field forms at the interface which introduces a barrier to minority carrier flow to the rear surface. The minority carrier concentration is thus maintained at higher levels in the undoped region and the BSF has a net effect of passivating the rear surface.

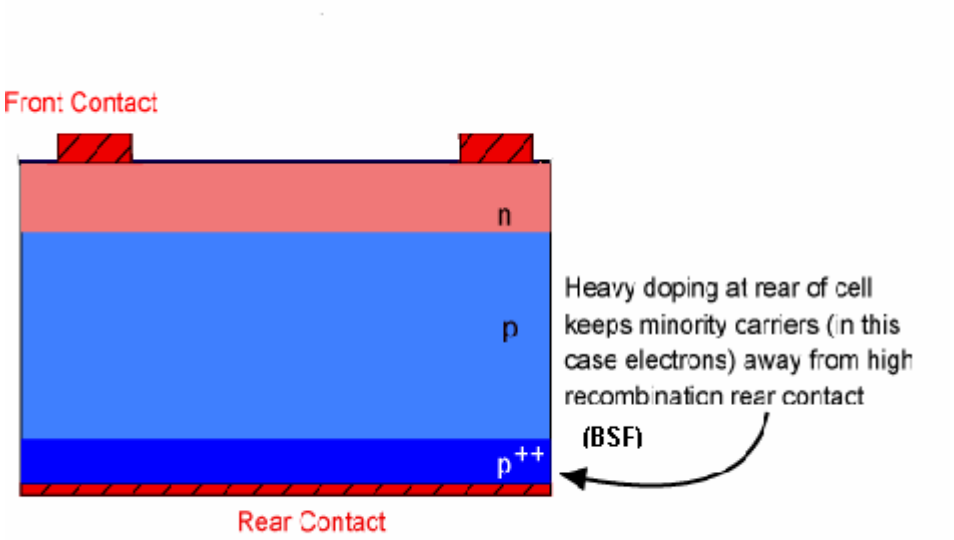


Figure 3.7: *Cross sectional view of conventional silicon solar cells with a BSF layer.[18]*

The BSF layer is obtained by providing a lower resistivity, highly doped layer of the same type as the base layer on the back surface (for e.g. p+ layer at the back of the p type base layer).The HIGH LOW JUNCTION establishes an energy barrier for the minority carriers, minimizing the loss of these carriers at the back of the cell where the recombination velocity is high i.e. this junction acts as a low recombination velocity surface. This improves open circuit voltage and current output. At the same time it makes a lower resistance ohmic contact for minority carriers [18] (PVCDROM, University of New South Wales website).

In this process a thin layer of aluminium (~ 2-3 μm) is coated at the back surface of the wafer in the vacuum coating unit followed by alloying with silicon at 850 ˚C in RTP to form a highly doped p+ layer.

Procedure is described below:-

1) The aluminium source to be deposited on the wafers is boiled in tri-chloro ethylene solution.
2) Then it is placed in a tungsten boat (holder).
3) The boat is connected between the electrodes.
4) Silicon wafers are mounted in a zig capable of holding 4-5 wafers of 50 mm diameter, the zig with wafers is then loaded in the vacuum chamber.
5) Now the high vacuum of the order of ~2x10 $^{-6}$ Torr is created in the chamber with the help of vacuum pumps. When the desired pressure is attained, current is applied through the electrodes using a low tension source which heats the boat and Al resulting into the melting and finally evaporation of Al on increasing the current further.
6) The evaporated aluminium gets deposited on the exposed area of the wafers.
7) The thickness of the Al layer so formed is approximately 2 μm.

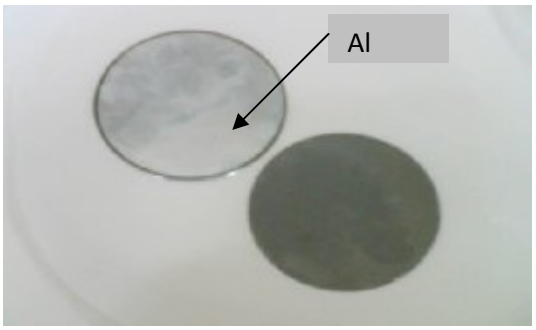


Figure 3.8: *Bare and aluminium coated silicon wafer*

3.7 Sintering

Sintering of AL-coating at ~850^{o}C for 2 min in hydrogen ambient is done to make p^{+} layer (BSF layer).This is done to firm the binding of aluminium (Al) with the silicon wafer. The eutectic of Al-Si binary alloy is 577˚C therefore for diffusion of Al into silicon, sintering should be done at temperature higher than eutectic. Sintering is done in RTP as it has been mentioned in chapter 2. Detailed procedure of sintering will be discussed in firing of contacts in the last section of this chapter.

3.8 Metal contacts deposition

For front and back contacts on solar cells, Ti and Ag layers were deposited sequentially on full rear surface whereas in grid pattern on the front side through a suitable metal mask. This process is also carried out in the vacuum evaporation coating unit.

Procedure is described below:-

1) The Ti and Ag metal evaporants to be deposited on the wafers are boiled in tri-chloro ethylene solution to remove grease or any other impurities.

2) Then Ti is placed in a spiral shaped tungsten boat (holder) and silver is placed in the flat molybdenum boat.

3) Silicon wafers are mounted in a zig capable of holding 4-5 wafers of 50 mm diameter; the zig with wafers is then loaded in the vacuum chamber. For front side metal coating, wafers front side is placed on the mask (side facing the metal source to be evaporated)

4) Now the high vacuum of the order of ~$2x10^{-6}$ Torr is created in the chamber with the help of vacuum pumps. When the desired pressure is attained, current is applied through the electrodes using a low tension source which heats the boat and hence the metal resulting into the melting and finally evaporation of the metal on increasing the current further. Ti of thickness ~ 40 nm is evaporated followed by Ag of thickness ~ 2 μm.

5)Now the process is repeated to obtain a similar coating on the back surface of the wafers also.

3.9 Firing the Contacts/Sintering

Sintering is the process which is performed to make front and back ohmic contacts on the wafer. This is done to make the contacts firm and durable. Also the ohmicity of the contacts improves due to sintering because the metal used for making contacts diffuses minimally into silicon. For this purpose, Ti/Ag coated wafers are sintered in non-oxidizing ambient using RTP at required temperature.

Procedure is described below:-

1) For sintering in RTP, recipe is prepared which includes evacuating process chamber by pump, filling of inert atmosphere such Ar or N2, ramping the temperature to the desired sintering temperature and time etc.

2) Switch On the water chillier required for dissipate the heat from RTP.
3) Open the process chamber and load the wafer on the wafer holder made of quartz pins.
4) Vacuum is developed, Argon gas is made to pass through the tube. This expels the air and other non-desirable gases out of the tube.
5) Now nitrogen gas is made to pass through the tube to RTP.
6) Start the process, wait for completion of process.
7) Unlock the chamber, start purging.
8) Wait till the temperature come down to prevent the thermal shock. Then open the chamber take out the wafer.
9) Close the chamber.

3.10 Edge isolation

The solar cells prepared were scribed using laser scriber to remove edge shunting. Solar cells of ~ 2 .4 x 2.4 cm^2 were diced from the 50 mm round wafers.

Finally, after performing all the above steps silicon nanostructured solar cell are ready for testing.

3.11 Solar Cell Testing/ characterization

Finally, the performance of the solar cells was characterized by the measuring I-V, spectral response, quantum efficiency and analysis of efficiency, and other solar cells parameters which will be discussed in chapter 4.

Chapter 4 Results and Discussion

4.1 Samples Details

Boron doped p-type (100) orientation silicon wafers (resistivity ~ 1±0.2 Ω cm) thickness ~ 300 μm and diameter ~ 50 mm were used in the present study. We have made number of samples of silicon nanowire using different concentration of silver oxide (Ag_2O) in different volumes of HF solutions. Based on our number of experimental results, optimum parameters particularly, Ag_2O molar concentration and HF concentration have been optimized for fabrication of silicon nanowires array using Ag_2O+HF etching system. Therefore, the results of only representative samples obtained under optimum preparation condition will be discussed along with possible mechanism. It was concluded that aqueous HF solution (25 % by volume) containing 0.05 M Ag_2O is the optimum for the etching of silicon wafers (p-type, (100)) to produce the vertically aligned silicon nanowires structure as will be discussed in the following section. Scanning electron Microscopy (SEM) was used extensively to examine/investigate the morphology of the etched silicon wafers under various etching conditions.

Etching of the wafers was carried out by varying the following parameters:

(i) Ag_2O molar concentration for fixed aqueous HF solution concentration (0.01-0.1 M)

(ii) Variation of HF concentration for fixed (optimized Ag_2O molar concentration) (10-50 %)

(iii) Etching time (15 min-15 hours)

Note: Etching of the wafers was carried out at room temperature (~ 30 ˚C).

Summary of the experimental parameters for the best samples is presented in table 1.

Table 4.1 *Samples details and preparation conditions*

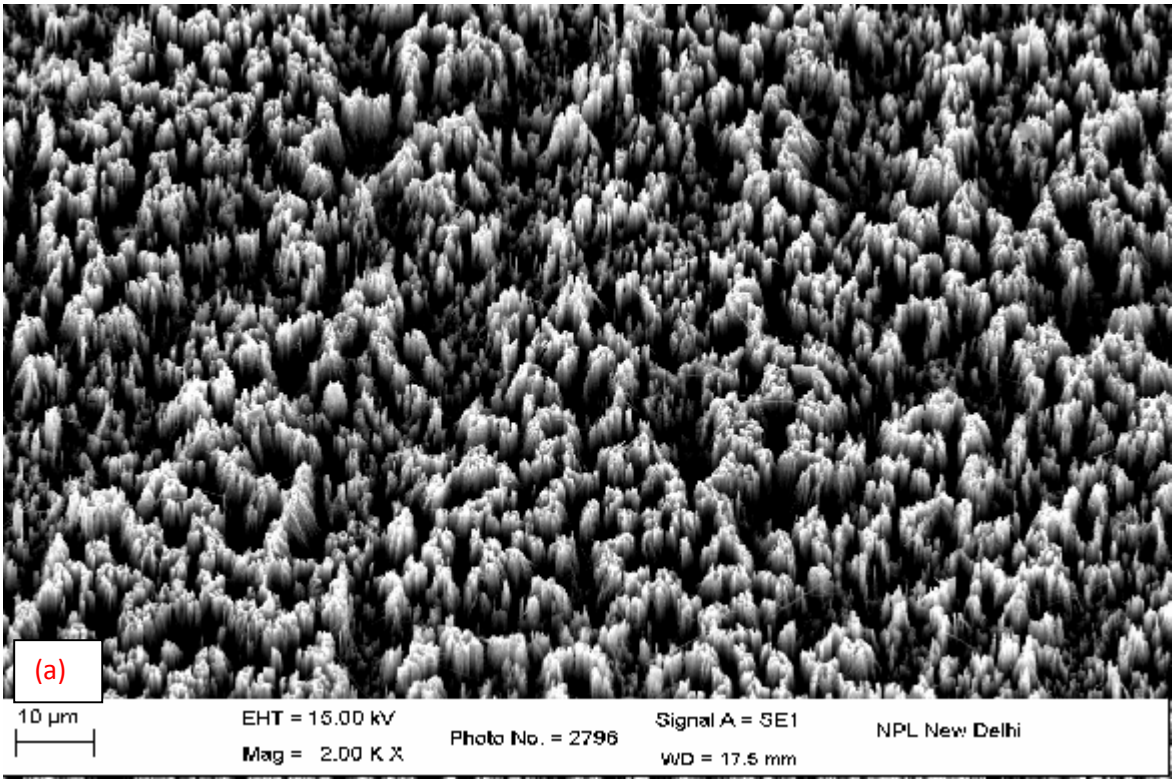
Sample Name	Ag_2O Molar conc.	HF Conc.	Etching Time
Sample 1	0.02 M	25%	1 hour
Sample 2	0.05 M	25%	1 hour

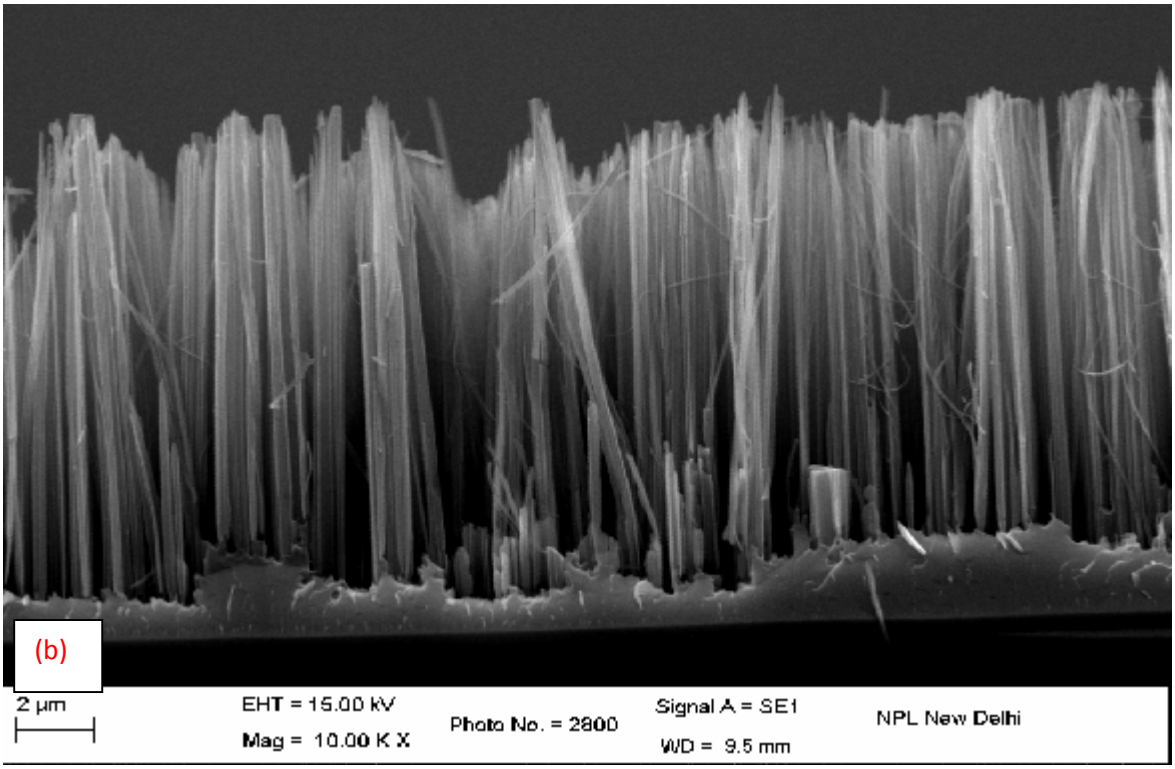
The silicon nanowires based silicon wafers (after removing Ag) have almost black/brown appearance which indicated for very low surface reflectivity of the samples in the visible optical range (400-800 nm). This motivated us to investigate their surface reflection properties. Therefore, surface reflectivity measurement result of one representative sample (sample 1) will also be discussed. Finally, an attempt was made to investigate the application of silicon nanowires in solar cells. Hence, solar cells were fabricated on nanowires array based silicon wafers using the process steps as discussed in chapter 3. In order to compare the solar cell performance parameters, a planar reference solar cell (without silicon nanowires) was also fabricated in the same batch (i.e. under identical fabrication conditions). The results of solar cells performance measurements such as I-V characteristics, efficiency, short circuit current, open circuit voltage, parasitic resistances (series and shunt), spectral response and quantum efficiency the both the solar cells (with nanowires and planar cells) will be discussed.

4.2 Results and discussion

4.2.1 Fabrication and Surface morphology of etched silicon samples (SEM analysis); Silicon nanowires

Fig. 4.1 (a) shows the top view of the SEM image of the etched silicon wafers in Ag_2O +HF+DI water etchant system containing 0.02 M Ag_2O for 1 hour. As can be seen uniform etching of the wafers is obtained evolving one-dimensional structures. Cross-section view of the sample is shown in Fig. 4.1(b) and corresponding magnified view in Fig. 4.1c. Fig.4.1(b) and (c) clearly show that vertically aligned silicon nanowires array of length 20-25 microns is obtained in 1 hour at room temperature.


(a)
10 µm
EHT = 15.00 kV
Mag = 2.00 K X
Photo No. = 2796
Signal A = SE1
WD = 17.5 mm
NPL New Delhi


(b)
2 µm
EHT = 15.00 kV
Mag = 10.00 K X
Photo No. = 2800
Signal A = SE1
WD = 9.5 mm
NPL New Delhi

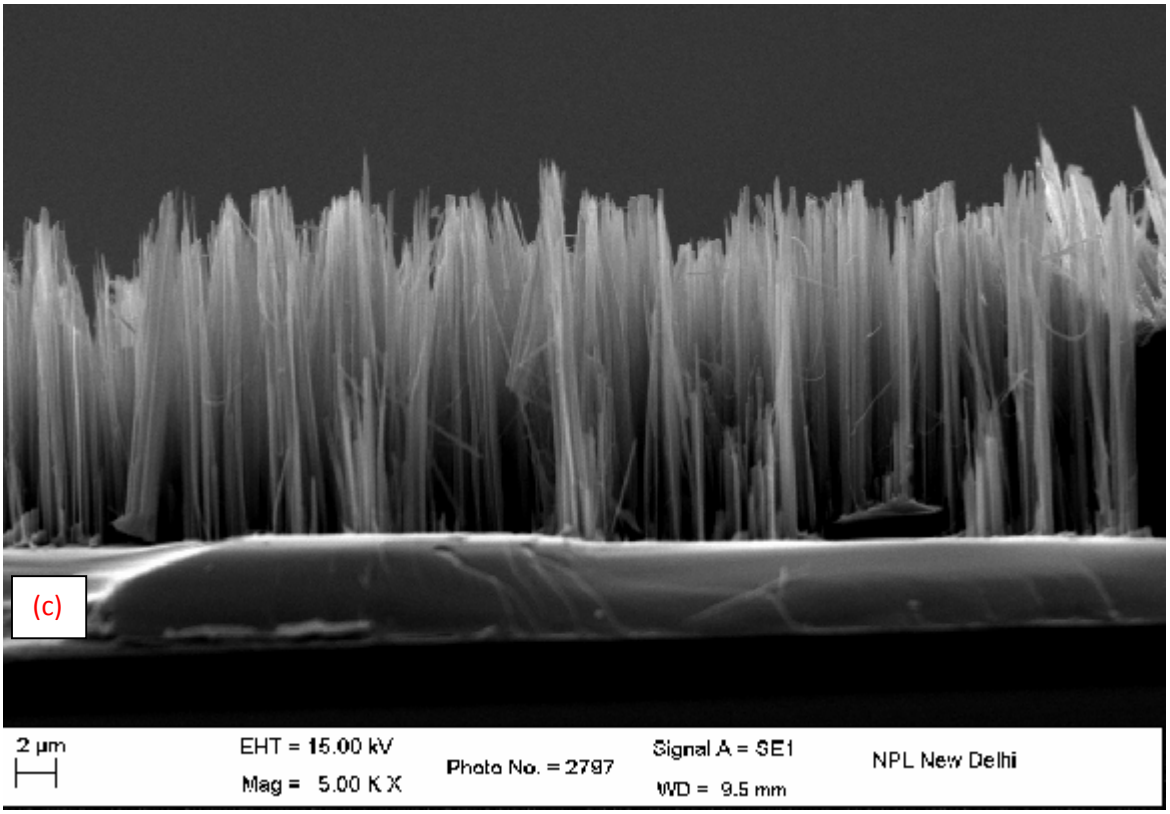
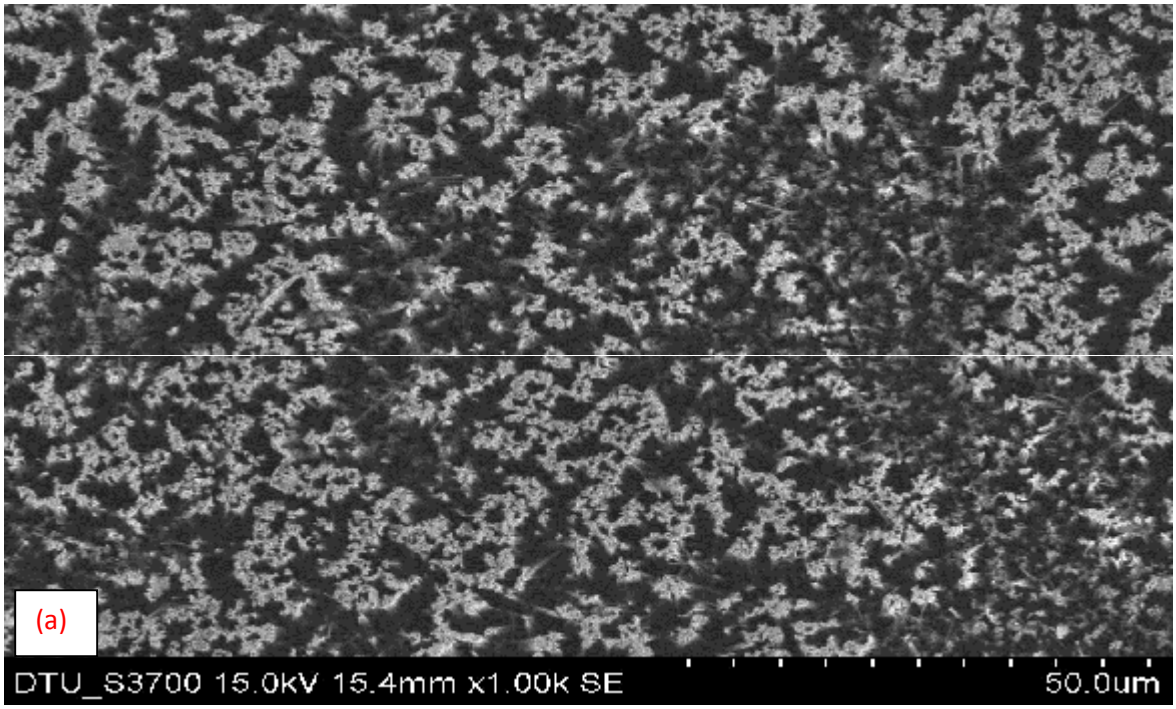
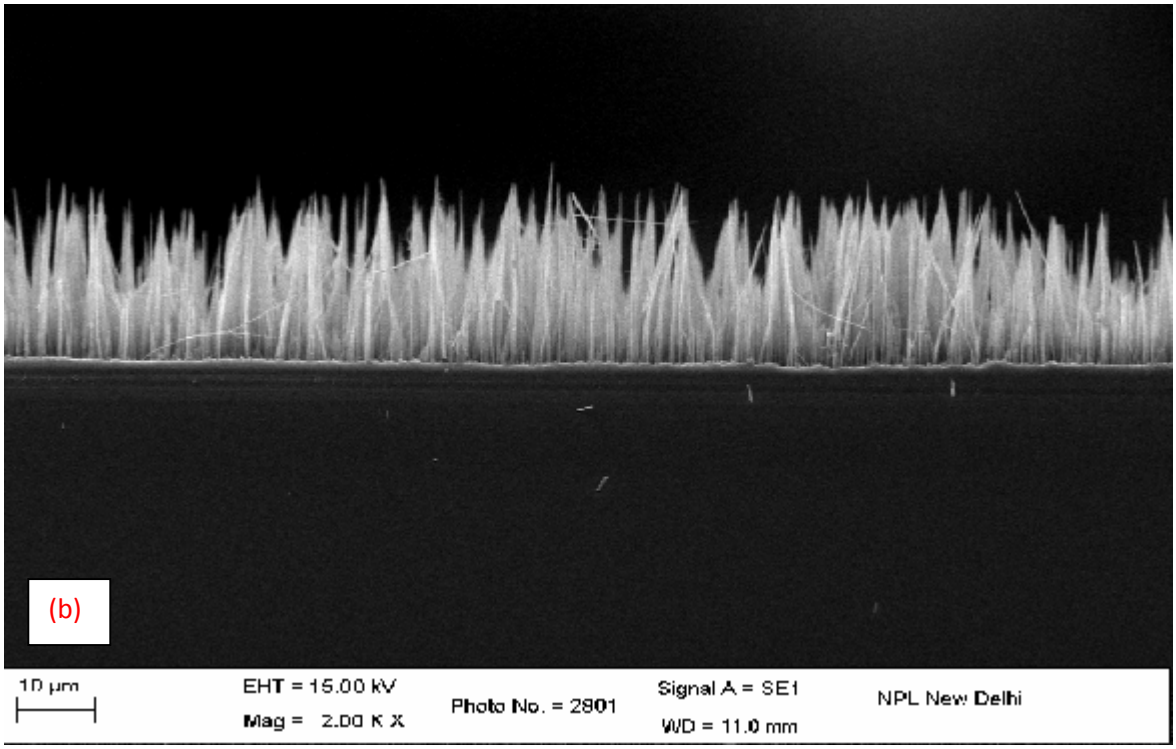


Figure: 4.1 *Scanning electron microscopy (SEM) pictures of Silicon nanowires with 0.02M Ag_2O concentration with 1 hour etching (a) Top view (b) cross-sectional view with 10K X magnification (c) cross-sectional view with 5K X magnification.*

Similarly, Fig. 4.2 (a) shows the top view of the SEM image of samples etched in 0.05 M Ag_2O solution for 1 hour. Fig. 4.2 (b) and 4.2 (c) shows the cross-sectional SEM image of vertically aligned silicon nanowire arrays prepared for 1 hour. The length of silicon nanowires in sample 2 is more than that observed in sample 1. One very important observation in sample 2 is that silicon nanowires have very sharp tips in contrast to uniform diameter of nanowires of sample 1.


(a)
DTU_S3700 15.0kV 15.4mm x1.00k SE
50.0um


(b)
10 µm
EHT = 15.00 kV
Mag = 2.00 K X
Photo No. = 2801
Signal A = SE1
WD = 11.0 mm
NPL New Delhi

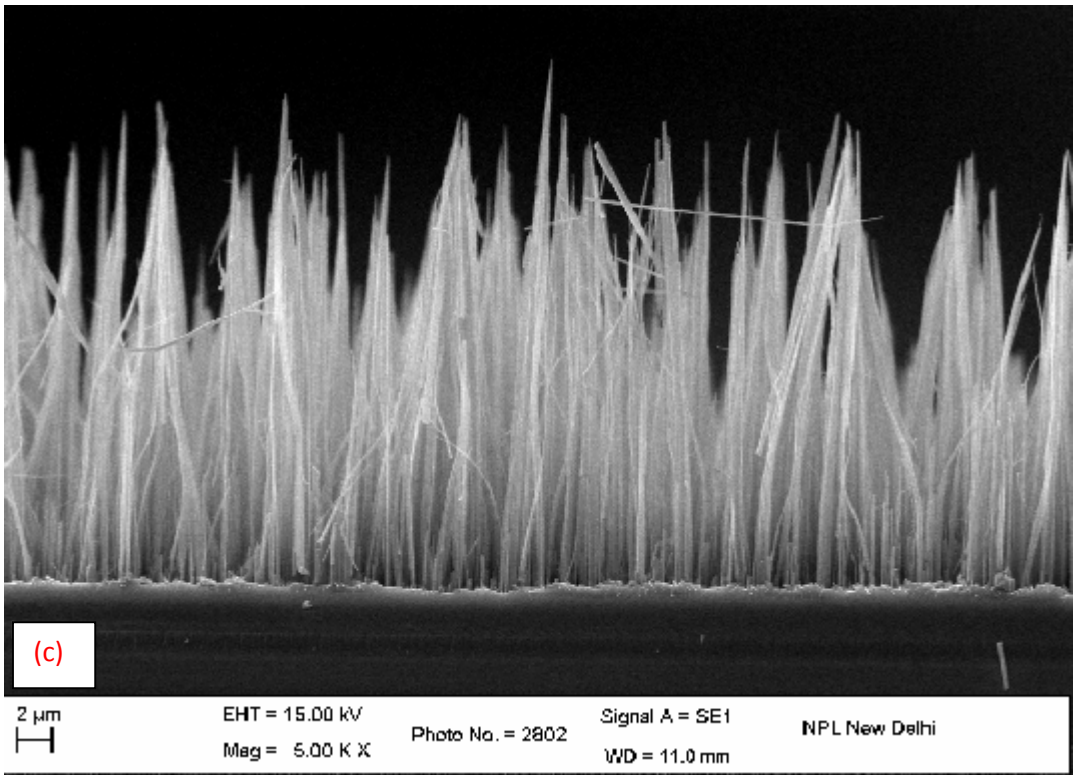


***Figure**: 4.2 Scanning electron microscopy (SEM) pictures of Silicon nanowires with 0.05M Ag_2O concentration with 1 hour etching (a) Top view (b) cross- sectional view with 2K X magnification (c) cross-sectional view with 5K X magnification*

4.2.2 Chemical reaction involved in Si-NW Growth

It is well-accepted that the chemical or electrochemical reactions occur preferentially near the noble metal. Various possible cathode and anode reactions have been proposed to describe the metal-assisted chemical etching analogous to the anodic etching of Si in HF.

It is well accepted that the H 2 O 2 is reduced at the metal (cathode reaction):

$$H_2O_2 + 2H^+ \rightarrow 2H_2O + 2h^+ \quad (1)$$

Meanwhile, Li and Bohn and Harade et al. proposed that the reduction of protons into hydrogen was another cathode reaction in addition to reaction (1):

$$2H^+ \rightarrow H_2 \uparrow + 2h^+ \quad (2)$$

At the anode, the Si substrate is oxidized and dissolved. There are numerous models proposed for the dissolution process of Si (anode reaction), which can be catalogued into three groups:

(RI) Direct dissolution of Si in tetravalent state

$$Si + 4h^+ + 4HF \rightarrow SiF_4 + 4H^+ \quad (3)$$

$$SiF_4 + 2HF \rightarrow H_2SiF_6 \quad (4)$$

(RII) Direct dissolution of Si in divalent state

$$Si + 4HF_2^- \rightarrow SiF_6^{2-} + 2HF + H_2 \uparrow + 2e^- \quad (5)$$

(RIII) Si oxide formation followed by dissolution of oxide

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O \quad (6)$$

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O \quad (7)$$

Model RII and RIII differ in whether Si oxide is formed at the surface of the Si substrate before the dissolution of Si and whether H_2 is generated accompanying the dissolution of Si. It seems that model RII happens because hydrogen is generated in a typical etching.

Chartier et al. proposed a mixed reaction composed of divalent and tetravalent dissolution for the dissolution of Si in metal-assisted chemical etching:

$$Si + 6HF + nh^+ \rightarrow H_2SiF_6 + nH^+ + \frac{4-n}{2}H_2 \uparrow \quad (8)$$

and the overall reaction is:

$$Si + \frac{n}{2}H_2O_2 + 6HF \rightarrow nH_2O + H_2SiF_6 + \frac{4-n}{2}H_2 \uparrow \quad (9)$$

4.2.3 Mechanism Involved in Silicon nanowire (Si-NW) preparation

The mechanism of formation of vertically aligned Si-NW arrays can be understood as being a self-assembled Ag-induced selective etching process based on localized microscopic electrochemical cell model as presented schematically in Fig.4.5. The process

is based on the continuous galvanic displacement of Si by Ag^+ via $Ag^+ \rightarrow Ag$ reduction on the silicon surface and hence forming many local Nano-electrochemical cells on the silicon surface. The deposited Ag nanoparticles act as active cathode and silicon surface in contact with the Ag nanoparticles as active anode.

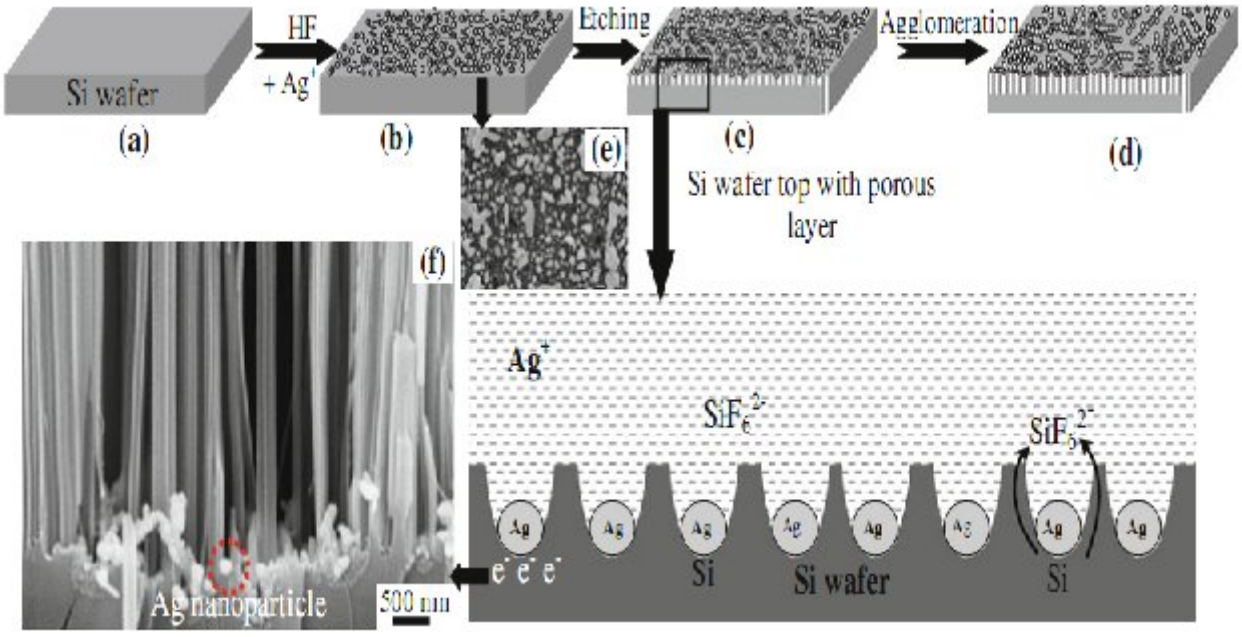


Figure 4.3: *Schematics of the Si-NWs growth mechanism by Ag-induced selective chemical etching of silicon surface in HF–Ag_2O solution via self-assembled Nano-electrochemical cell model.*

In brief, Ag^+ ions get reduced to Ag onto the silicon surface by injecting holes into the Si valence band and oxidizing the silicon surface locally in contact with Ag. The oxidized surface is subsequently etched away by HF. The deposited Ag Nano clusters are initially uniformly distributed throughout the surface of the silicon wafer (as shown schematically in Fig. 4.5 b). Further reduction of Ag^+ occurs on the Ag Nano clusters being an active cathode by electron transfer from the underlying wafer (Ag being relatively highly electronegative than the silicon and hence provide easy injection path for holes), but does not occur on the uncovered Si surface. The increasing size of the Ag clusters via this mechanism is shown schematically in Fig. 4.5 c and d. The complete self-assembled Ag-induced redox reaction is presented schematically in magnified view of Fig. 4.5c. In the next step, Ag Nano clusters agglomerate to form the dendritic structures and hence a non-compact Ag film (as shown in Fig. 4.5d). The dimensions of the nanowires are primarily

controlled by these Ag Nano- clusters and their network after they get trapped into the silicon. Once the Ag Nano-clusters get trapped into the silicon pores, they move deeper and deeper resulting into the 1-D nanostructures or Si-NWs.

4.2.4 Optical Property: Surface Reflectivity

Figure 4.5 shows the comparative spectral dependent surface reflectivity of nanowires array based silicon sample 1 and that of polished silicon. It is clearly seen that reflectivity of nanowires based sample is reduced significantly to around 10% as compared to ~35% of polished silicon in the entire spectral range of interest 400-1100 nm. Therefore, silicon nanowire can have potential application in silicon solar cells as an effective light trapping surface.

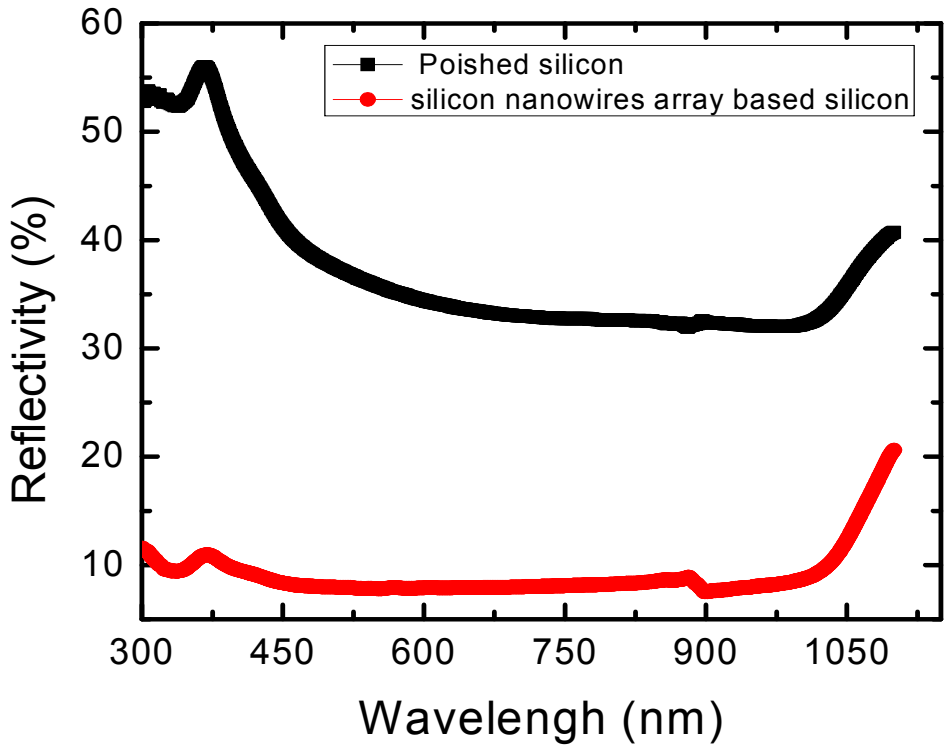
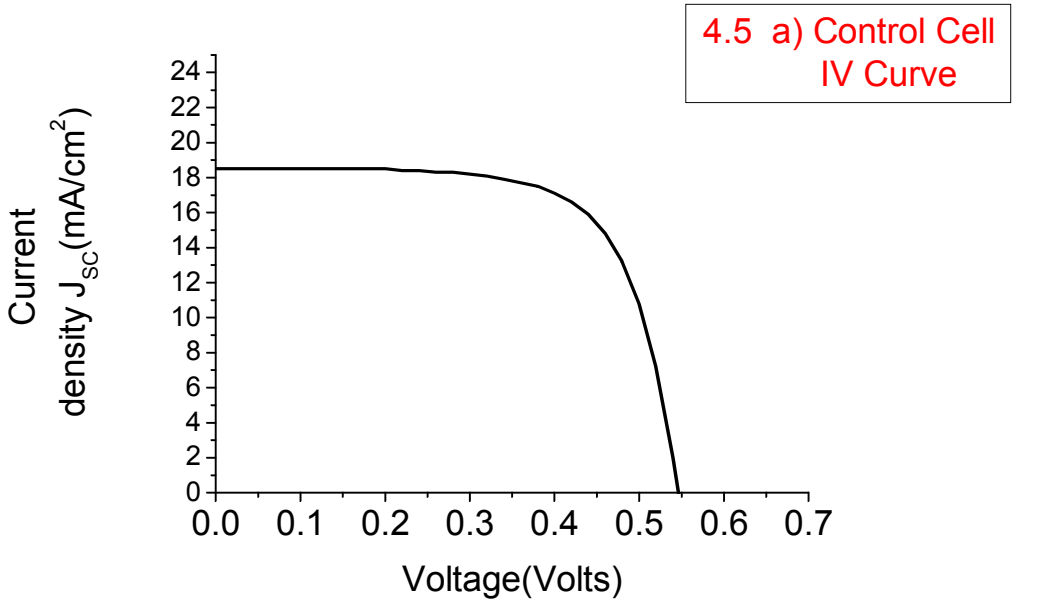


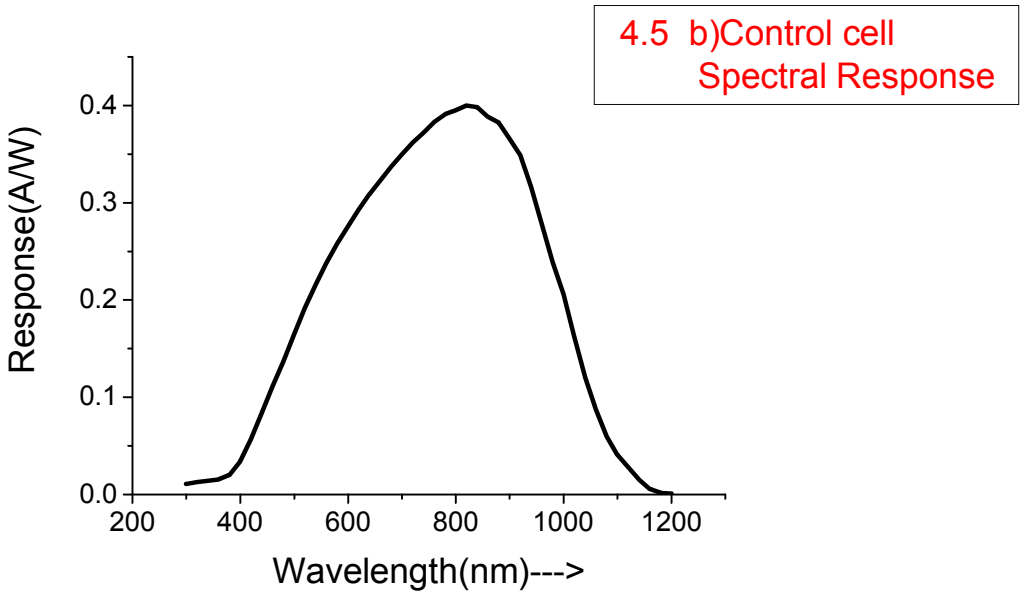
Figure 4.4 *Comparative spectral dependence surface reflectivity plots of silicon nanowires array based sample and polished silicon surface.*

4.2.5 Solar cells performance

4.2.5.1 I-V curves, Spectral Response graphs and Quantum efficiency (QE) graphs

Figure 4.3 and figure 4.4, as shown below, shows the I-V characteristics, Spectral response and quantum efficiency of planar reference silicon solar cells and silicon nanowires based solar cells. The comparative solar cell performances viz. short circuit density Jsc, open circuit voltage Voc, fill factor, FF, power, efficiency η, series Rs and shunt Rsh resistances etc. of the two solar cells are summarized in table 2.





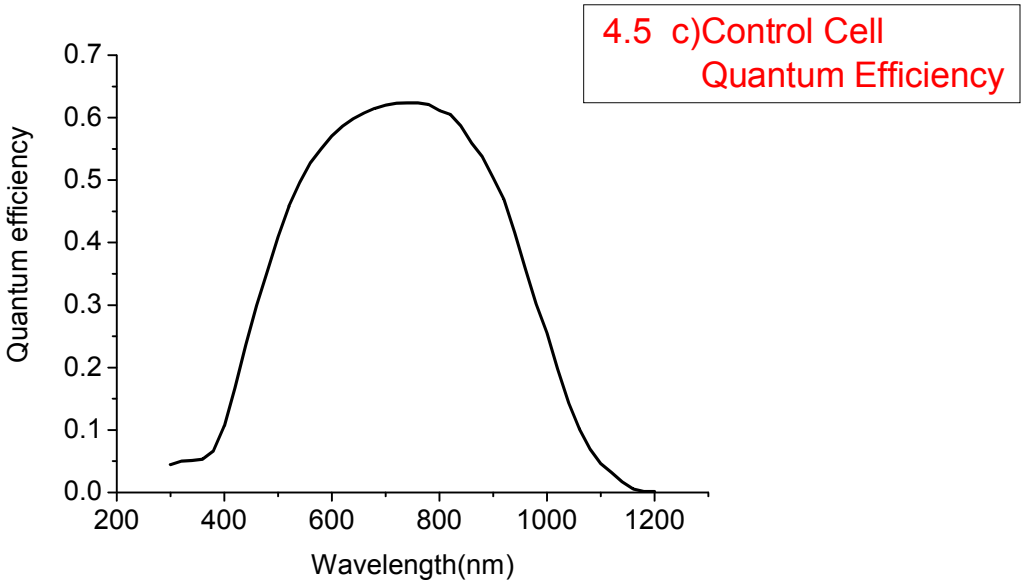
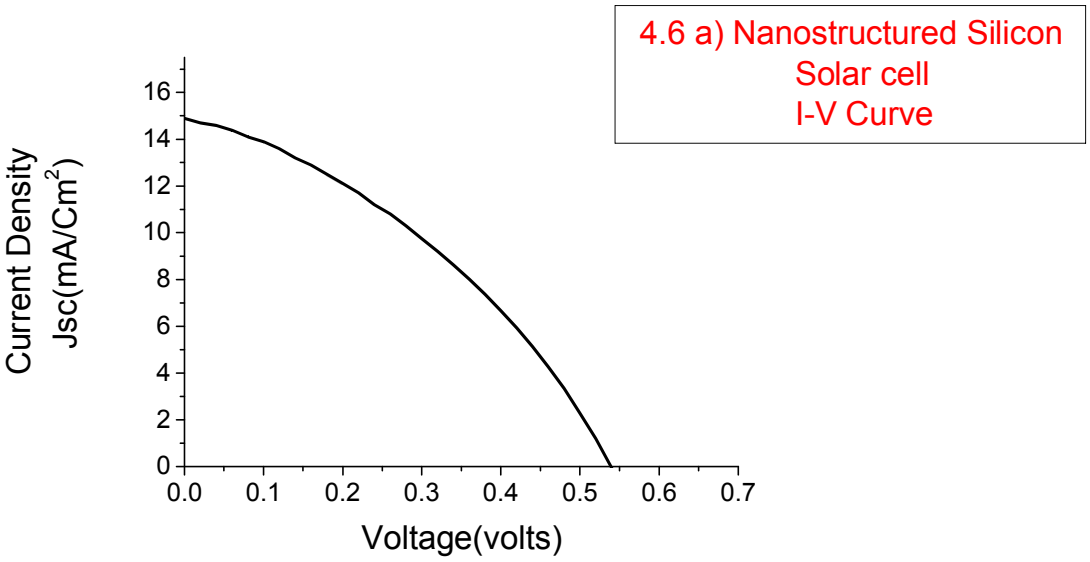


Figure: 4.5 *a) I-V curve of control cell*

b) Spectral response of control cell

c) Quantum efficiency (QE) of control cell



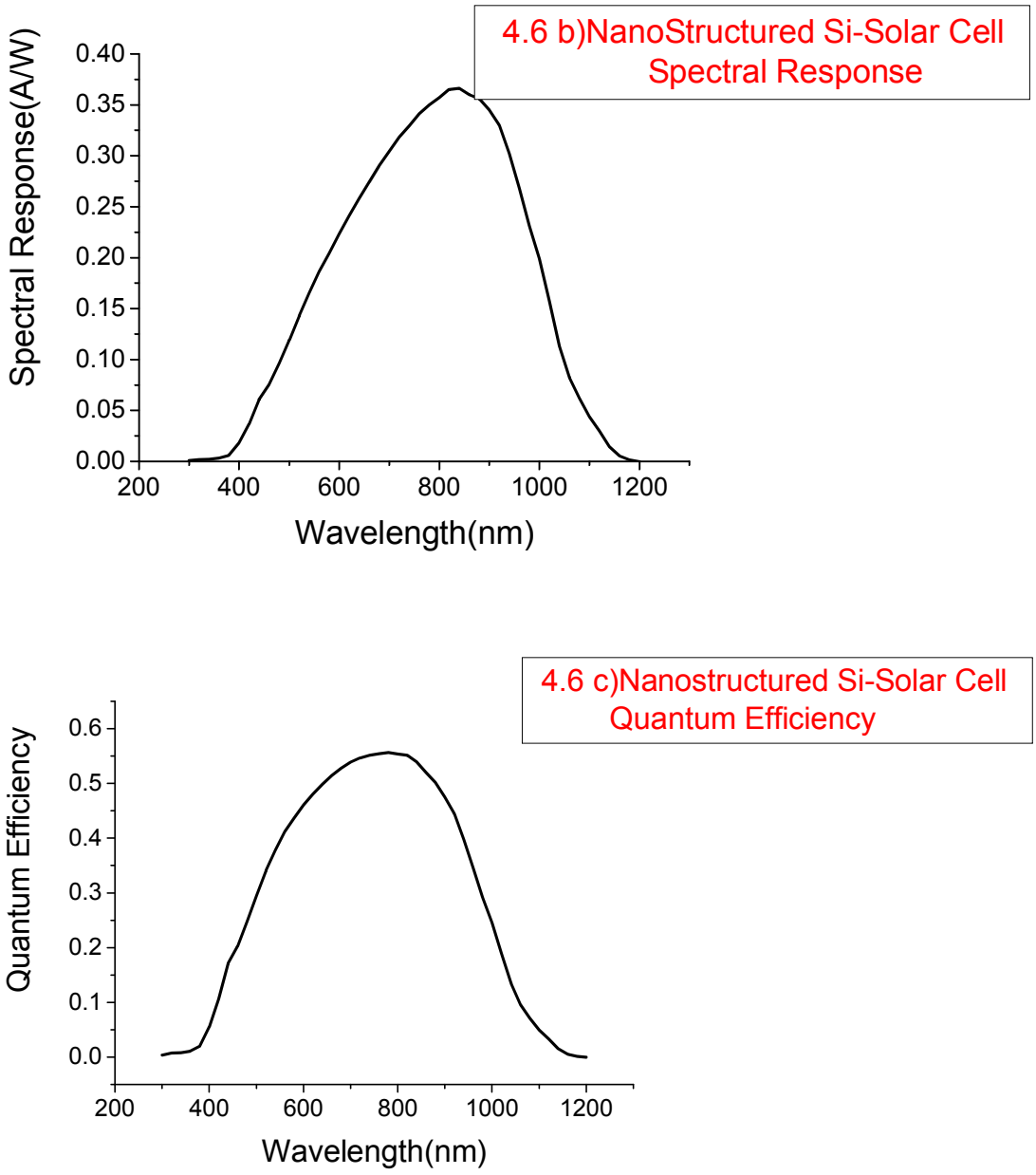


Figure: 4.6 *a) I-V curve of Nanostructured Si-Solar Cell*

b) Spectral response of Nanostructured Si-Solar Cell

c) Quantum efficiency of Nanostructured Si-Solar Cell

Parameters	***Control cell***	***Nanostructured Si-solar Cell***
J_{sc}	*18.49163 (mA/cm^2)*	*14.85226 (mA/cm^2)*
V_{oc}	*0.546439 (V)*	*0.538992 (V)*
Maximum Power	*7.001319 (mW)*	*2.946335 (mW)*
Max.Power Voltage	*0.440000 (V)*	*0.320000 (V)*
Max.Power Current	*15.91208 (mA)*	*9.207299 (mA)*
Fill Factor	*0.692887*	*0.36805*
Conversion efficiency	*7.001319 (%)*	*2.946335 (%)*
Series Resistance	*1.1465114 (ohm)*	*3.5384410 (ohm)*
Shunt Resistance	*1125.826424 (ohm)*	*41.2296954 (ohm)*

Table 4.2 *List of parameters of Control cell and Nanostructured Si-Solar cell*

From the table 4.2, it can be concluded that the performance of the silicon nanowires based solar cells is very poor as compared to that of the planar reference solar cell. This is in contrast to expected improvement in the performance due to increased absorption of light in the silicon nanowires array. The main reasons for the poor cell characteristics could be due to increased surface area causing to enhanced recombination of the generated minority carriers, which also result in to lowering of the open circuit voltage,. Also, poor quality metal contacts due to rough and fragile surface cause high series resistance and possibility of cross connection i.e. shorting of junction which is reflected in the very low shunt resistance value of the nanowires based solar cells as shown in table 2. Hence the nanowires based solar cells fill factor of the As a result the fill factor value is very low and conversion efficiency of only ~ 3% could be achieved in nanowires based solar cells as compared to the over 7% of reference planar cell. However, these are the preliminary results under non-optimal processing conditions. In principle, silicon nanowires prepared by electro-less wet chemical etching of silicon wafers i.e. via top down approach in aqueous HF solution containing Ag_2O have potential to be implemented in silicon solar cells but it requires a lot of efforts for the optimization of parameters write from growth of nanowires, their length, diameter, density, diffusion condition i.e. emitter

quality suitable for nanowire structures, metal contact to have as good quality as that on planar cells etc. to fully utilize the potential of silicon nanowires array in photovoltaics.

Chapter 5 :Conclusion

5.1 Conclusion

Silicon nanowires array have been produced using the electroless chemical etching of Silicon under Ag_2O-HF solution and these SiNWs have beeen incorporated in silicon nanostructured solar cell.From the literature, it is clear that silicon nanowires have high optical absorbance,which is useful trait for any photovolatic material as power dervied from these are comes from absorbed light.

Silicon nanowires were observed to have photoconductive characteristics when left in their undoped state and when coated with p-type or n-type layer. Hence when p-type silicon nanowire is diffused with n-type material, this junction will results in enchanced photovoltaic response. However, device formed from silicon nanowire in this project are low on efficiency but have demonstrable photovoltaic charcteristics. The problem behind this low efficiency is the non firm contact of silver (Ag) with the silicon nanowire due to the large surface area of silicon nanowires.This problem can be eradicated by selectively growing the SiNWs on the silicon.

Hence, a prototype silicon nanowire based photovoltaic device was produced by silicon nanowires (SiNWs). This device, although of low efficiency, had a demonstrable photocurrent. This indicates that silicon nanostructured solar cells can be produced that incorporate silicon nanowires. With optimisation, the device would be expected to have higher efficiency and demonstrate the advantages of using silicon nanowires. These advantages include a high absorbance of light, improved resistance to photodegradation due to the crystalline content and the ease and low cost of manufacturing.

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