A 3-Tap FIR Filter with Cascaded Distributed Amplifiers For Equalization Up to 20 Gb/s

A Dissertation

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by

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Certificate

*It is certified that, Anushri Kocher, Roll No. 12264, student of Master of Engineering, Electronics & Communication, Department of Electronics & Communication Engineering, Delhi College of Engineering, has submitted the dissertation entitled "***A 3-Tap FIR filter with Cascaded Distributed Tap Amplifiers For Equalization up to 20 Gb/s***" under my guidance towards partial fulfillment of the requirements for the award of the degree of Master of Engineering (Electronics & Communication).*

This dissertation is a bonafide record of project work carried out by her under my guidance and supervision. Her work is found to be excellent and her discipline impeccable during the course of the project.

I wish her success in all her endeavors.

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Abstract

The goal of this project is to design a 3 tap finite impulse response (FIR) programmable analog filter. The filter is intended for dispersion compensation. First, we have designed one adaptive equalizer using a 3 tap FIR filter, using ADS software of Agilent technologies. Then we have proposed a novel filter topology where we have replaced each tap gain with a distributed amplifiers to make it programmable. The same lumped LC ladders that provide the tap delays also serve as artificial transmission lines for the distributed tap amplifiers.

In this work, we also discuss the design of distributed amplifier MMICs for frequency range of 0.5- 20 GHz. Finally, we design an equalizer with FIR filters having programmable tap gain; it is done by replacing the each tap of FIR filter with distributed amplifiers. They can be used as a linear equalizer or as a part of decision feedback amplifiers.

In this project, the designed distributed amplified is basically a **Traveling Wave Amplifier**. It is commonly used as a general purpose wideband power stage in communication systems, microwave instrumentation, and optical systems. Ideally it is suited for broadband applications that require a flat gain response and excellent port matches over 2-50 GHZ frequency range. Dynamic gain control and low frequency extension capabilities are designed into these devices.

All circuits in this project have been designed using ADS (Advanced Design System) software of Agilent technologies. Schematics of various circuits and also their output results are included.

Acknowledgement

Any accomplishment requires the efforts of many people and this work is no exception. I appreciate the contribution and support, which various individuals have provided for the successful completion of this dissertation. It may not be possible to mention all by name but the following were singled out for their exceptional help.

My primary thanks goes to my project guide Professor Asok Bhattacharya, Professor & Head, Department of Electronics and communication Engineering, Delhi college of Engineering, who provided me an opportunity to work under his guidance. His scholastic guidance and sagacious suggestions helped me to complete the project in this advanced field. His immense generosity and affection bestowed on me goes beyond his formal obligations as guide.

I would like to thank whole Agilent Technologies team, for perpetual encouragement, generous help and inspiring guidance.My sincere thanks to Mrs. Deepthy Chauhan, Operating Manager (Quality Assurance Team) EMG-EESOF group, Agilent Technologies, for her initial help that eventually led to this project.

Finally, I thank God for guiding me and taking care of me all the time. My life is so blessed because of Him. I am highly obliged and would require your support in future pursuits.

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Chapter 1

Introduction

1.1 Motivation

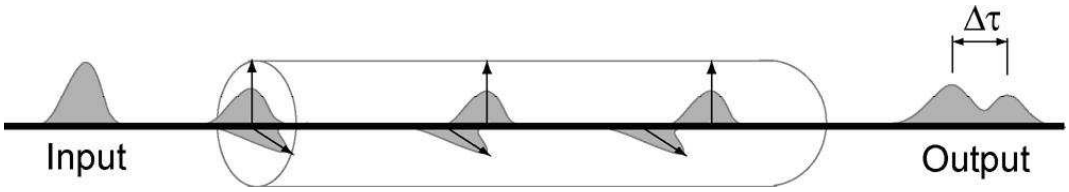
In this project, we have used Finite Impulse Response (FIR) filter with programmable tap gains for equalization purpose. For this purpose, we have replaced taps of FIR filter with distributed amplifiers, so that the tap gain of FIR filter becomes programmable.

Equalization is done basically in digital communication systems to reduce inter symbol interference (ISI). Many digital communication systems are subjected to ISI and can be characterized by a FIR filter with additive white Gaussian noise source. In our schematic of equalizer we have also modelled ISI by a FIR filter with a source of white Gaussian noise.

Finite Impulse Response filters with programmable tap gains are essential building blocks in many communication integrated circuits. They are used on their own as a linear equalizer or as a part of decision feedback equalizers.

The communication channel is a convolution of transmitter filter, propagating medium, and the receiver filter. Therefore, it can be modelled as FIR filter.

At receiver, ISI must be compensated in order to reconstruct the transmitted symbols. This is referred as channel equalization.



At high data rates, an integrated circuit equalizer may be used to perform dispersion compensation. Both chromatic and polarization mode dispersion can cause ISI in Single Mode Fiber. Chromatic dispersion is the result of the wavelength dependency of the refractive index of the fiber. It can be compensated for using relatively inexpensive optical components and therefore is not considered further here. Polarization-mode dispersion (PMD) results from birefringence, a difference in refractive index experienced by light in two orthogonal polarization modes. Ellipticity of a fiber cross section due to asymmetric stresses applied during or after manufacturing cause birefringence and, hence, PMD. Electronic PMD compensation is more attractive than optical compensation because it allows greater integration with existing circuitry, leading to more compact, less expensive solutions. This is especially true for wavelength-division multiplexed systems, in which every channel needs PMD compensation. Also, because PMD fluctuates with changes in temperature and environment, PMD compensators must be able to adapt to varying channel conditions within milliseconds. Fast and accurate adaptation is more easily performed with electronic dispersion compensators.

1.2 Technical Challenges

In this project we are using distributed amplifier as a tap for programmable tap gain. One of the challenges of working with distributed amplifiers is the need to find a bias network that works over same frequency range. Conventional RF chokes typically have either too low a self-resonance frequency to work at the high end of the frequency range, or not enough

inductance to avoid loading the RF circuit at the low end of the band. Conical inductors are one possible solution but are bulky and expensive.

A problem is typically encountered when mounting and biasing this type of MMICs as a part of large hybrid system.

1.3 Organization of the report

Till now, we have briefly described the main objective of the project and the technical challenges which we have faced during completion of this project. The remainder of this report is organized as follows:

In chapter 2, we have explained about equalizer and different types of equalizers in detail. We have also discussed the basic procedure for equalizing a signal.

In chapter 3, we have completely explained about adaptive equalizer and also given various algorithms. Different types of adaptive equalizers are also described.

In chapter 4, we have presented a schematic of adaptive equalizer, which we have designed using ADS software. Also, we have presented various simulation windows. In the schematic, we have simply designed an adaptive equalizer using a 3 tap FIR filter, where tap gains are constant.

In chapter 5, we have discussed approach of equalizer with programmable tap gains. There, we have discussed distributed amplifier in detail. Various types of distributed amplifiers and their specific advantages and disadvantages are also discussed in detail. We have also designed a distributed amplifier and the schematic, layout of that distributed amplifier is shown there. We have also given simulation window related to that distributed amplifier.

Finally chapter 6 summarizes the whole test report.

Chapter 2

Equalization

2.1 What is an Equalizer?

Time dispersive channel can cause Inter Symbol Interference (ISI). For example, in a multipath scattering environment, the receiver sees delayed versions of a symbol transmission, which can interfere with other symbol transmissions. An equalizer attempts to mitigate ISI and thus improve the receiver's performance. This chapter describes the various equalizer features.

Types of Equalizer:

- Linear Equalizer
- Symbol spaced Equalizer
- Fractionally Spaced Equalizer
- Decision Feedback Equalizer
- MLSE (Maximum-Likelihood System Estimation) Equalizer: 'It uses viterbi algorithm'

Linear and decision-feedback equalizers are **adaptive equalizers** that use an adaptive algorithm when operating. There are various algorithms such as:

- Least mean square (LMS)
- Signed LMS, including these types: sign LMS, signed regressor LMS, and sign-sign LMS
- Normalized LMS
- Variable-step-size LMS
- Recursive least squares (RLS)
- Constant modulus algorithm (CMA)

We have described about adaptive equalizer in detail in next chapter.

2.2 A Brief History

Previous analog FIR filter implementations at data rates of 10 GB/s generally operate in continuous-time using a travelling wave filter (TWF) architecture. For instance, at data rates of 40-49 GB/s, programmable TWFs have been reported in InP/In- GaAs and SiGe technologies consuming several hundred milliwatt. At 10 Gb/s, TWFs have been implemented with much lower power consumption including a 7-tap (50-ps tap spacing) design in 0.18- m SiGe BiCMOS consuming 40 mW and a 4-tap equalizer with 33-ps tap spacing in 0.18- m CMOS consuming only 7.3 mW. In, a 30-Gb/s equalizer in 90-nm CMOS was presented, making use of a crossover TWF topology to extend the bandwidth of each tap in the FIR filter by a factor of two.

2.3 Basic Procedure for Equalizing a Signal

Equalizing a signal using any communication software involves these three easy steps:

1. Create an equalizer object that describes the equalizer class and the adaptive algorithm that you want to use. An equalizer object must contains information about the equalizer, such as the name of the equalizer class, the name of the adaptive algorithm, and the values of the weights.

2. Adjust properties of the equalizer object if necessary, to tailor it to your needs. For example, you can change the number of weights or the values of the weights.

3. Apply the equalizer object to the signal you want to equalize, using the equalize method of the equalizer object.

Chapter 3

Different Types of Equalizer

This section gives a basic introduction to adaptive equalizer and provides a background for analysis of adaptive equalizer.

3.1 Symbol spaced Equalizer

A symbol-spaced linear equalizer consists of a tapped delay line that stores samples from the input signal. Once per symbol period, the equalizer outputs a weighted sum of the values in the delay line and updates the weights to prepare for the next symbol period. This class of equalizer is called *symbol-spaced* because the sample rates of the input and output are equal. Below is a schematic of a symbol-spaced linear equalizer with **N** weights, where the symbol period is **T**.

3.1.1 Updating the set of weights

The algorithms for the Weight Setting and Error Calculation blocks in the schematic are determined by the adaptive algorithm chosen from the list given above. The new set of weights depends on these quantities:

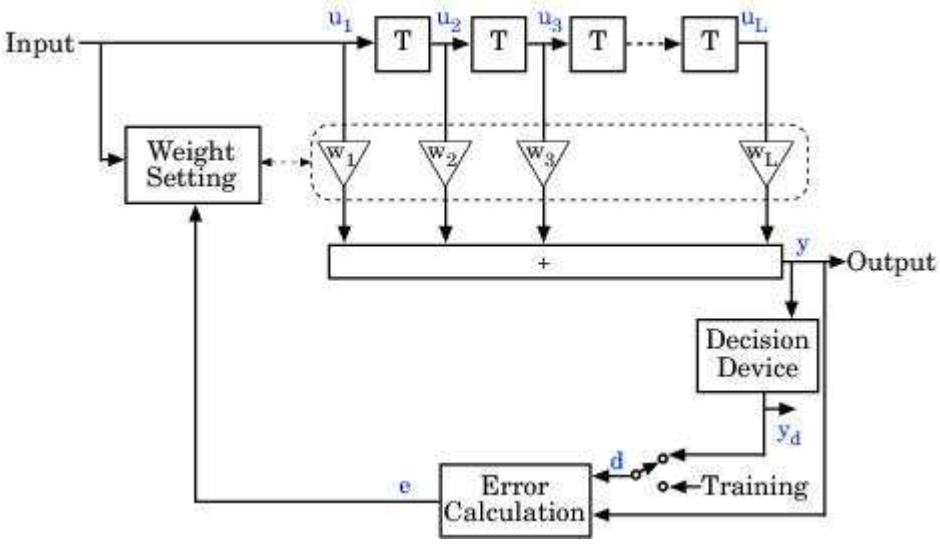


Figure 3.1: Schematic of a Symbol Spaced Equalizer

- The current set of weights
- The input signal
- The output signal

For adaptive algorithms other than CMA, a reference signal, d, whose characteristics depend on the operation mode of the equalizer

3.1.2 Reference Signal and Operation Modes

The table below briefly describes the nature of the reference signal for each of the two operation modes.

Operation Mode of Equalizer	Reference Signal
Training mode	Preset known transmitted sequence
Decision-directed mode	Detected version of the output signal, denoted by y_d in the schematic

In typical applications, the equalizer begins in training mode to gather information about the channel, and later switches to decision-directed mode.

3.1.3 Error Calculation

The error calculation operation produces a signal given by the expression below, where **R** is a constant related to the signal constellation

$$e = \begin{cases} d - y & \text{Algorithms other than CMA} \\ y\ (\mathbf{R} - |\mathbf{y}|^{\mathbf{2}}) & \text{CMA} \end{cases} \tag{3.1}$$

3.2 Fractionally Spaced Equalizer

A fractionally spaced equalizer is a linear equalizer that is similar to a symbol-spaced linear equalizer, as described in Symbol spaced equalizers. By contrast, however, a fractionally spaced equalizer receives **K** input samples before it produces one output sample and updates the weights, where K is an integer. In many applications, **K** is 2. The output sample rate is $1/\mathbf{T}$, while the input sample rate is $\mathbf{K}/\mathbf{T}$. The weight-updating occurs at the output rate, which is the slower rate.

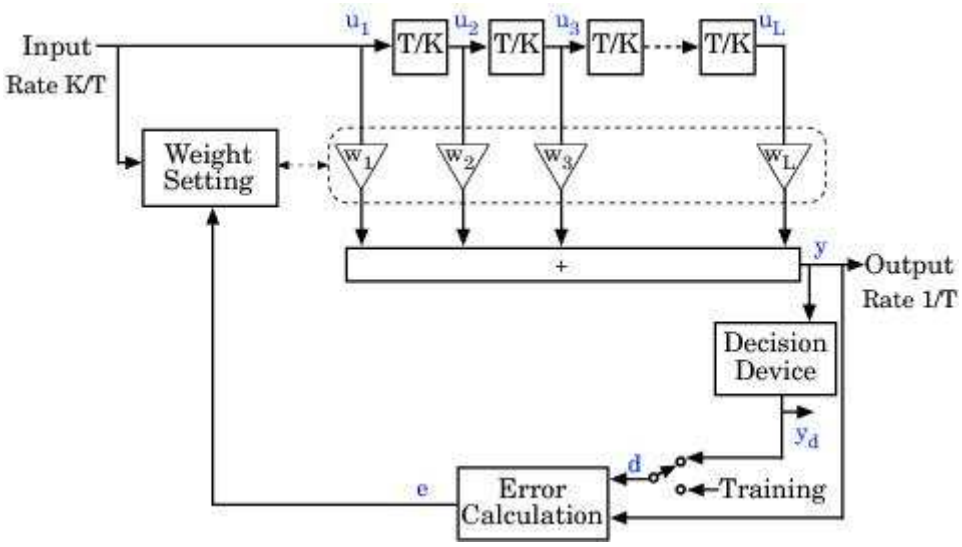


Figure 3.2: Schematic of a Fractionally Spaced Equalizer

3.3 Disadvantage of Linear Equalizer

In above discussion, we have explained two types of linear equalizer, symbol spaced equalizer and fractionally spaced equalizer. These equalizers results in ISI reduction but they also result in noise enhancement, because this we need an equalizer which an also cancel noise effects with ISI reduction. Below this we are going to describe a nonlinear equalizer, through which we can also reduce noise effects.

3.4 Decision-Feedback Equalizers

A decision-feedback equalizer is a nonlinear equalizer that contains a forward filter and a feedback filter. The forward filter is similar to the linear equalizer described in Symbol spaced equalizers, while the feedback filter contains a tapped delay line whose inputs are the decisions made on the equalized signal. The purpose of a DFE is to cancel intersymbol interference while minimizing noise enhancement. By contrast, noise enhancement is a typical

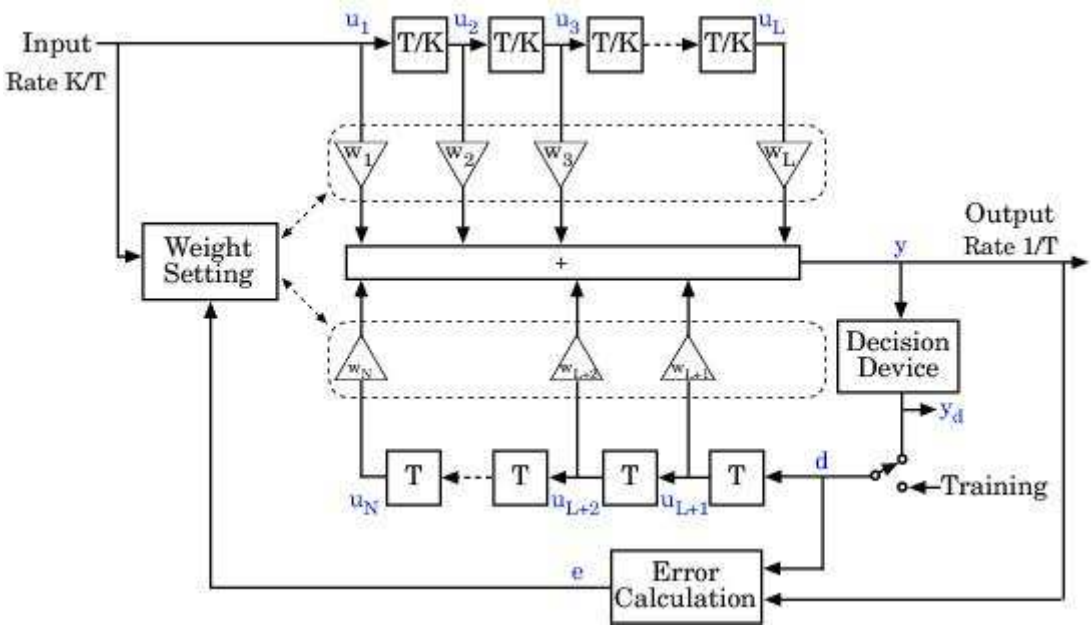


Figure 3.3: Schematic of a Decision Feedback Equalizer

problem with the linear equalizers described earlier.

Below is a schematic of a fractionally spaced DFE with **L** forward weights and $\mathbf{N} - \mathbf{L}$ feedback weights. The forward filter is at the top and the feedback filter is at the bottom. If **K** is 1, the result is a symbol-spaced DFE instead of a fractionally spaced DFE.

In each symbol period, the equalizer receives **K** input samples at the forward filter, as well as one decision or training sample at the feedback filter. The equalizer then outputs a weighted sum of the values in the forward and feedback delay lines, and updates the weights to prepare for the next symbol period.

Note: The algorithm foe weight setting block in the schematic jointly optimizes the forward and feedback weights. Joint optimization is especially important for RLS adaptive algorithm.

3.5 Choosing an Adaptive Algorithm

Configuring an equalizer involves choosing an adaptive algorithm and indicating your choice when creating an equalizer object. Although the best choice of adaptive algorithm might depend on your individual situation, here are some generalizations that might influence your choice:

- The LMS algorithm executes quickly but converges slowly, and its complexity grows linearly with the number of weights.
- The RLS algorithm converges quickly, but its complexity grows with the square of the number of weights, roughly speaking. This algorithm can also be unstable when the number of weights is large.
- The various types of signed LMS algorithms simplify hardware implementation.
- The normalized LMS and variable-step-size LMS algorithms are more robust to variability of the input signal's statistics (such as power).
- The constant modulus algorithm is useful when no training signal is available, and works best for constant modulus modulations such as PSK.
- However, if CMA has no additional side information, it can introduce phase ambiguity. For example, CMA might find weights that produce a perfect QPSK constellation but might introduce a phase rotation of 90, 180, or 270 degrees. Alternatively, differential modulation can be used to avoid phase ambiguity.

Chapter 4

Adaptive Equalizer

This section describes how to equalize a signal by using the equalize function to apply an adaptive equalizer object to the signal. The equalize function also updates the equalizer.

4.1 Equalizing Using a Training Sequence

In typical applications, an equalizer begins by using a known sequence of transmitted symbols when adapting the equalizer weights. The known sequence, called a training sequence, enables the equalizer to gather information about the channel characteristics. After the equalizer finishes processing the training sequence, it adapts the equalizer weights in decision-directed mode using a detected version of the output signal. To use a training sequence when invoking the equalize function, include the symbols of the training sequence as an input vector. NOTE: As an exception, CMA equalizers do not use a training sequence. If an equalizer object is based on CMA, you should not include a training sequence as an input vector.

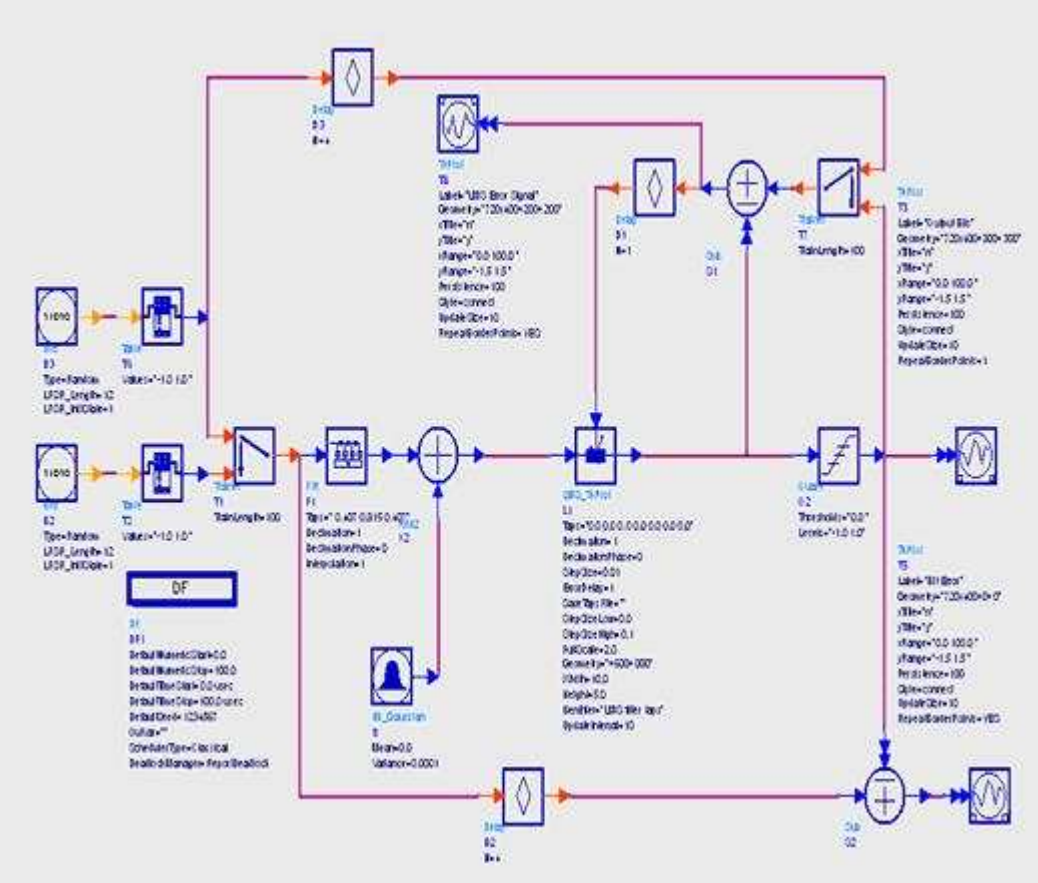


Figure 4.1: SCHEMATIC

4.2 Schematic of adaptive equalizer

I have designed equalizer circuit sing ADS (Advanced design system) software. In below figure I am presenting the schematic of adaptive equalizer using ADS software.

In the above schematic, I have used following components:

- Binary random bits output
- Indexed look up table output
- Initial sample trainer

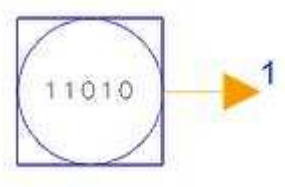


Figure 4.2: Symbol of Binary Random Bit Generator

- Delay component
- FIR Filter
- IID Gaussian distributed noise output
- Interactive LMS adaptive filter
- Quantizer

Now I am going to explain each component used in above schematic and also their description.

4.2.1 Binary Random Bits Output

Pin Outputs

Pin	Name	Description	Signal Type
1	output	output bit stream	int

Parameters:

Name	Description	Default	Symbol	Unit	Type	Range
Type	type of bit sequence, random or pseudo random: Random, Prbs	Random			Enum	
Prob Of Zero	probability of bit value being zero (used when Type = Random)	0.5			real	[0, 1]
LFSR Length	Linear Feedback Shift Register length (used when Type = Prbs)	12	L		int	[2, 31]
LFSR Initial State	Linear Feedback Shift Register initial state (used when Type = Prbs)	1			int	$[1, 2^{\mathbf{L-1}}]$

Bits generated are random or pseudo random binary bit sequences. When type = random, Bits generated is a random output binary sequence for which the probability of each bit being zero is equal to probability of zero.
If P (0) ¡ 0, it is considered as 0
If P (0) ¿ 1, it is considered as 1

When Type = Random,

(The LFSR Length and LFSR Initial State parameters are ignored in this mode.) The random bit sequence is generated by making use of the random number generator. Therefore the bit pattern will be different for each instance of bits. Therefore, the bit Pattern will be different for each instance of the Bits

The output bit sequence is also dependent on the value of the Default Seed parameter in the data flow controller (DF), which provides the initial seed for the random number generator.

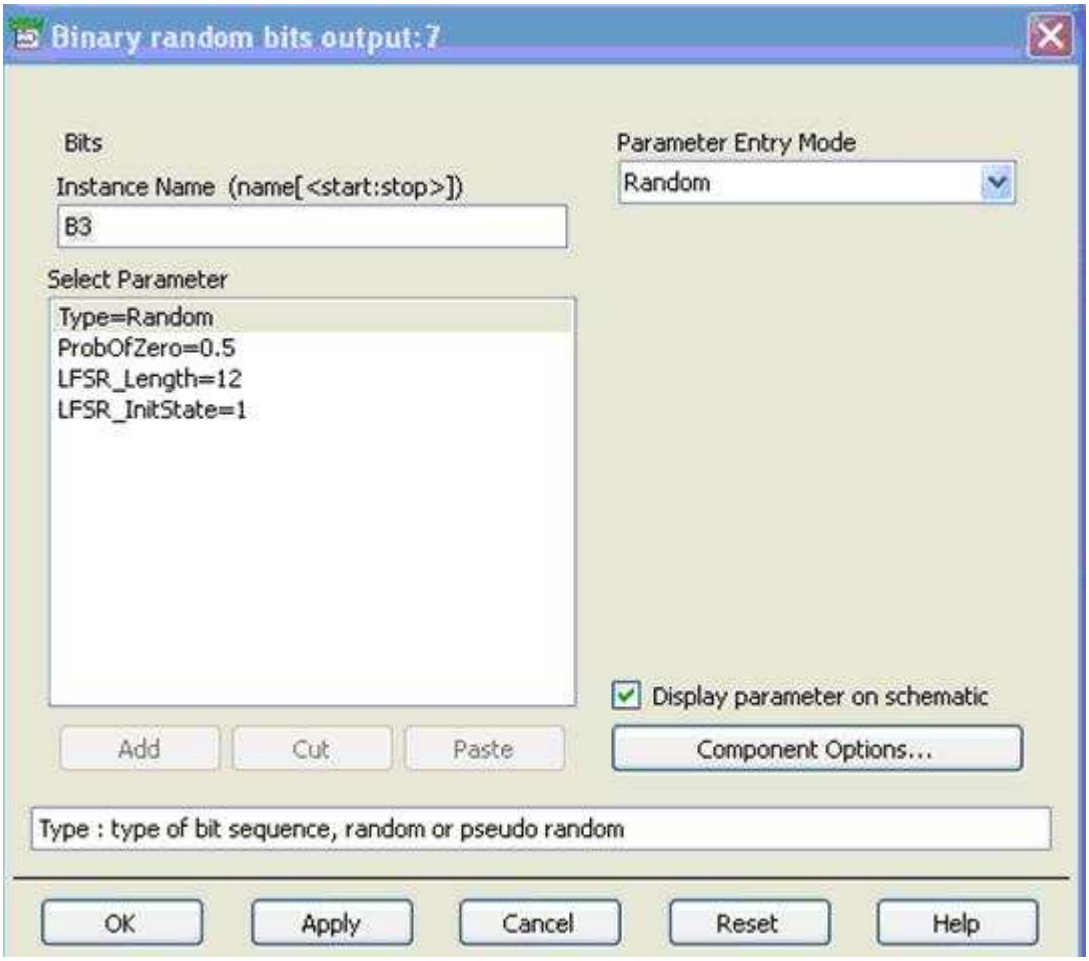


Figure 4.3: Screen-shot of Binary Random Bits Output

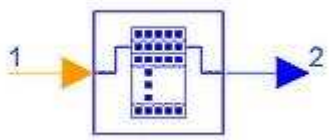


Figure 4.4: Symbol of Indexed Look Up Table Output

When Default Seed = 0,

The initial seed value is obtained from the system time so the output bit sequence generated for each simulation will be different even if nothing else changes on the design.

When Default Seed > 0,

The output bit sequence generated for each simulation, though statistically random, has the same initial Seed starting condition and therefore results in reproducible simulations.

4.2.2 Indexed Look Up Table Output

Parameters:

Name	Description	Default	Unit	Type	Range
Values	table of values to output	$\{-1,\ 1\}$		real array	

Pin Outs:

Pin	Name	Description	Signal Type
1	Input		int
2	Output		real

Description: Table implements a real-valued lookup table indexed by an integer-valued input. The input values must be between 0 and $\mathbf{N-1}$, inclusive, where **N** is the size

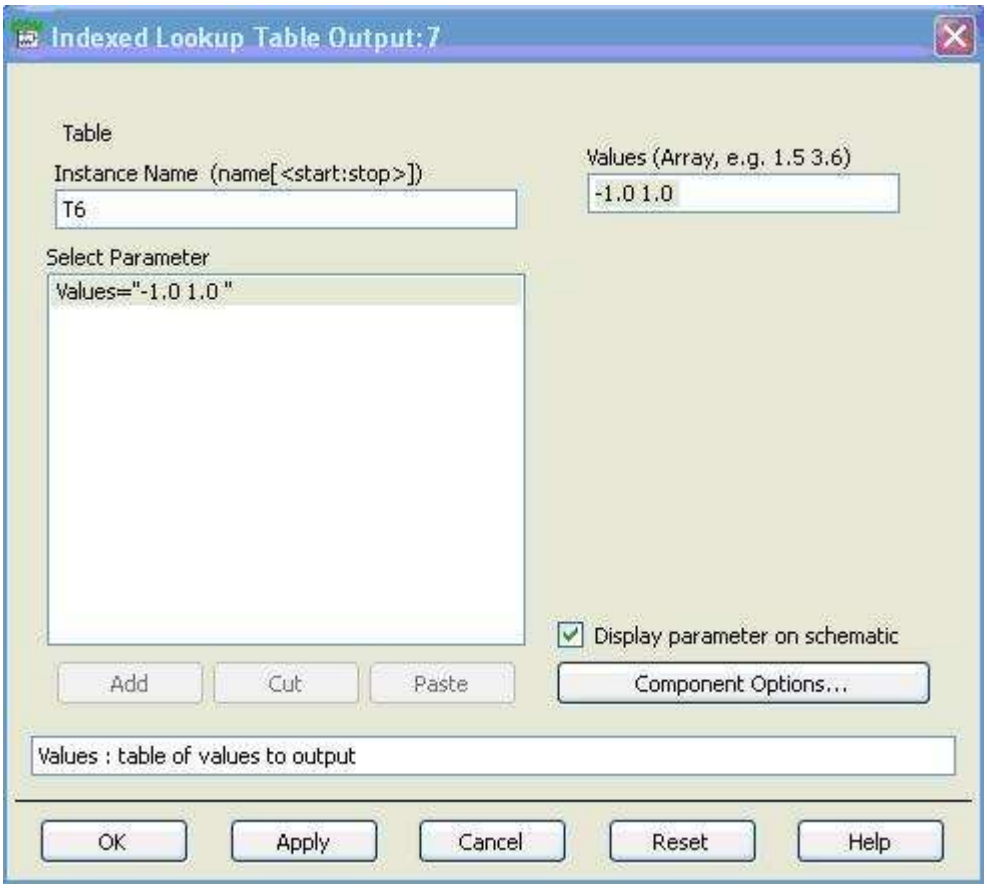


Figure 4.5: Screen-shot of Indexed Look Up Table Output

(number of elements) of the *Values* parameter. **N** must be less than 20,000. The first element of the Values parameter is indexed by an input with value 0.

The last element of the *Values* Parameter is indexed by an input with value $\mathbf{N-1}$. An error occurs if the input value is outside the interval $[0,\ \mathbf{N-1}]$.

Example: Let's assume the *Values* parameter is set to $\{-1.0, -0.333, 0.333, 1.0\}$, the 4 signal levels of a PAM-4 system. If the input signals values are 0, 0, 3, 1, 0, 1, 3, 2, 3, 1, 0, 2, and then the output signal values will be -1.0, -1.0, 1.0, -0.333, -1.0, -0.333, 1.0, 0.333, 1.0, -0.333, -1.0, 0.333. .

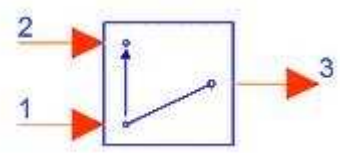


Figure 4.6: Symbol of Initial Sample Trainer

4.2.3 Initial Sample Trainer

Parameters:

Name	Description	Default	Unit	Type	Range
Train Length	number of training samples to use	100		int	

Pin Outs:

Pin	Name	Description	Signal Type
1	train	Input Pin	Any type
2	decision	Input Pin	Any type
3	output	Output Pin	Any type

Description: Trainer passes the value of the train input to the output for the first Train Length Samples, and then passes the decision input to the output. This component is designed for use with adaptive

equalizers that require a training sequence at startup, but it can be used whenever one sequence is used during a startup phase, and another sequence after that. During the startup phase, the decision inputs are discarded. After the startup phase, the train inputs are discarded.

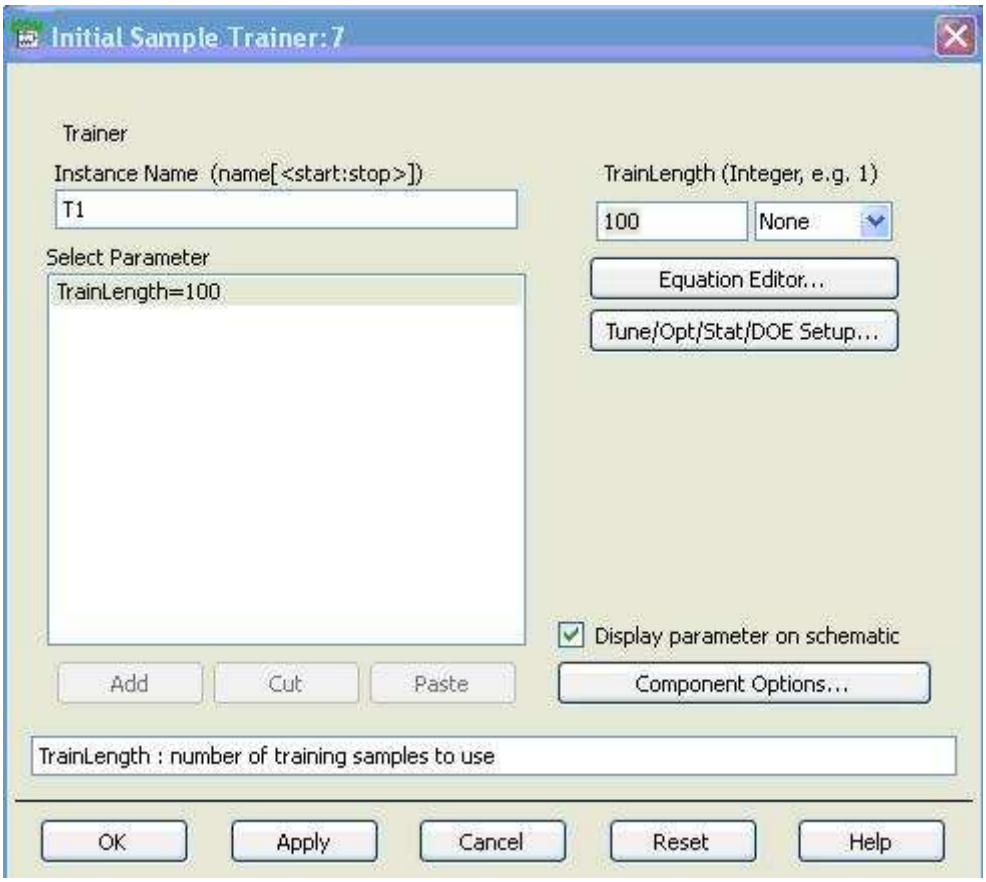


Figure 4.7: Screen-shot of Initial Sample Trainer

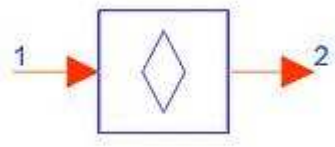


Figure 4.8: Symbol of Delay Component

4.2.4 Delay Component

Parameters:

Name	Description	Default	Type	Range
N	**N**	1	int	$[0, 8)$

Pin Outs:

Pin	Name	Description	Signal Type
1	Input	multiple	any type
2	Output	multiple	any type

Description: This component delays input tokens from output by **N** samples. The initial **N** output tokens have a null value.

4.2.5 FIR Filter

Parameters:

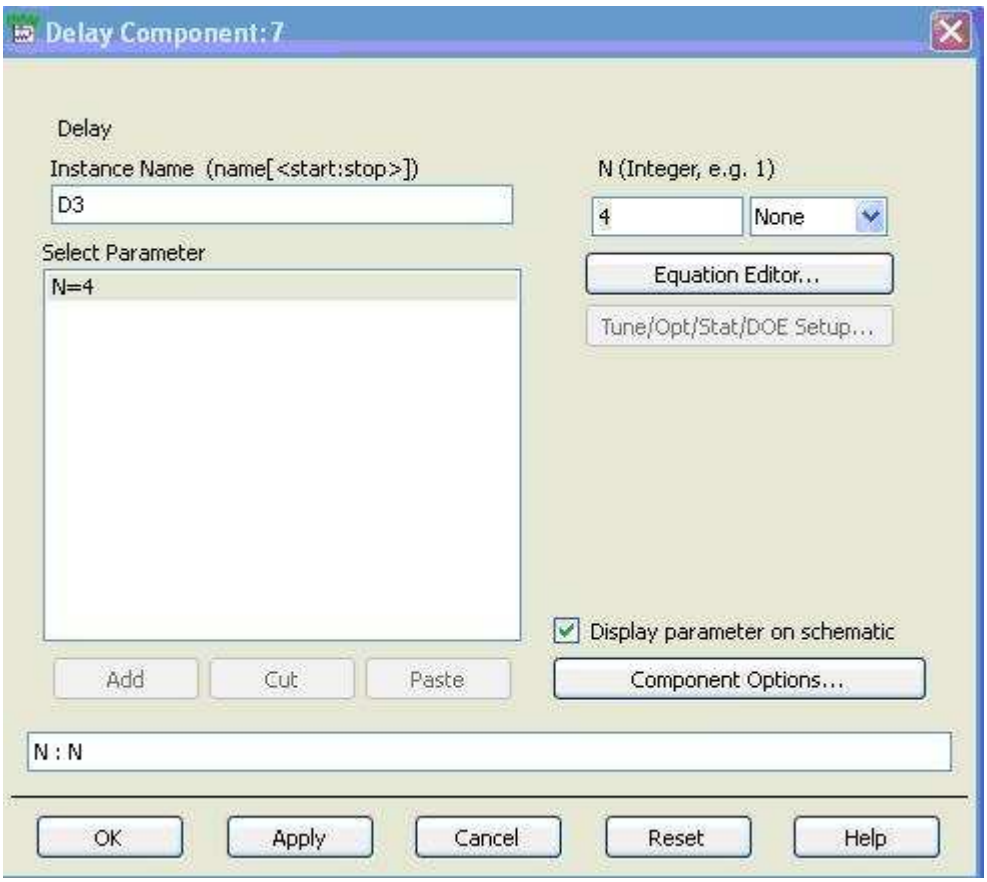


Figure 4.9: Screen-shot of Delay Component

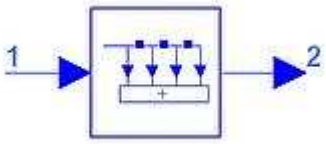


Figure 4.10: Symbol of FIR Filter

Name	Description	Default	Type	Range
Taps	filter tap values	-.040609, -.001628, .17853, .37665, .37665, .17853, -.001628, -.040609	real array real array real array real array	
Decimation	decimation ratio	1	int	$[1, 8)$
Decimation Phase	decimation phase	0	int	[0, Decimation-1]
Interpolation	interpolation ratio	1	int	$[1, 8)$

Pin Outs:

Pin	Name	Description	Signal Type
1	Signal In	Input Pin	Real
2	Signal Out	Output Pin	Real

Description: FIR implements a finite-impulse response filter with multirate capability. The default tap coefficients correspond to an eighth-order, equiripple, linear-phase, low pass filter. The cutoff frequency is approximately one-third of the Nyquist frequency.

The filter coefficients are specified by the Taps parameter. The filter coefficients may be specified directly or these may be read from a file.

This filter efficiently implements rational sample rate changes. When the Decimation ratio is = 1, the filter behaves exactly as if it were followed by a Down Sample component; similarly, when the Interpolation ratio is set, the filter behaves as if it were preceded by an Up Sample component. However, the implementation is much more efficient than it would be using Up-Sample and Down Sample. A polyphase structure is used internally, avoiding unnecessary use of memory and unnecessary multiplication by 0. Arbitrary sample-rate conversions by rational factors can be accomplished this way.

The Decimation Phase parameter is somewhat subtle. It is equivalent to the Phase parameter of the Down Sample component. When decimating, samples are conceptually discarded (although a polyphase structure does not actually compute the discarded samples).

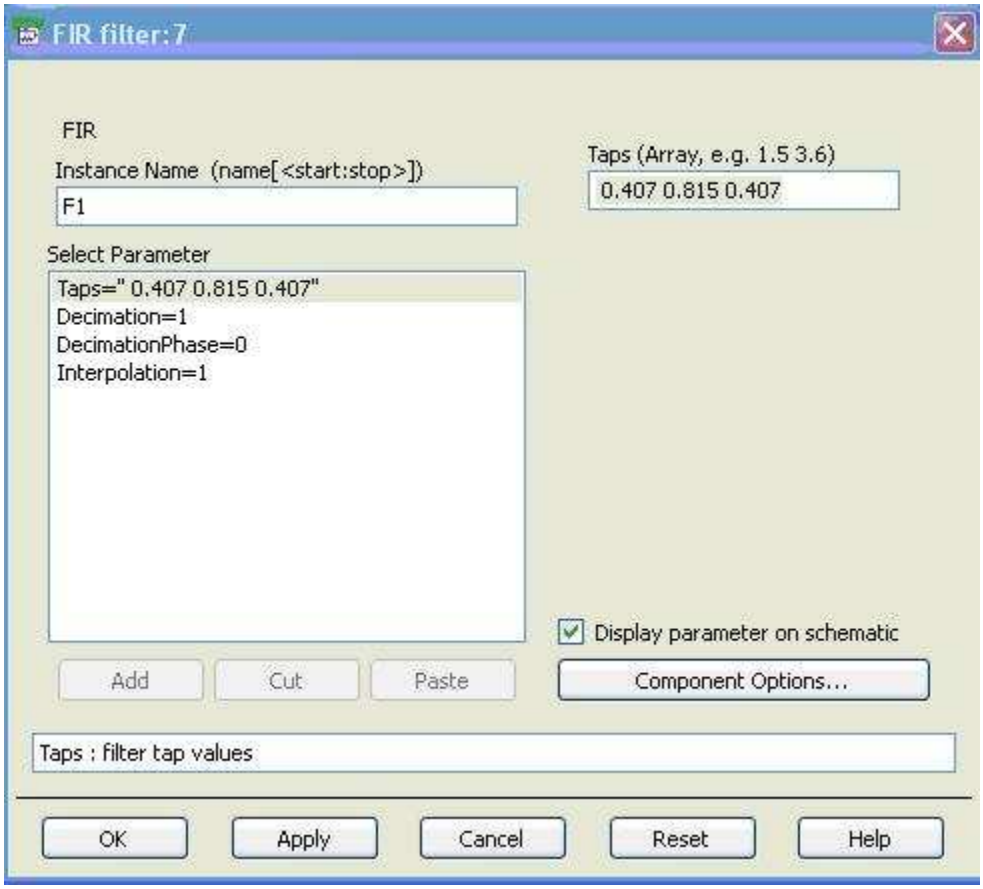


Figure 4.11: Screen-shot of FIR Filter

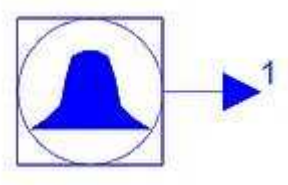


Figure 4.12: Symbol of IID Gaussian Distributed Noise Output

For example, to decimate by a factor of 3, one of every 3 outputs is selected. The Decimation Phase parameter determines which of these is selected. If Decimation Phase is 0 (default), the most recent samples are selected.When designing a multi-rate filter, avoid accidentally introducing aliasing. One may assume that the filter sample rate is the product of the Interpolation parameter and the input sample rate. Equivalently, one may use the product of the Decimation parameter and the output sample rate.

4.2.6 IID Gaussian Distributed Noise Output

Parameters:

Name	Description	Default	Type	Range
Mean	mean of distribution	0.0	Real	(-8, 8)
Variance	variance of distribution	1.0	Real	(-8, 8)

Pin Outs:

Pin	Name	Description	Signal Type
1	Output		real

Description: IID Gaussian generates an identically independently distributed white Gaussian pseudo-random process with mean (default 0) and variance (default 1) specified by the Mean and Variance parameters.

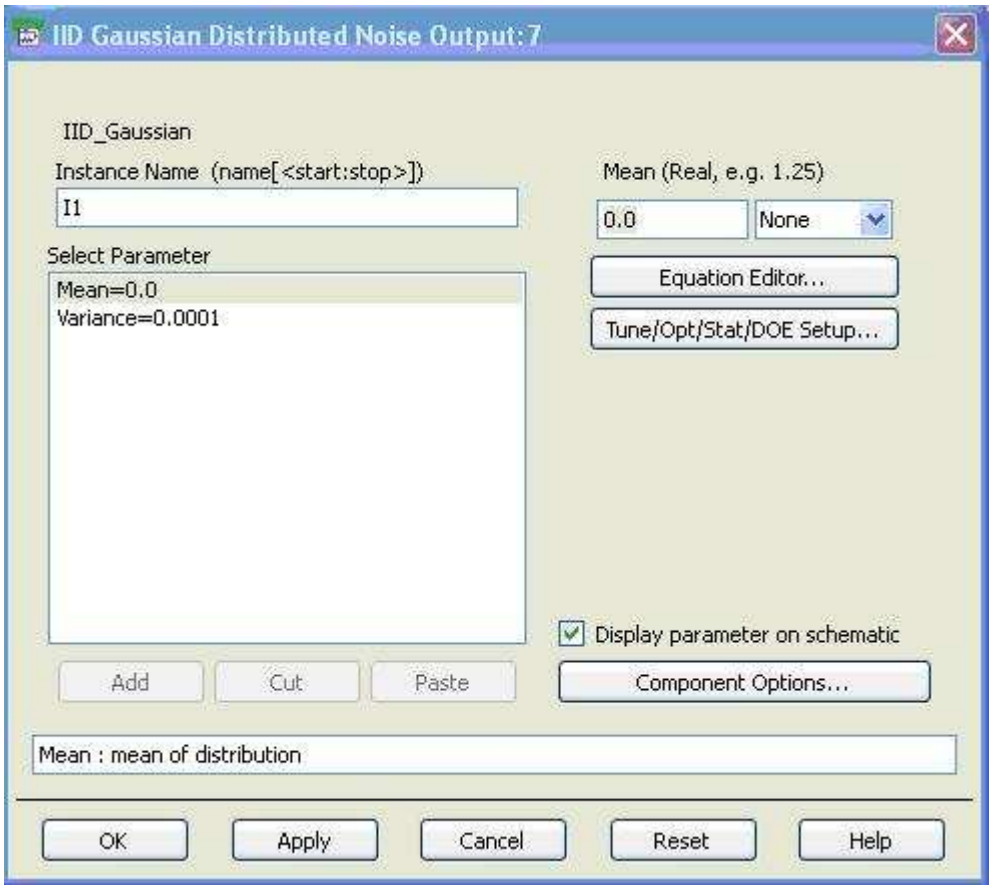


Figure 4.13: Screen-shot of IID Gaussian Distributed Noise Output

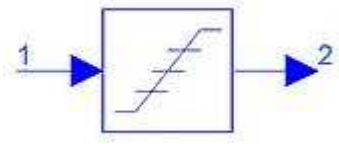


Figure 4.14: Symbol of Quantizer

The noise is random for each IID Gaussian instance. The noise is dependent on the value of the Default seed in the data flow controller (DF). When Default Seed = 0, the noise generated for each simulation is different. When Default Seed ¿ 0, the noise generated for each simulation, though random, has the same initial seed starting condition and thus results in reproducible simulations.

4.2.7 Quantizer

Parameters:

Name	Description	Default	Type	Range
Thresholds	quantization thresholds, in increasing order	0.0	real array	
Levels	Output levels. If empty use 0, 1, 2, ...	real array		

Pin Outs:

Pin	Name	Description	Signal Type
1	Input		real
2	Output		real

Description: Quant quantizes the input value to one of $\mathbf{N+1}$ possible output levels using **N** thresholds.

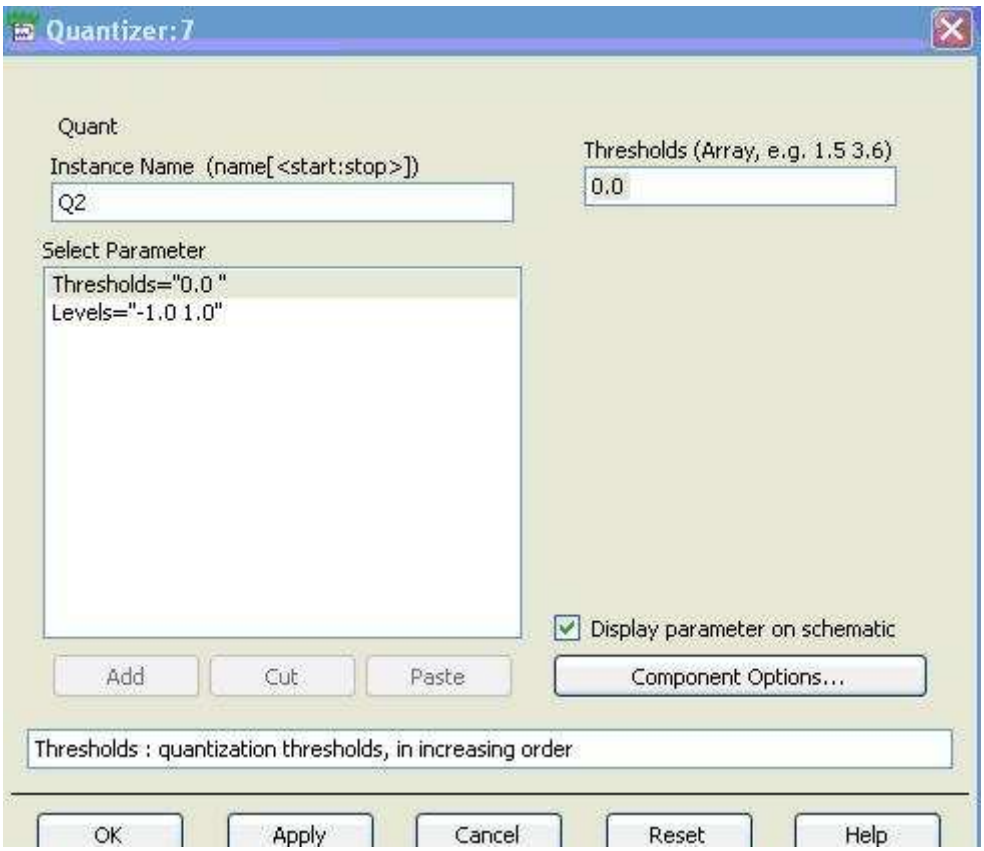


Figure 4.15: Screen-shot of Quantizer

- For input $\geq n^{\text{th}}$ threshold, but $>$ all previous thresholds, the output will be the n^{th} level.
- For input $>$ all thresholds, the output is $\mathbf{N+1}$ th level.
- For input $<$ all thresholds, the output is 0th level.

If the level is specified, there must be one more level than thresholds. The default value for level is 0, 1, 2, ..., **N**. This component takes on the order of log N steps to find the right level, whereas the linear quantizer component LinQuantIdx takes a constant amount of time. Therefore, for linear quantization, use the LinQuantIdx component. Assume that the Thresholds parameter is set to (8.1, 9.2, and 10.3) and that the Levels parameter is not set so that the default values of (0.0, 1.0, 2.0, 3.0) are used. An input of -1.5 would give an output of 0.0; an input of 8.2 would give an output of 1.0; and, an input of 15.5 would give an output of 3.0.

4.3 Results

Here I am presenting different simulation results (data display windows) opened after completion of simulation. Note that I have run all simulations on Windows XP 64 bit platform.

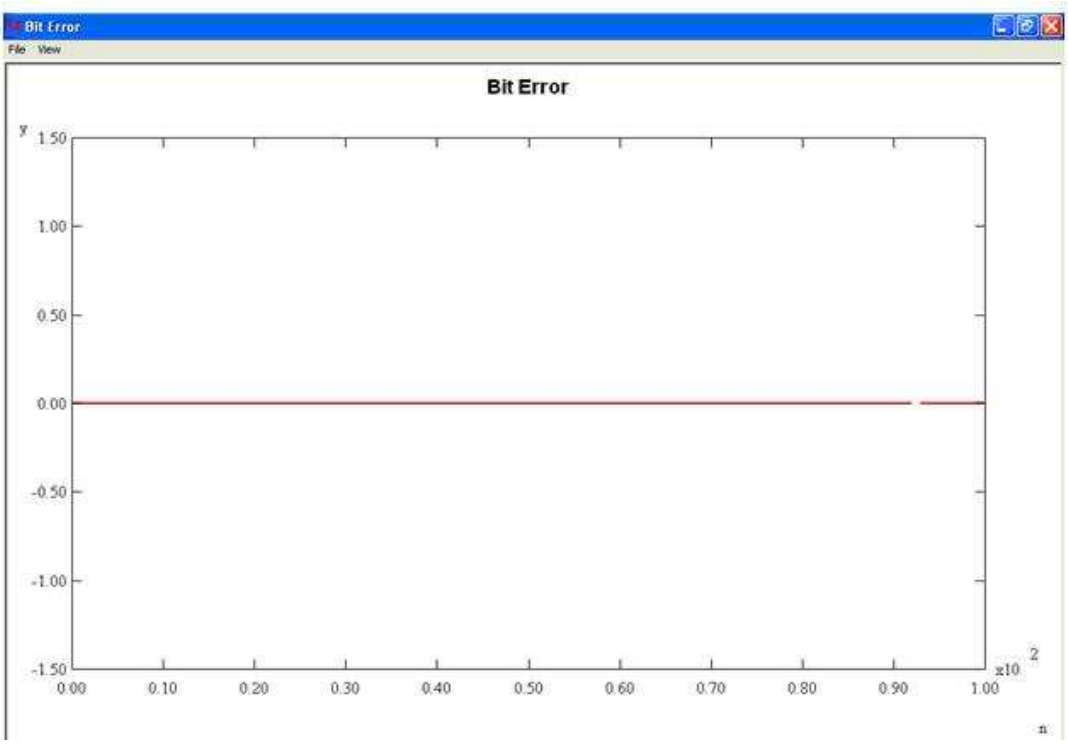


Figure 4.16: Screen-shot of Bit Error Window

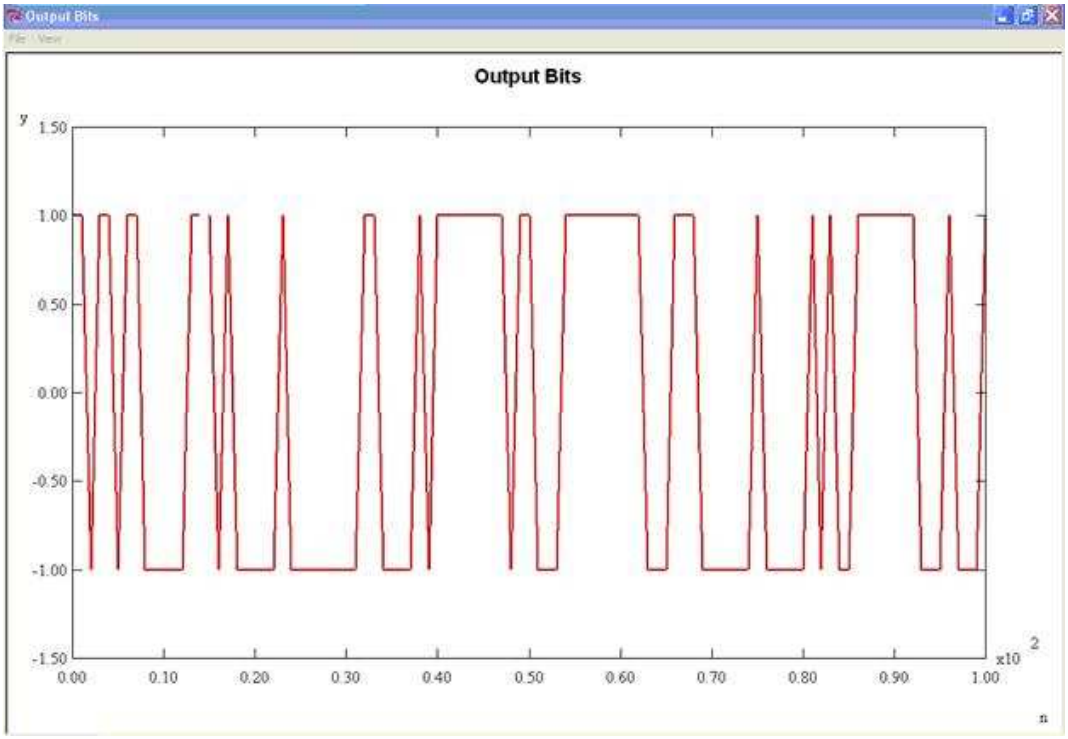


Figure 4.17: Screen-shot of Output Bits

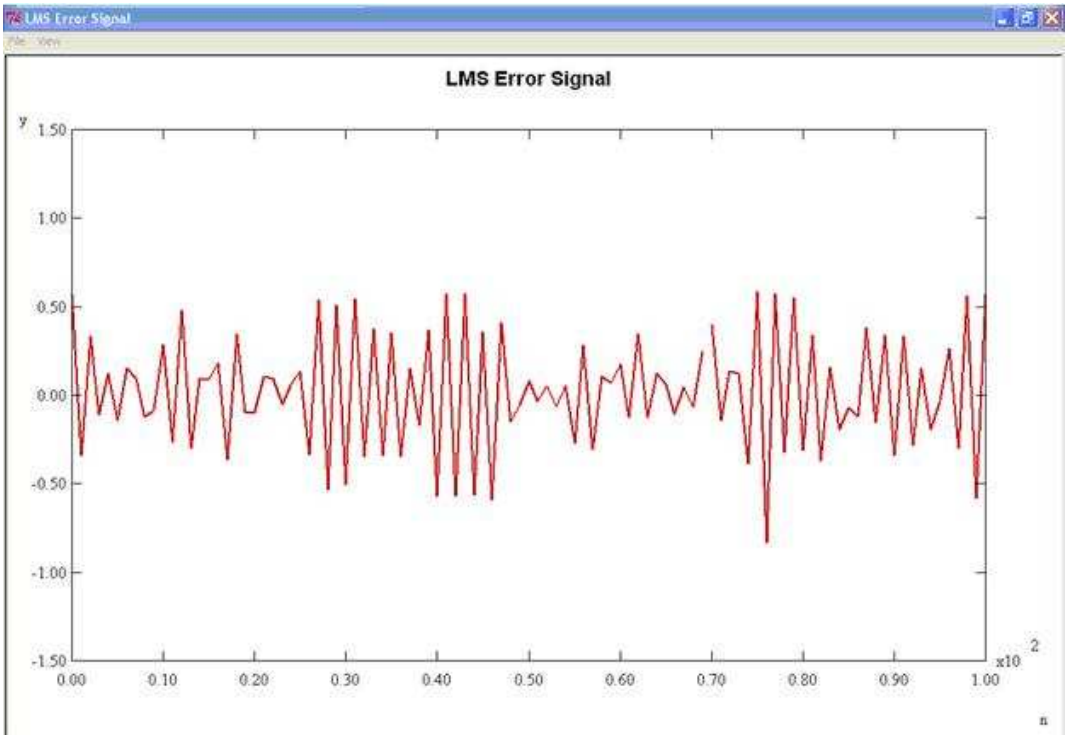


Figure 4.18: Screen-shot of LMS Error Signal

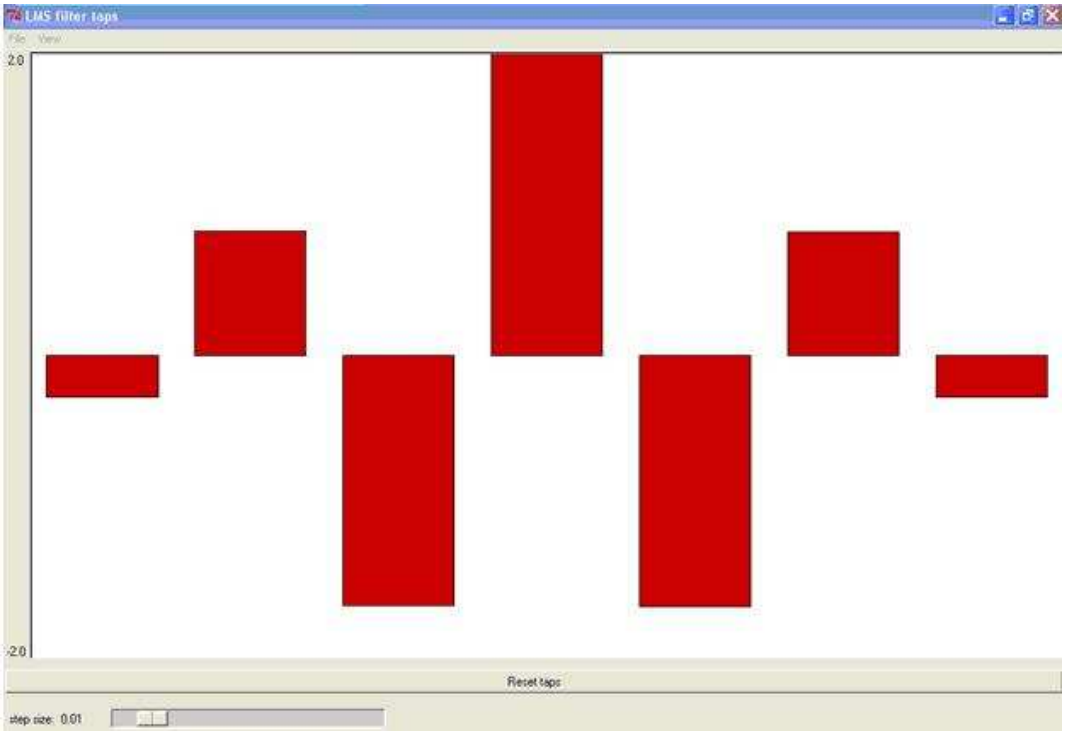


Figure 4.19: Screen-shot of Filter Taps

Chapter 5

Equalizer Using Programmable FIR Filter

5.1 Designing Programmable Equalizer

This work focuses on the programmable filter required for linear equalization in a receiver. A novel filter topology is employed, whereby each tap gain comprises a cascade of two distributed amplifiers with adjustable gain. The same lumped LC ladders that provide the tap delays also serve as artificial transmission lines for the distributed tap amplifiers.

A simple block diagram of 3-tap traveling wave filter is shown in Fig. 5.3. To create

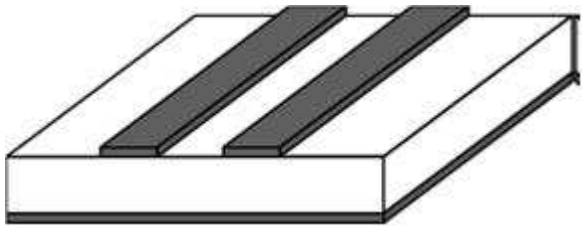


Figure 5.1: ... several mm needed to achieve required delay

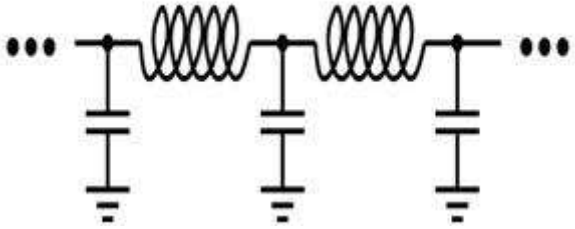


Figure 5.2: ... forms a low-pass network

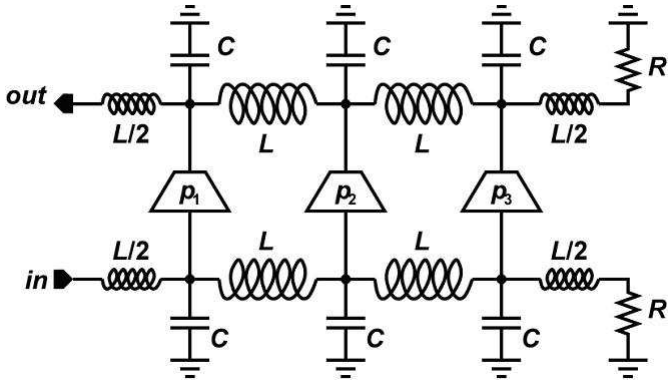


Figure 5.3: 3-Tap Traveling Wave Filter

a programmable Fir filter, we are replacing each tap of Fir filter with a cascade of two distributed amplifier. To create a distributed amplifier we are going to use FET as an active device.

5.2 Distributed Amplifier

Distributed amplifiers are circuit designs that incorporate transmission line theory into traditional amplifier design to obtain a larger gain-bandwidth product than is realizable by conventional circuits.

5.2.1 History

The design of the distributed amplifiers (DA) was first formulated by William S. Percival in 1936. In that year Percival proposed a design by which the transconductances of individual vacuum tubes could be added linearly without lumping their element capacitances at the input and output, thus arriving at a circuit that achieved a gain-bandwidth product greater than that of an individual tube. Percival's design did not gain widespread awareness however, until a publication on the subject was authored by Ginzton, Hewlett, Jasberg, and Noe in 1948. It is to this later paper that the term distributed amplifier can actually be traced. Traditionally, DA design architectures were realized using valve technology.

5.2.2 Current Technology

More recently, III-V semiconductor technologies, such as GaAs] and InP have been used. These have superior performance resulting from higher bandgaps (higher electron mobility), higher saturated electron velocity, higher breakdown voltages and higher-resistivity substrates. The latter contributes much to the availability of higher quality-factor (Q-factor or simply Q) integrated passive devices in the III-V semiconductor technologies.

To meet the marketplace demands on cost, size, and power consumption of monolithic microwave integrated circuits (MMICs), research continues in the development of mainstream digital bulk-CMOS processes for such purposes. The continuous scaling of feature sizes in current IC technologies has enabled microwave and mm-wave CMOS circuits to directly benefit from the resulting increased unity-gain frequencies of the scaled technology. This device scaling, along with the advanced process control available in today's technologies, has recently made it possible to reach an fT of 170 GHz and a maximum oscillation frequency (fmax) of 240 GHz in a 90nm CMOS process.

5.2.3 Theory of Operation

The operation of the DA can perhaps be most easily understood when explained in terms of the traveling-wave tube amplifier (TWTA). The DA consists of a pair of transmission lines with characteristic impedances of Z0 independently connecting the inputs and outputs of several active devices. An RF signal is thus supplied to the section of transmission line connected to the input of the first device. As the input signal propagates down the input line, the individual devices respond to the forward traveling input step by inducing an amplified complementary forward traveling wave on the output line. This assumes the delays of the input and output lines are made equal through selection of propagation constants and lengths of the two lines and as such the output signals from each individual device sum in phase. Terminating resistors Zg and Zd are placed to minimize destructive reflections.

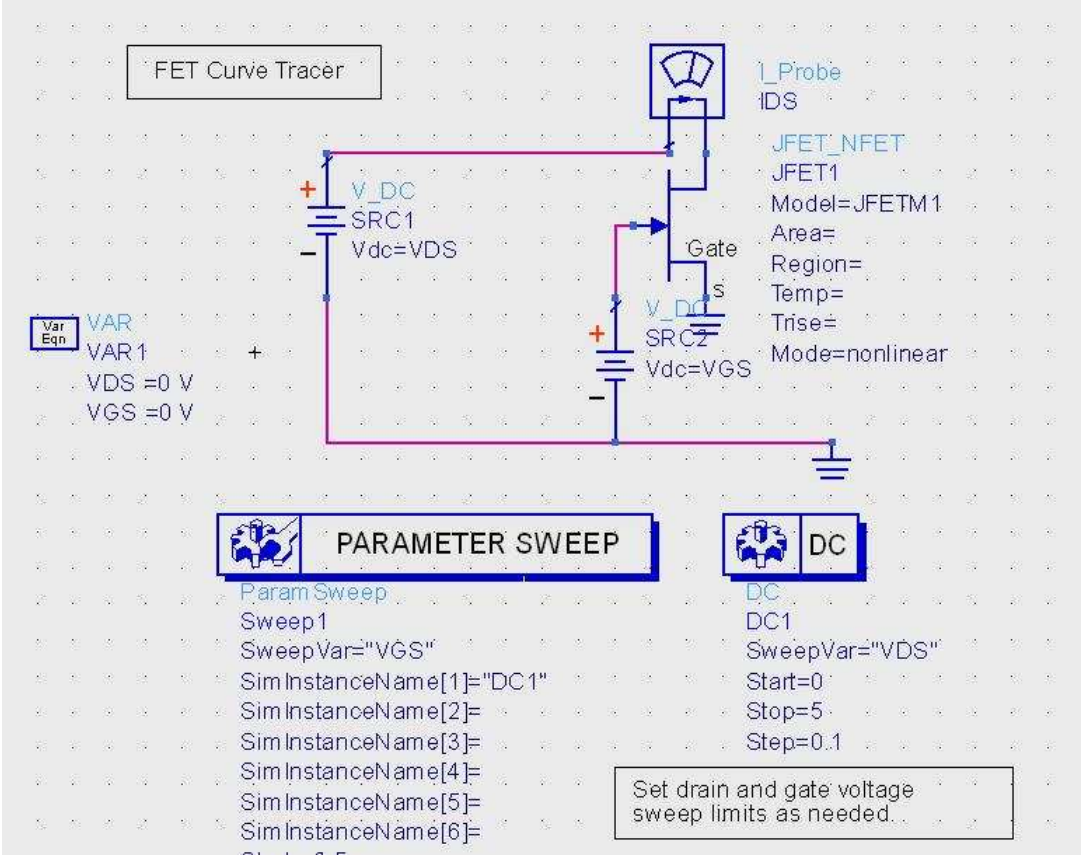
The transconductive gain of each device is gm and the output impedance seen by each transistor is half the characteristic impedance of the transmission line. So that the overall voltage gain of the DA is:

$$\mathbf{A}_v = n * g_m * \frac{Z_0}{2}, \tag{5.1}$$

where n is the number of stages.

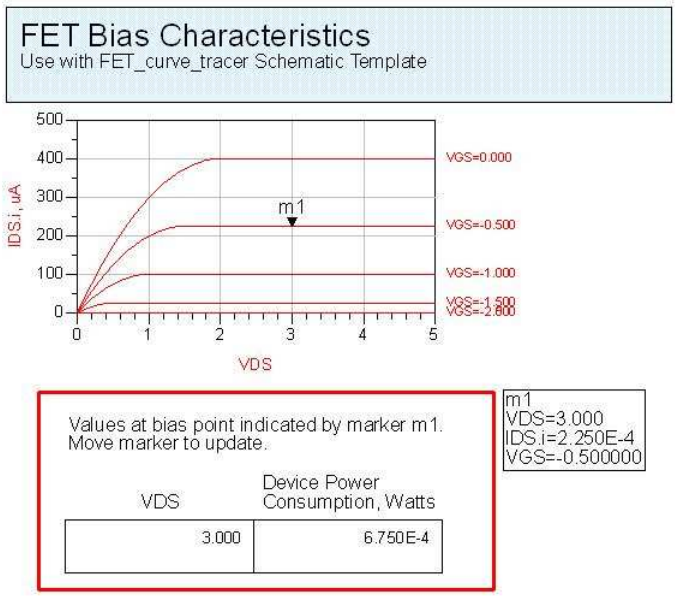
Neglecting losses, the gain demonstrates a linear dependence on the number of devices (stages). Unlike the multiplicative nature of a cascade of conventional amplifiers, the DA demonstrates an additive quality. It is this synergistic property of the DA architecture that makes it possible for it to provide gain at frequencies beyond that of the unity-gain frequency of the individual stages. In practice, the number of stages is limited by the diminishing input signal resulting from attenuation on the input line. Means of determining the optimal number of stages are discussed below. Bandwidth is typically limited by impedance mismatches brought about by frequency dependent device parasitics.

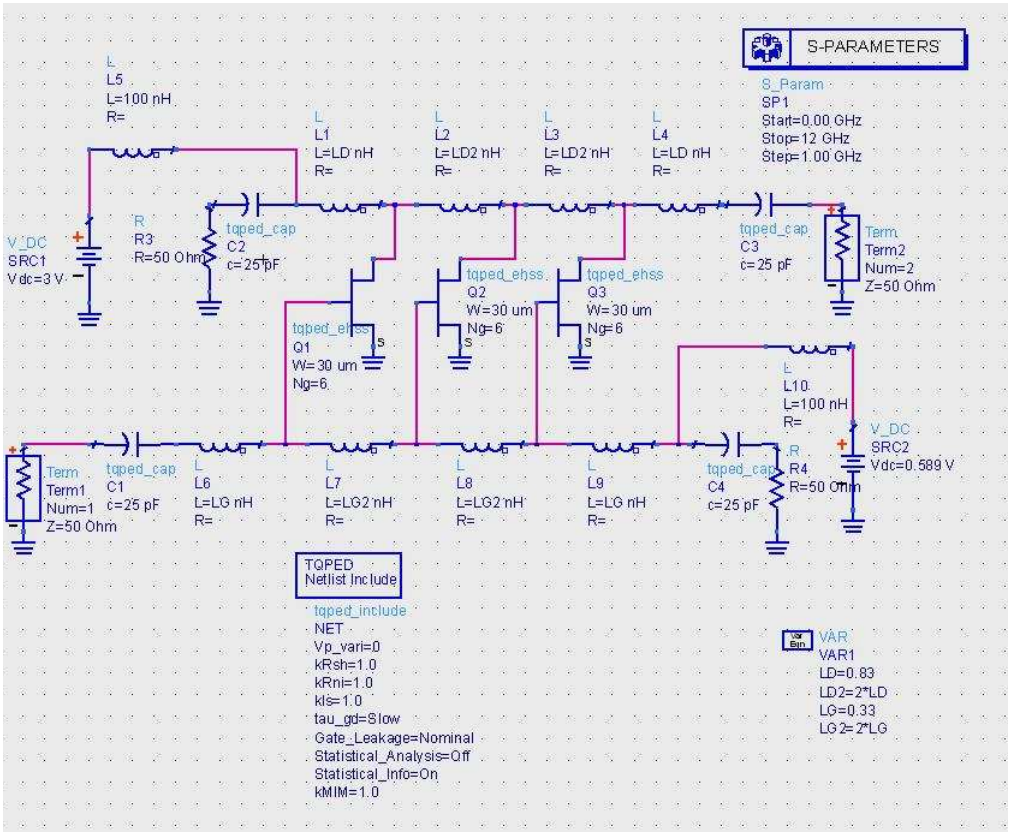
The DA architecture introduces delay in order to achieve its broadband gain characteristics. This delay is a desired feature in the design of another distributive system called



the distributed oscillator.

5.3 Design of Distributed Amplifier Using FET


FET Bias Characteristics
Use with FET_curve_tracer Schematic Template
IDS.i, uA
VDS
VGS=0.000
VGS=-0.500
VGS=-1.000
VGS=-1.500
VGS=-2.800
m1
Values at bias point indicated by marker m1.
Move marker to update.
VDS
Device Power Consumption, Watts
3.000
6.750E-4
m1
VDS=3.000
IDS.i=2.250E-4
VGS=-0.500000


S-PARAMETERS
S_Param
SP1
Start=0.00 GHz
Stop=12 GHz
Step=1.00 GHz
L5
L=100 nH
R=
L1
L=LD nH
R=
L2
L=LD2 nH
R=
L3
L=LD2 nH
R=
L4
L=LD nH
R=
V_DC
SRC1
Vdc=3 V
R3
R=50 Ohm
tqped_cap
C2
c=25 pF
tqped_ehss
Q1
W=30 um
Ng=6
tqped_ehss
Q2
W=30 um
Ng=6
tqped_ehss
Q3
W=30 um
Ng=6
tqped_cap
C3
c=25 pF
Term
Term2
Num=2
Z=50 Ohm
L
L10
L=100 nH
R=
V_DC
SRC2
Vdc=0.589 V
Term
Term1
Num=1
Z=50 Ohm
tqped_cap
C1
c=25 pF
L
L6
L=LG nH
R=
L
L7
L=LG2 nH
R=
L
L8
L=LG2 nH
R=
L
L9
L=LG nH
R=
tqped_cap
C4
c=25 pF
R
R4
R=50 Ohm
TQPED
Netlist Include
tqped_include
NET
Vp_vari=0
kRsh=1.0
kRni=1.0
kIs=1.0
tau_gd=Slow
Gate_Leakage=Nominal
Statistical_Analysis=Off
Statistical_Info=On
kMIM=1.0
VAR
VAR1
LD=0.83
LD2=2*LD
LG=0.33
LG2=2*LG

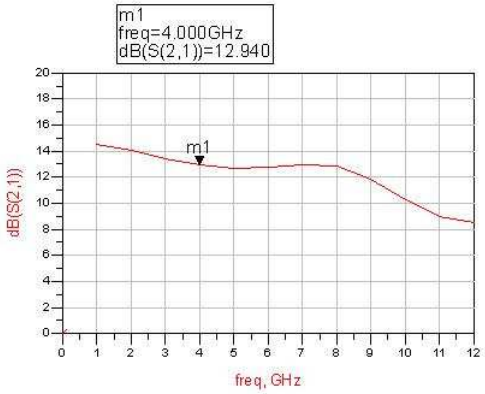


Figure 5.4: Simulation Result

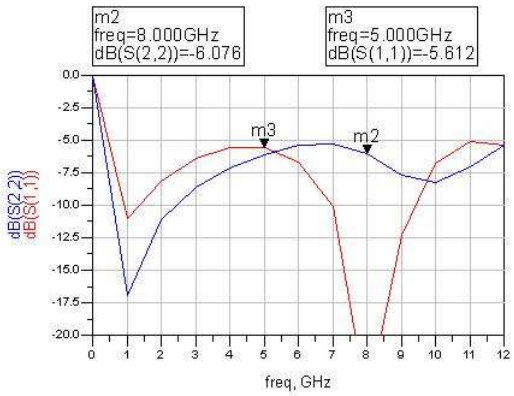


Figure 5.5: Simulation Result

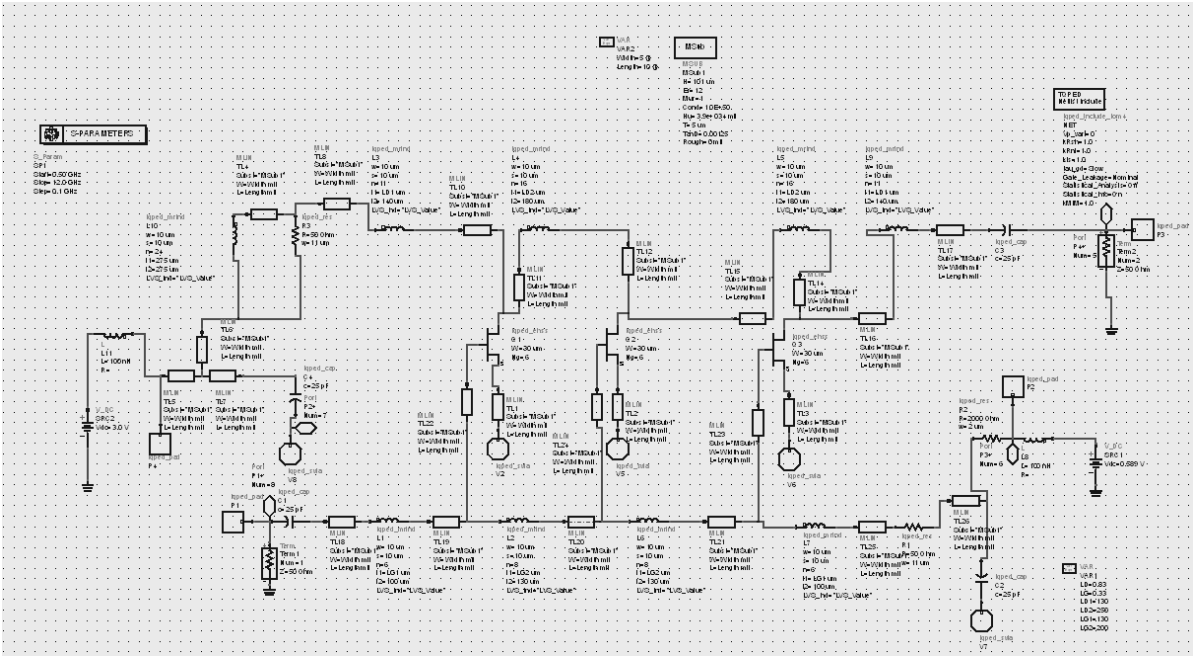


Figure 5.6: Actual Design of the Distributed Amplifier

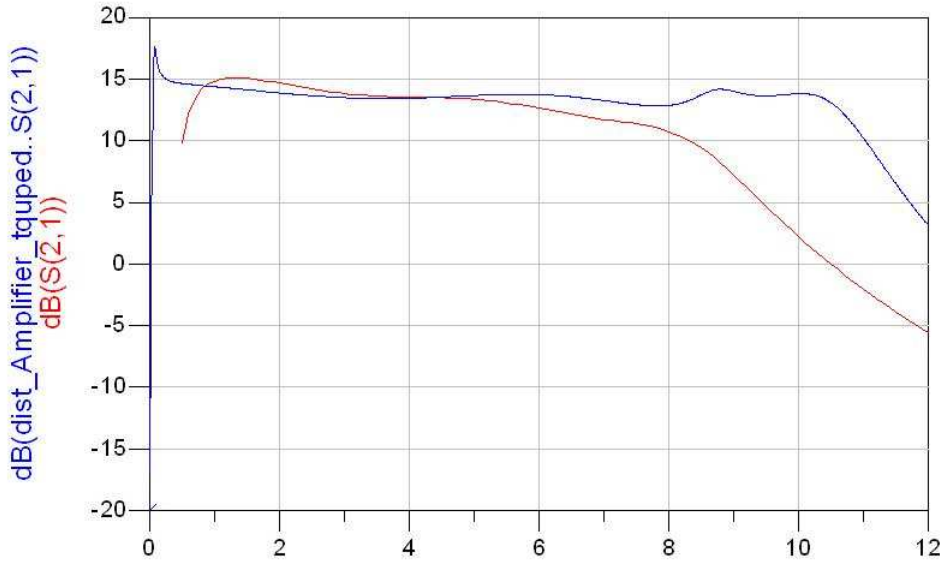


Figure 5.7: Simulated Response

Chapter 6

Conclusions

We finally achieved the goal of this project which was to design a 3 tap finite impulse response (FIR) programmable analog filter. The filter is designed for dispersion compensation purpose. First, we have designed one adaptive equalizer using a 3 tap FIR filter, using ADS software of Agilent technologies. Then we have proposed a novel filter topology where we have replaced each tap gain with a distributed amplifiers to make it programmable. The same lumped LC ladders that provide the tap delays also serve as artificial transmission lines for the distributed tap amplifiers. In this work, we also discuss the design of distributed amplifier MMICs for frequency range of 0.5- 20 GHz. Finally, we design an equalizer with FIR filters having programmable tap gain; it is done by replacing the each tap of FIR filter with distributed amplifiers. They can be used as a linear equalizer or as a part of decision feedback amplifiers.In this project, the designed distributed amplified is basically a Traveling Wave Amplifier.

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