A
Dissertation
on

Tunable Operational Transconductance Amplifier and its Applications

Submitted in partial fulfilment of the requirement
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CERTIFICATE

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This is to certify that the project entitled "**Tunable Operational Transconductance Amplifier and its Applications**" has been completed by **Anjani Kumari** in partial fulfilment of the requirement of **Master in Technology** in **VLSI Design and Embedded Systems**.

This is a record of her work carried out by her under my supervision and support. This is a beneficial work in field of signal processing using ota based technologies and resources.

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ABSTRACT

Over the past decade there has been increasing recognition of the importance of access to communication infrastructures and services for economic and social development. Generally, in communication systems, the processing of signal is accomplished in a single or a set of mixed-signal IC most of which are based on CMOS technology. OTA is a popular choice to implement filters, multipliers, oscillators, and several other important building blocks while satisfying the requirement of high frequency stability, wide input voltage range etc.

Applications of the operational transconductance amplifier are mainly constrained by the non-linearity and small input voltage range, especially when the dimensions are approaching deep-submicron scale. Tunable OTA produces better results than the conventional one in terms of linearity, tunability and frequency response. The motivation of this work is to explore different techniques to improve its performance and to find new structures for applications in field of communication systems.

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Introduction

In the past few decades the field of communication and signal processing has grown at a very rapid pace compared to any other area of technology and, is still growing the same way. This growth is the combined result of the advancement in technology and enhanced circuit designs resulting from a lot of research work done in search of superior circuit design, improvement in the existing options, designing new blocks as alternatives.

At early stage, operational amplifiers were the most popular choice as the building blocks for a wide range of such electronic circuits. Their popularity in circuit design was largely based on the fact that characteristics of the op-amp circuits with negative feedback (such as their gain) are set by external components with little dependence on temperature changes and manufacturing variations in the op-amp itself. But their applications were constrained because of its frequency limitation and instability in open loop configuration. Thus other alternatives were to be searched for high frequency applications.

Operational transconductance amplifiers were the next choice to replace op-amp in most of their applications because of its ability to overcome the above mentioned shortcomings of the op-amp. Beside all these, OTA has a very useful feature of tunability, that is, its transconductance can be changed by using a control voltage and hence can be used as controlled parameter in the circuits that needs to be tuned. Because of all these merits, nowadays OTA based circuits are extensively used to form several active basic building blocks for signal processing systems such as filters, multipliers, oscillators, controlled impedances, etc[1].

There are two modes depending upon the output: single ended and fully differential [2]. Advantages of the differential structure include: improved output voltage swing, less susceptibility to common mode noise, and cancellation of even-order nonlinearities [3]. But the fully differential configuration lacks the current mirror capability of one of the current mirrors as achieved in the single ended configuration and hence is capable of producing only half of the bias current at output which can be

solved by using a double shell structure. Single-stage OTAs tend to be more power efficient than two-stage OTAs, because no power is wasted in driving the compensation capacitance in single-stage OTAs [12].

1.1 Motivation

Communication has always been one of the important needs of human beings as we all are social animal but nowadays it has become an integral part of our life. Now the advancement in technology has made it much cheaper to communicate and to transfer data even through large distances. VLSI technology has a major contribution in the cost reduction, as the large scale production of chips helps to reduce the cost to minimal values.

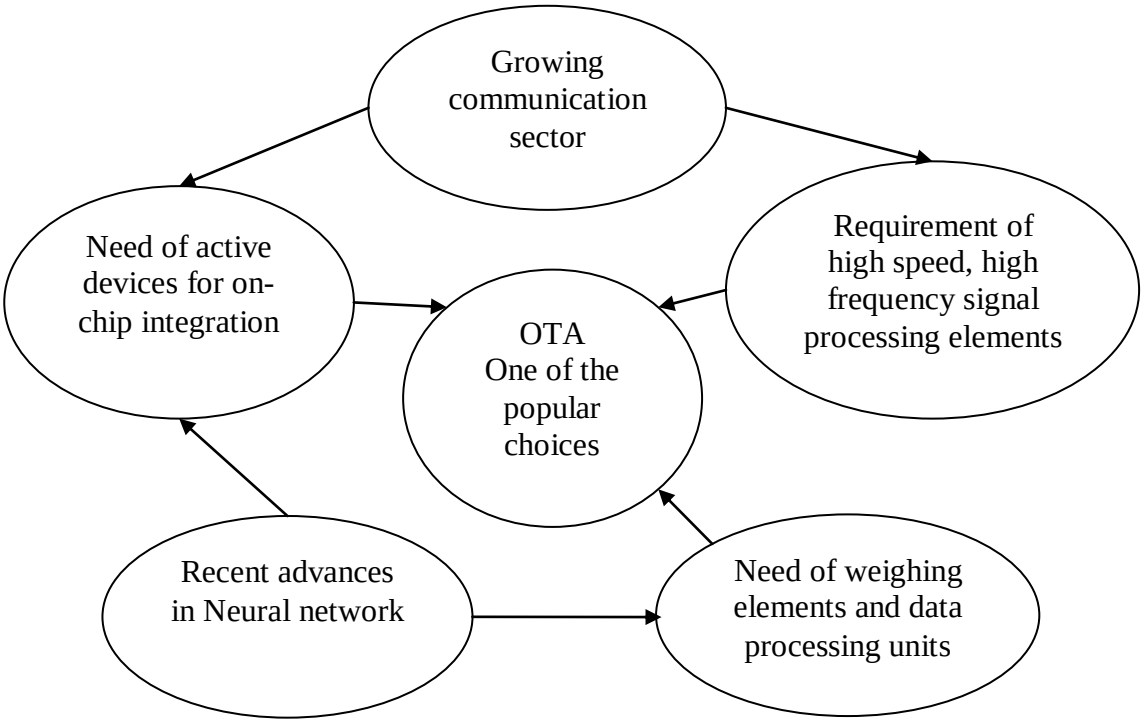

Figure 1. Flow diagram for choosing OTA

Filters, multipliers, oscillators, ADC, DAC and several other important subsystems of such signal processing systems can be actively implemented with the help of operational transconductance amplifier and thus can be fabricated on chip thereby reducing the size of the end product as well as the cost.

1.2 Related work

A lot of work has been done in the field of Operational transconductance amplifier but improvement has always been an endless process as there are always better options yet to be explored. A number of models has been proposed to improve the performance of the existing circuits which is usually on a trade off based between some of the characteristic parameters. One of such example is the usefulness of underlap channel design in improving gain–bandwidth trade-off in Analog circuit design [4], which is based on an innovative device architecture.

Several circuit techniques for improving the linearity of MOS transconductors have been reported in the literature. In [5], linearization is achieved by cross-coupling multiple differential pairs, and properly scaling their W/L ratios and tail currents to cancel the third-order harmonic distortion. A combination of the techniques in [5] and source degeneration with a MOS transistor operating in the triode region yields better linearity performance [6], [7]. Using passive resistor source degeneration in the cross-coupled double differential pair [8] reports superior linearity, but the auxiliary differential pair reduces the effective transconductance and adds more noise. An adaptive biasing scheme using unsymmetrical and symmetrical differential pairs approach to linearize CMOS OTA was developed by Nedungadi and Viswanathan [9]. And still the many other options are being explored achieve better performance than the existing ones.

1.3 Problem Statement

With advancement in technology and demand for superior products high frequency response becomes a critical parameter to be considered. However as the technology is moving to shorter dimensions linearity issue is always an agenda because many hidden effects come into play to cause the non-linearity as the dimension reduces, and it is crucial to achieve high linearity for satisfactory performance of the circuits as well as for the tunability of the transconductance.

As the traditional techniques have their certain shortcomings like small gain, non-linearity and frequency limitations. So for achieving the better tunability even with

the *large circuit* and better linearity and frequency response we are using the **Tunable operational transconductance amplifier** to achieve better performance over the conventional architectures.

Our objective is to use the Tunable OTA for building the basic blocks used in the analog signal systems. Here we are using the new configuration of the operational transconductance amplifier, so that we can get more linear relationship between the output and the controlling voltage.

1.4 Scope of Project

Our approach is to use the *Tunable operational transconductance amplifier* in the field of signal processing by implementing different subsystems like filters, oscillators, multipliers etc with it. Tunable OTA increases the bandwidth, linearity, gain etc without much increasing the complexity of the circuit.

Beside the above mentioned applications in analog signal processing, the TOTA can also be used in neural networks, ADC, DAC. The beauty of the circuit is its simple approach to overcome the limitations of conventional OTA and its applications. The proposed circuits gives much better results than the one with conventional OTA.

1.5 Organization of Thesis

The remainder part of this thesis is organised in the following sections:---

Section 2: It contains the Operational Transconductance Amplifier. It presents the basic introduction of OTA and its internal circuit description. The DC and AC analysis are also discussed here.

Section 3: This section describes the linearization techniques. The mobility compensation and body driven approaches described here. Here the recent innovative underlap channel MOS architecture are also given.

Section 4: In this Section the detail description of Tunable Operational Transconducatnce amplifier is given. It provides the information about the active resistance and cascading of balanced OTA.

Section 5: This section describes different basic buiding blocks implemented using the Tunable OTA.

Section 6: It contains the results obtained from simulation.

Section 7: In this section the conclusion of the thesis work and the future scope of the work are presented.

Section 8: This section gives the references details of the thesis.

Appendix A: Expansions of the Abbreviations used.

Appendix B: Design parameters and model files used for simulation.

Operational Transconductance Amplifier Fundamentals

2.1 Introduction to OTA:

Operational transconductance amplifier is a voltage controlled current source (VCCS) that takes the differential voltage as input and provide current as the output, which is in contrast to the conventional op-amp, which is a voltage-controlled voltage source (VCVS)[10]. It is a transconductor type device, which means that the input voltage controls an output current by means of the device transconductance. The output current is related to the differential input voltage by the following relation:

$$I_O = g_m (V_+ - V_-) \quad (2.1)$$

What is important and useful about the OTA's transconductance parameter g_m is that it is controlled by an external current, the amplifier bias current, I_{BIAS} ,and is given as follows:

$$g_m = \sqrt{2 I_{BIAS} \beta} \quad (2.2)$$

Thus its transconductance can be varied by varying just the bias current. OTA is basically an op-amp without an output buffer and hence can drive only capacitive load[11]. It has been used as a replacement for the conventional op-amp in both first and second-order active filters because of its several advantages over the conventional op-amp. Conventional op-amp required lots of complex feedback networks to attain stable configuration. Figures 2 & 3 shows the basic schematic and equivalent circuit of OTA.

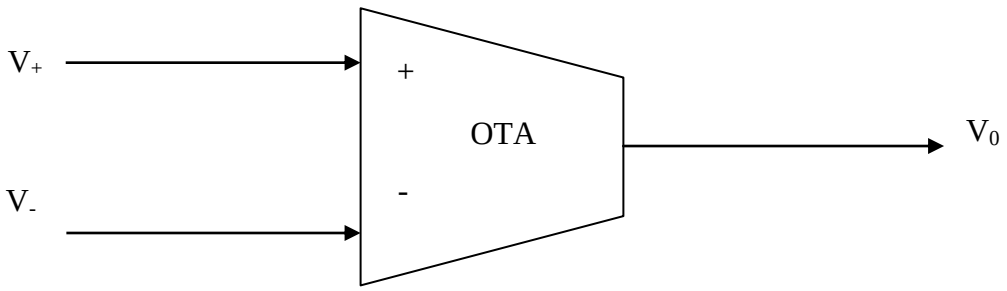

Figure 2. Symbol of OTA

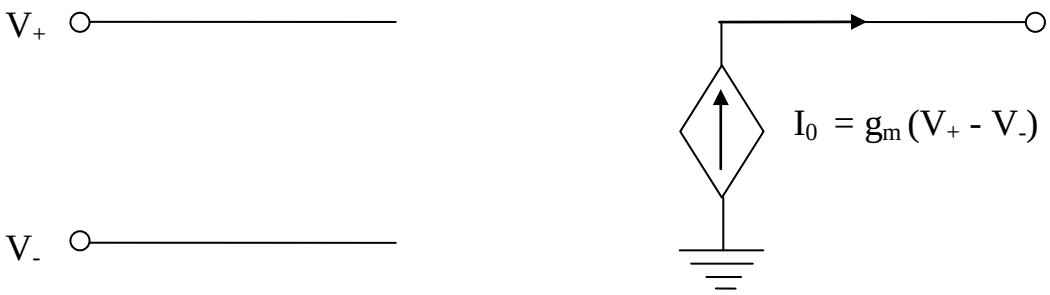

Figure 3. Equivalent Circuit of OTA

Characteristics of Ideal OTA can be summarized as follows

Input impedance (Z_{in}) = ∞

Output Impedance (Z_0) = ∞

Inverting input current I_{0-} = Non-inverting input current I_{0+}

Bandwidth = ∞

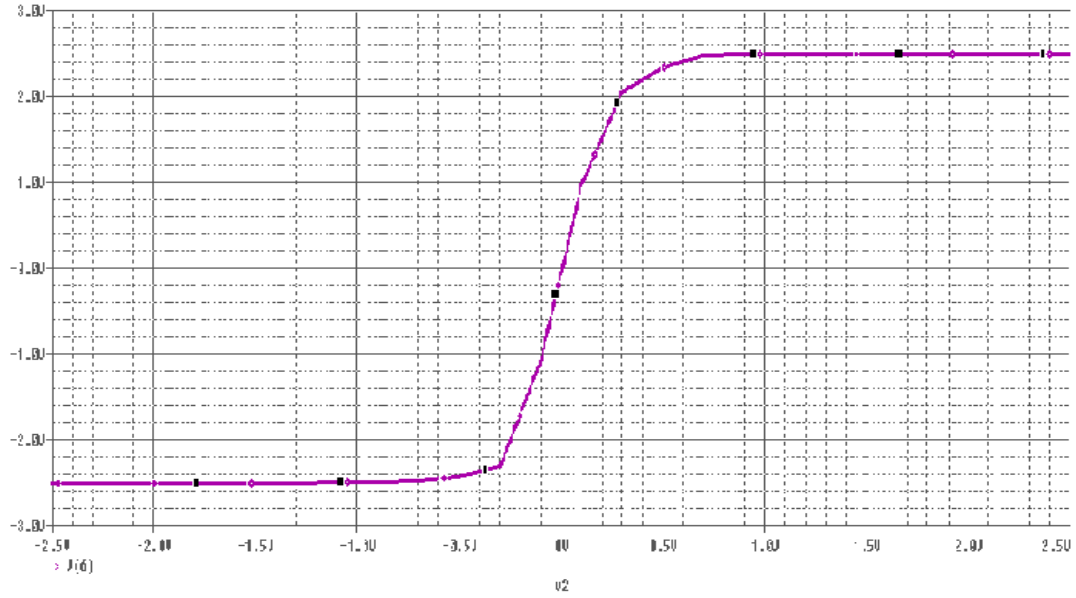

Figure 4. Output Characteristic of OTA

The high output impedance makes the frequency compensation a very easy process, as it can be achieved just by adding a capacitor at the output which is not possible in the case of op-amp as its output impedance is low, thereby lowering the value of time constant.

2.2 INTERNAL CIRCUIT OF OTA

It basically consists of three kinds of sub-circuit:

1. Differential pair
2. Current source
3. Current mirrors

The internal circuit of OTA consist of a differential input stage while the remaining part of the OTA is composed of current mirrors. The geometry of these mirrors, is kept such that the current gain is unity. Thus the output current is precisely defined by the differential input amplifier. The output transfer characteristic of the amplifier is shown in the figure 4. The shape of this characteristic remains constant and is independent of supply voltage. Only the maximum current is modified by the bias current.

2.2.1. Differential pair

Differential amplifiers are well-known electronic devices for amplifying a voltage difference between two input signals. Differential amplifiers are utilized to amplify, and produce an output signal which is a function of the difference between two differential, or complementary, input signals and to thereby enable the detection of relatively weak signal levels while inherently rejecting noise common on the differential input lines.

A differential amplifier usually comprises two electrical paths that are independently coupled to a voltage source at one end, and are together coupled to a voltage or current source at an opposite end. Each electrical path usually comprises a transistor element and a resistance element. They are used to amplify analog, as well as digital signals, and can be used in various implementations to provide an amplified output in response to differential inputs. Many electronic devices use them internally[13].

The output of an ideal differential amplifier is given by:

$$V_0 = A_d (V_+ - V_-) \quad (2.3)$$

Where V_+ and V_- are the input voltages and A_d is the differential gain. In practice, however, the gain is not quite equal for the two inputs. This means, that if V_+ and V_- are equal, the output will not be zero, as it would be in the ideal case.

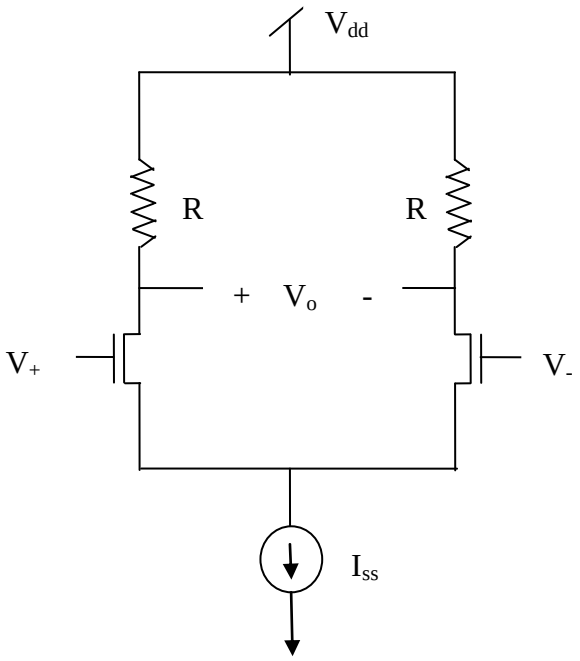

Figure 5. Differential Amplifier

A more realistic expression for the output of a differential amplifier thus includes a second term.

$V_0 = A_d (V_+ - V_-) + Ac (V_+ - V_-)/2$ (2.4)

A_c is called the common-mode gain of the amplifier. As differential amplifiers are often used when it is desired to null out noise or bias-voltages that appear at both inputs, a low common-mode gain is usually considered good.

Common-mode rejection ratio: It is usually defined as the ratio between differential-mode gain and common-mode gain, indicates the ability of the amplifier to accurately cancel voltages that are common to both inputs. Common-mode rejection ratio (CMRR):

$CMRR \approx A_d / A_c$ (2.5)

Differential amplifier circuits are widely used in the electronics industry and are generally preferred over their single-ended counterparts because of the following advantages:

1. Better common-mode noise rejection.
2. Reduced harmonic distortion.
3. Increased output voltage swing.

2.2.2 Current mirror

A current mirror is a circuit designed to copy a current through one active device by controlling the current in another active device of a circuit, keeping the output current constant regardless of loading [14]. The current being 'copied' can be, and sometimes is, a varying signal current. Conceptually, an ideal current mirror is simply an ideal current amplifier. The current mirror is used to provide bias currents and active loads to circuits.

Operation

M1 in Figure 6, will operate in saturation region as its source and drain are shorted, hence its drain current I_{D1} is neglecting the channel length modulation will be

$$I_{D1} = I_{REF} = \frac{\beta_1 (V_{GS} - V_{TH})^2}{2} \tag{2.6}$$

$$I_{D2} = \frac{\beta_2 (V_{GS} - V_{TH})^2}{2} \tag{2.7}$$

From eqn (6) and (7), we can get that

$$I_{OUT} = \frac{\beta_1}{\beta_2} I_{REF} = \frac{(W/L)_1}{(W/L)_2} I_{REF} \tag{2.8}$$

Thus the topology presented allows precise copying of the current with no dependence on the process and temperature. The ratio of I_{OUT} and I_{REF} is given by the ratio of device dimensions, a quantity that can be controlled with reasonable accuracy.

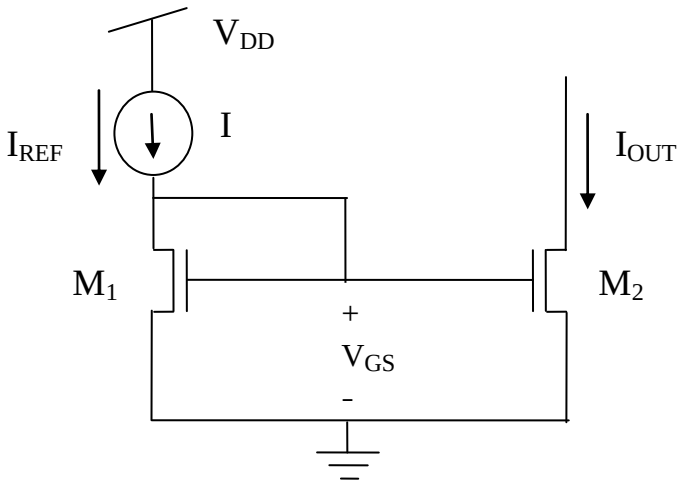

Figure 6. Current Mirror

Desired features

1. Generate an output current equal to input current multiplied by desired current gain factor
2. Current gain is independent of input frequency
3. Output current independent of output voltage to common node

A conventional single stage configuration of the operational transconductance amplifier is shown below:

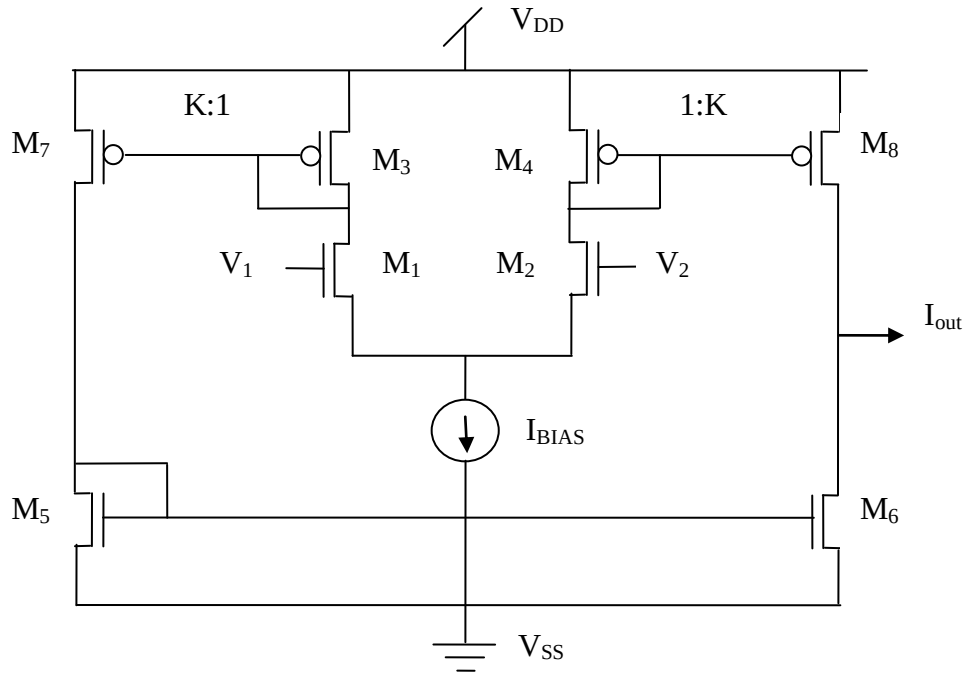

Figure 7. Conventional Single Stage OTA

The OTA employs a differential input pair and three current mirrors. The differential input pair comprises of transistors $M_{1,2}$. The differential pair is biased by current source. Mirrors formed by $M_{3,7}$ and $M_{4,8}$ reflect currents generated in the differential pair to the output shell. The current generated by the mirror of $M_{3,7}$ is then reflected to the output via the mirror formed by $M_{5,6}$. The mirror gain factor, K, indicates the gain in mirrors formed by $M_{3,5}$ and $M_{4,6}$ with the following relations: $\beta_7=K\beta_3$, $\beta_8=K\beta_4$.

2.2 Operation

The conventional OTA (Figure 7) uses a differential pair in conjunction with three current mirrors to convert an input voltage into an output current. Common mode signals ($V_+ = V_-$) are, ideally, rejected. For a common mode input voltage, the currents

are constant and will be:

$i_{d1} = i_{d2} = I_{BIAS}/2$, and $i_{out}=0$

A differential input signal will generate an output current proportional to the applied differential voltage based on the transconductance of the differential pair. Slew rate (SR) is directly proportional to the maximum output current and is defined as the maximum rate of change of the output voltage. For a single stage amplifier, the slew rate is the output current divided by the total load capacitance. The conventional OTA suffers the consequence that high speed requires large bias currents which translates to large static power dissipation. Wireless and battery powered systems require high slew rate and gain bandwidth values with low static power dissipation.

2.3 SIGNAL ANALYSIS

2.3.1 Open Loop Gain

Figure 7, will be referenced to determine the open loop gain.

The output current, in terms of the mirror gain factor (K), is given by:

$$i_{out} = Ki_{d2} - Ki_{d1} \quad (2.9)$$

where,

$$i_{d1} = g_{m1}V_{i-} \quad (2.10)$$

$$i_{d2} = g_{m2}V_{i+} \quad (2.11)$$

Assuming: $gm_1=gm_2$, and substituting (2.10), (2.11) into (2.9):

$$i_{out} = Kg_m(V_{i+} - V_{i-}) \quad (2.12)$$

This indicates the transconductance gain of the OTA is given by:

$$G_m = Kg_m \quad (2.13)$$

The output resistance is a cascode resistance and is given by:

$$R_{out} = r_{06}||r_{08} \quad (2.14)$$

Combining (2.12) and (2.14), the output voltage is then given by:

$$V_{out} = i_{out} = Kg_m(V_{i+} - V_{i-})(r_{o6}||r_{o8}) \quad (2.15)$$

and the open loop gain is:

$$A_o = \frac{V_{out}}{V_{on}} = Kg_m(r_{o6}||r_{o8}) \quad (2.16)$$

2.3.2 AC Analysis

Figure 8, will be referenced for AC analysis. Gain bandwidth of the conventional single stage OTA is limited mainly by the low impedance, high frequency, poles at

node A and B, in conjunction with the high impedance, low frequency pole at the output node [16].

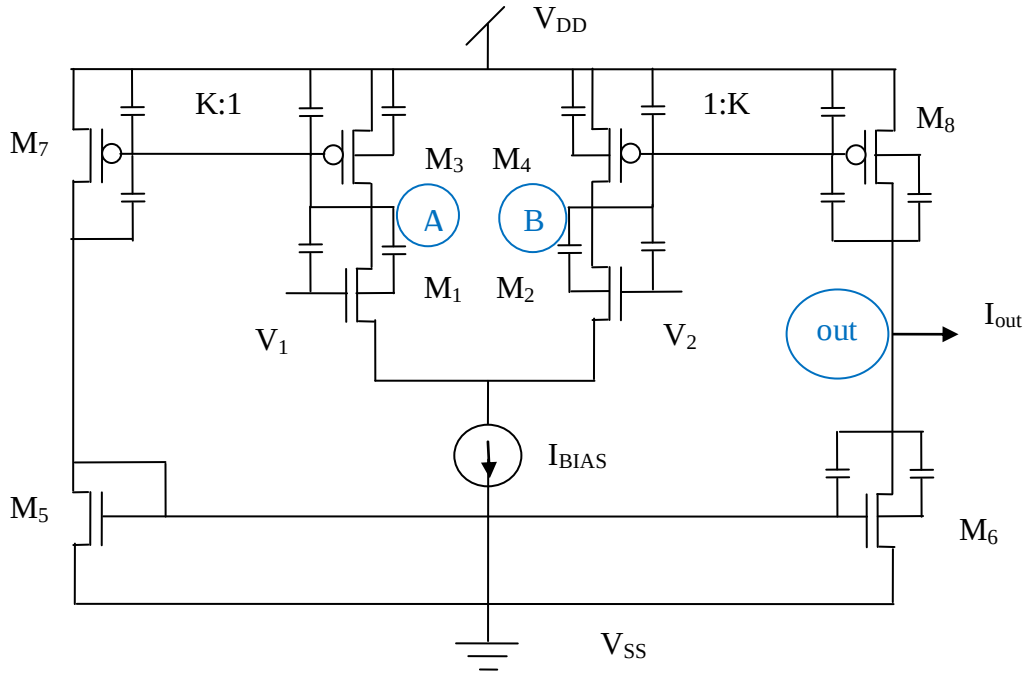

Figure 8. Conventional Single Stage OTA for AC Analysis

The following analysis will define the high frequency pole and will assume nodes A and B are equivalent nodes in terms of resistance and parasitic capacitance (M_1=M_2, M_3=M_4, and M_7=M_8). The resistance at nodes A and B is dominated by the diode connected resistance ($1/g_m$) of M3,4 and is given by:

$$R_{A,B} = \frac{1}{g_{m\,3,4}} || \, r_{o\,1,2} \tag{2.17}$$

The parasitic capacitance at A and B is given by:

$$C_{A,B} = C_{gd\,1.2} + C_{db\,1,2} + C_{gs\,3,4} + C_{db\,3,4} + C_{gd\,7,8} + C_{gs\,7,8} \approx C_{gs\,3,4} + C_{gs\,7,8} \tag{2.18}$$

Combining (2.16), (2.17), and the relation $C_{gs7,8} = KC_{gs3,4}$ the pole at A,B is:

$$f_{pA,B} = \frac{1}{2\pi C_{A,B} R_{A,B}} = \frac{g_{m\,3,4}}{2\pi C_{gs\,3,4}(K+1)} \tag{2.19}$$

The output node capacitance is dominated by the load capacitance (C_L) and is:

$$C_{OUT} = C_{dg\,6} + C_{db\,6} + C_{dg\,8} + C_{db\,8} + C_L \approx C_L \tag{2.20}$$

Combining (2.14) and (2.19), the dominant pole/bandwidth of the OTA is given by:

$$f_{pOUT} = \frac{1}{2\pi C_{OUT} R_{OUT}} = \frac{1}{2\pi C_L (r06||r08)} \quad (2.21)$$

This analysis indicates the relation between the phase margin and the mirror gain factor (K). Equation (2.18) indicates the high frequency pole $f_{pA,B}$ is inversely proportional to K. An increase in K will result in a decrease in $f_{pA,B}$ and consequently a decrease in phase margin. The bandwidth of the conventional OTA is given in Equation (2.20) and is inversely proportional to the load capacitance (C_L).

2.3.3 Gain Bandwidth

Equations (2.16) and (2.20) are combined for the gain bandwidth (GB) product:

$$GB = \frac{Kg_m}{2\pi C_L} \quad (2.22)$$

This relation indicates that the GB is directly proportional to K.

2.3.4 Maximum Output Current

The maximum output current of the conventional OTA is limited by the mirror gain factor (K) and the bias current and is given by:

$$I_{OUT}^{MAX} = KI_{BIAS} \quad (2.23)$$

2.3.5 Slew Rate

The slew rate (SR) is given by:

$$SR = \frac{I_{OUT}^{MAX}}{C_L} = \frac{KI_{BIAS}}{C_L} \quad (2.24)$$

The slew rate therefore, increases linearly with K.

2.4 DC Analysis

2.4.1 Input Common Mode Range

The common mode range (CMR) is defined as the range of voltage (V_{IN}^{MAX}, V_{IN}^{MIN}) for which the input differential pair will remain in saturation. This range is determined by the amplifier structure, transistor sizes, and bias current. For the differential input stage with diode connected loads, the minimum and maximum input voltages can be found by analysis of Figure 9.

2.4.1.1 Minimum Input Voltage

The minimum input voltage can be expressed as:

$$V_{IN}^{MIN} = V_{SS} + V_{DSMB2}^{SAT} + V_{GS1} = V_{SS} + V_{DSMB2}^{SAT} + V_{DS1}^{SAT} + V_{THN1} \quad (2.25)$$

and substituting

$$V_{DS}^{SAT} = \sqrt{\frac{2I_D L}{W\beta}} \quad (2.26)$$

The minimum input voltage becomes:

$$V_{IN}^{MIN} = V_{SS} + \sqrt{\frac{2I_{BIAS}\ L_{MB\,2}}{W_{MB\,2}\beta_N}} + \sqrt{\frac{2I_{BIAS}\ L_1}{W_1\beta_N}} + V_{THN\,1} \quad (2.27)$$

where V_{THN1} is body effected and may be larger than the zero bias threshold voltage. The minimum input voltage is therefore limited by the V_{DS}^{SAT} drop requirements across M_1,M_{B2} and a threshold drop across M_1. The minimum input voltage is inversely proportional to the widths of transistors M_1,M_{B2} and directly proportional to the bias current. To reduce V_{IN}^{MIN} the bias current must be reduced or the widths of the input transistors must be increased.

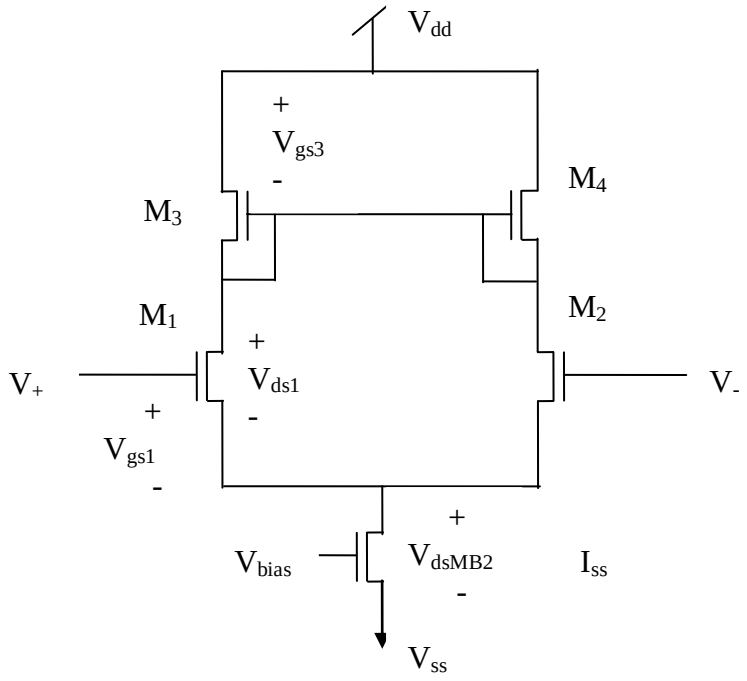

Figure 9. Input Differential Pair With Diode Connected Load.

2.4.1.2 Maximum Input Voltage

The maximum input voltage (V_{IN}^{MAX}) can be expressed:

$$V_{IN}^{MAX} = V_{DD} - V_{GS\,3} - V_{DS\,1}^{SAT} = V_{DD} - V_{DS\,1}^{SAT} - V_{THP\,3} + V_{THN\,1} \quad (2.28)$$

and with substitution of (2.25):

$$V_{IN}^{MAX} = V_{DD} - [\sqrt{\frac{2I_{BIAS}\ L_3}{W_3\beta_P}} - V_{THP\,3}] + V_{THN\,1} \quad (2.29)$$

Again, V_{THN1} is body effected and will be larger than anticipated. In this case, the body effect actually increases input range by contributing to V_{IN}^{MAX} . These results indicate the bias current must be reduced and the width of M_3 must be increased to increase V_{IN}^{MAX} .The maximum input voltage is, therefore, only limited by a V_{GS} drop across M_3. For this reason, the input voltage range is typically limited by V_{IN}^{MIN} . The common mode range of the NMOS differential pair is capable of swinging further in the positive direction than the negative direction.

2.4.2 Output Voltage Range

The output voltage range is defined as V_{OUT}^{MAX} , V_{OUT}^{MIN} which represents the maximum output swing available. The output range of the conventional OTA is reduced just becase of the V_{DS}^{SAT} of the M_6 AND M_8.

$$V_{OUT}^{MAX} = V_{DD} - V_{DS\,8}^{SAT} \quad (2.30)$$

And,

$$V_{OUT}^{MIN} = V_{SS} - V_{DS\,6}^{SAT} \quad (2.31)$$

2.5 Input Offset Voltage

Ideally, if both inputs of the OTA are grounded, the output voltage should be zero. Practically, a nonzero output voltage (offset) will be present and is due to random and systematic errors.

2.5.1 Random Offset

Random errors are due to mismatches in the input stage as a result of fabrication including (but not limited to): threshold voltage differences and geometric differences. Random errors can be estimated via Monte Carlo simulations [4].

2.5.2 Systematic Offset

Systematic errors are inherent to the design. Systematic errors can be the result of

non-symmetries in the OTA design, creating voltage and current mismatches. The systematic offset can be determined via simulation and will be evident in the DC sweep simulation as the offset from the zero-zero intercept where the input voltage and output voltage should both equal zero.

2.6 Advantages of OTA

1. Transconductance can be controlled electronically by adjusting the biasing current. Hence, provides the applications that their features can be tuned electronically
2. The OTA-C filter uses transconductors and capacitors as integrators which work in open loop, thus potentially having the best high frequency characteristics compared to active-RC.
3. The OTA-C filter uses transconductors and capacitors as integrators which work in open loop, thus potentially having the best high frequency characteristics compared to active-RC and MOSFET-C configurations which involve local feedback around the active elements.
4. The wide continuous tuning ability of the OTA also allows the filter to maintain precise filtering characteristics against process variation and temperature drift.

Linearization Techniques

3.1 Linearity

Linearity basically means that the output should reflect a linear change in the input or that the change in the output for should be directly proportional to any change in the input. Good linearity means that the OTA have a flat G_m curve for all input ranges.

3.2 Linearity issue in OTA

In an advanced CMOS process, as the dimensions are reaching deep-submicron region, short-channel effects influence the performance seriously, especially in linearity. But because of the open loop operation mode and inherent large signal non-linear behaviour of the transistors, linearity do put up issues. Therefore, additional circuitry is needed to linearize the transconductance of the OTA. Also at such small dimensions, the supply voltage decreases and device characteristics deteriorate further.

Normally, the circuit parameters are often synthesized by the ideal transfer function for simplicity which generally results in the variation of the output from the desired response especially at the frequencies closed to the OTA opened-loop bandwidth.
At high frequency the parasitics come into the picture which are usually neglected at low frequencies.

3.3 Linearization methods for OTA

There is a lot of literature on the methods for increasing the linearity of OTA, as it is the key problem in the implementation of signal processing blocks using OTA. There are three types of linearization techniques for OTA:

1. Attenuation,
2. Source degeneration,
3. Cancelling nonlinear terms.
4. Cross-coupling multiple differential pairs
5. Using adaptive biasing technique

These schemes will improve the overall performance at the expense of reduction of the OTA's G_m.

3.4 Models for linearization

Several models of OTA had been proposed to improve the linearity. Some of which are discussed below.

3.4.1 Linear CMOS OTA with wide input voltage range using mobility compensation.

A new OTA has been proposed using the mobility compensation technique and common-mode control circuit, which shows a good linearity without sacrificing its input swing range. The circuit introduces the parallel combination of Gm path at the triode and the subthreshold region transistors, respectively. It has the advantages of wide input range as well as good linearity.

To improve linearization of Gm, the basic idea is attenuation of the input signals by a factor k. The technique employing source degeneration is often used for it. The source degeneration factor N is a multiplication of G_m and source degeneration resistor. While the circuit reduces the signal transconductance, G_m, by (1+N), the third harmonic distortion is reduced by the square of the same factor. Then, the linear range of the input is increased by a factor (1+N). An advanced technique minimizes the algebraic sum of nonlinear terms yielding ideally only a linear term. This can be done by combination of the several different values of G_m. Cross-coupling of multiple differential pairs, and properly scaling their W/L ratios and tail currents to cancel the third-order harmonic distortion.

3.4.1.1. OTA architectures

We classify the OTAs into two categories:

1. Fully differential(FD) type and
2. Pseudo-differential (PD) type.

The FD shown in Figure 10. is typically based on a source-coupled differential pair with a tail current source, and the PD shown, has two independent inverters without tail current source.

Avoiding the voltage drop across the tail current source, in the PD structure, allows achieving wider input range. Thus, the structure is obviously more suitable for realization of low voltage circuits than the FD structure. However, the circuit has a problem that the signal gain of CM is high because the output resistance of the tail current source, which functions as the source degeneration [17] for CM signal, is removed.

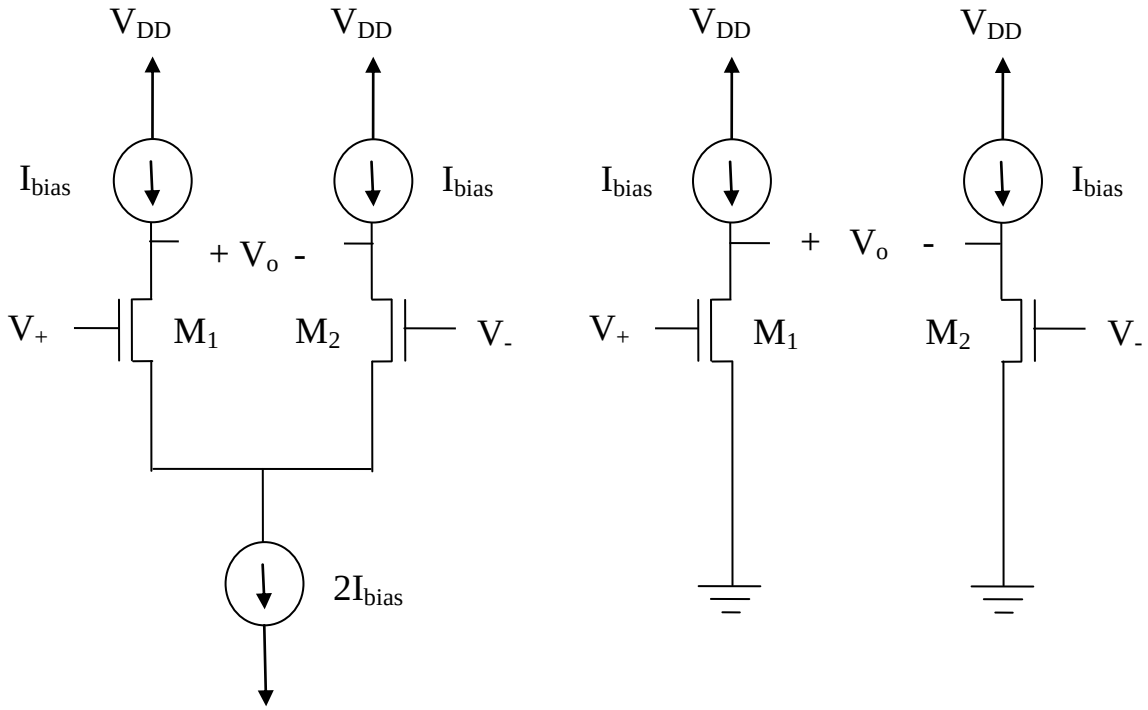

Figure 10. Fully differential and Pseudo differential configuration

In a G_m-C filter, high CM gain of the integrator composed of an OTA and a capacitor makes the circuit unstable. The negative feedback for a differential-mode (DM) signal works as a positive feedback for CM signal in a resonator of the two integrators feedback loop. The CM gain of each integrator must be less than 0-dB to keep the circuit stable for all frequency. Therefore, a CM control circuit to reduce the CM gain is necessary in the pseudo-differential OTA.

3.4.1.2 Pseudo-differential self-regulated OTA

Figure 11, shows a pseudo-differential self-regulated OTA based on transistors operating in triode region [18,19]. Transistors M_l and M_2 operate in the triode region.

MOSFET operating in the triode region can provide linear I_{DI} versus V_{GS} during its drain-source voltage is constant. Transistors M_3, M_4 and amplifier A form a regulated-gain-control (RGC) loop. They force each drain voltage of M_1 and M_2 to be equal to V_{Tune} for the input levels. Therefore, we get a constant V_{DS} independent of the common-mode input voltage level, and linear G_m given by, βV_{DS}.

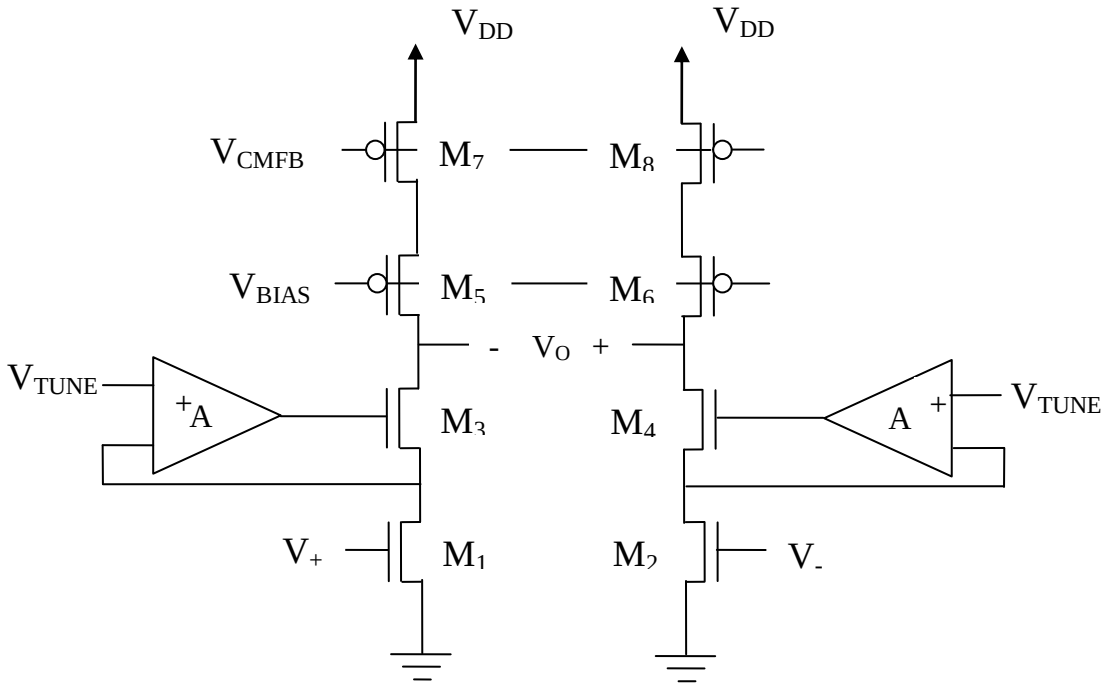

Figure 11. Pseudo differential self regulated OTA

The tuning voltage, V_{Tune}, adjusts the OTA's G_m. However, V_{DS} must be low enough to ensure each input transistor remains in the triode region. This circuit introduces small G_m comparison with the circuit working at saturation region. The input common-mode level is tightly controlled and V_{DS} must track V_{tune} so as to keep constant I_D .

The amplifier A is composed of a single-ended differential amplifier and a level shifter. In order to have the gain-boosting effect, the amplifier gain at the cut-off frequency has to be greater than 20-dB (=10V/V). It is important to maximize the bandwidth of the RGC loop to achieve good linearity at high frequencies. For short-channel devices, the effective carrier mobility μ_{eff} is a function of both lateral and

vertical electric fields. The short-channel effects limit the OTA linearity. The RGC loop reduces the lateral electric field effect.

3.4.1.3 Mobility compensation technique

The OTA using self-regulated technique can overcome the effect of the lateral field due to the constant V_{DS}. However, a vertical field originating from the gate voltage also influences carrier velocity. The effect of the vertical field on the mobility is often modelled by changing it to an effective mobility given by

$$\mu_{eff} = \frac{\mu_o}{1+\theta(V_{GS}+V_{THN})} \quad (3.1)$$

where μ_0 is the zero field mobility of carriers and μ_0 is the mobility reduction coefficient. Equation (3.1) means that the mobility is decreased as the gate-source voltage, V_{GS}, increases of the input transistor.

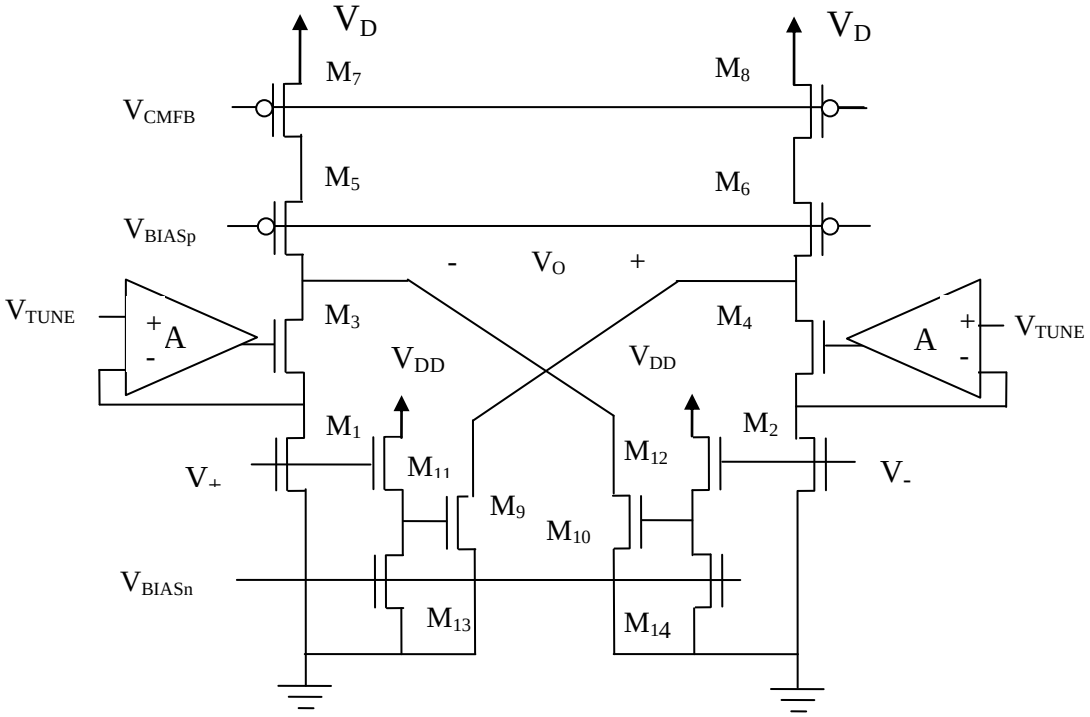

Figure 12. Pseudo differential self regulated OTA with mobility compensation technique

The Pseudo-differential self-regulated OTA with mobility compensation (MC) technique is shown in Figure 12. In order to compensate the nonlinearity caused by mobility reduction effect, we employ transistors M_9 and M_{10} operating in their sub-

threshold regions. The concept of distortion reduction comes from that the third-order harmonic terms of the triode and the sub-threshold region devices have opposite signs. The level shifters consisting of the transistors M_{l1}-M_{14} force M_9 and M_{10} to operate in their sub-threshold regions.

Thus, the parallel connection of the triode and the sub-threshold region OTAs cancels the distortion term with a proper aspect ratio, and increases linearity of Gm remarkably. In addition, the input range of this configuration of OTA is comparable to that of the self-regulated OTA.

3.4.2 CMOS OTA based on body driven MOSFETs

A triode-based OTA with enhanced trans-conductance linearity is presented. By using the BD technique, the trade-off between input and tuning ranges is relaxed. In addition, a new CMFB technique is developed to stabilize the CM output voltage upon trans-conductance tuning without appreciably increasing the total power consumption.

3.4.2.1 Principle of operation

The body driven OTA is shown in Figure 13. The OTA core, which consists of MOSFETs – M_1 – M_8 and regulation amplifiers A, provides differential outputs (V_{out+} and V_{out-}). As M_1 and M_2 operate in triode region, the trans-conductance tuning of the OTA is managed by controlling the source–drain voltage (V_{SD}) of M_1 and M_2 . This is realized by the negative FB loop that is comprised of the regulation amplifier A and the cascode MOSFETs M_3 – M_4. Ideally, it is ensured to be $V'_{DD} - V_{tune}$.

Besides offering the tuning capability, the local FB boosts the output impedance, thus enhancing the dc gain. Compared to the conventional pseudo-differential trans-conductors[20,21] M_1 and M_2 are BD to achieve lower distortion[22-24]. The p-type MOSFETs are chosen to be BD in this design because n-well CMOS process is used. The sources of other p-type MOSFETs are tied to their own substrates, respectively.

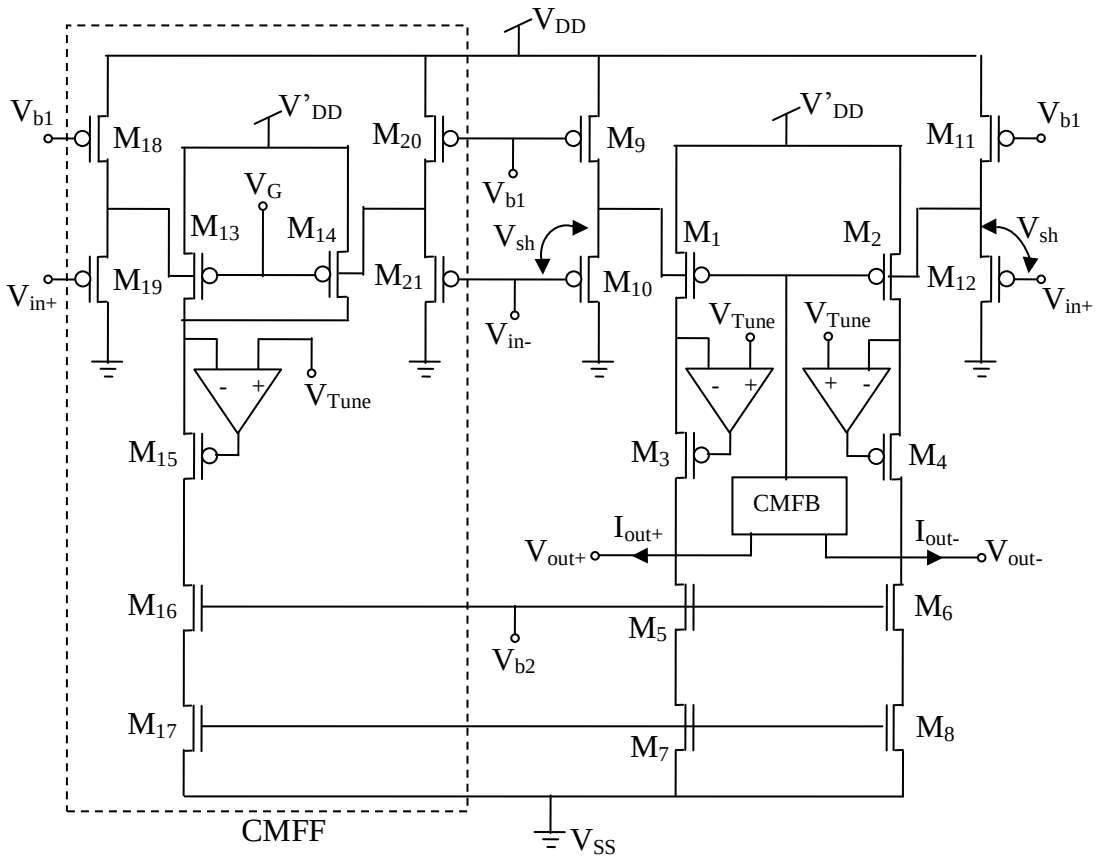

Figure 13. Body Driven MOSFET based OTA

The OTA core itself does not suppress CM signal. Inherently, it has the same gain for both differential-mode and CM signals. In order to suppress the input CM component, CMFF circuit (shown within the dotted block in Figure 9.) is employed to adjust the bias of the OTA core. Except for M_{13} and M_{14} whose width are half of the width of M_1 and M_2 , the rest of the CMFF transistors match the OTA core. By applying differential input signals ($V_{in+} = V_{CM} + V_{in}/2$ and $V_{in+} = V_{CM} + V_{in}/2$) to CMFF circuit, the transconductance current induced by V_{CM} is sensed and then cancelled out at the OTA outputs. $M_9 - M_{12}$ and $M_8 - M_{21}$ constitute level shifters to bring the output CM voltage and input CM voltage to the same level. This is necessary for unity-gain FB systems and filter designs, where the outputs of one OTA are normally the inputs of the next OTA stage. The biasing voltages V_{b1} and V_{b2} are provided externally for easy tuning.

In the actual implementation, these bias voltages can be easily generated from bandgap reference circuits and poly resistors. Tuning bits may be added to the resistors for extra tunability.

3.4.2.1 Transconductance and Output Impedance Analysis

The triode behaviour of the p-MOSFET is described by

$$I_D = \beta\{V_{SB} - |V_{T0}| - \gamma\sqrt{2|\varphi_F| - V_{SB}} + \gamma\sqrt{2|\varphi_F|} - {}^{nV_{SD}}/_{2}\}V_{SD} \quad (3.2)$$

For M_1 and M_2,

$$V_{SB} = V_{DD} - (V_{sh} + V_{CM} \pm {}^{V_{in}}/_{2}) \quad (3.3)$$

where V_{sh} denotes the level-shifting voltage. Based on the fact that

$${}^{V_{in}}/_{2} \ll 2|\varphi_F| - V_{DD} + (V_{sh} + V_{CM}) \quad (3.4)$$

Taylor series expansion is performed on eqn (7) to get the simplified expression

$$I_D = \beta\{V_o \pm K\,{}^{V_{in}}/_{2} - {}^{nV_{SD}}/_{2}\}V_{SD} \quad (3.5)$$

V_o refers to the saturation voltage

$$V_o = V_{SG} - |V_{T0}| - \gamma\sqrt{2|\varphi_F| - V_{SB\,0}} + \gamma\sqrt{2|\varphi_F|} \quad (3.6)$$

Where $V_{SB\,0}$ denotes the source–body voltages of and at the dc operating point.

$$V_{SB\,0} = V_{DD} + (V_{sh} + V_{CM}) \quad (3.7)$$

K is defined as

$$K = {}^{\gamma}/_{2}\sqrt{(2|\varphi_F| - V_{SB\,0})} \quad (3.8)$$

If I_{CM} is equal to

$$I_{CM} = \beta(V_o - nV_{SD}/2)V_{SD} \quad (3.9)$$

The output currents are obtained as

$$I_{out+,out-} = I_{1,2} - I_{CM} = \pm\beta K V_{SD}\, V_{in}/2 \quad (3.10)$$

As shown in Equation (3.10), the output currents are linearly related to and the transconductance linearly depends on the tuning voltage.

Tunable OTA

4.1 Introduction

To improve the behaviour of the circuit a Tunable Operational Transconductance Amplifier (TOTA)[25] is implemented using two cascaded Balanced OTA through an active resistor. A resistor is required to convert the current output of the first stage to a voltage output. This voltage output is then fed to the second stage of Balanced OTA. A normal resistor is difficult to fabricate on a silicon chip. Thus, an Active resistor (Active-R) is implemented by using two NMOS transistors whose resistance can be varied by varying the dimensions of the transistors.

The resistance value is derived and it is seen that the Active-R value is directly proportional to the length of the channel and inversely proportional to the width. A small value of resistor is desired in this work. This is because; the input voltage range for a Balanced OTA is limited and becomes nonlinear at large input voltages. Thus if the value of resistance of Active-R is sufficiently large, the transconductor behaves non-linear to even small differential voltages. In addition to this, large value of length would lead to larger parasites and large transistors contribute to the noise in the circuit. Standard specifications are simulated, suitable for Balanced and Tunable OTA comparison and from the simulation results, it can be seen that the Tunable OTA has better specifications and in addition, post layout simulations are performed for Tunable OTA to check for the practical implementation of the OTA circuit.

4.2 Balanced OTA (BOTA)

It is the simplest OTA structure implemented using a differential amplifier and three pairs of current mirrors. Balancing is achieved by coupling between the device sources and current mirrors.

All the MOS devices are operated in Saturation region, the transistor Drain Current I_D is characterized by a square law model given by:

$I_D = \beta(V_{GS} - V_{TH})^2$, for $V_{GS} > V_{TH}$ (4.1)

and $I_D = 0$, for $V_{GS} \leq V_{TH}$

β is the transconductance parameter of the transistor,

$\beta = \mu_n C_{ox} W/2L$ (4.2)

where μ_n = carrier mobility(electrons)

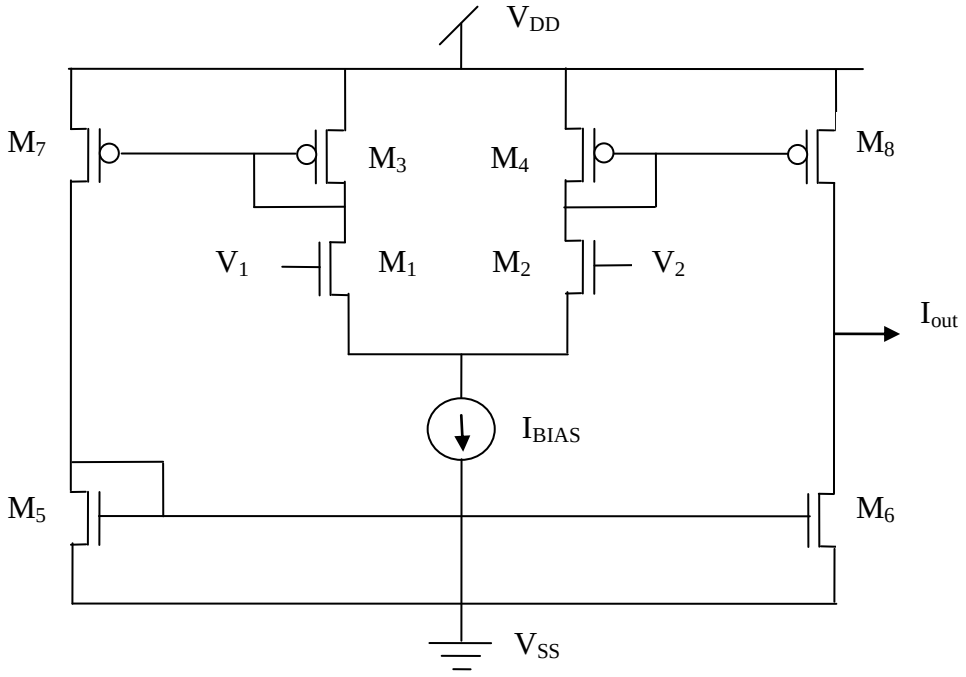

Figure 14. Schematic of Balanced OTA

C_{ox} is the gate oxide capacitance per unit area, W is the effective channel width; L is the effective length of the channel. The Balanced OTA in Figure.1 is formed by coupling the device sources and current mirrors, where,

$V_{in} = V_2 - V_1$ (4.3)

i_o is the differential output current and I_{BIAS} is the bias current.

Let us assume that all the transistors have unity gain (i.e.,W/L=1).

$i_o = i_2 - i_1$ (4.4)

From the differential amplifier, the output current in terms of input voltage, bias current and process parameters can be derived and the expression for the output current is given by:

$$i_o = g_m V_{in} = V_{in}\sqrt{2\beta I_{BIAS}\left(1 - \frac{\beta V_{in}^2}{2I_{BIAS}}\right)} \quad (4.5)$$

provided that,

$$-\sqrt{\frac{I_{BIAS}}{\beta}} \leq V_{in} \leq \sqrt{\frac{I_{BIAS}}{\beta}} \quad (4.6)$$

The small signal transconductance gain (gm) of the circuit is given by:

$$g_m = \frac{\partial i_o}{\partial V_{in}} = \sqrt{2\beta I_{BIAS}} \quad (4.7)$$

If, $-\sqrt{\frac{I_{BIAS}}{\beta}} \leq V_{in} \leq \sqrt{\frac{I_{BIAS}}{\beta}}$

$$i_o = g_m V_{in} = V_{in}\sqrt{2\beta I_{BIAS}} \quad (4.8)$$

4.3 Active Resistor (Active-R)

Transconductance gain (g_m) of an OTA can be varied by bias current I_{BIAS} but as it is within the square root thus making its characteristics non-linear. A Balanced OTA is a basic building block for Tunable OTA. Tunable OTA comprises of two stages of BOTA and a resistor connected in between the two stages. The first stage converts the differential input signal voltage into a signal current io to flow into a resistor (Active-R). The voltage across the resistor is V_R given by:

$V_R = i_0R = V_{in}g_mR$

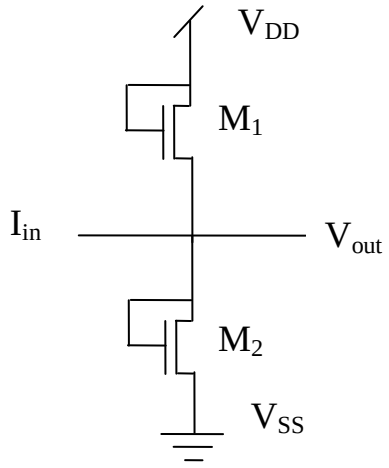

Figure 15. Schematic of Active Resistance

Active-R can be designed using one of the following ways:

- Active-R using 2-NMOS diode connected load [25].
- Active-R using grounded OTA.

Since OTA consumes lot of area, Active-R is chosen to be designed using NMOS diode connected MOSFETs in this work. The derivation for the value of diode connected NMOS Active-R is as follows:

$$I_{in} = I_2 - I_1 \tag{4.9}$$

Where,

$$I_1 = \beta(V_{DD} - V_O - V_{TH})^2 \tag{4.10}$$

$$I_2 = \beta(V_O - V_{SS} - V_{TH})^2 \tag{4.11}$$

By the principle of algebraic identities, we have

$$(A + B)^2 - (A - B)^2 = 4AB$$

Therefore,

$$I_{in} = 4\beta(V_{DD} - V_{TH})V_O \tag{4.12}$$

$$=> I_2 - I_1 = 4\beta(V_{DD} - V_{TH})V_O \tag{4.13}$$

$$=> V_O = \frac{I_2 - I_1}{4\beta(V_{DD} - V_{TH})} \tag{4.14}$$

$$=> R = \frac{V_O}{I_2 - I_1} = \frac{1}{4\beta(V_{DD} - V_{TH})} \tag{4.15}$$

$$=> R = \frac{1}{4K_N^{'}(V_{DD} - V_{TH})W/L} \tag{4.16}$$

Where, $K_N^{'} = \frac{\mu_n C_{OX}}{2}$ (4.17)

Thus, we can observe that the value of resistance is inversely proportional to the process Transconductance parameter and thus is inversely proportional to the effective width and directly proportional to the effective length. So it can be used as a parameter to set the resistance value but since it is a process parameter it can't be changed once the device is manufactured. It can be seen as an advantage also as it is not dependent on the operating conditions and hence the variation is less.

Tunable OTA is implemented by cascading two balanced OTA and the active resistor, both of which has been explained above. OTA's The schematic of Tunable OTA is shown in figure 16.

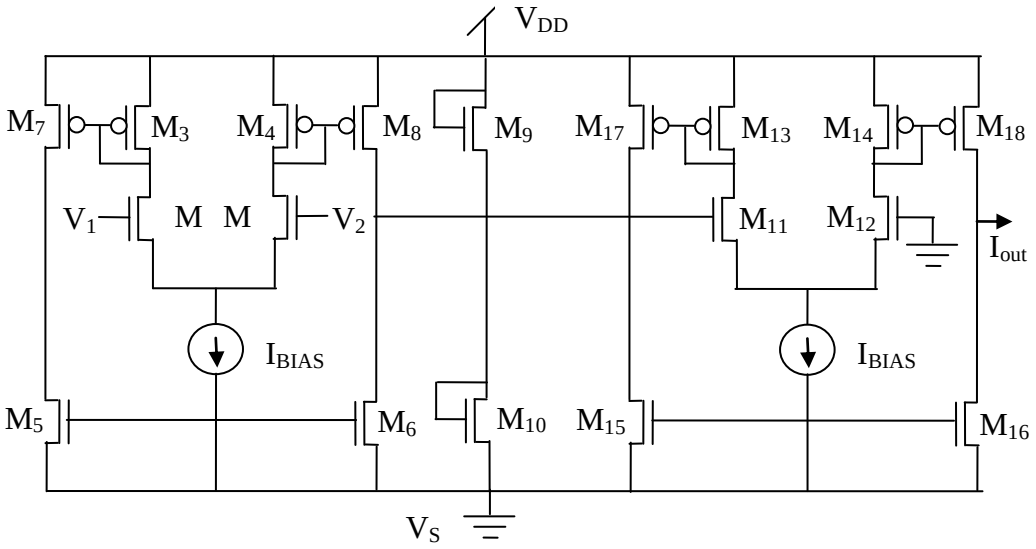

Figure 16. Schematic of Tunable OTA

The Total Current i_{out} is given by:

$$i_{out} = g_{m2} V_R \tag{4.18}$$

$$i_{out} = \frac{g_{m2} g_{m1} V_{in}}{4\beta (V_{DD} - V_{TH})} \tag{4.19}$$

$$g_{m1} = \sqrt{2\beta_1 I_{BIAS1}} \tag{4.20}$$

$$g_{m2} = \sqrt{2\beta_2 I_{BIAS2}} \tag{4.21}$$

If $I_{BIAS1} = I_{BIAS2} = I_{BIAS}$ then the expression for total current is given by:

$$i_{out} = I_{BIAS} \sqrt{2\beta_1 \beta_2} V_{in} \frac{1}{2\beta (V_{DD} - V_{TH})} \tag{4.22}$$

$$i_{out} = g_{mT} V_{in} \tag{4.23}$$

$$g_{mT} = I_{BIAS} \beta_T \tag{4.24}$$

$$\beta_T = \sqrt{\beta_1 \beta_2} \frac{1}{2\beta (V_{DD} - V_{TH})} \tag{4.22}$$

β is the transconductance parameter of Active-R transistors.

We can say that the transconductance of the tunable is linear with respect to tail currents. Therefore, linearity with respect to transconductance gain is achieved by just cascading of OTAs through a resistor.

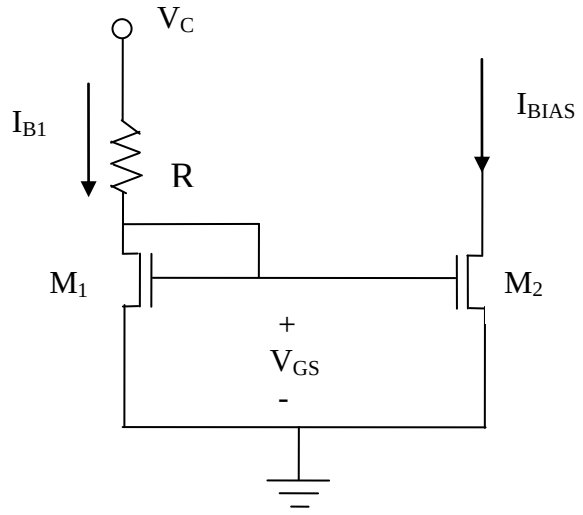

Figure 17. Current mirror used as current source for bias current

Performance of conventional op-amp degrade at high frequencies as its output is a voltage and is thus limited to only a few megahertz, to attain good performance at high frequencies large amount of compensation techniques are required. Each of these compensation techniques would require numbers of resistors and capacitors which are difficult to implement on the chip and lead to more and more parasitics. Thus a circuit with current mode output called as 'Operational Transconductance Amplifier' can be used to replace it. One of the configurations of OTA, called as 'Balanced OTA' is designed using a design procedure for better CMRR, Bandwidth and Slew rate.

The improved version of Balanced OTA is then used as a basic building block to implement 'Tunable OTA' possessing better performance than that of Balanced OTA and Improved Balanced OTA. Tunable OTA is implemented by cascading two Balanced OTAs through an active resistor. Two cascaded NMOS transistors implement an active-resistor. The value of resistor is chosen such that the distortion is kept at low level. A detail mathematical analysis of Balanced OTA, Active Resistor and Tunable OTA is studied.

Applications

Tunable OTA can be used in to implement several important circuits that form subsystems like filters, multipliers, oscillators in communication and signal processing systems, neural cells in the growing neural networks techniques. Some of these are discussed below:

5.1 Filters:

Filters are the most common and vital circuits in any signal processing system. When it comes to high frequencies, operational transconductance amplifiers (OTAs) have proven to be the best candidate for the implementation of continuous time filters. Moreover, the transconductance can be tuned continuously allowing the filter to be compensated for process tolerances and temperature variations.

As filters are very important blocks, lots of work has been done on its configuration to improve its performance. Universal C-g_m filter[26] is one of the famous configuration, with which all forms of filters can be realized.

UNIVERSAL C FILTER USING TOTA

A Bi-Quad Filter is a filter which displays a transfer function that is the ratio of two quadratic equations. This design of Bi-Quad filter uses three Tunable OTAs which are controllable by three voltages. The circuit of the universal C-filter is shown below:

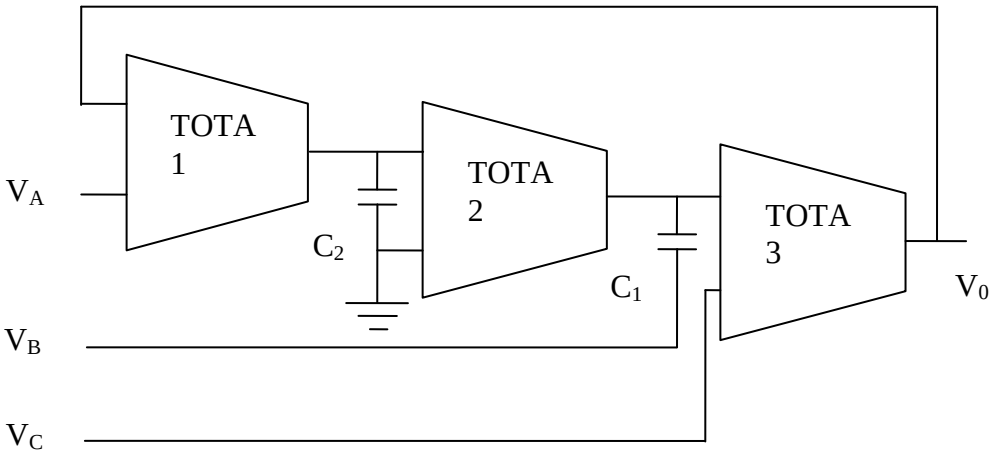

Figure 18. Universal OTA-C filter

By controlling the inputs to the three input voltage terminal, a low pass, high pass, band pass, notch and all pass filters can be implemented. The relationship between the output voltage and the three control voltages (V_A, V_B and V_C) is given as under:

$$V_O = \frac{(s^2 C_1 C_2 V_C + sC_1 g_{m3} V_B + g_{m1} g_{m2} V_A)}{(s^2 C_1 C_2 + sC_1 g_{m3} + g_{m1} g_{m2})} \quad (5.1)$$

Thus the circuit can be used as different filters by setting the values of V_A, V_B and V_C as under :

Table 5.1

Filter type	**Voltage conditions**	**Output voltage**
Low pass	$V_A = V_{in}$ and $V_B = V_C = 0v$	$\frac{(g_{m1} g_{m2} V_{in})}{(s^2 C_1 C_2 + sC_1 g_{m3} + g_{m1} g_{m2})}$
High pass	$V_C = V_{in}$ and $V_A = V_B = 0v$	$\frac{(s^2 C_1 C_2 V_{in})}{(s^2 C_1 C_2 + sC_1 g_{m3} + g_{m1} g_{m2})}$
Band pass	$V_B = V_{in}$ and $V_A = V_C = 0v$	$\frac{(sC_1 g_{m3} V_{in})}{(s^2 C_1 C_2 + sC_1 g_{m3} + g_{m1} g_{m2})}$
Notch	$V_A = V_C = V_{in}$ and $V_B = 0v$	$\frac{(s^2 C_1 C_2 + g_{m1} g_{m2}) V_{in}}{(s^2 C_1 C_2 + sC_1 g_{m3} + g_{m1} g_{m2})}$
All pass	$V_A = V_C = -V_B = V_{in}$	$\frac{(s^2 C_1 C_2 - sC_1 g_{m3} + g_{m1} g_{m2}) V_{in}}{(s^2 C_1 C_2 + sC_1 g_{m3} + g_{m1} g_{m2})}$

5.2 Multiplier

An analog multiplier is a basic building block of many signal processing circuits. They have several applications in modulation, detection, frequency translation, automatic gain controlling, Fuzzy systems and neural networks. Usually, the variable transconductance technique which operates on Gilbert's translinear circuit is widely used for the design of multiplier circuits in Bipolar and CMOS technologies [27]. The other approaches in CMOS technology are based on square-law characteristics of MOS transistor which are biased in saturation region [28] and that based on the current-voltage characteristics of MOS transistor in the non-saturation region [29]. But each of the structure proposed so far, requires a squarer followed by an adder to

implement the multiplication function, but using the tunable OTA multiplication function can be implemented directly, which require neither a squarer nor an adder.

From Equation 2.2 it can be seen that the transconductance of conventional OTA is given by following relationship:

$$g_m = \sqrt{2I_{BIAS}\beta}$$

Thus g_m is proportional to the square root of the bias current while from Equation 4.24 it is clear that in tunable OTA, the tranconductance is given as follows:

$$g_{mT} = I_{BIAS}\beta_T$$

Hence in the tunable OTA the transconductance is directly proportional to the bias current which in turn can be made proportional to the control voltage applied at one of the MOSFET in the current source circuit by small amendment in the circuit of the current source. The conventional current source, used in OTA have the following structure:

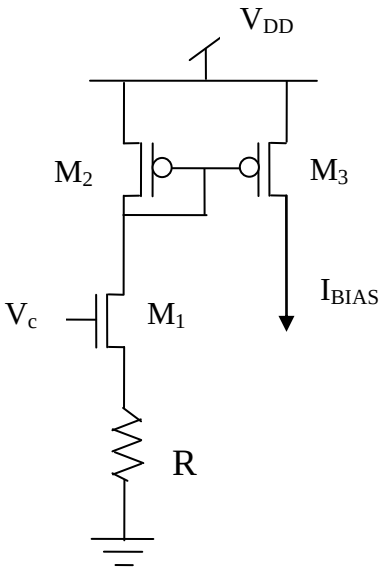

Figure 19. Conventional Current Source

The bias current produced by the current source shown above is given by:

$$I_{BIAS} = \frac{(V_C - V_{GS\,1})}{R} \qquad (5.2)$$

Hence the V_{GS1} term in the expression prevents the linear proportionality of the bias current to the control voltage, now with small manipulation in the circuit the objective of making I_{BIAS} directly proportional to V_C can be accomplished.

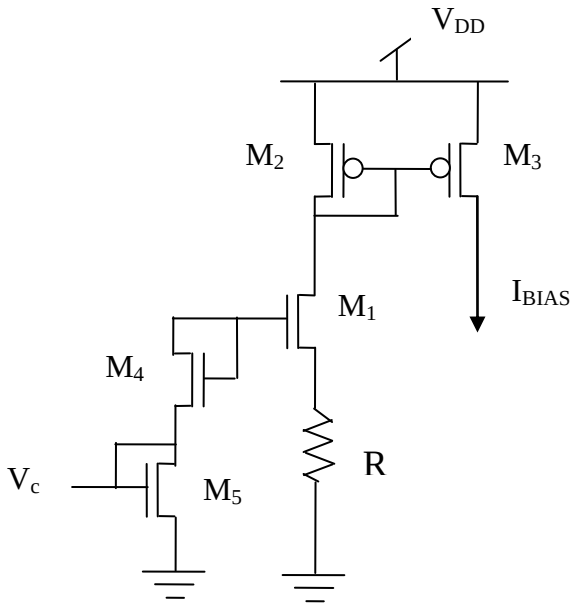

Figure 20. Modified Current Source

Now in the above circuit the above circuit it can be calculated that the bias current provided by the modified current source is

$$I_{BIAS} = \frac{(V_C + V_{GS\,4} - V_{GS\,1})}{R} \tag{5.3}$$

If $V_{GS4} = V_{GS1}$, then

$$I_{BIAS} = \frac{V_C}{R} \tag{5.4}$$

Thus the output is given by

$$I_{out} = g_{mT}\,(V_{in+} - V_{in-}) \tag{5.5}$$

If V_{in-} is zero, then

$$I_{out} = g_{mT}\,V_{in+} \tag{5.6}$$

$$I_{out} = \beta_T I_{BIAS} V_{in+} \tag{5.7}$$

$$I_{out} = \frac{\beta_T V_C V_{in+}}{R} \tag{5.8}$$

So by applying one signal at the control voltage (V_C) and other at one of the input voltage terminal(Vin+ or Vin-), the two signals can be multiplied directly but with again of β_T/R.

Results

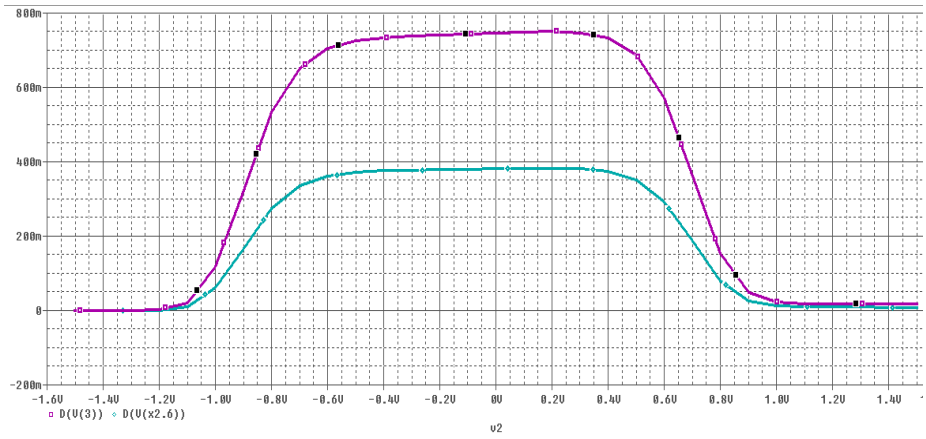

Figure 21. Transconductance G_m

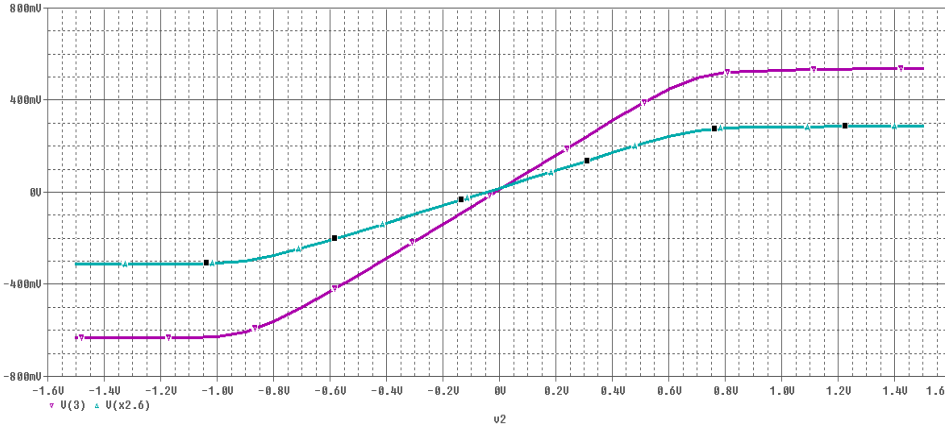

Figure 22. Input-Output Characteristic

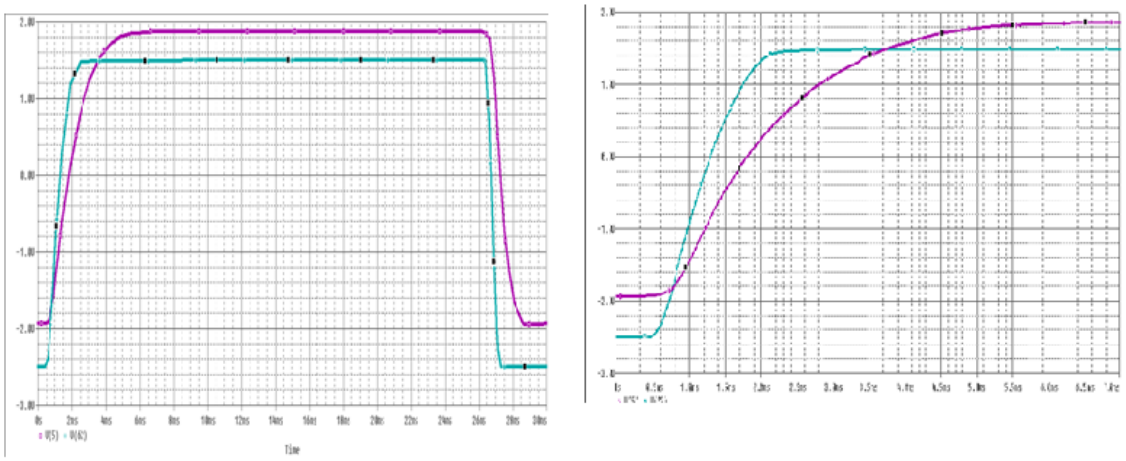

Figure 23. Slew Rate and Settling Time

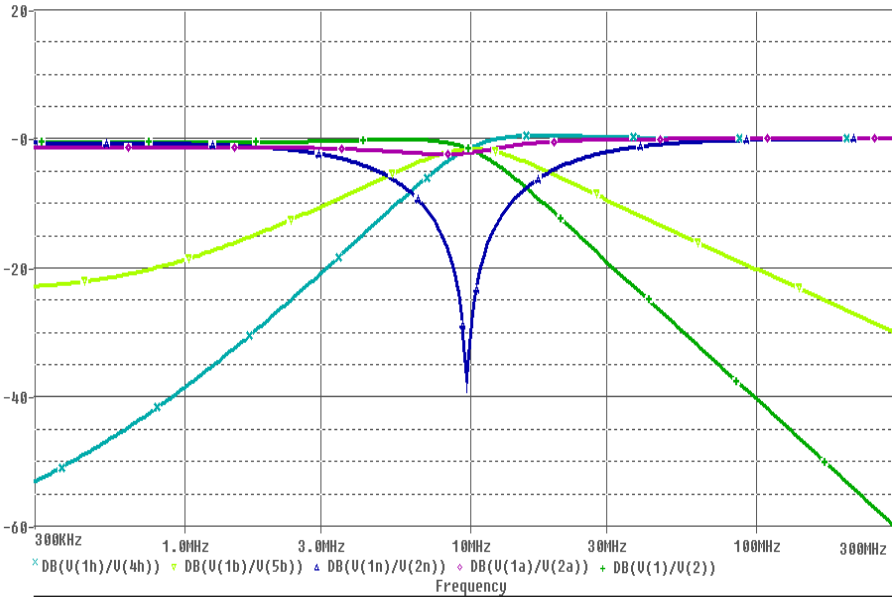

Figure 24 Output of Universal G_m-C Filter

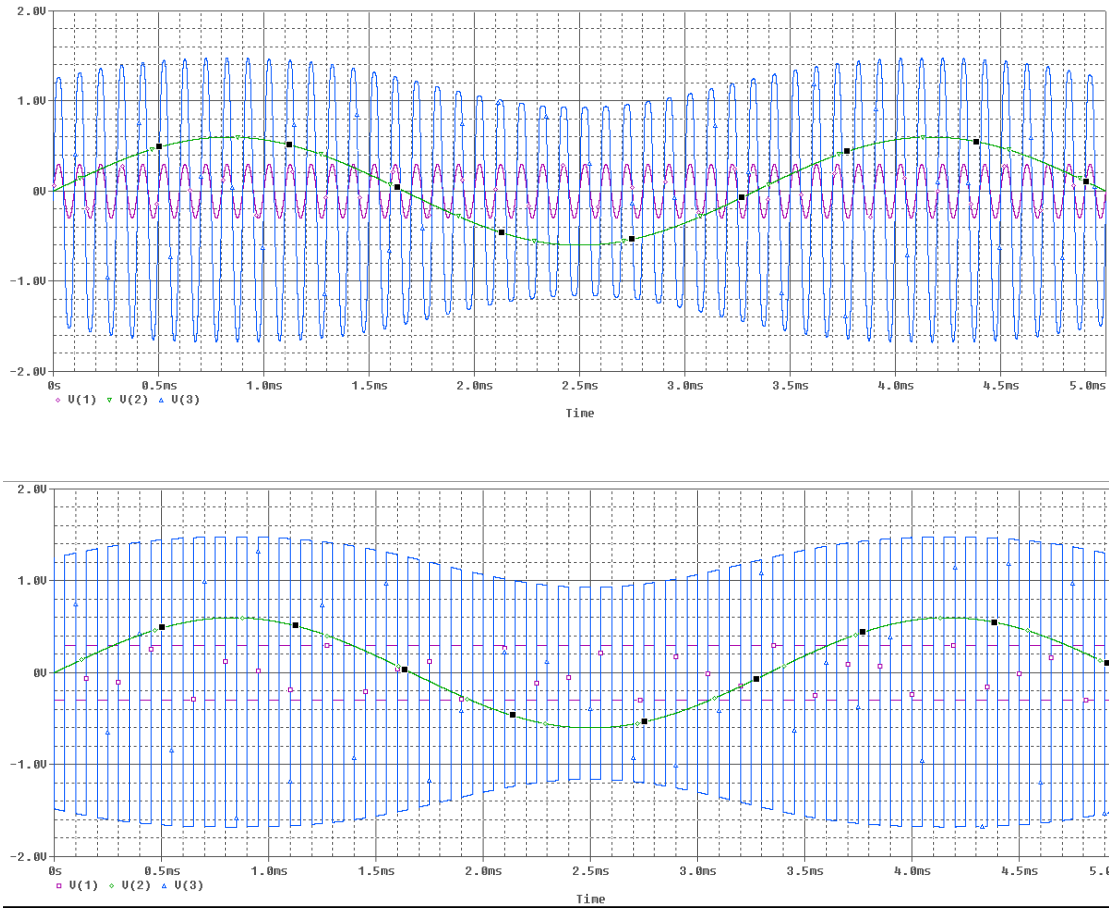

Figure 25. Output Voltage of Multiplier

Conclusion and future Work

Conclusion:

Several different models have been proposed to improve the linearity and harmonic distortion in the OTA transconductance. Mobility compensation accounts for the short channel effect by considering vertical field effect on mobility degradation to improve the linearity. But due to extensive ratio matching of the transistors it is difficult to implement. Common mode gain is high due to PD. The compensation is based on adjusting the aspect ratio which may not be matched to the demand. The calculation involves third harmonics which is very sensitive to process variation. Maintaining V_{ds} at constant value is a difficult task to achieve. CMFB and CMFF used to supress CM signal are complex and consumes significant power and heavily relies on high-resolution current mirrors and good-matching MOSFETS and works upto 97MHz.

Compared with the triode-based OTA, body driven mosfet achieves much better linearity for the same input swing range and shows considerable improvement in linearity and harmonic distortion but the noise is increased due to small g_{mb}.

Tunable OTA is implemented by cascading two Balanced OTAs through an active resistor. The value of resistor is chosen such that the distortion is kept at low level. And the following inferences cab be made:

i. The bandwidth of the tunable OTA is in the range of GHz which makes it suitable for high frequency applications.
ii. The input voltage range and the gain is improved compared to the conventional OTA.
iii. Due to the use of active components it is suitable for IC fabrication.
iv. Because of the linear proportionality of the transconductance it can be tuned linearly using a control voltage.

Application of the tunable OTA has been demonstrated in the form of filters and multiplier.

Future Work:

Tunable OTA has been used to implement filters and multiplier in the presented work, but the area of its utility is very broad and hence a lot of possible work is yet to be done. Tunable OTA can be combined with other concepts like local feedback, bootstrapping etc, to further improve the performance. It can be used to design voltage controlled oscillator as the transconductance can be tuned linearly using the control voltage and hence the frequency.

Neural Networks is one of such fields where it may prove to be beneficial. Because of its high linearity and good input voltage range it is likely to suit the requirements of the weighing element in the circuits and hence can be used to form the CNN cell in such networks.

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Appendix A

S.No	Abbreviations	Expansions
1.	ADC	Analog to digital converter
2.	BOTA	Balanced Operational Transconductance Amplifier
3.	BD	Body Driven
4.	CM	Common Mode
5.	CMFB	Common Mode Feedback
6.	CMFF	Common Mode Feedforward
7.	CMRR	Common Mode Rejection Ratio
8.	CMOS	Complementary Metal Oxide Semiconductor
9.	DAC	Digital to Analog Converter
10.	FB	Feedback
11.	FD	Fully Differential
12.	GB	Gain Bandwidth product
13.	IC	Integrated Circuits
14.	MC	Mobility Compensation
15.	MOSFET	Metal-oxide-semiconductor Field Effect Transistor
16.	OTA	Operational Transconductance Amplifier
17.	PD	Pseudo-differential
18.	RGC	Regulated Gain Control
19.	SR	Slew Rate
20.	TOTA	Tunable Operational Transconductance Amplifier
21.	VCCS	Voltage Controlled Current Source
22.	VCO	Voltage Controlled Oscillator
23.	VCVS	Voltage Controlled voltage Source

Appendix B

Design parameters: W/L ratios of the transistors in Figure 4.3 are as follows:

MOS	W(nm)	L(nm)
M1,M2	7200	180
M3,M4	1080	180
M5,M6	1080	180
M7,M8	1080	180
M2,M2 of current mirror	3960	180

Simulations have been performed using PSPICE at 180nm technology and the model file used have the following parameters:

```
.MODEL NMOS NMOS (                      LEVEL   = 7
+ TNOM    = 27          TOX     = 4.1E-9
+XJ     = 1E-7          NCH     = 2.3549E17     VTH0    = 0.3750766
+K1     = 0.5842025     K2      = 1.245202E-3   K3      = 1E-3
+K3B    = 0.0295587     W0      = 1E-7          NLX     = 1.597846E-7
+DVT0W   = 0            DVT1W   = 0             DVT2W   = 0
+DVT0    = 1.3022984    DVT1    = 0.4021873     DVT2    = 7.631374E-3
+U0     = 296.8451012   UA      = -1.179955E-9  UB      = 2.32616E-18
+UC     = 7.593301E-11  VSAT    = 1.747147E5    A0      = 2
+AGS    = 0.452647      B0      = 5.506962E-8   B1      = 2.640458E-6
+KETA   = -6.860244E-3  A1      = 7.885522E-4   A2      = 0.3119338
+RDSW   = 105           PRWG    = 0.4826        PRWB    = -0.2
+WR     = 1             WINT    = 4.410779E-9   LINT    = 2.045919E-8
+XL     = 0             XW      = -1E-8         DWG     = -2.610453E-9
+DWB    = -4.344942E-9  VOFF    = -0.0948017    NFACTOR = 2.1860065
+CIT    = 0             CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0            ETA0    = 1.991317E-3   ETAB    = 6.028975E-5
+DSUB    = 0.0217897    PCLM    = 1.7062594     PDIBLC1 = 0.2320546
```

```
+PDIBLC2 = 1.670588E-3    PDIBLCB = -0.1          DROUT   = 0.8388608
+PSCBE1  = 1.904263E10    PSCBE2  = 1.546939E-8   PVAG    = 0
+DELTA   = 0.01           RSH     = 7.1           MOBMOD  = 1
+PRT     = 0              UTE     = -1.5          KT1     = -0.11
+KT1L    = 0              KT2     = 0.022         UA1     = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11      AT      = 3.3E4
+WL      = 0              WLN     = 1             WW      = 0
+WWN     = 1              WWL     = 0             LL      = 0
+LLN     = 1              LW      = 0             LWN     = 1
+LWL     = 0              CAPMOD  = 2             XPART   = 0.5
+CGDO    = 6.7E-10        CGSO    = 6.7E-10       CGBO    = 1E-12
+CJ      = 9.550345E-4    PB      = 0.8           MJ      = 0.3762949
+CJSW    = 2.083251E-10   PBSW    = 0.8           MJSW    = 0.1269477
+CJSWG   = 3.3E-10        PBSWG   = 0.8           MJSWG   = 0.1269477
+CF      = 0              PVTH0   = -2.369258E-3  PRDSW   = -1.2091688
+PK2     = 1.845281E-3    WKETA   = -2.040084E-3  LKETA   = -1.266704E-3
+PU0     = 1.0932981      PUA     = -2.56934E-11  PUB     = 0
+PVSAT   = 2E3            PETA0   = 1E-4          PKETA   = -3.350276E-3  )
.MODEL PMOS PMOS (                               LEVEL   = 7
+ TNOM    = 27            TOX     = 4.1E-9
+XJ      = 1E-7           NCH     = 4.1589E17     VTH0    = -0.3936726
+K1      = 0.5750728      K2      = 0.0235926     K3      = 0.1590089
+K3B     = 4.2687016      W0      = 1E-6          NLX     = 1.033999E-7
+DVT0W   = 0              DVT1W   = 0             DVT2W   = 0
+DVT0    = 0.5560978      DVT1    = 0.2490116     DVT2    = 0.1
+U0      = 112.5106786    UA      = 1.45072E-9    UB      = 1.195045E-21
+UC      = -1E-10         VSAT    = 1.168535E5    A0      = 1.7211984
```

+AGS = 0.3806925 B0 = 4.296252E-7 B1 = 1.288698E-6

+KETA = 0.0201833 A1 = 0.2328472 A2 = 0.3

+RDSW = 198.7483291 PRWG = 0.5 PRWB = -0.4971827

+WR = 1 WINT = 0 LINT = 2.943206E-8

+XL = 0 XW = -1E-8 DWG = -1.949253E-8

+DWB = -2.824041E-9 VOFF = -0.0979832 NFACTOR = 1.9624066

+CIT = 0 CDSC = 2.4E-4 CDSCD = 0

+CDSCB = 0 ETA0 = 7.282772E-4 ETAB = -3.818572E-4

+DSUB = 1.518344E-3 PCLM = 1.4728931 PDIBLC1 = 2.138043E-3

+PDIBLC2 = -9.966066E-6 PDIBLCB = -1E-3 DROUT = 4.276128E-4

+PSCBE1 = 4.850167E10 PSCBE2 = 5E-10 PVAG = 0

+DELTA = 0.01 RSH = 8.2 MOBMOD = 1

+PRT = 0 UTE = -1.5 KT1 = -0.11

+KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9

+UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4

+WL = 0 WLN = 1 WW = 0

+WWN = 1 WWL = 0 LL = 0

+LLN = 1 LW = 0 LWN = 1

+LWL = 0 CAPMOD = 2 XPART = 0.5

+CGDO = 7.47E-10 CGSO = 7.47E-10 CGBO = 1E-12

+CJ = 1.180017E-3 PB = 0.8560642 MJ = 0.4146818

+CJSW = 2.046463E-10 PBSW = 0.9123142 MJSW = 0.316175

+CJSWG = 4.22E-10 PBSWG = 0.9123142 MJSWG = 0.316175

+CF = 0 PVTH0 = 8.456598E-4 PRDSW = 8.4838247

+PK2 = 1.338191E-3 WKETA = 0.0246885 LKETA = -2.016897E-3

+PU0 = -1.5089586 PUA = -5.51646E-11 PUB = 1E-21

+PVSAT = 50 PETA0 = 1E-4 PKETA = -3.316832E-3)