DESIGN AND ANALYSIS OF HIGH EFFICIENCY LDMOS POWER AMPLIFIER

A Dissertation Submitted towards the Partial Fulfillment of Award of Degree of

MASTER OF TECHNOLOGY
in
MICROWAVE AND OPTICAL COMMUNICATION ENGINEERING

Submitted by

TUSHAR N. KHARBIKAR
2K09/MOC/15

Under the Supervision of

MR. AVINASH RATRE
Asst. Professor
Department of Electronics & Communication Engineering

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
IN ASSOCIATION WITH
DEPARTMENT OF APPLIED PHYSICS

DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)

Main Bawana Road, Shahabad Daulatapur, New Delhi – 110042
June-2011

CERTIFICATE

This is to certify that the dissertation titled **"Design and Analysis of High Efficiency LDMOS Power Amplifier"** is the bonafide work of Tushar N. Kharbikar (2K09/MOC/15) under our guidance and supervision in partial fulfillment of requirement towards the degree of Master of Technology in Microwave and Optical Communication Engineering from Delhi Technological University, New Delhi.

Mr. Avinash Ratre
Assistant Professor & Supervisor
Electronics and Communication Engineering
Delhi Technological University
Delhi
Date: /06/2011

Dr. Rajiv Kapoor
Head of Department
Electronics and Communication Engineering
Delhi Technological University
Delhi
Date: /06/2011

ACKNOWLEDGEMENT

I would like to take the opportunity to acknowledge my indebtedness towards all the people who have helped me in all my tasks and works.

My sincere gratitude is directed to my supervisor; Mr. Avinash Ratre. He actively involved himself in the project and offered useful support at every stage of my project, reviewed my schematics, answered my all questions and provided me with books and reading material.

I would like to acknowledge my friends and teachers at *Delhi Technological University*, *Delhi* who were kind enough to help me during my course work and teaching me with the best of their knowledge.

To the class of 2009-11, thank you for the very interesting and enjoyable two years!

I owe my loving thanks to my Parents, my brother, my sister and friends. They have supported me very much during my study and research. Without their encouragement and understanding it would have been impossible for me to finish this work.

Thank You all !!

Tushar N. Kharbikar
2K09/MOC/15
M.Tech (Microwave and Optical Communication Engineering)
Department of Electronics and Communication Engineering
Delhi Technological University

Abstract

Linearity and efficiency are the two most important characteristics of RF power amplifier. Both these characteristics are complementary to each other. One characteristic must be achieved in order to achieve other one.

For future Worldwide Interoperability for Microwave Access (WiMAX) application which is intended to work on 3.5GHz frequency, linear power output is needed. To achieve high efficiency with the given output power requirement, Class AB is the only solution seen.

In class AB amplifier, all harmonics are shorted to achieve desired performance. In practice, to achieve shorts at all harmonic frequencies is almost impossible. The most obvious solution for this problem is to tune the harmonics to achieve the desired results.

Class J is one such topology of power amplifier. Here, second harmonic impedance is tuned so that fundamental and second harmonic assist each other to provide desired power output with increased efficiency.

Silicon is cheapest semiconductor material available. Now-a-days, compound semiconductors such as Gallium Nitride (GaN), Gallium Arsenide (GaAs), Silicon Carbide (SiC) are occupying the market of devices for applications in frequency range above 2GHz.

Si-LDMOS technology is promising technology emerged for design of power amplifiers below 1 GHz. Some recent research shows the usefulness of LDMOS technology at 2 GHz.

This work focuses on designing a high efficiency power amplifier for 3.5GHz applications using Si-LDMOS technology. For this, NXP semiconductors' BLF6G38S-25, a 25 W LDMOS power MOSFET is used. Two topologies are designed, Class AB and Class J.

With Class AB amplifier, drain efficiency of 64% and power added efficiency (PAE) of 62.15% is achieved. The output power at this efficiency is 44.8dBm. Power back-off performance is good with PAE of 39.46%. Linearity of this power amplifier is in acceptable limit.

Class J amplifier gives superior performance at same biased level and input power level. Maximum drain efficiency is 69.36% and PAE is 67.36% with output power of 44.7dBm is achieved for input power level of 23dBm. Power back-off performance is also better than corresponding class AB power amplifier with 49.6% PAE at 3dB back-off.

Advanced Design System (ADS) v2008 Update 2 is used as platform for simulations.

Table of Content

Acknowledgement iii

Abstract iv

Table of content v

List of figure viii

List of Table xii

Chapter 1 Introduction 1

1.1 Background 1
1.2 Motivation 2
1.3 Objective 2
1.4 Outline of Thesis 3

Chapter 2 Principle of class A/AB/B/C/D/E/F 4

2.1 Reduced conduction angle power amplifier 4
2.1.1 Class A 5
2.1.2 Class B 7
2.1.3 Class AB 8
2.1.4 Class C 8
2.2 Switching mode power amplifier 9
2.2.1 Class D 9
2.2.2 Class F 11
2.2.3 Class E 12

Chapter 3 RF Power Amplifier Design Parameters 15

3.1 Power Output Capability (C_p) 15
3.2 Power Added Efficiency (PAE) 15
3.3 1-dB compression point ($P_{1\text{-}dB}$) 16
3.4 Intermodulation Distortion (IMD) 16
3.5 Adjacent Channel Power Ratio (ACPR) 17
3.6 Intercept Point (IP) 18
3.7 Amplitude Modulation to Phase Modulation (AM-PM) Conversion 19

Chapter 4 Harmonic Tuned Class-J Power Amplifier 20

4.1 Improvement of the efficiency of power amplifier 20
4.2 Short all the harmonics: Class-AB/B operation 21
4.3 How the harmonics tune the fundamental frequency waveform 22
4.4 Solutions for class-J operation 23
4.5 Sub-optimum class-J operation 29
4.6 Conclusion 34

Chapter 5 Silicon Lateral-Diffused MOSFETs 35

5.1 Device Cell Structure 36
5.2 RF properties of Si-LDMOS 37

Chapter 6 Overview of Advanced Design System 38

6.1 DC Simulation 38
6.1.1 DC Simulation Concept
6.1.2 Simulation Assumptions
6.2 AC Simulation 39
6.2.1 AC Simulation Concept
6.3 S- Parameter Simulation 39
6.4 LSSP Simulation 40
6.4.1 LSSP Simulation Concept
6.4.2 LSSP Simulation Process
6.4.3 Comparing LSSP and S-Parameter Simulations
6.5 Harmonic Balance Simulation 41
6.6 XDB Simulation 42
6.6.1 Gain Compression Concept
6.6.2 Performing a Gain Compression Simulation
6.7 Envelope Simulation 43
6.7.1 Theory of Operation for Circuit Envelope Simulation
6.7.2 When to Use Circuit Envelope Simulation
6.7.3 Advantage over Harmonic Balance:
6.7.4 How to Use Circuit Envelope Simulation

Chapter 7 Simulation and Design 46

7.1 Device Characterization 46
7.1.1 Device Model Used
7.1.2 DC Simulation
7.1.3 AC simulation
7.1.4 Small Signal S-Parameter Simulation

7.1.5 Large Signal S-Parameter Simulation
7.1.6 Stability Analysis
7.2 Input Network Design 51
7.2.1 Input Bias Network
7.2.2 Input Matching Network Design
7.3 Design of Class AB Amplifier 54
7.3.1 Load Pull Analysis
7.3.2 Output Matching Network
7.3.3 Overall Circuit and its Verification
7.3.3.1 Overall Circuit Design
7.3.3.2 Verification
7.4 Design of Class J Amplifier 60
7.4.1 Load Pull Analysis
7.4.1.1 Fundamental Load Pull Simulation
7.4.1.2 Second Harmonic Load Pull Simulation
7.4.2 Output Matching Network
7.4.3 Overall Circuit and its Verification
7.4.3.1 Overall Circuit Design
7.4.3.2 Verification

Chapter 8 Conclusion and Future Work 69

8.1 Conclusion 69
8.2 Future Work 69

References 70

Appendix 72

A: Layout of Class AB amplifier 72
B: Layout of Class J amplifier 73

List of Figures

Figure 2.1: Reduced conduction angle 4
Figure 2.2: Drain voltage and Drain current in class-A operation 5
Figure 2.3: Drain voltage and Drain current of class-B operation 7
Figure 2.4: Drain voltage and Drain current of class-C operation 8
Figure 2.5: The drain efficiency and output power versus conduction angle 8
Figure 2.6: Class-D circuit topology. 9
Figure 2.7: Class-D voltage and current waveforms 9
Figure 2.8: Class-D^{-1} circuit topology 10
Figure 2.9: Class-D^{-1} voltage and current waveforms 10
Figure 2.10: Drain current and voltage of sub-optimum class-F power amplifier 11
Figure 2.11: Third order harmonic shaped waveform 11
Figure 2.12: Square waveform with different number of odd-order harmonics. 12
Figure 2.13: Drain voltage waveform varies with different number of harmonics. 13
Figure 2.14 Table of optimum load for class-E operation harmonics 14
Figure 3.1: 1-dB compression point 16
Figure 3.2: Intermodulation Distortion 17
Figure 3.3 Plot of Adjacent Channel Power 18
Figure 3.4 Plot showing Third Order Intercept Point 18
Figure 4.1: Drain current and voltage of class-AB/B PA 21
Figure 4.2: Drain current and voltage of an ideal switching PA 21
Figure 4.3: Drain voltage and current of class-AB/B 22
Figure 4.4 Phase relation of fundamental and second harmonic waveforms 23
Figure 4.5: The drain current and voltage have reversed phase relation intrinsically. 24
Figure 4.6: The fundamental and second harmonic loads 27
Figure 4.7: The loads of solution 2 28
Figure 4.8 (a) Drain voltage and current waveforms for solution 1of class-J operation 28
Figure 4.8 (b) Drain voltage and current waveforms for solution 2of class-J operation 28
Figure 4.9: the imaginary part of the load shift on the smith chart 30
Figure 4.10: Drain current and voltage waveforms for optimal load 31
Figure 4.11 (a): Drain current and voltage waveforms when the phase angle of fundamental

harmonic load is $\frac{\pi}{5}$ 31

Figure 4.11 (b): Drain current and voltage waveforms when the phase angle of fundamental harmonic load is $\frac{\pi}{3}$ 31

Figure 4.12 (a): The influence of amplitude ratio of fundamental and second harmonic voltage. A/B=9. 32

Figure 4.12 (b): The influence of amplitude ratio of fundamental and second harmonic voltage. A/B=2. 33

Figure 4.12 (c): The influence of amplitude ratio of fundamental and second harmonic voltage. A/B=1. 33

Figure 4.13: Imaginary part of load shifts with frequency (green arrow) 34

Figure 5.1: Power Device family tree 35

Figure 5.2: Lateral-Diffused (LD) MOSFET Structure. 36

Figure 6.1: Gain curve showing x dB compression 42

Figure 6.2: Modulated signal in the time domain 43

Figure 6.3: Extraction of time domain data in frequency domain 43

Figure 6.4: Amplitude and Phase reconstruction 44

Figure 6.5: Time domain to frequency domain conversion using FFT 44

Figure 7.1: I-V curve of BLF6G38S-25 with different drain and gate bias voltage 47

Figure 7.2: Transconductance curve for various values of V_{DS} and for G_m vs V_{GS} for particular V_{DS} 48

Figure 7.3: Simulated S-parameter for frequency range of 3GHz to 4GHz 48

Figure 7.4: S-parameter at 3.5GHz 49

Figure 7.5 Source (Red) and load stability (blue) circle for V_{DS}=28V and frequency range of 3GHz to 4GHz 50

Figure 7.6(a): Stability factor from DC to 10GHz 50

Figure 7.6(b): Zoomed graph of stability factor from 3GHz to 4GHz 50

Figure 7.7: MAG (blue), associated power gain (red) and transducer gain (pink) 51

Figure 7.8: Input bias network design 52

Figure 7.9: V_{GS} as function of potentiometer 52

Figure 7.10: Source pull simulation (marker m3 shows source matching point) 53

Figure 7.11 Input design network 53

Figure 7.12 Return loss of network of figure 7.11 53

Figure 7.13: Input matching network implemented using microstrip line 54

Figure 7.14(a): PAE (red) and power (blue) contours 55
Figure 7.14(b): Drain efficiency 55
Figure 7.14(c): Simulated load impedance from fundamental load pull simulation 55
Figure 7.15 Output matching network 56
Figure 7.16: Simulated load impedance. Fundamental (red), second harmonic (blue) 56
Figure 7.17: Output matching network using microstrip line 57
Figure 7.18: Overall circuit of Class AB amplifier 57
Figure 7.19: Circuit implemented using microstrip line 58
Figure 7.20: PAE and Drain efficiency 58
Figure 7.21: Output power spectrum 58
Figure 7.22: Drain voltage spectrum 58
Figure 7.23: Drain current (red) and voltage (blue) 58
Figure 7.24: AM to AM conversion 59
Figure 7.25: AM to PM conversion 59
Figure 7.26: PAE (red) and gain (blue) for both tones 59
Figure 7.27: Third order IMD 60
Figure 7.28: Fifth order IMD 60
Figure 7.29: Output spectrum and zoomed spectra for centre frequency of 3.5 GHz 60
Figure 7.30(a): PAE (red) and power (blue) contours 61
Figure 7.30(b): Drain efficiency 61
Figure 7.30(c): Simulated load impedance from fundamental load pull simulation 61
Figure 7.31: PAE and Pdel as function of imaginary part of second harmonic load 62
Figure 7.32: Output matching network 63
Figure 7.33: Simulated load impedance. Fundamental (red), second harmonic (blue) 64
Figure 7.34: Output matching network using microstrip line 64
Figure 7.35: Overall circuit of Class J amplifier 65
Figure 7.36: Circuit implemented using microstrip line 65
Figure 7.37: PAE and Drain efficiency 66
Figure 7.38: Output power spectrum 66
Figure 7.39: Drain voltage spectrum 66
Figure 7.40: Drain current (red) and voltage (blue) 66
Figure 7.41: AM to AM conversion 66
Figure 7.42: AM to PM conversion 66
Figure 7.43: PAE (red) and gain (blue) for both tones 67

Figure 7.44: Third order IMD 67
Figure 7.45: Fifth order IMD 67
Figure 7.46: Output spectrum and zoomed spectra for centre frequency of 3.5 GHz 68

List of Tables

Table 1.1: Design goal 3
Table 2.1 Bias point and conduction angle of different classes 4
Table 4.1: Phase angle of fundamental load versus drain efficiency 32
Table 4.2: Ratio of A/B versus drain efficiency 33
Table 7.1: Limiting values of NXP's BLF6G38S-25 model 46
Table 7.2: Large signal S-parameter at 3.5GHz 49
Table 7.3: Small signal S-Parameter data 52
Table 7.4: Impedance presented by output matching network 56
Table 7.5: Impedance presented by output matching network 64

Dedicated to My Family

Chapter 1
Introduction

1.1 Background

During last decade the phenomenal growth of personal wireless communications has made remarkable impacts to modern life. Nowadays billions of people use mobile cellular phones to communicate everyday with the coverage penetrating to massive areas around the whole world. Wireless data networking infrastructures are widely being deployed into public zones to offer wireless computing and internet services through laptops. Accordingly the revolution of communications has also been pushing the evolution of wireless systems and innovation of the internal radio frequency (RF) circuits, including the RF power amplifier (PA).

RF power amplifier is a circuit for converting DC supply power into a significant amount of RF output power. As a critical module in the transmit chain, it is typically the final stage of a wireless transmitter to drive the antenna. The modulated RF signal is amplified by the PA to a nominal power level and then sent through antenna to radiate for propagation.

RF power amplifiers are usually the most power-hungry building blocks in the transceivers (i.e. transmitter plus receiver) of wireless mobile terminals. For instance cellular handsets PA can consume more than 70% of the DC battery power during transmit period. There is increasing demand for highly efficient RF power amplifiers to meet the ever-growing need for power saving, compact and low cost solutions.

Indeed the higher the DC to RF conversion efficiency, the less amount of electrical charge is drawn from the battery for PA to transmit the same amount of RF power. That helps to considerably prolong the battery operation time to satisfy end users. High-efficiency RF PA also reduces the portion of battery power transformed into heat. The result is less stress for the active transistors inside PA and more importantly decreasing heat sink metal and its associated cost.

The ways of pursuing RF power amplifiers with high efficiency, are related to the modulation schemes of communication systems. Mainly there are two existing categories of modulation schemes for personal wireless applications: constant-envelope modulation and non-constant envelope modulation. The constant-envelope modulation schemes have been widely accepted by systems such as Globe System for Mobile Communications (GSM), Bluetooth and RFID. Linearity requirements of a PA are less stringent due to the usage of constant-envelope signals, e.g. GMSK (in GSM). In such a case, a non-linear PA with high efficiency can be considered: it maintains the modulated information while efficiently utilizing the limited battery power resource. In contrast to a linear PA (e.g. class A PA), where output signal amplitude presumably to be linearly controlled by the input signal amplitude, a non-linear PA's output signal is controlled by the phase and frequency information of its modulated input signal.

On the other hand, the non-constant envelope modulation applies to growing wireless systems such as wideband Code Division Multiple Access (WCDMA) and Worldwide

Interoperability for Microwave Access (WiMAX). The used shaped-pulse modulations (e.g. QAM, QPSK) or multiple carriers (OFDM) allow high data rate but occupy wider spectrum bandwidth and need highly linear components, particularly power amplifiers to transmit RF signals with time-varying envelope and phase. In such case a linear PA (typically controlled current sources) is required to lower the inter-modulation and adjacent channel interference of amplified signals. Oftentimes it operates at back-off for adequate linearity. Staying away from its peak input/output power in most of the time, however, wastes the supplied DC bias power designed for the maximum output capability and causes low PA efficiency.

1.2 Motivation

Silicon LDMOS is the basic technology being used up to 1 GHz frequency for design of RF power amplifier. But upper band is captured by other solid state semiconductor technologies. At frequencies more than 2 GHz, compound materials are used to develop active devices. Various work shows successful working of GaN pHEMTs and GaAs HBT with efficiency more than 70% for output power of 2 to 10 W.

Since these technologies are very much costlier, use of these devices increases the cost of instruments where they are used. In order to provide cost effective solution of power amplifier for users, Silicon technology can be used. Silicon has developed base and many foundries are working on improving the properties.

WiMAX is developing technology. Three bands are released for WiMAX as 2.3GHz, 2.5GHz and 3.5GHz. In the USA, the biggest segment available is around 2.5 GHz, and is already assigned, primarily to Sprint Nextel and Clearwire. Elsewhere in the world, the most-likely bands used will be the Forum approved ones, with 2.3 GHz probably being most important in Asia. Some countries in Asia like India and Indonesia will use a mix of 2.5 GHz, and 3.5 GHz. Pakistan's Wateen Telecom uses 3.5 GHz.

Class AB amplifier provides good compromise between linearity and efficiency. But to achieve this, it is necessary to present short for all harmonics at drain terminal. This is difficult to achieve in practical design. The solution for this is to use harmonic tuned amplifier. Here, the harmonic impedance are tuned in such way to increase the efficiency while maintaining the linearity.

All these facts leads to the objective of this project work.

1.3 Objective

The main objective of this project work is to design a highly efficient radio frequency power amplifier to be used in future WiMAX application. Two amplifiers are intended to design. One is Class AB amplifier and another is Class J amplifier

Si-LDMOS technology is used for active device. Another objective is to evaluate the possibility of using this technology at higher frequency band.

Table 1.1 shows the design goal established for this work

	Class AB	Class J
Output power	44dBm	44dBm
Power Added Efficiency	More than 60%	More than 65%
Drain efficiency	More than 60%	More than 65%
Efficiency at 3dB power back off	More than 45%	More than 50%

Table 1.1: Design Goal

1.4 Outline of Thesis

- Chapter 2 presents the working principle of different classes of power amplifier
- Chapter 3 gives brief overview of performance parameters on which power amplifier are characterized
- Chapter 4 gives detailed study of Class J amplifier
- Chapter 5 describes physical structure of Silicon Lateral Diffused MOSFET in detail with some description on RF properties of Si-LDMOS
- Chapter 6 presents description of simulation components present in Advanced Design System EM design software
- Chapter 7 contains the design of class AB and class J amplifier and simulation results
- Chapter 8 summarizes whole thesis with some points on future work.

Chapter 2
Principle of class A/AB/B/C/D/E/F

In this chapter, the principles of some basic operation classes of power amplifiers.

Operation classes for power amplifiers:

For different ways of device operation, people classify the power amplifiers to different classes. Class A/AB/B/C can be classified to one category. When the power amplifier operates at class A/B/C/AB, the transistor operates like a current source. Class D/E/F/J can be classified to another category. In these classes the transistor operates like a switch.

2.1 Reduced conduction angle power amplifier

Let's first talk about the class A/B/C/AB power amplifier. The difference of these classes is the conduction angle (figure 2.1).

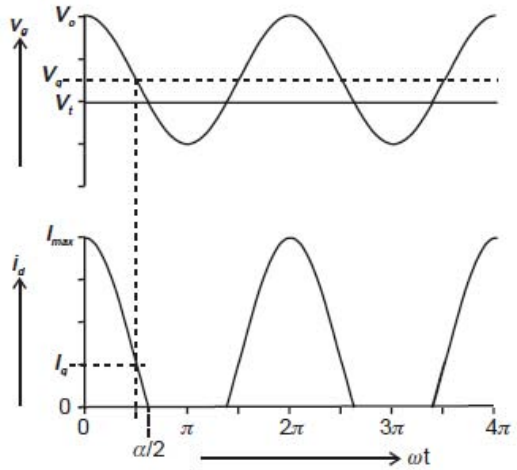


Figure 2.1: Reduced conduction angle when operating as a power amplifier' α' represents the conduction angle of power amplifier [1]

Class	Gate bias point	Current	Conduction angle
A	0.5	0.5	2pi
AB	0-0.5	0-0.5	Pi-2pi
B	0	0	pi
C	<0	0	0-pi

Table 2.1 Bias point and conduction angle of different classes (the signal voltage and current swing are normalized to 1) [1]

2.1.1 Class A:

From these classes, class-A has the highest linearity and the transistor is equivalent to a current source. The drain current and voltage waveforms of class-A operation are given in figure 2.2:

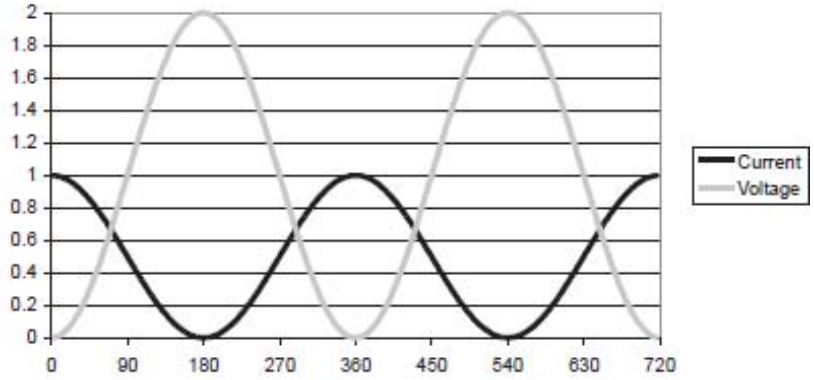


Figure 2.2: Drain voltage and Drain current in class-A operation [1]

In order to enable the power amplifier operate in its linear region, the amplifier's gate and drain bias voltage should be chosen properly. The swing of the drain current for class-A operation should be between zero and Imax (with I_{max} being the saturation current of the transistor.). The swing of the drain voltage should be between zero and breakdown voltage of the device. The conduction angle is 2π for class-A operation means the device is on all the times. It also means that the device loses power all the times.

Let's calculate the maximum efficiency and output power of class-A operation:

The drain current for an amplifier with reduced conduction angle:

$$i_d(\theta) = I_q + I_{pk}\cos\theta \ , -\alpha / 2 < \theta < \alpha/2;$$

$$= 0, -\pi < \theta < -\alpha/2; \ -\alpha/2 < \theta < \pi \qquad [1] \qquad (2.1)$$

where $i_d(\theta)$ is the drain current, I_q is the quiescent current, I_{pk} is the amplitude of drain current, I_{max} is the peak value of drain current, α is the conduction angle.

$$\cos(\alpha/2) = -\frac{I_q}{I_{pk}} \text{ and } I_{pk} = I_{max} - I_q \qquad (2.2)$$

So,

$$id(\theta) = \frac{I_{max}}{1-\cos(\alpha/2)}(\cos\theta - \cos(\alpha/2)) \qquad (2.3)$$

The DC component is as follows:

$$I_{dc} = \frac{1}{2\pi}\int_{-\alpha/2}^{\alpha/2}\frac{I_{max}}{1-\cos(\alpha/2)}(\cos\theta - \cos(\alpha/2))\,d\theta$$

$$= \frac{I_{max}}{2\pi} \frac{2\sin(\alpha/2) - \alpha\cos(\alpha/2)}{1-\cos(\alpha/2)} \quad (2.4)$$

The magnitude of nth harmonic is:

$$I_n = \frac{1}{\pi}\int_{-\alpha/2}^{\alpha/2} \frac{I_{max}}{1-\cos(\alpha/2)}(\cos\theta - \cos(\alpha/2))\cos n\theta \, d\theta \quad (2.5)$$

The fundamental harmonic component of drain current is:

$$I_1 = \frac{I_{max}}{2\pi} \frac{\alpha - \sin\alpha}{1-\cos(\alpha/2)} \quad (2.6)$$

For class-A operation, the conduction angle is 2π. So, the dc component of drain current is:

$$I_{dc}(class\ A) = \frac{I_{max}}{2} \quad (2.7)$$

The fundamental harmonic component of drain current:

$$I_1(class\ A) = \frac{V_{max}}{2} \quad (2.8)$$

The DC and fundamental harmonic component of drain voltage:

$$V_{dc}(class\ A) = \frac{V_{max}}{2} \quad (2.9)$$

$$V_1(class\ A) = \frac{V_{max}}{2} \quad (2.10)$$

The DC dissipation power of class-A operation power amplitude:

$$P_{dc} = V_{dc}I_{dc} = \frac{V_{max}I_{max}}{4} \quad (2.11)$$

The output power for class-A operation:

$$P_{out} = \frac{1}{2}V_1I_1 = \frac{V_{max}I_{max}}{8} \quad (2.12)$$

The maximum drain efficiency of class-A operation:

$$\eta = \frac{P_{out}}{P_{dc}} = \frac{1}{2} = 50\% \quad [1] \quad (2.13)$$

So, for class-A operation, the maximum drain efficiency 50%.

2.1.2 Class B:

The class-B amplifier has half-sine drain current waveform and the drain voltage waveform is full-sine wave. Obviously, the overlap of the drain current and voltage is less, which means the dc power dissipation is less and therefore its efficiency is higher. However, the linearity of class-B operation is not as good as class-A operation.

The voltage and current waveform of class-B amplifier is in figure 2.3:

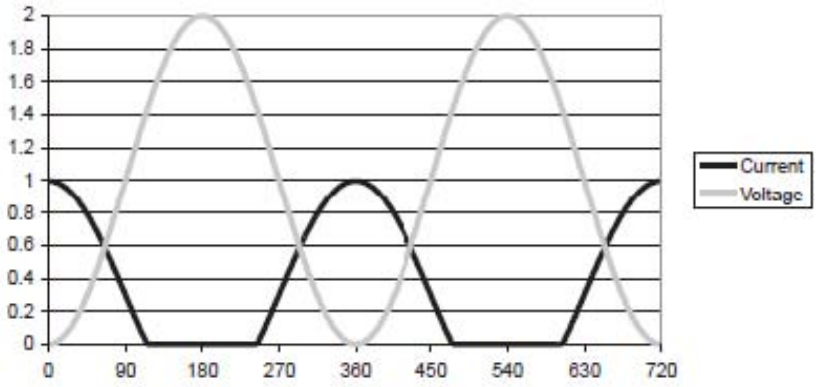


Figure 2.3: Drain voltage and Drain current of class-B operation [1]

The efficiency of class-B operation:

From equations (2.4) to (2.6), we can obtain the dc and fundamental harmonic components of drain current. The conduction angle of class-B operation is π.

$$I_{dc}(class\ B) = \frac{I_{max}}{\pi} \qquad [1] \qquad (2.14)$$

$$I_1(class\ B) = \frac{I_{max}}{2} \qquad (2.15)$$

The dc and fundamental harmonic components of drain voltage:

$$V_{dc}(class\ B) = \frac{V_{max}}{2} \qquad (2.16)$$

$$V_1(class\ B) = \frac{V_{max}}{2} \qquad (2.17)$$

The dc and output power:

$$P_{dc} = V_{dc}I_{dc} \qquad (2.18)$$

$$P_{out} = \frac{1}{2}\ I_1V_1 \qquad (2.19)$$

The maximum drain efficiency for class-B operation:

$$\eta = \frac{P_{out}}{P_{dc}} = \frac{\pi}{4} \approx 78.5\% \qquad [1] \qquad (2.20)$$

The theoretical maximum class-B operation is 78.5%.

2.1.3 Class AB:

Class-AB is a compromise between class A and B. The conduction angle for class-AB operation is between π and 2π. The larger the conduction angle is typically the better the linearity is, but the lower the efficiency is, and vice versa. So, the theoretical maximum drain efficiency is between 50% and 78.5%.

2.1.4 Class C:

In class-C operation the conduction angle is between 0 and π. By using equation (2.4) to (2.6), we can calculate the drain efficiency of class-C operation. It isn't a constant and depends on the conduction angle. If the conduction angle is 0, theoretically we can obtain 100% drain efficiency. However, this also means that there is no power deliver to the load. So, 0^o conduction angle is meaningless. In this class of operation we need to make a trade-off between efficiency and output power. The lower the conduction angle is, the higher the efficiency is and less output power is.

The waveforms of class-C operation:

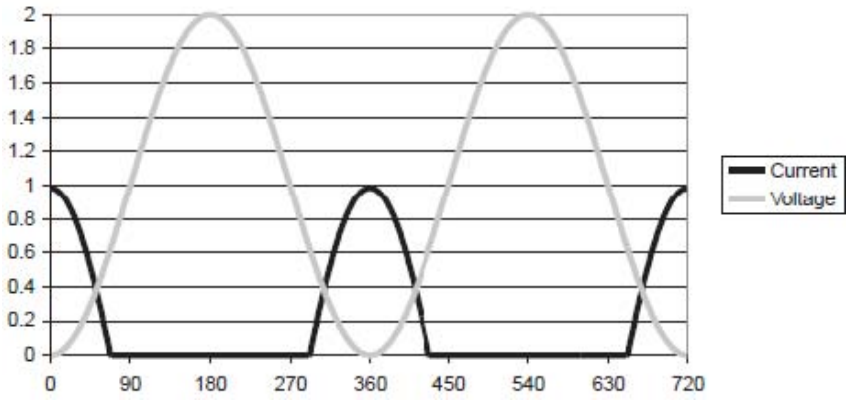


Figure 2.4: Drain voltage and Drain current of class-C operation [1]

The drain efficiency and output power versus conduction angle (figure 2.5):

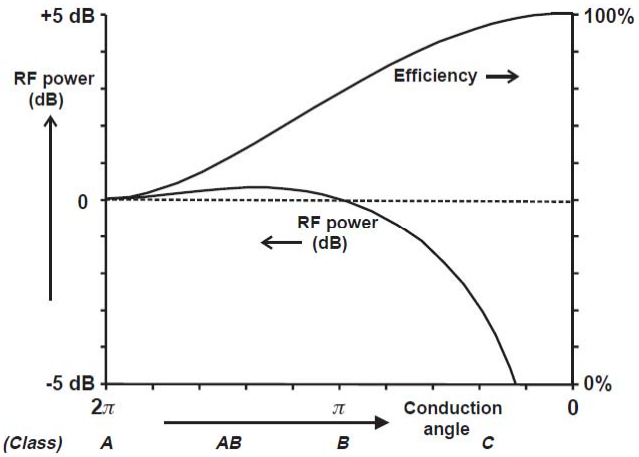


Figure 2.5: The drain efficiency and output power versus conduction angle [1]

2.2 Switching mode power amplifier

Class-D, class-E and class-F power amplifiers are switching mode power amplifier. The transistor acts like a switch. The theoretical maximum drain efficiency for these classes can be as high as 100%. However, due to the non-ideal conditions of device (limited switching time, parasitic and etc), 100% drain efficiency is difficult to reach [2]. Comparing with class-C operation, class-E and class-F power operation don't need to make a compromise between efficiency and output power.

2.2.1 Class D

The class-D power amplifier (or voltage mode class-D VMCD) is the only class which requires two transistors working out of phase 180^{o}. The circuit topology is shown in figure 2.6; the load network has a series resonant circuit to pass the current at the fundamental frequency to the load and to block all other current components. Hence the voltage and current waveforms are a square (odd component) and sinusoidal (even component) waveforms, respectively, see figure 2.7.

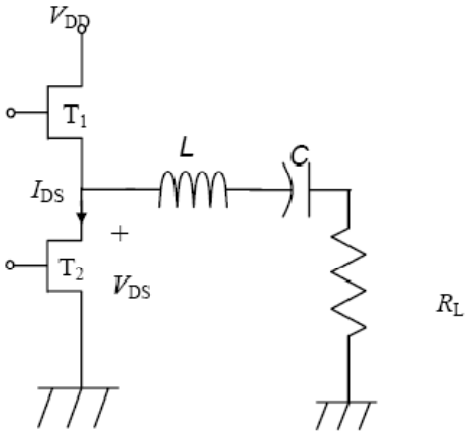


Figure 2.6: Class-D circuit topology.

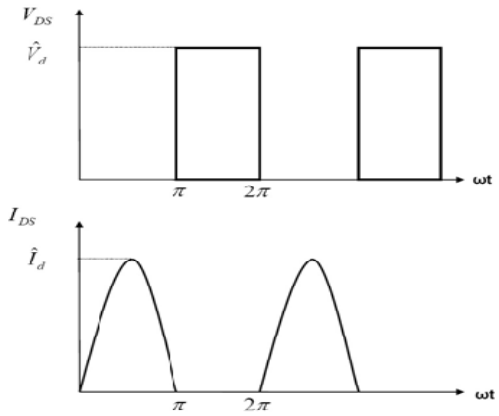


Figure 2.7: Class-D voltage and current waveforms.

There is another class which is complementary to class-D called D^{-1} (or current mode class-D CMCD). Its circuit topology could be as the circuit shown in figure 2.8. The class-D^{-1} load network has a parallel resonant circuit with the load to pass the fundamental frequency and to short the odd harmonics. This topology allows the current to have square waveform and the voltage sinusoidal waveform as shown in figure 2.9. This class has an advantage over class-D, in that it can tune out the transistor output capacitance, which comes from grounding the source in both transistors, and include it as a part of the resonant circuit. Therefore, we can still achieve high efficiency, but not 100% due to the knee region. Also, class-D PA may exceed the breakdown voltage for T1 in figure 2.6, because its source terminal is not grounded

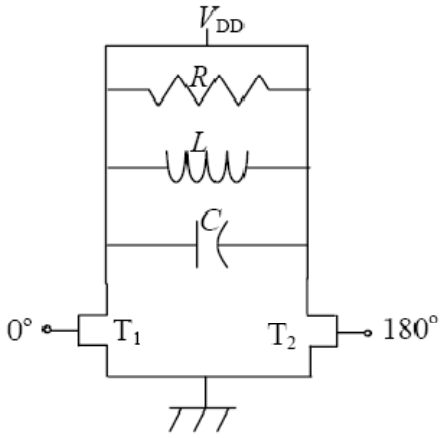


Figure 2.8: Class-D^{-1} circuit topology.

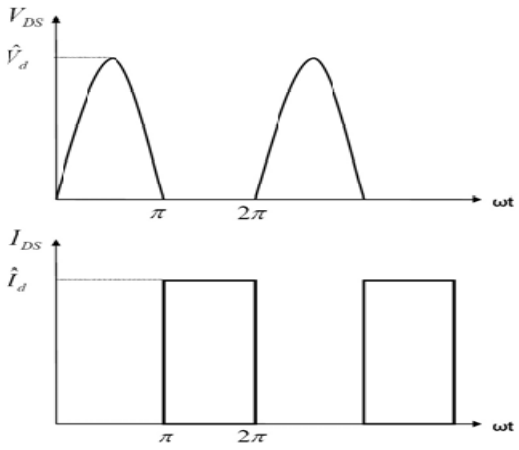


Figure 2.9: Class-D^{-1} voltage and current waveforms.

Another reason of degrading the efficiency from the theoretical value is the transistor output capacitance which is significant at high frequency, is large due to the size required for the high output power application. The susceptance of the output capacitance is very high for the high frequency and cannot be ignored (i.e.; Y=jB=jωCds). Also another reason of not achieving the theoretical efficiency is that the transistors do not work as ideal switches, which can be toggled between ON state and OFF state instantaneously. Within the finite turn-on and turn-off time, the voltage and the current overlap, and cause the transistor losses (switching loss). This drawback is addressed in the time domain design and analysis in Class-E amplifiers.

2.2.2 Class F:

For an ideal class-F power amplifier, the voltage waveform should be an ideal square waveform. When the transistor on, the drain voltage is zero. In other words, the drain voltage is shaped to minimize the overlap of drain voltage and current. However, normally the ideal square waveform condition is hard to meet and drain voltage waveform is a sub-optimum square waveform. The waveforms of sub-optimum class-F power amplifier are:

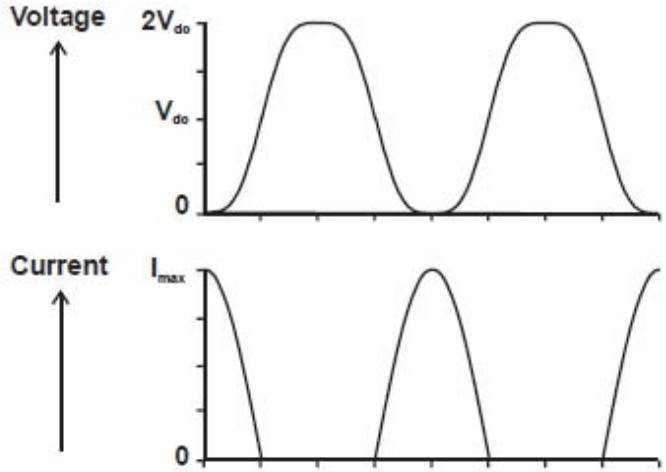


Figure 2.10: Drain current and voltage of sub-optimum class-F power amplifier

The square waveform only contains odd-order harmonics. There are three factors which influent the shape of waveform.

1. The phase relations between fundamental and higher order harmonics. For ideal square waveform, the peak of fundamental and the valleys of higher order harmonics should be synchronized.
2. The amplitude relations of fundamental and higher order harmonics.

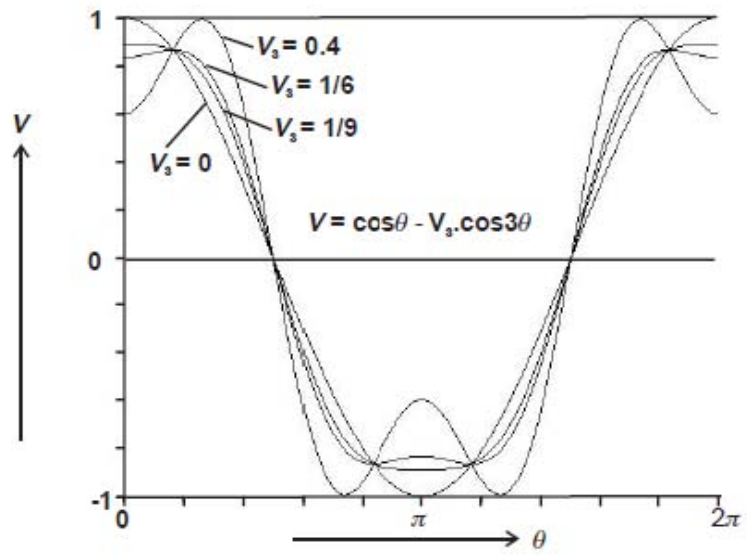


Figure 2.11: Third order harmonic shaped waveform (different amplitude of third harmonic) [1]

The fundamental harmonic is:

$$V_1 = \cos\theta \quad [1] \qquad (2.21)$$

The third harmonic is:

$$-V_3 \cos(3\theta) \qquad (2.22)$$

The superimposition of these two harmonics:

$$V = \cos\theta - V_3 \cos(3\theta) \qquad (2.23)$$

The amplitude ratio of fundamental and third harmonic is very important too. As shown in figure 2.11, when the ratio is 1/6, the superimposition waveform is very flat. When the ratio is less than 1/9, the superimposition is still looks like a sinusoid.

3. The number of harmonics:

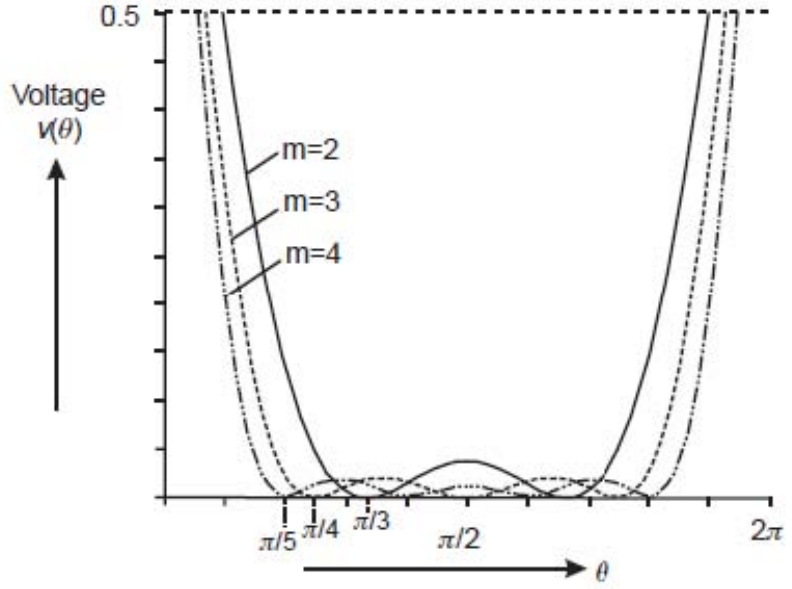


Figure 2.12: Square waveform with different number of odd-order harmonics. m represents the number of odd-order harmonics [1]

We can see from figure 2.8 that when the number of odd-order harmonics increases, the waveform becomes more and more like an ideal square waveform.

So, with finite number of harmonics or other non-ideal conditions, the efficiency of class-F power amplifier drops from theoretical value of 100%

2.2.3 Class E:

Class-E power amplifier is also a kind of switching mode amplifier. For an ideal class-E operation, three requirements for drain voltage and current should be meet [2]:

1. The rise of the voltage cross the transistor at turn-off should be delayed until after the transistor is off.
2. The drain voltage should be brought back to zero at the time of transistor turn-on.
3. The slope of the drain voltage should be zero at the time of turn-on.

These conditions can only be met by controlling an infinite number of harmonics. When the number of harmonics is limit, the efficiency drops from theoretical value of 100% and we call that kind of operation sub-optimum class-E. The drain voltage waveform varies with different

number of harmonics are shown in figure 2.13.

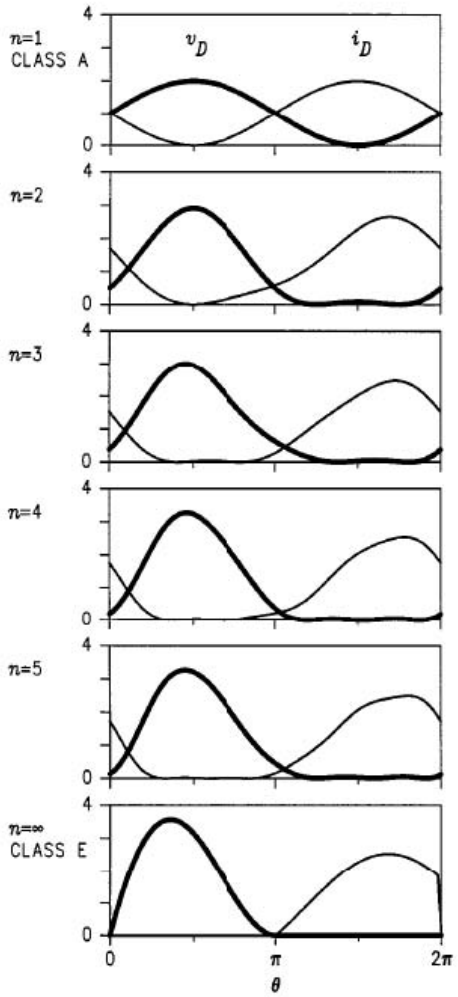


Figure 2.13: Drain voltage waveform varies with different number of harmonics. n represents the number of harmonics [3]

When the harmonic number is 2, the drain voltage only contains fundamental and second harmonic components. We call it class-J operation. The detail discussion on class-J operation is in later chapter. So, class-J is also a kind of sub-class E operation. When the number of harmonic increases to infinite, there is no overlap of drain voltage and current (figure 2.13) and 100% efficiency can be achieved. However, in practical situations, it's a very hard task due to the existence of on resistor or other parasitics of the transistors. Basically, the class-E power amplifier we call is in sub-class E operation.

The equations to calculate the optimum fundamental load for class-E operation:

$$R = \frac{0.58\times V_{dd}^2}{P_{out}} \tag{2.24}$$

The table of optimum harmonics load for ideal class-E operation [3]:

k	$\lvert V_k \rvert$	$\lvert I_k \rvert$	Z_k for R=1	Z_k for R_1=1
0	1.000	0.5762		
1	1.639	0.8691	1.5260 + j1.1064	1 + j0.725
2	0.8477	0.3120	−j2.7233	−j1.7846
3	0.2222	0.1224	−j1.8155	−j1.1897
4	0.1433	0.1056	j1.3616	−j0.8923
5	0.08001	0.07344	−j1.0893	−j0.7138
6	0.05907	0.06536	−j0.9038	−j0.5923
7	0.04082	0.05246	−j0.7781	−j0.5099
8	0.03236	0.04774	−j0.6778	−j0.4448
9	0.02470	0.04081	−j0.6052	−j0.3966
10	0.02045	0.03773	−j0.5420	−j0.3552

Figure 2.14 Table of optimum load for class-E operation harmonics

Chapter 3

RF Power Amplifier Design Parameters

Overview

The RF power amplifier (PA), a critical element in transmitter units of communication systems, is expected to provide a suitable output power at a very good gain with high efficiency and linearity. The output power from a PA must be sufficient for reliable transmission. High gain reduces the number of amplifier stages required to deliver the desired output power and hence reduces the size and manufacturing cost. High efficiency improves thermal management, battery lifetime and operational costs. Good linearity is necessary for bandwidth efficient modulation. However these are contrasting requirements and a typical power amplifier design would require a certain level of compromise. There are several types of power amplifiers which differ from each other in terms of linearity, output power or efficiency. Parameters which quantify the various aspects of amplifier performance such as 1-dB compression point, input intercept point, intermodulation distortion, power output capability, power added efficiency and adjacent channel power ratio are discussed in this chapter.

3.1 Power Output Capability (C_p)

The power output capability, C_p, is defined as the RF output power produced when the device has a peak drain voltage of 1 volt and a peak drain current of 1 ampere [3]. This is a unit less quantity. If the power amplifier uses two or more transistors, then the number of transistors is included in the denominator.

If P_0 is the RF output power, $I_{d,\,pk}$ is the peak drain current, $V_{d,\,pk}$ is the peak drain voltage and N is the number of transistors, then

$$C_P = \frac{P_0}{N I_{d,pk} V_{d,pk}} \tag{3.1}$$

Usually the power output capability of a Class A amplifier is the highest since it is operated at the centre of the load line allowing room for maximum voltage and current swings. Based on this, another parameter called the power utilization factor (PUF) is defined as the ratio of RF power delivered by a device in a particular mode to the power delivered by operating the device as a Class A amplifier.

3.2 Power Added Efficiency (PAE)

Efficiency or drain efficiency is simply defined as the ratio of output power at the drain to the input power supplied to the drain by the dc supply.

$$\eta_d = \frac{P_0}{P_{dc}} \tag{3.2}$$

Drain efficiency is usually not enough to characterize RF power amplifier performance. This is due to the substantial RF power at the input of the amplifier, especially in amplifiers with low gain. Power added efficiency (PAE) includes the effect of input drive power and is defined as:

$$PAE = \frac{P_0 - Pdrive}{P_{dc}} \quad (3.3)$$

3.3 1-dB compression point ($P_{1\text{-dB}}$)

When a power amplifier is operated in its linear region, the gain is a constant for a given frequency. However when the input signal power is increased, there is a certain point beyond which the gain is seen to decrease. The input 1-dB compression point is defined as the power level for which the input signal is amplified 1 dB less than the linear gain. The 1-dB compression point can be input or output referred and is measured in terms of dBm. A rapid decrease in gain will be experienced after the 1-dB compression point is reached. This gain compression is due to the non-linear behaviour of the device and hence the 1-dB compression point is a measure of the linear range of operation.

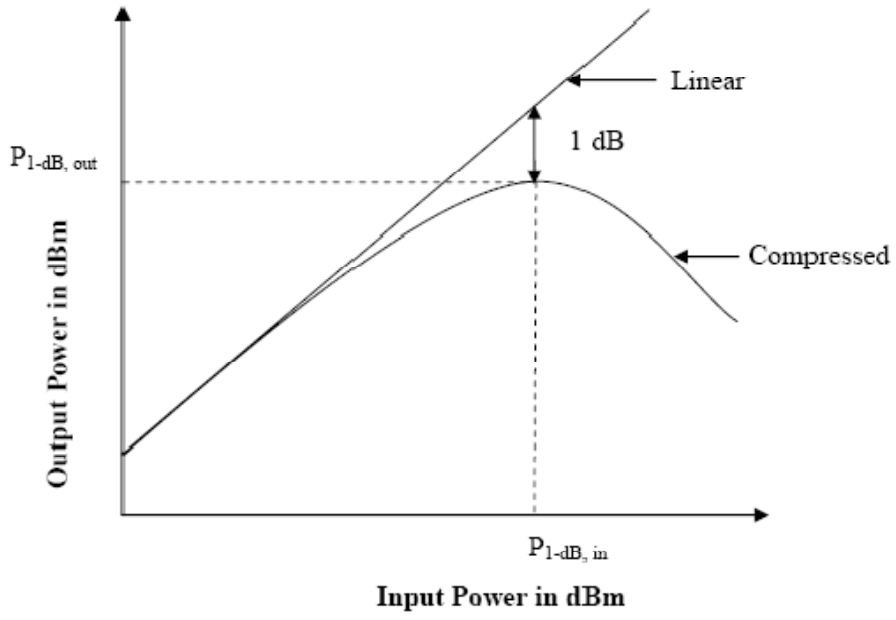


Figure 3.1: 1-dB compression point

3.4 Intermodulation Distortion (IMD)

Intermodulation distortion is a nonlinear distortion characterized by the appearance, in the output of a device, of frequencies that are linear combinations of the fundamental frequencies and all harmonics present in the input signals [1]. A very common procedure to measure the

intermodulation distortion is by means of a two-tone test. In a two-tone test a nonlinear circuit is excited with two closely spaced input sinusoids. This would result in an output spectrum consisting of various intermodulation products in addition to the amplified version of the two fundamental tones and their harmonics. If f_1 and f_2 are the fundamental frequencies then the intermodulation products are seen at frequencies given by

$$f_{IMD} = mf_1 \pm nf_2 \tag{3.4}$$

where m and n are integers from 1 to ∞.

The ratio of power in the intermodulation product to the power in one of the fundamental tones is used to quantify intermodulation. Of all the possible intermodulation products usually the third order intermodulation products (at frequencies $2f_1$-f_2 and $2f_2$-f_1) are typically the most critical as they have the highest strength. Furthermore they often fall in the receiver pass band making it difficult to filter them out.

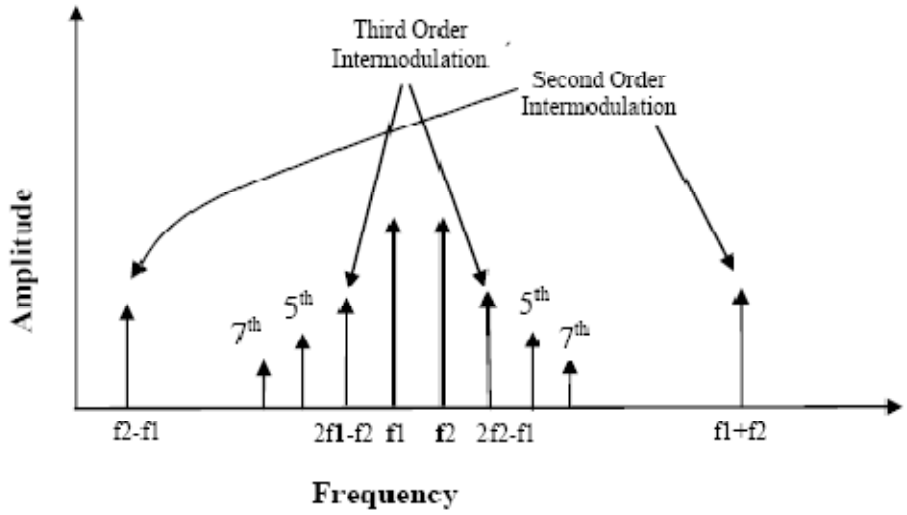


Figure 3.2: Intermodulation Distortion

3.5 Adjacent Channel Power Ratio (ACPR)

In many modern communication systems, the RF signal typically has a modulation band that fills a prescribed bandwidth on either side of the carrier frequency. Similarly the intermodulation products also have a bandwidth associated with them. The IM bandwidth is three times the original modulation band limits for third order products, five times the band limits for fifth order products and so on. Thus the frequency band of the intermodulation products from the two tones stretches out, leading to leakage of power in the adjacent channel. This leakage power is referred to as adjacent channel power. The adjacent channel power ratio (ACPR) is the ratio of power in the adjacent channel to the power in the main channel. ACPR values are widely used in the design of power amplifiers to quantify the effects of intermodulation distortion and hence also serve as a measure of linearity.

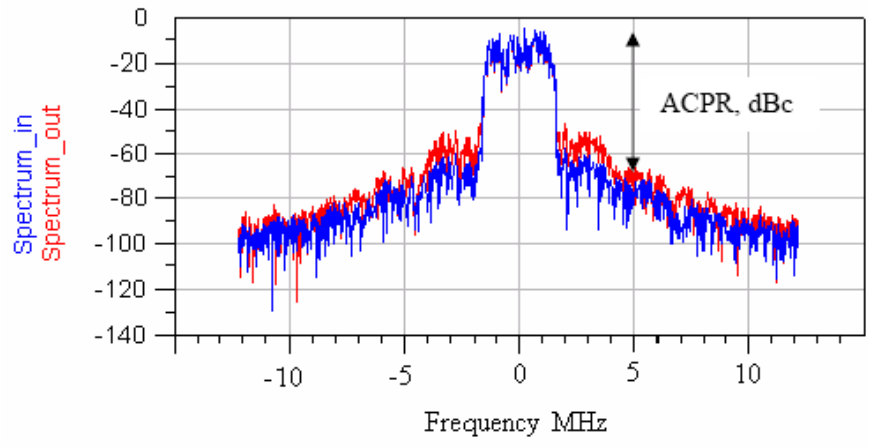


Figure 3.3 Plot of Adjacent Channel Power

3.6 Intercept Point (IP)

The intercept point is the point where the slope of the fundamental linear component meets the slope of the intermodulation products on a logarithmic chart of output power versus input power. Intercept point can be input or output referred. Input intercept point represents the input power level for which the fundamental and the intermodulation products have equal amplitude at the output of a nonlinear circuit. In most practical circuits, intermodulation products will never be equal to the fundamental linear term because both amplitudes will compress before reaching this point. In those cases intercept point is measured by a linear extrapolation of the output characteristics for small input amplitudes. Since the third order intermodulation products, among the IM products, are of greatest concern in power amplifier design, the corresponding intercept point called the third order intercept point (IP3) is an important tool to analyze the effects of third order nonlinearities. In fact intercept point serves as a better measure of linearity in comparison to intermodulation products as it can be specified independent of the input power level [1].

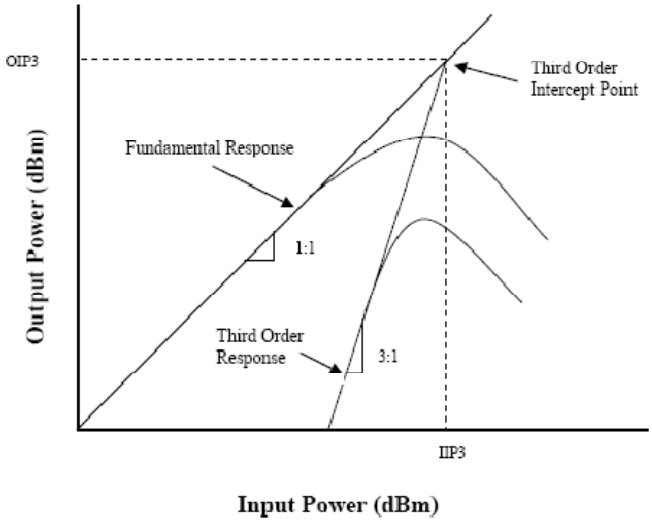


Figure 3.4 Plot showing Third Order Intercept Point

3.7 Amplitude Modulation to Phase Modulation (AM-PM) Conversion:

An amplifier driven under strongly nonlinear conditions produces phase distortion in addition to amplitude distortion. The phase distortion is a serious problem in systems with phase modulation such as QPSK. This phase distortion is characterized by AM-PM conversion which is defined as the change in phase of the output signal when the drive level at the input is increased toward and beyond the compression point. The AM-PM effects are usually caused by the storage elements in the circuit like the gate-source junction capacitances and parasitics associated with inductors under nonlinear conditions.

Chapter 4
Harmonic Tuned Class-J Power Amplifier

In the previous chapters, the principles of operation of classes for power amplifiers and their performance parameters are discussed. In this chapter, the principles of class-J operation will be discussed. The definition of class-J operation is use of a second harmonic termination to tune the shape of drain voltage waveform. In this way, the performance of power amplifier can be improved. More details are discussed in following sections.

4.1 Improvement of the efficiency of power amplifier

When a power amplifier is designed, efficiency (drain efficiency, PAE) is an important performance. The equation for calculating the drain efficiency is:

$$Drain\_eff = \frac{P_{fund}}{P_{dc}} \tag{4.1}$$

Drain_eff represents the drain efficiency. P_{fund} and P_{dc} represent fundamental harmonic power and DC power respectively.

From the equation 4.1, it can be found that there are two ways to improve the efficiency performance.

(1) One is to increase the fundamental harmonic power. This means that all the output power should be at the fundamental frequency and there is no power dissipation at higher order harmonics. So, even if the harmonics are used to tune the waveform of drain voltage or drain current, the higher order harmonics' loads (higher than order 2) should be pure reactive. However, because of some parasitic resistance of the device, there is always some loss of at these higher order harmonics. But, this loss is typically small compared with the fundamental harmonic power. So, what is needed to do is to keep all the higher order harmonics' loads reactive to minimize this loss.

(2) The second way to improve the efficiency is to minimize the dc power dissipation. The DC power is as follow:

$$P_{dc} = \frac{1}{T}\int I_d \times V_d dt \tag{4.2}$$

From equation 4.2, it can be deduced that to reduce the DC power dissipation, the product of current and voltage needs to be reduced, consequently the overlap of the drain current and voltage should be made as low as possible at all times (Figure 4.1 and 4.2):

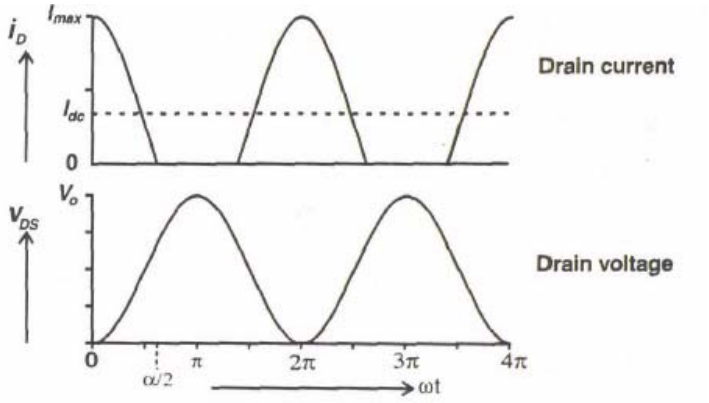


Figure 4.1: Drain current and voltage of class-AB/B PA

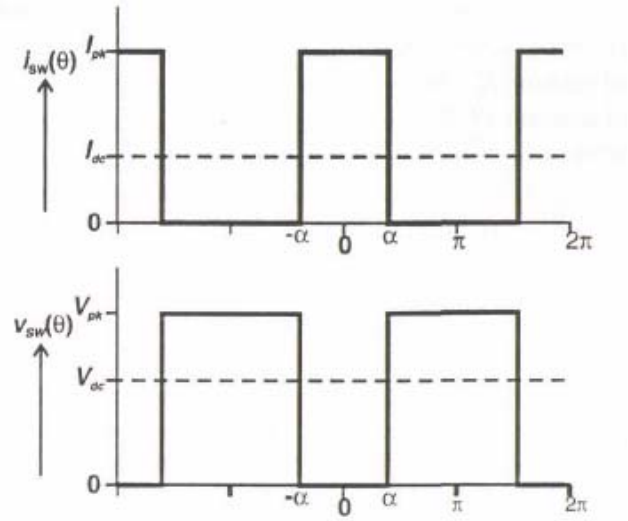


Figure 4.2: Drain current and voltage of an ideal switching PA [1]

By applying the Fourier transform to the waveform in figure 4.1, the DC components of drain current and voltage is obtained. If the current and voltage are both high across the active device, DC components always exist at the same time and there will be power dissipation. Note that in figure 4.2, the ideal switching mode power amplifier has no drain current and voltage simultaneous, that means there is no power dissipation. All the DC power is transformed to signal power. For this ideal switching PA, the efficiency is 100%. But, this kind of PA is not easy to realize, so the harmonics can be used to tune the waveform in figure 4.1 and make the overlap of drain current and voltage as small as possible.

4.2 Short all the harmonics: Class-AB/B operation:

Before investing in the influence of harmonics on the efficiency performance of power amplifier, first study the operation of class-AB/B. For class-AB/B power amplifier, all the harmonics are shorted except the fundamental harmonic. The drain current and drain voltage of class-AB/B power amplifier are as follow:

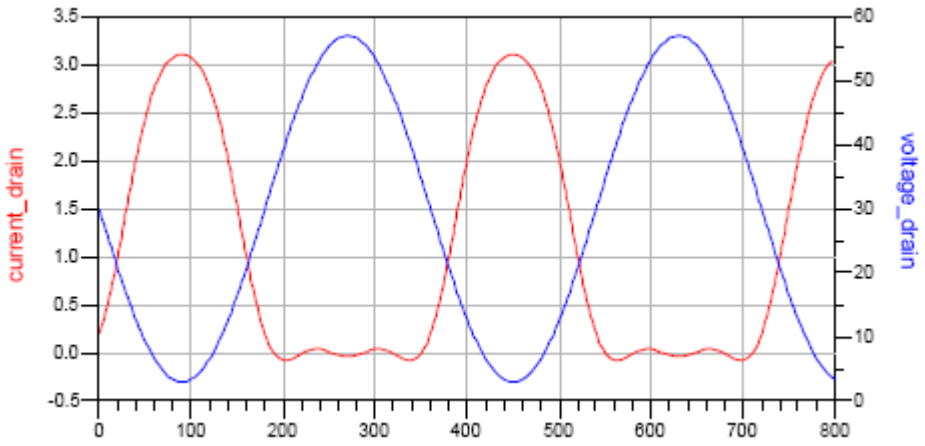


Figure 4.3: Drain voltage and current of class-AB/B operation (blue, drain voltage, red, drain current. X axis is phase of waveforms in degrees. Y axis is in Amperes and volts for current and voltage respectively)

The drain current of the class-AB/B power amplifier is half-sine wave. The equation for the half-sine wave is as follow:

$$half\_\sin(\theta) = 1 + \frac{\pi}{2} \times \sin(\theta) + \sum_{n=1}^{\infty} -2 \times \frac{1}{n^2-1} \times \cos(n\theta), n = 2K, \forall n, k \epsilon N \text{ [6]} \qquad (4.3)$$

Here all the currents are normalized to the DC component. So, the DC current equals 1, the amplitude of fundamental harmonic current will be $\frac{\pi}{2}$. The amplitudes for higher order harmonics are defined as $\frac{-2}{n^2-1}$. From the equation, it can be seen the half-sine wave contains only even-order harmonics and the fundamental harmonic. Θ represents the phase angle. The drain voltage of class-AB/B operation contains only the fundamental harmonic since all harmonics except the fundamental harmonic are shorted.

Obviously, if, to make the drain voltage sharper, can be used the harmonics, the overlap of the drain current and voltage can be reduced and the efficiency will increase.

4.3 How the harmonics tune the fundamental frequency waveform

For class-F operation, the odd order harmonics are used to shape the drain voltage to a square waveform. For class-E operation, the drain voltage waveform is shaped by the harmonics so that the drain voltage and the slope of drain voltage is zero when the transistor is on. However, the harmonic tune conditions for ideal class-E/F operations are difficult to meet. Due to the existence of output capacitance of transistor, higher order harmonics are therefore difficult to tune. So, typically just the second harmonic can be tuned in a practical matching network. This is main motivation for the use of class-J operation. The question is now how does the second harmonic affect the performance of PA. Let's discuss it step by step.

First, have a look on how the second harmonic affects the drain voltage waveform (figure 4.4):

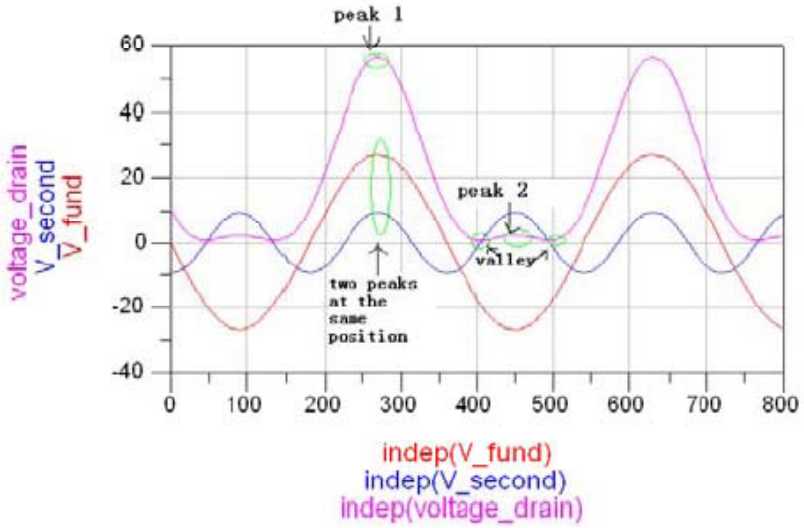


Figure 4.4 Phase relation of fundamental and second harmonic waveforms (x axis, phase angle in degree, y axis, voltage in V. Red, fundamental harmonic voltage. Blue, second harmonic voltage. Pink, superimposition of these two voltage)

Figure 4.4 shows us that the drain voltage becomes shaper after tuning by second harmonic. This is what is needed. For our first impression, the efficiency performance will be improved. However, is the problem really so simple? Let's calculate the theoretical efficiency of class-J operation.

4.4 Solutions for class-J operation

If the waveform only contains dc, fundamental and second harmonic components, it is called as pseudo half sinusoidal (PHS) [6]. The PHS of drain current is as follow:

$$PHS\_I_{sin}(\theta) = I_{dc} + I_{fund} + I_{second} = I_{dc} \times \left(1 + \frac{\pi}{2} \times \sin(\theta) - \frac{2}{3} \times \cos(2\theta)\right) \quad [6] \quad (4.4)$$

$PHS\_I_{sin}(\theta)$ is the drain current, I_{dc} is the dc current, I_{fund} is the fundamental harmonic current and I_{second} is the second harmonic current. For simplicity, the currents are normalized to DC current:

$$I_{dc} = 1 \quad (4.5)$$

$$I_{fund} = \frac{\pi}{2} \times \sin(\theta) \quad (4.6)$$

$$I_{second} = -\frac{2}{3} \times \cos(2\theta) \quad (4.7)$$

Now the composition of current is known, in order to obtain the loads, knowledge about the composition of voltage is also needed. From figure 4.8, it works out that the voltage waveform and current have reverse sign (fundamental component of drain voltage has a 180 degrees phase reversal with the drain current and the second harmonic component of drain voltage has a 360 degrees phase reversal of drain current), which is due to the nature of the schematic (see figure

4.5).

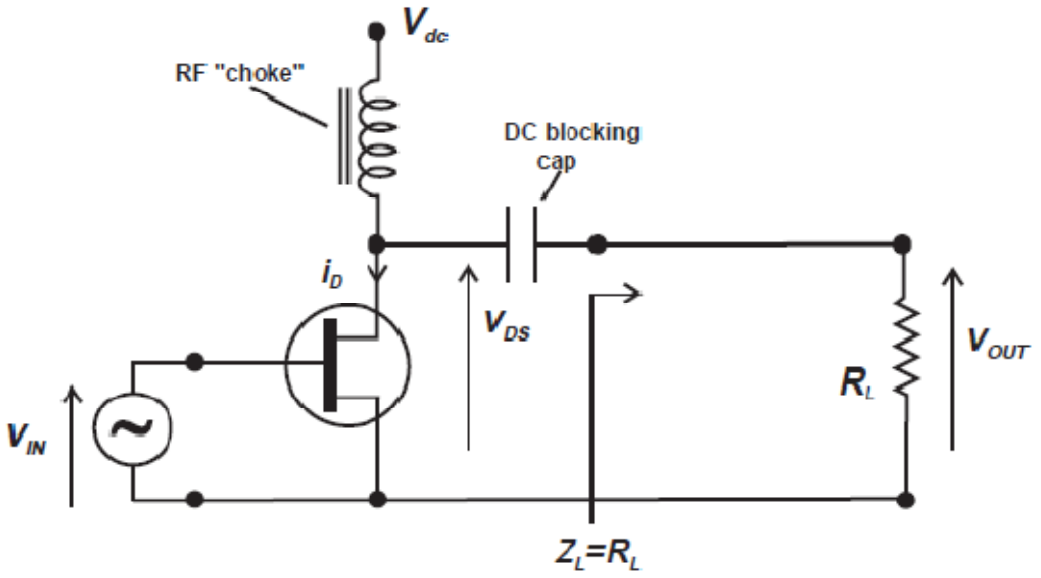


Figure 4.5: The drain current and voltage have reversed phase relation intrinsically. (see i_D and V_{DS} in the graph)

In the previous expressions of drain current and voltage, this phase reversal hasn't been taken into account yet.

The load for the second harmonic: on first sight it might seems that the second harmonic load can be arbitrary value. Actually, as discussed in section 1, in order to transform as much power from dc to fundamental frequency as more as possible, the power dissipation at higher order harmonics should be minimized. Therefore, the second harmonic load used, should be pure reactive. It can be inductive or capacitive. Inductive load means the second harmonic voltage will lead 90 degrees with the drain current. And a capacitive load means the second harmonic voltage will lag 90 degrees with the drain current. So, to synchronize the peak of the fundamental and second harmonic waveform like that in figure 4.4, the fundamental load should make the fundamental voltage lead or lag 45 degrees with the drain current. This also means that: for the typical class-J operation, there are two solutions for the fundamental and second harmonic loads. Let's discuss both of them.

The pseudo half sine (PHS) form of drain voltage:

$$PHS\_Vsin(\theta) = 1 + A \times \sin(\theta) - B \times \cos(2\theta) \qquad [6] \quad (4.8)$$

A and B is the amplitude of fundamental and second harmonic voltage respectively. All of the amplitudes are normalized to Vdc.

If we obtain the derivative of this equation and make it equal to zero, we can get the two peaks and two valleys of *PHS_Vsin* [1]:

$$peak_{1,2} = 1 \pm A + B @ \theta_1 = \frac{\pi}{2}, \theta_2 = \frac{3\pi}{2} \qquad [6] \qquad (4.9)$$

$$min_{1,2} = 1 - B - \frac{A^2}{8B} @\theta_1 = \pi + arcsin\left(\frac{A}{4B}\right)$$

$$@\theta_2 = 2\pi - arcsin\left(\frac{A}{4B}\right) \quad (4.10)$$

The minimum value of PHS waveform should be zero:

$$min_{1,2} = 0 => 1 - B - \frac{A^2}{8B} = 0 => A^2 = 8B(1-B) \quad (4.11)$$

$$A^2 = 8B(1-B) => B = \frac{1}{2} + \frac{1}{2}\sqrt{1 - \frac{A^2}{2}} \quad (4.12)$$

From equation 4.12, the maximum and minimum values of A and B are obtained respectively:

$$1 - \frac{A^2}{2} \geq 0 => \frac{A^2}{2} \leq 1 => A \leq \sqrt{2} \quad (4.13)$$

$$A_{Max} = \sqrt{2} \;\&\; B_{min} = \frac{1}{2} \quad [6] \quad (4.14)$$

The first solution: The first solution can be derived by checking the drain current and voltage relationship.

From equation 4.9, the drain current equation is given by:

$$I_{Drain}(\theta) = \frac{I_{peak}}{\pi} + \left(\frac{I_{peak}}{2}\right) \times \sin(\theta) - \frac{2 \times I_{peak}}{3 \times \pi} \times \cos(2\theta) \quad (4.15)$$

$$I_{dc} = \frac{I_{peak}}{\pi} \quad (4.16)$$

$$I_{fund} = \frac{I_{peak}}{2} \times \sin(\theta) \quad (4.17)$$

$$I_{second} = \frac{2 \times I_{peak}}{3 \times \pi} \times \cos(2\theta) \quad (4.18)$$

For the first solution, if the load for second harmonic is capacitive. The second harmonic voltage should lead 90 degrees with the phase of drain current：

$$V_{second} = -B\cos\left(2\theta + \pi - \frac{\pi}{2}\right) = -B\cos\left(2\left(\theta + \frac{\pi}{4}\right)\right) \quad (4.19)$$

B is amplitude of V_{second}, the π in the equation is caused by the reverse phase relation of drain current and voltage as shown in figure 4.5.

In order to synchronize the peaks of the fundamental and second harmonic voltage wave, the fundamental harmonic voltage waveform should lags 45 degrees with the phase of drain current:

$$V_{fund} = A \times \sin\left(\theta + \pi + \frac{\pi}{4}\right) \quad (4.20)$$

where A is the amplitude of V_{fund}. The π is caused by the reverse phase relation of drain current

and voltage as shown in figure 4.5.

Now the drain efficiency can be calculated. The output voltage on the load is V_{out} and I_{out} (see figure 4.5):

$$V_{out}(\theta) = V_{fund\_out} + V_{second\_out}$$

$$= A \times Vdc \times \sin\left(\theta + \frac{\pi}{4}\right) - B \times Vdc \times \cos\left(2\theta - \frac{\pi}{2}\right) \quad (4.21)$$

$$I_{out}(\theta) = I_{fund\_out} + I_{second\_out}$$

$$= \left(\frac{I_{peak}}{2}\right) \times \sin(\theta) - \frac{2 \times I_{peak}}{3 \times \pi} \times \cos(2\theta) \quad (4.22)$$

The output voltage and the current flow into the load have in-phase relation and they don't contain DC component.

Now, calculate the output power and efficiency of class J operation. The DC power dissipation can be calculated from the DC components of drain voltage and current:

$$P_{dc} = I_{dc} \times V_{dc} = \frac{I_{peak}}{\pi} \times V_{dc} \quad (4.23)$$

The output power can be calculated from the output voltage and current on the load:

$$P_{out} = \frac{1}{2} \times Re\left[V_{fund_{out}} \times conj\left(I_{fund_{out}}\right)\right]$$

$$= \frac{1}{2} \times Re\left[AV_{dc}e^{jw\left(\frac{\pi}{4}\right)} \times \frac{I_{peak}}{2}\right]$$

$$= \frac{\mathrm{I_{peak} \times V_{dc}}}{4} \times \cos\left(\frac{\pi}{4}\right) \times \mathrm{A} \quad (4.24)$$

The drain efficiency:

$$\eta = \frac{P_{out}}{P_{dc}} = \frac{\pi}{4} \times \frac{1}{\sqrt{2}} \times A \quad (4.25)$$

The maximum efficiency can be obtained when A reaches its maximum value. As found previously, the maximum value for A is √2 . So, the maximum efficiency is:

$$\eta_{max} = \frac{P_{out}}{P_{dc}} = \frac{\pi}{4} \times \frac{1}{\sqrt{2}} \times \sqrt{2} = \frac{\pi}{4} \approx 78.5\% \quad [6] \quad (4.26)$$

So, the theoretical highest drain efficiency of class-J operation is 78.5% and if we want to achieve this peak efficiency, we need to choose A as √2 and B as 1/2.

$$A = \sqrt{2} \quad [6] \quad (4.27)$$

$$B = \frac{1}{2} \quad (4.28)$$

Therefore, the drain voltage is:

$$V_{drain}(\theta) = V_{dc} + \sqrt{2} \times V_{dc} \times \sin\left(\theta + \pi + \frac{\pi}{4}\right) - \frac{1}{2} \times V_{dc} \times \cos\left(2\theta + \pi - \frac{\pi}{2}\right) \quad (4.29)$$

$$V_{fund} = \sqrt{2} \times V_{dc} \times \sin\left(\theta + \pi + \frac{\pi}{4}\right) \quad (4.30)$$

$$V_{second} = -\frac{1}{2} \times V_{dc} \times \cos\left(2\theta + \pi - \frac{\pi}{2}\right) \quad (4.31)$$

The π in equations (4.29) and (4.30) is due to the nature of schematic (see figure 4.5). So, it should be eliminated when the loads are calculated. From equations (4.16) to (4.17) and equations (4.30) to (4.31), the fundamental and second harmonic loads are calculated:

$$Zload_{fund} = \frac{2\sqrt{2} \times V_{dc}}{I_{peak}} \angle \frac{\pi}{4} \quad (4.32)$$

$$Zload_{second} = \frac{3 \times V_{dc} \times \pi}{4 \times I_{peak}} \angle -\frac{\pi}{2} \quad (4.33)$$

Let's choose the values of V_{dc} and I_{peak} to check the loads on the Smith chart.

Assume V_{dc}=30 V and I_{peak}=2.5 A.

$$Zload_{fund} = 34 \angle \frac{\pi}{4} \quad (4.34)$$

$$Zload_{second} = 28.3 \angle -\frac{\pi}{2} \quad [6] \quad (4.35)$$

The loads on the Smith chart (figure 4.6):

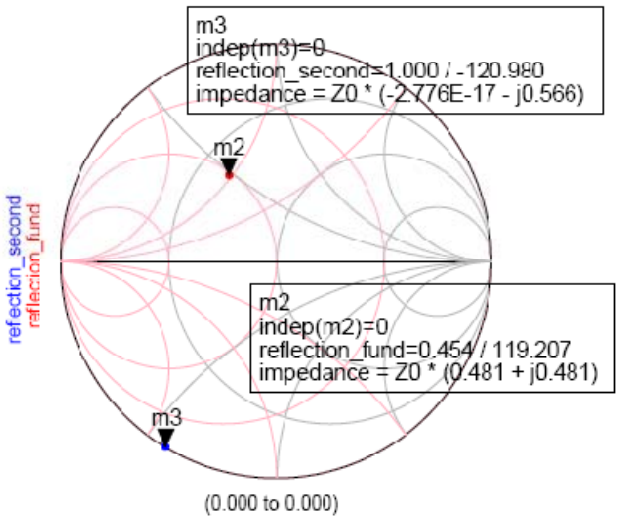


Figure 4.6: The fundamental and second harmonic loads (red, fundamental harmonic, blue, second harmonic, normalized to 50 Ohms)

An alternative solution on the Smith chart, where the load for second harmonic of solution 2 is inductive (figure 4.7):

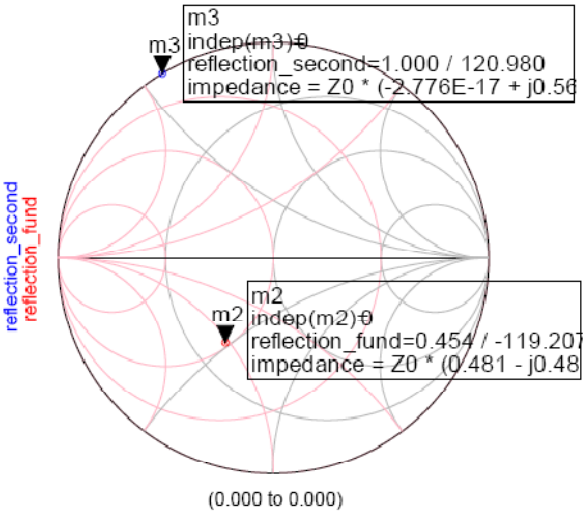


Figure 4.7: The loads of solution 2 (red, fundamental harmonic, blue, second harmonic, normalized to 50 Ohms)

The drain voltage and current waveform for solution 1 and 2:

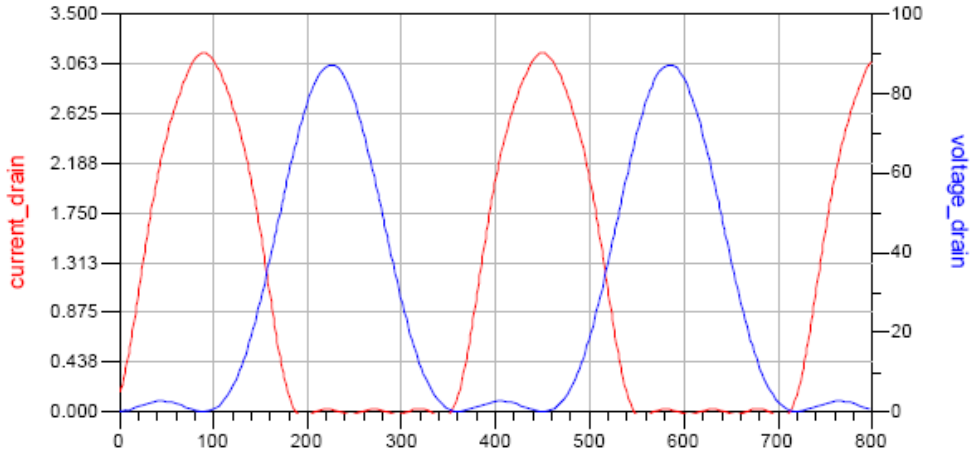


Figure 4.8 (a) Drain voltage (blue) and current (red) waveforms for solution 1of class-J operation

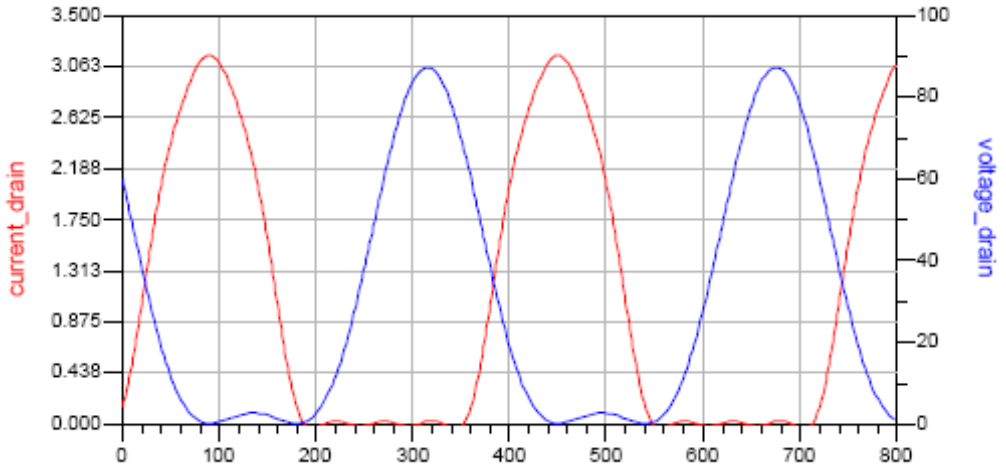


Figure 4.8 (b) Drain voltage (blue) and current (red) waveforms for solution 2of class-J operation

So, the two solutions for class-J operation are:

$$Zload_{fund} = \frac{2\sqrt{2}\times V_{dc}}{I_{peak}} \angle \pm \frac{\pi}{4} \quad (4.36)$$

$$Zload_{secomd} = \frac{3\times V_{dc}\times \pi}{4\times I_{peak}} \angle \mp \frac{\pi}{2} \quad (4.37)$$

$$P_{outpeak} = \frac{1}{4} \times V_{dc} \times I_{peak} \quad (4.38)$$

The loads in terms of peak power are:

$$Z_{fund} = \frac{V_{dc}^2}{\sqrt{2}\times P_{outpeak}} \angle \pm \frac{\pi}{4} \quad (4.39)$$

$$Z_{second} = \frac{3\pi\times V_{dc}^2}{16\times P_{outpeak}} \angle \mp \frac{\pi}{2} \quad [6] \quad (4.40)$$

V_{dc} is the dc voltage component of drain voltage and I_{peak} is the peak amplitude of drain current.

In this section, the efficiency that class-J operation can provide together with the optimal loads for fundamental and second harmonics is discussed. This can be called as ideal class-J operation. For ideal class-J operation, the maximum drain efficiency is 78.5%, which is the same as that of class-B operation. However, this efficiency is reached without providing a perfect short for the second and higher order harmonics, something that is not always practical (for example, there is a series inductor of package) in wideband design. So, for single frequency design, we should test which class is works best for our device. While for wideband design, we can make use of the 2nd harmonic termination to achieve better results, when second harmonic shorts are not practical. In the next section, some practical considerations will be discussed.

4.5 Sub-optimum class-J operation

In last section, the solutions for ideal class-J operation are obtained. From equations (4.36) to (4.40) we can see: for fixed values of dc voltage and I_{peak} or a peak output power, the optimal loads for fundamental and second harmonics are constants for a given operating frequency.

But if to design a wideband power amplifier, we will have constant values for the components of our matching network (for example, an fixed inductor, capacitor or transmission line). Use of these components will result in a not constant reactance versus frequency. For example, when we have an inductive load, the load is given by:

$$G_{loadfund} = g_{fund} + \frac{1}{jwL_{fund}} \quad (4.41)$$

g_{fund} is the conductance of the load, and with the frequency changes, the imaginary part $\frac{1}{jwL_{fund}}$ will shift on the smith chart (figure 4.9):

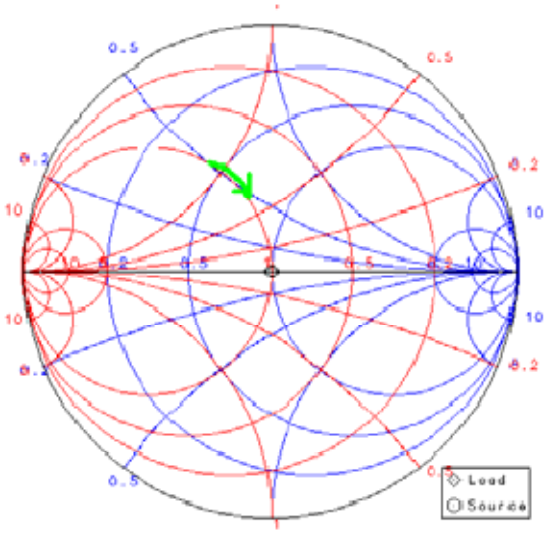


Figure 4.9: With increasing frequency, the imaginary part of the load will shift on the smith chart in the direction of the green arrow

Another complication is that the reactance of parasitic output capacitance of the device $j\omega C_{parasitic}$ will also change with frequency. Even worse this parasitic output capacitance is not a linear capacitor with supply voltage. In fact it is a very strong function of supply voltage, which will cause the optimum load shift on the Smith chart with supply voltage modulation as well. So, for a wideband power amplifier, it's almost impossible to match every load of different frequency to the optimum load. This is the reason why we discuss here sub-optimal class-J operation.

For optimum class-J, two conditions should be met:

1. The peak of the fundamental voltage waveform should synchronize with the second harmonic voltage waveform (as shown in figure 4.4). And only this condition is met, the superimposition of these two waveforms will have two peaks and two valleys.
2. The amplitude ratio of fundamental and second harmonic voltage should be a certain value. From equation (4.35) we know the amplitude ratio of fundamental and second harmonic voltage is A/B. For the optimal load, A=√2, $B = \frac{1}{2}$. So, $\frac{A}{B} = 2\sqrt{2} = 2.828$

For sub-optimal class-J operation, we indeed have used the second harmonic to tune the drain voltage waveform, but we don't meet the two conditions above exactly.

First, as we have discussed above, for wideband power amplifier, the fundamental loads for every frequency can't be matched to the optimal load. So, let's discuss how are the waveforms like, if the load deviates from the optimum value. For example:

When it's the optimum load is given by:

$$Zload_{fund} = \frac{2\sqrt{2}\times V_{dc}}{I_{peak}} \angle \frac{\pi}{4} \qquad (4.42)$$

The waveform is:

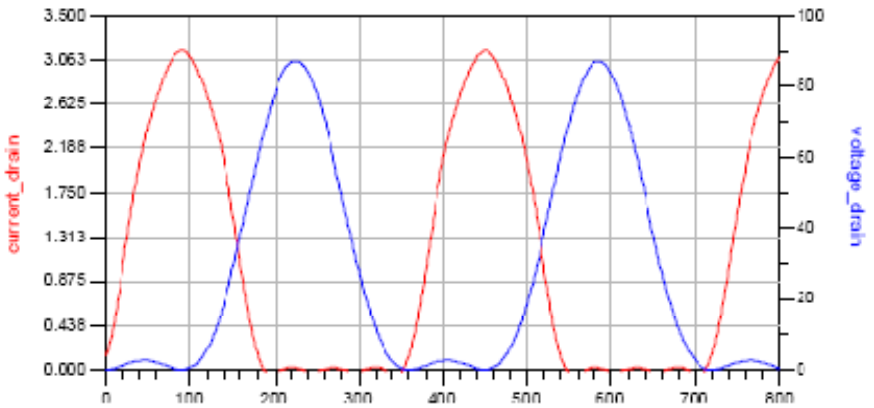


Figure 4.10: Drain current and voltage waveforms for optimal load

When the phase angle changes to $\frac{\pi}{5}$and $\frac{\pi}{3}$, the waveforms are:

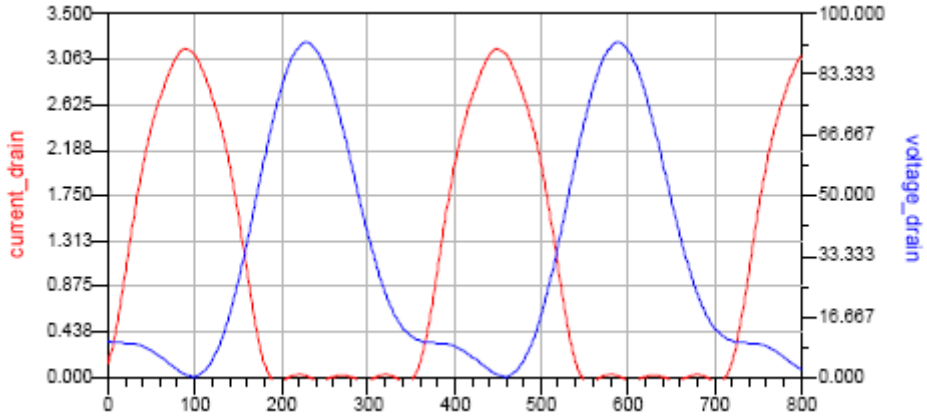


Figure 4.11 (a): Drain current and voltage waveforms when the phase angle of fundamental harmonic load is $\frac{\pi}{5}$

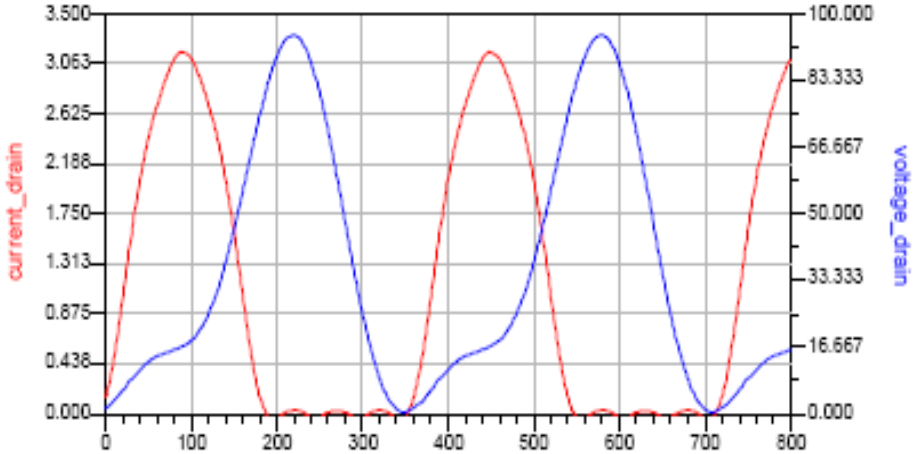


Figure 4.11 (b): Drain current and voltage waveforms when the phase angle of fundamental harmonic load is $\frac{\pi}{3}$

Phase angle of fundamental load	Drain efficiency
Pi/5	69.2%
Pi/4	78.5%
Pi/3	62.4%

Table 4.1: Phase angle of fundamental load versus drain efficiency

We can see, when the fundamental load have phase angle different from the optimal load, the waveforms of drain voltage also differ (compare figure 4.11). The related theoretical drain efficiency performance for different phase angles of fundamental load is shown in table 4.1.

Because of some parasitical series resistance of device, the second harmonic load is also not pure reactive. This will also change the phase angle of second harmonic voltage and causing similar problems as above.

Second, as we have previously discussed above, another factor which affect the shape of drain voltage waveform is amplitude ratio of fundamental and second harmonic voltage. The ratio for optimal class J is $\frac{A}{B} = 2\sqrt{2} = 2.828$.

What happens if we change this ratio? To investigate this, the ratio of 9, 3, 1 respectively is chosen and the drain voltage waveform is checked:

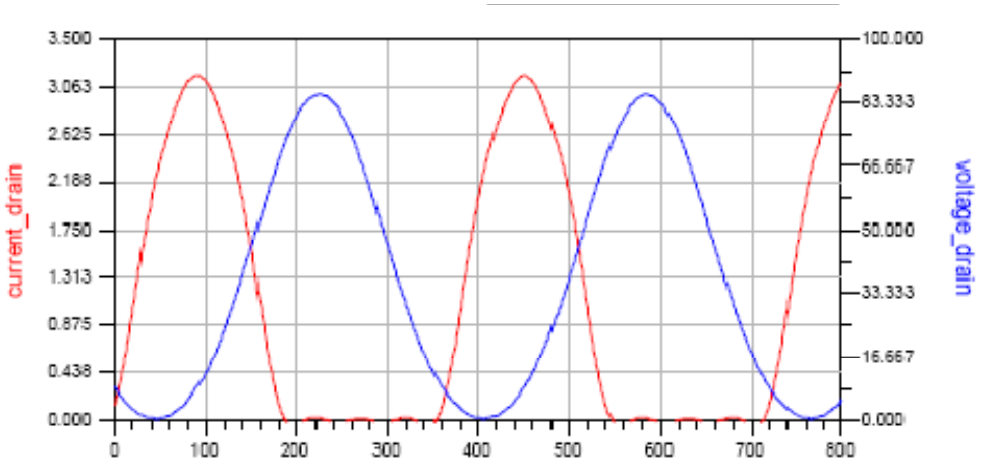


Figure 4.12 (a): The influence of amplitude ratio of fundamental and second harmonic voltage. A/B=9. The DC voltage is adjusted to 38.5 V to make the drain voltage valley reach 0.

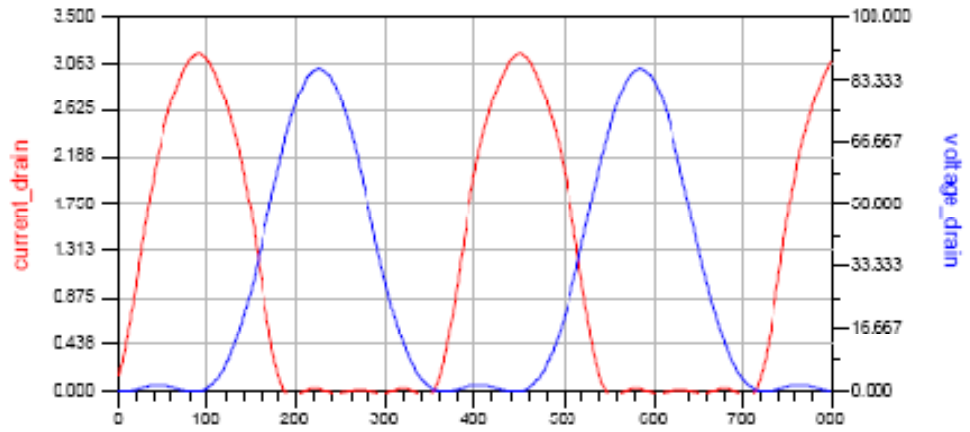


Figure 4.12 (b): The influence of amplitude ratio of fundamental and second harmonic voltage. A/B=2. The DC voltage is 30 V to make the drain voltage valley reach 0.

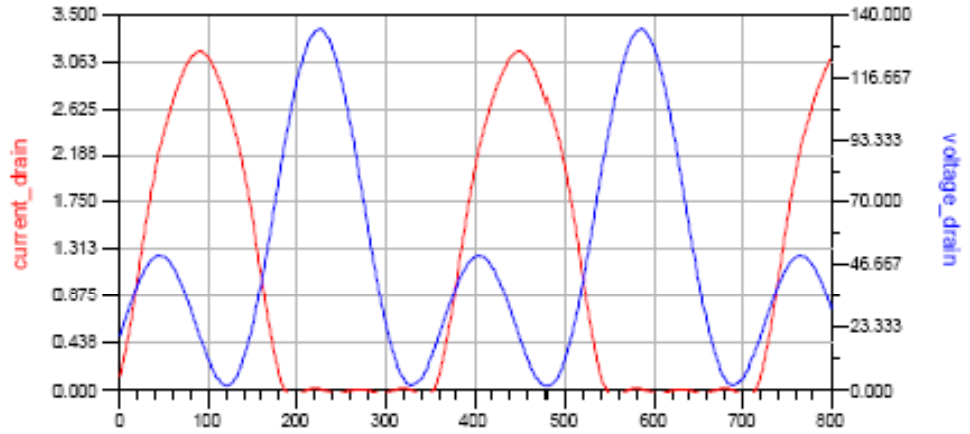


Figure 4.12 (c): The influence of amplitude ratio of fundamental and second harmonic voltage. A/B=1. The DC voltage is adjusted to 50 V to make the drain voltage valley reach 0.

When the efficiency for different ratio of A and B is calculated, the following results are obtained:

Ratio of A/B	Drain efficiency
9	64.9%
3	76.2%
1	56.5%

Table 4.2: Ratio of A/B versus drain efficiency

We can see: when the ratio is 9, the amplitude of second harmonic voltage is much smaller than that of fundamental harmonic voltage. The drain voltage is almost the same as the waveform of class-AB/B. When the ratio decreases to 3, the voltage waveform is more flat in this lower range, so. it's close to the optimal class-J waveform. When the ratio reduces to 1, the amplitudes of the fundamental and second harmonic voltage waveform are equal. The lower peak of the drain voltage becomes higher. The higher peak of fundamental voltage becomes shaper, which will exceed the breakdown voltage when the supply voltage of PA is high.

When the ratio of A/B is around 3, the efficiency performance is the best. When the ratio become higher or lower than 3, efficiency drops.

Two factors will affect the amplitude ratio. One is the phase angle and load value of fundamental harmonic load. The other is the value of second harmonic reactive load. If we have an inductive load, the imaginary part of the load will shift with frequency on the smith chart as shown in figure 4.12.

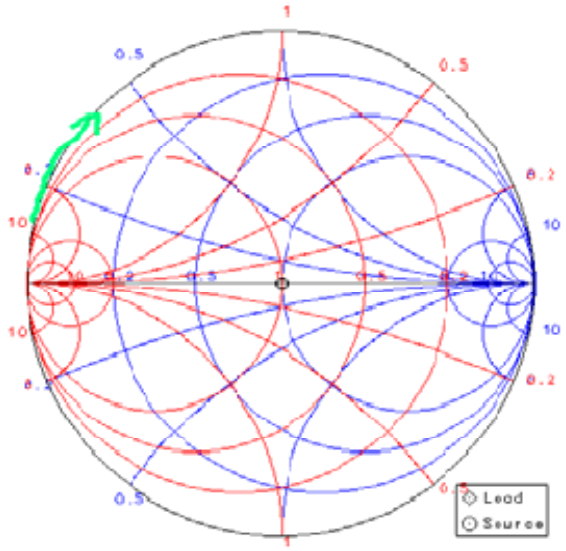


Figure 4.13: Imaginary part of load shifts with frequency (green arrow)

The amplitude of second harmonic voltage is determined by the values of second harmonic load: jωL. When ω or L increases, the amplitude of second harmonic voltage will increase. So, the value of L cam be used to tune the ratio A/B.

4.6 Conclusion:

In this chapter, we discussed the principles of class-J and sub-optimum class-J operation. The optimum class-J operation can give us a peak drain efficiency of 78.5%.We can obtain class-J waveform if we use second harmonic to tune the drain voltage waveform of class-AB/B operation. This kind of operation is meaningful when we can't perfectly short the second harmonic.

Chapter 5
Silicon Lateral-Diffused MOSFETs

Until the mid-1990s, the cellular RF power amplification applications were based upon utilizing either silicon bipolar transistors or gallium arsenide MESFETs. The introduction of the high voltage lateral-diffused (LD) MOSFET in the latter part of the 1990s altered the market dynamics. Articles written in this timeframe describe the LD-MOSFET as a novel technology that is starting to challenge the entrenched position of the silicon bipolar transistor because of reduced distortion, while being more competitive than the gallium arsenide devices due to significantly lower cost. However, significant concerns regarding the ruggedness and reliability of the LD-MOSFETs were prevalent in the industry.

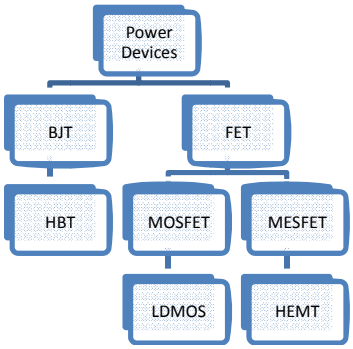


Figure 5.1: Power Device family tree

Within a few years, the LD-MOSFETs had successfully displaced the silicon bipolar transistors and shut out the gallium arsenide devices from the cellular base-station market. Improvements in its efficiency and linearity provided significant cost-performance benefits to the end user. In addition, these devices could be operated using a single 28-V supply. However, the drift of the threshold voltage of the transistor during operation at the quiescent operating point continued to haunt the technology. The drift in threshold voltage, arising from an injection of hot-electrons into the gate oxide, created a major problem in obtaining stable performance. Fortunately, further structural and process enhancements during the last few years have brought the threshold drift to below 5 percent over a 20 year time span. This is believed to be satisfactory for operation of the transistors in power amplifiers without adding costly bias adjustment circuitry. Manufacturers continue to optimize the device structure and process to improve up on the efficiency, linearity, and gain by scaling down the channel length and gate oxide thickness while monitoring any degradation in the drift and reliability. In addition, methods for reducing the thermal impedance are a high priority because a rise in channel temperature is detrimental to the gain and linearity.

In this chapter, the basic operating principles of the LDMOSFET structure will be discussed. Although the exact values for the doping profiles, the gate oxide thickness, and channel length may vary from manufacturer to manufacturer, the basic structure for the LDMOSFET used in the industry is similar to that described in this chapter.

5.1 Device Cell Structure

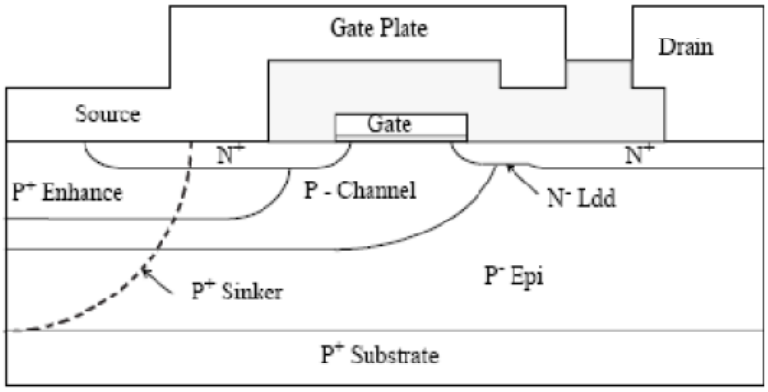


Figure 5.2: Lateral-Diffused (LD) MOSFET Structure.

A cross-section of the basic cell structure for the Lateral-Diffused (LD) MOSFET is illustrated in figure 5.2. The device is fabricated by starting with a P-type epitaxial layer grown on a heavily doped P^+ substrate. As implied by the name, the channel is formed by the difference in lateral extension of the P-base and N^+ source regions produced by their diffusion cycles. Both regions are self-aligned to the left-hand-side of the gate region during ion-implantation to introduce the respective dopants.

In order to enable high voltage operation with short channel lengths, a lightly doped drain (LDD) region is formed on the right-hand-side of the gate by implantation of an N-type dopant. The charge in the LDD region and its length along the surface between the gate edge and the drain edge must be optimized to maximize the breakdown voltage. A highly doped, deep P+ sinker region is also incorporated in the structure to connect the source region to the P+ substrate. This allows mounting the chip to the flange of the RF package to create a source connected ground plane without the detrimental effects of source wire-bonds.

The doping concentration and length of the P-base region is designed to avoid reach-through breakdown. The Reduced Surface (RESURF) effect is utilized to distribute the electric field into the LDD region. It has been found that a charge of about 1 x 1012 cm^{-2} is optimal for obtaining the highest breakdown voltage. When the charge is too low, a high electric field is created at the drain side of the LDD region reducing the breakdown voltage. In contrast, if the LDD charge is too high, a high electric field is created at the gate edge resulting in low breakdown voltages. In order to obtain a breakdown voltage of 75-80 V, it is necessary to make the length of the LDD region between the gate and the drain at least 5 microns. The breakdown voltage can also be limited by the maximum voltage that can be supported in the vertical direction under the N^+ drain region. This breakdown voltage is determined by the thickness and doping concentration of the P-type epitaxial layer.

The high electric field at the gate edge in the LD-MOSFET structure has been a major drawback because it enhances hot electron injection into the gate oxide. Unlike power switching MOSFETs, the RF power MOSFETs operate under a constant quiescent DC voltage and current

under class A and class AB conditions. If the electric field at the gate oxide is large, the electrons can gain sufficient energy to be launched into the gate oxide and become captured by traps in the oxide. The charge contributed by the trapped electrons causes a shift in the threshold voltage which is referred to as the *drift phenomenon* in LD-MOSFETs. This instability in LD-MOSFETs has been a major concern for the industry resulting in various proposed solutions.

Drain current flow in the LD-MOSFET structure is induced by the application of a positive bias to the gate electrode. This produces an inversion layer at the surface of the P-base region under the gate electrode. This inversion layer channel provides a path for transport of electrons from the source to the drain when a positive drain voltage is applied. Due to the high electric field at the edge of the gate during high voltage operation, the channel length of the LD-MOSFET must be sufficiently long to avoid reach-through of the depletion layer in the P_{base} region. Consequently, the LD-MOSFETs operate with channel pinch-off as the drain voltage increases resulting in a square law relationship between the drain current and the gate voltage. In the LD-MOSFET structure, the drain current flows along the surface from the drain electrode to the top surface source electrode. The current is then re-directed via the deep P+ sinker region into the P+ substrate. The on-resistance of the structure is determined not only by the resistance of the channel and drift region but also by the resistance of the P-type substrate.

For a typical LD-MOSFET designed to support 75-80 V, although the length of the LDD region is about 5 microns, the cell pitch is about 1.5 microns because of the space taken by the deep P+ diffusion and the interdigitated metal contacts for the drain and source.

The width of the drain metal is insufficient to allow bonding wires to connect the drain to the package terminal. It is necessary to carry the drain current along the drain metal fingers in the orthogonal direction to the transistor cell cross-section shown in figure 5.2 to a drain bonding pad. As the drain current is collected along the finger, the current level, and hence the current density in the drain metal, becomes larger towards the drain bonding pad. The drain metal must be sufficiently thick so that electromigration failures are mitigated during device operation. It is commonplace to use gold metallization in RF LD-MOSFETs, instead of the usual aluminium metal used in power MOSFETs, because of its enhanced resistance to electromigration effects.

5.2 RF properties of Si-LDMOS

In a Si-LDMOS transistor, the length of the channel region determines the properties of the system at high frequency. In fact, the shorter channel length improves the linearity since the transistor always works in velocity saturation. In high frequency operation, telecommunication applications such as WiMax, GaAs based HEMT and MESFET are used due its higher saturation velocity compared to Si. Currently an interest is growing towards Si-LDMOS technology in communication area due to its cost/scalability business model. Since Si is a developed material, the structure of LDMOS gives an excellent high power characteristics, linearity, power gain and offers a wide range of frequency in the order of GHz. The recent investigation shows an improvement in RF characteristics of Si-LDMOS, which surpass BJT and even approaches to SiC-MESFET performance.

Chapter 6

Overview of Advanced Design System

6.1 DC Simulation

6.1.1 DC Simulation Concept

The simulators compute the response of a given circuit to a particular stimulus by converting, based on certain assumptions, a system of nonlinear ordinary differential circuit equations into a system of nonlinear algebraic equations and then solving them numerically. The various simulators convert ordinary differential equations to algebraic equations differently and use different numerical techniques for solving the resulting algebraic equations, leading to the many different simulator flavors (DC, AC, S-parameter, transient, harmonic balance, circuit envelope).

For example, the DC and the harmonic balance simulators treat the d/dt operator differently, leading to different algebraic equations. The numerical simulation techniques rely on various iterative processes to achieve mathematical convergence toward an equilibrium point in the nonlinear algebraic equations that describe the circuit. Once this equilibrium point is reached to within certain tolerances, a solution is said to have been found. The specific assumptions taken for the DC simulator are described in Simulation Assumptions.

6.1.2 Simulation Assumptions

DC voltages and currents are signals of zero frequency. The simulator uses this concept when performing a DC simulation, and the following conditions apply:

- Independent sources are constant valued.
- Linear elements are replaced by their (real) conductance at zero frequency.
- Capacitors, micro-strip gaps, AC coupled lines, and similar items are treated as open circuits.
- Inductors, conductive discontinuities, and similar items are treated as short circuits.
- Time-derivatives are constant (zero).
- Transmission lines are replaced by DC conductance values calculated from their length, cross-sectional area, and conductivity.
- Scattering parameter (S-parameter) files must include zero frequency data to operate properly at DC (this is also required for harmonic balance analysis). Otherwise, the simulator extrapolates each S-parameter for the zero-frequency case, and uses the real part as the DC response.
- The simulator has built-in safeguards against nodes that are DC-isolated (that have no DC path to ground), as well as against DC source-inductor loops. Nevertheless, try to avoid these conditions.

6.2 AC Simulation

6.2.1 AC Simulation Concept

When an AC small-signal simulation is run, the system first computes the DC operating point of the circuit. Whenever a linear simulation such as a linear AC simulation requires a single-point DC bias simulation to be run first, it is referred to as a *bias-dependent* linear simulation. The most common example is the case of a linear amplifier that uses a biased transistor as the active element. The DC bias simulation is executed automatically and transparently (unless an error causes the DC simulation to fail to converge).

Following the DC bias simulation, the simulator linearizes all nonlinear devices about their bias points. A linearized model captures the small incremental changes of current due to small incremental changes of voltage. These are the derivatives of the transistor model equations, which are evaluated at the DC bias point. Nonlinear resistors and current sources are replaced by linear resistors whose values are set by the small signal conductance dI/dV. Current sources that depend on voltages other than the voltage across the source are replaced by linear dependent current sources dI_1/dV_2. Nonlinear capacitors are replaced by linear capacitors of value dQ/dV.

The resulting linear circuit is then simulated over the specified frequency range. Small-signal AC simulation is also performed before a harmonic-balance (spectral) simulation to generate an initial guess at the final solution.

Use the AC controller to:

- Perform a swept-frequency or swept-variable small-signal linear AC simulation.
- Obtain small-signal transfer parameters, such as voltage gain, current gain, transimpedance, transadmittance, and linear noise.

Simulation can be performed repeatedly while sweeping some parameter. If changing these parameters affects the DC operating point, the DC operating point and linearized circuit will be recomputed at each step.

6.3 S- Parameter Simulation

S-parameters are used to define the signal-wave response of an n-port electrical element at a given frequency. Detailed discussions of S-parameters can be found in standard textbooks on electrical circuit theory.

- S-parameter simulation is a type of small-signal AC simulation. It is most commonly used to characterize a passive RF component and establish the small-signal characteristics of a device at a specific bias and temperature.
- If the circuit contains any nonlinear devices, a DC simulation is performed first. Following the DC bias simulation, the simulator linearizes all nonlinear devices about their bias points. A linearized model captures the small incremental changes of current due to small incremental changes of voltage. These are derivatives of the transistor model

equations, which are evaluated at the DC bias point. Nonlinear resistors and current sources are replaced by linear resistors whose values are set by the small signal conductance dI/dV. Current sources that depend on voltages other than the voltage across the source are replaced by linear dependent current sources dI_1/dV_2. Nonlinear capacitors are replaced by linear capacitors of value dQ/dV.

- The linear circuit that results is analyzed as a multiport device. Each port is excited in sequence, a linear small-signal simulation is performed, and the response is measured at all ports in the circuit. That response is then converted into S-parameter data, which are in turn sent to the dataset. S-parameter simulation normally considers only the source frequency in a noise analysis. Use the *Enable AC Frequency Conversion* option if you also want to consider the frequency from a mixer's upper or lower sideband.

6.4 LSSP Simulation

6.4.1 LSSP Simulation Concept

Unlike small-signal S-parameters, which are based on a small-signal simulation of a linearized circuit, large-signal S-parameters are based on a harmonic balance simulation of the full nonlinear circuit. Because harmonic balance is a large-signal simulation technique, its solution includes nonlinear effects such as compression. This means that the large-signal S-parameters can change as power levels are varied. For this reason, large-signal S-parameters are also called power-dependent S-parameters.

Like small-signal S-parameters, large-signal S-parameters are defined as the ratio of reflected and incident waves:

$$S_{ij} = \frac{B_i}{A_j} \tag{6.1}$$

The incident and reflected waves are defined as:

$$A_j = \frac{V_j + Z_{0j} I_j}{2\sqrt{R_{0j}}} \quad B_i = \frac{V_i - Z^*_{0i} I_i}{2\sqrt{R_{0i}}} \tag{6.2}$$

where

V_i and V_j are the Fourier coefficients, at the fundamental frequency, of the voltages at ports *i* and *j*, I_i and I_j are the Fourier coefficients, at the fundamental frequency, of the currents at ports *i* and *j*, Z_{0i} and Z_{0j} are the reference impedances at ports *i* and *j*, and R_{0i} and R_{0j} are the real parts of Z_{0i} and Z_{0j}.

This definition is a generalization of the small-signal S-parameter definition in that *V* and *I* are Fourier coefficients rather than phasors. For a linear circuit, this definition simplifies to the small-signal definition.

6.4.2 LSSP Simulation Process

The simulator performs the following operations to calculate the large-signal S-parameters for a two-port:

- Terminates port 2 with the complex conjugate of its reference impedance. Applies a signal with the user-specified power level P_1 at port 1, using a source whose impedance equals the complex conjugate of that port's reference impedance. Using harmonic balance, calculates the currents and voltages at ports 1 and 2. Uses this information to calculate S_{11} and S_{21}.
- Terminates port 1 with the complex conjugate of its reference impedance. Applies a signal of power $P_2 = |S_{21}|^2 P_1$ at port 2 using a source whose impedance equals the complex conjugate of the reference impedance of port 2. Using harmonic balance, calculates the currents and voltages at ports 1 and 2. Uses this information to calculate S_{12} and S_{22}.

6.4.3 Comparing LSSP and S-Parameter Simulations

S-parameter simulations are performed on linear circuits. LSSP simulations can be performed on nonlinear circuits and thus include nonlinear effects such as gain compression and variations in power levels.

Both LSSP and S-parameter simulations generate PortZ[] and S[] fields in the associated dataset. LSSP generates the additional field PortPower[], which contains the power, in dBm, seen at each port for the respective LSSP port frequencies.

6.5 Harmonic Balance Simulation

Harmonic balance is a frequency-domain analysis technique for simulating distortion in nonlinear circuits and systems. It is usually the method of choice for simulating analog RF and microwave problems, since these are most naturally handled in the frequency domain. Within the context of high-frequency circuit and system simulation, harmonic balance offers several benefits over conventional time-domain transient analysis.

Harmonic balance simulation obtains frequency-domain voltages and currents, directly calculating the steady-state spectral content of voltages or currents in the circuit. The frequency integration required for transient analysis is prohibitive in many practical cases. Many linear models are best represented in the frequency domain at high frequencies. Use the HB simulation to:

- Determine the spectral content of voltages or currents.
- Compute quantities such as third-order intercept (TOI) points, total harmonic distortion (THD), and intermodulation distortion components.
- Perform power amplifier load-pull contour analyses.
- Perform nonlinear noise analysis.

6.6 XDB Simulation

6.6.1 Gain Compression Concept

Gain compression is the difference, in dB, between a point on an idealized linear (small-signal) power-gain slope and a corresponding point on the actual power curve. That is, for a gain compression of *x* dB,

$$x = 10 * log_{10}(\frac{G_x}{G_{ss}}) \quad (6.3)$$

where G_x is the point on the idealized linear gain slope that is *x* dB directly below the point G_{ss} on the small-signal power curve, as illustrated below.

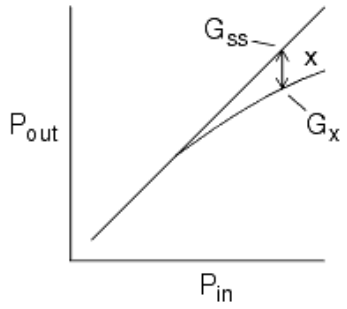


Figure 6.1: Gain curve showing x dB compression

The simulator stops its analysis when it reaches that point. The default setting is 1 dB. The XDB simulator uses a harmonic balance algorithm, and as such shares many of the parameters and options that the Harmonic Balance simulator provides. However, this simulation requires that the input and output of the component or circuit whose gain compression is being simulated be defined by an appropriate source and termination.

6.6.2 Performing a Gain Compression Simulation

Start by creating your design, then add current probes and identify the nodes from which you want to collect data for a successful analysis:

- Use port-type sources at the inputs, such as the P_1Tone under *Sources-Freq Domain*.
- Terminate outputs with port-impedance terminations. You can find this type of port under *Simulation-S_Param*. Verify the impedance value.
- The *Num* values in the port-impedance terminations are used to specify input and output ports.
- Add the Gain Compression control element to the schematic. Fill in the fields under the Freq and X dB tabs:
    - For Freq, set the fundamental frequency and order
    - For X db, specify the input and output ports, the frequency at each port, power variation for each port, and maximum input power.
- For a faster simulation of large circuits, use the Krylov option from solver tab
- You can use previous simulation solutions to speed up the simulation process. By enabling "Reuse Simulation Solutions" in the "Harmonic Balance Simulator."

6.7 Envelope Simulation

6.7.1 Theory of Operation for Circuit Envelope Simulation

The Envelope simulator combines features of time- and frequency-domain representation, offering a fast and complete analysis of complex signals such as digitally modulated RF signals.

Briefly, this simulator permits input waveforms to be represented in the frequency domain as RF carriers, with modulation "envelopes" that are represented in the time domain as shown in the following figure.

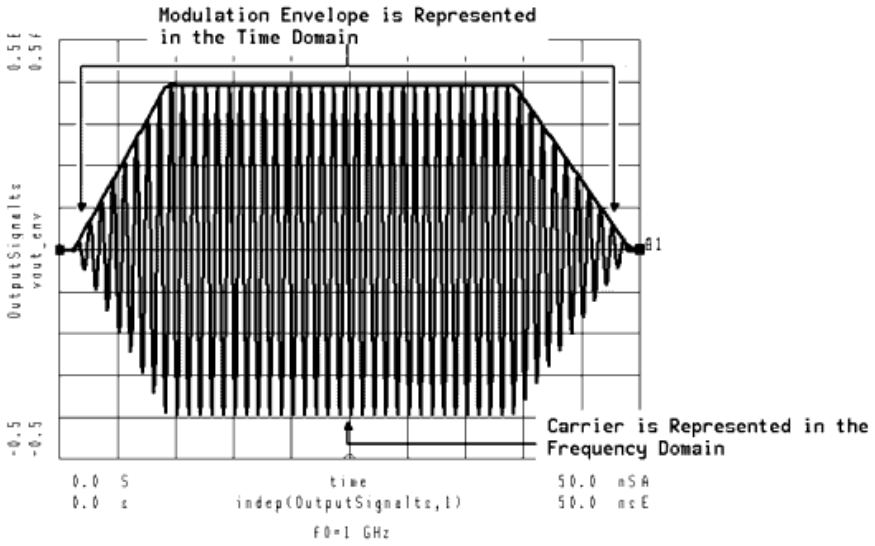


Figure 6.2: Modulated signal in the time domain

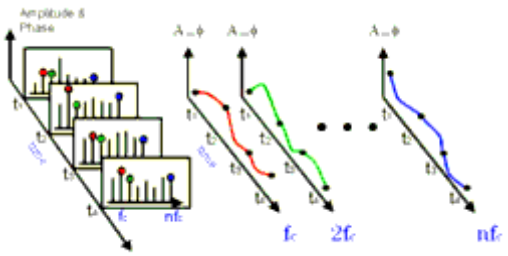


Figure 6.3: Extraction of time domain data in frequency domain

Extract data from time domain selecting the desired harmonic spectral line (fc in this case), it is possible to analyze:

- Amplitude vs. time (oscillator start up, pulsed RF response, AGC transients)
- Phase (f) vs. time (t) (VCO instantaneous frequency (df/dt), PLL lock time)

- Amplitude and phase vs. time (constellation plots, EVM, BER)

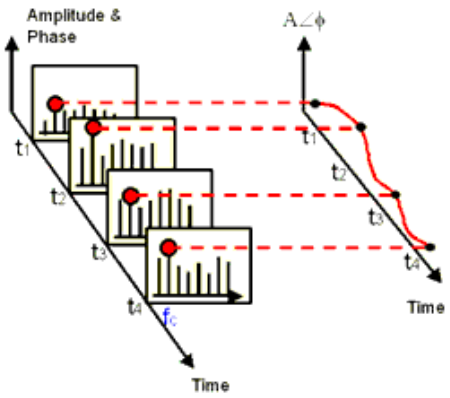


Figure 6.4: Amplitude and Phase reconstruction

Extract data from frequency domain by applying FFT to the selected time-varying spectral line it is possible to analyze:

- Adjacent channel power ratio (ACPR)
- Noise power ratio (NPR)
- Power added efficiency (PAE)
- Reference frequency feed through in PLL
- Higher order intermods (3rd, 5th, 7th, 9th)

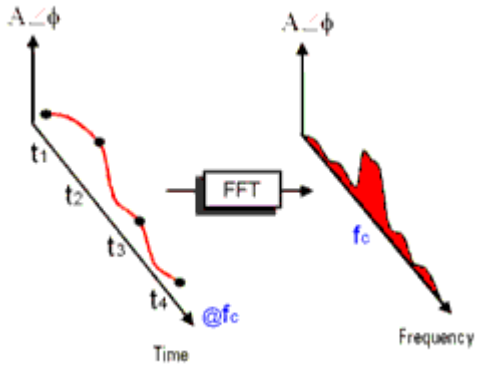


Figure 6.5: Time domain to frequency domain conversion using FFT

6.7.2 When to Use Circuit Envelope Simulation

Circuit Envelope is highly efficient in analyzing circuits with digitally modulated signals, because the transient simulation takes place only around the carrier and its harmonics. In addition, its calculations are not made where the spectrum is empty.

- It is faster than Harmonic Balance, assuming most of the frequency spectrum is empty.
- It compromises neither in signal complexity, unlike Harmonic Balance or Shooting Method, nor in component accuracy, unlike Spice, Shooting Method, or DSP.

- It adds physical analog/RF performance to DSP/system simulation with real-time co-simulation with ADS Ptolemy.
- It is integrated in same design environment as RF, Spice, DSP, electromagnetic, instrument links, and physical design tools.

6.7.3 Advantage over Harmonic Balance:

- In Harmonic Balance, if you add nodes or more spectral frequencies, the RAM and CPU requirements increase geometrically. The Krylov solver improves this, but it is still a limitation of Harmonic Balance because the signals are inherently periodic.
- Conversely the penalty for more spectral density in Circuit Envelope is linear: just add more time points by increasing *tstop*. The longer you simulate, the finer your resolution bandwidth.
- Doing a large number of simple one-tone HB simulations is effectively faster and less RAM intensive than one huge HB simulation.
- With a circuit envelope simulation the amplitude and phase at each spectral frequency can vary with time, so the signal representing the harmonic is no longer limited to a constant, as it is with harmonic balance.

6.7.4 How to Use Circuit Envelope Simulation

Start by creating your design, then add current probes and identify the nodes from which you want to collect data.

For a successful analysis, be sure to:

- Use either time domain or frequency domain sources in your circuit. In a circuit employing a mixer, provide a source for the LO.
- Add the Circuit Envelope controller to the schematic. (From the Component palette, choose Simulation-Envelope. Add the ENV component to the schematic.) Double-click to edit it. Fill in the fields under the Env Setup tab:
  - A Circuit Envelope simulation runs in the both the time and frequency domain. Set the stop time and time step (start time is 0). Time step defines the maximum allowed bandwidth (± 0.5/Time step) of the modulation envelope. The analysis bandwidth (1/Time step) should be at least twice as large as the modulation bandwidth to ensure accurate results at the maximum modulation frequencies.
  - Enter fundamental frequencies and order.

Chapter 7
Simulation and Design

7.1 Device Characterization

7.1.1 Device Model Used

NXP semiconductor (formerly Philips Semiconductor) is one of the leading foundries in manufacturing of Semiconductor devices. They are expert in RF power solution. They provide ADS model design kit of their products. These design kits are useful in analysis and design of hardware for RF application. One such product is used in this project.

A 25 Watt, Base station RF LDMOS power transistor form NXP Semiconductors is used for this project work. NXP's BLF6G38S-25 model is designed to work in frequency range of 3400MHz-3800MHz. Easy power control, integrated ESD protection, excellent ruggedness, high efficiency, excellent thermal stability, internally matched for ease of use, are some features of this transistor.

While selecting values for biasing, its limiting values must be taken into consideration. Some important limiting values are tabulated in table 7.1.

Parameter	***Min***	***Max***
V_{DS}	-	65V
V_{GS}	-0.5V	+13V
I_D	-	8.2A
T_{stg}	-65°C	+150°C
T_j	-	200°C
$R_{th(j\text{-}case)}$ For T_{case} = 80°C	1.8K/W (typical)	

Table 7.1: Limiting values of NXP's BLF6G38S-25 model

7.1.2 DC Simulation

According to the instructions for the BLF6G38S-25 ADS model, the valid range of gate voltage V_{gs} is from -0.5V to +13V and the threshold voltage is at 2.0V. The valid range of drain voltage V_{dd} is from 0V to 65V.

Before building up the circuit, the maximum allowed DC power dissipation must be found. From table 7.1, we notice that the maximum Operating Junction Temperature is 200°C and the Thermal Resistance, Junction to case is 1.8°C/W for a Case Temperature 80°C, 25W CW. Based on the above, we find:

$$P_{d\,max} = \frac{(T_j - T_c)}{R_{jc}} = \frac{200-80}{1.8} = 66.67\ Watts. \qquad (7.1)$$

The above result will limits the choice of the bias level to ensure a secure operation region for the transistor and to prevent it from self heat destruction.

Figure 7.1 below shows the I-V characteristic of the LDMOS transistor with Gate bias voltage swept from 0V to 13V. This information is important as a starting point of the design and it used to determine the DC bias condition for the transistor based on the amplifier class the design belongs to.

It is decided to operate at drain bias voltage of 28V, which is suggested by datasheet. As of Class J amplifier, the gate bias voltage of 2.3V is picked as indicated by the marker m1 in Fig. 7.1. This bias point is chosen because of the small quiescent current of 319mA through the transistor drain showing that the transistor is biased close to the cut-off region.

Figure 7.1 also shows curve for maximum power dissipation below which there is safe operating region of transistor.

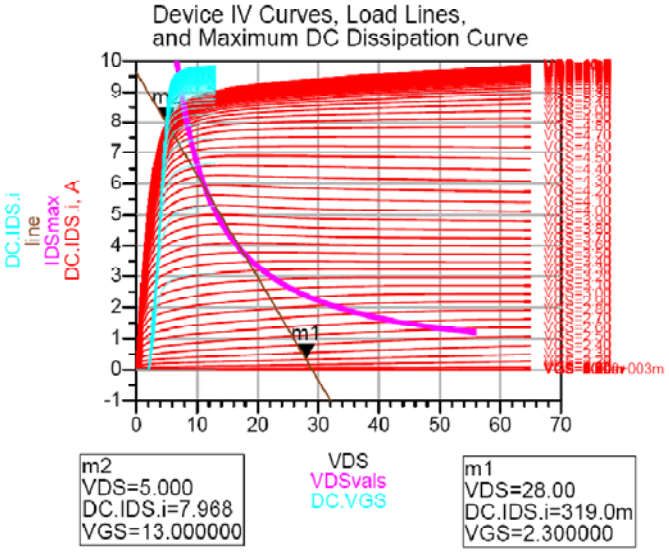


Figure 7.1: I-V curve of BLF6G38S-25 with different drain and gate bias voltage

7.1.3 AC simulation

By doing AC small signal simulation, transfer characteristics such as transconductance, transimpedance can be determined. Transconductance (G_m) specially is important while considering biasing point for conventional class power amplifier. For particular V_{DS}, the value of G_m changes with change in gate bias voltage. For conventional class amplifier, it is suggested to select gate bias such as to have maximum G_m.

The circuit is simulated for 3.5GHz AC signal which is operating frequency for this work. Marker m5 in figure 7.2 shows G_m is maximum at 2.7V while at Class J biasing Gm = 0.754 denoted by marker m3.

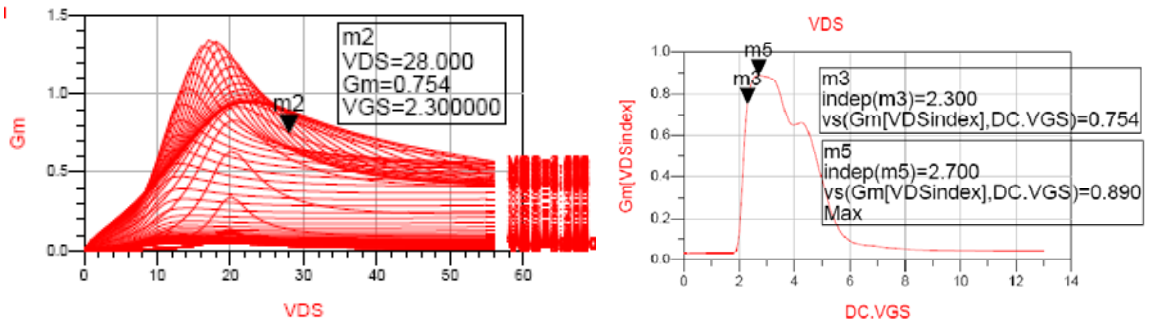


Figure 7.2: Transconductance curve for various values of V_{DS} and for G_m vs V_{GS} for particular V_{DS}

7.1.4 Small Signal S-Parameter Simulation

After choosing a suitable DC bias condition, the next step is to simulate the transistor to find S-parameters. The transistor is terminated with 50Ω at the input and output and simulated for frequency range of 3GHz to 4GHz. Figure 7.3 shows s-parameter variation for simulated frequency range.

Since the X-parameter[¶] file for large signal is not available from manufacturer. Small-signal S-parameters will be used instead during the design process. The ADS simulated S-parameters of the transistor for 3.5GHz shown in figure 7.4. It can be assumed that the BLF6G38S-25 transistor model using S-parameters for computation is accurate enough so that the simulated results will be able to accurately describe the actual PA performance.

[¶]X-parameter: A mathematical superset of S-parameters and are used for characterizing the amplitudes and relative phases of harmonics generated by nonlinear components under large input power levels.

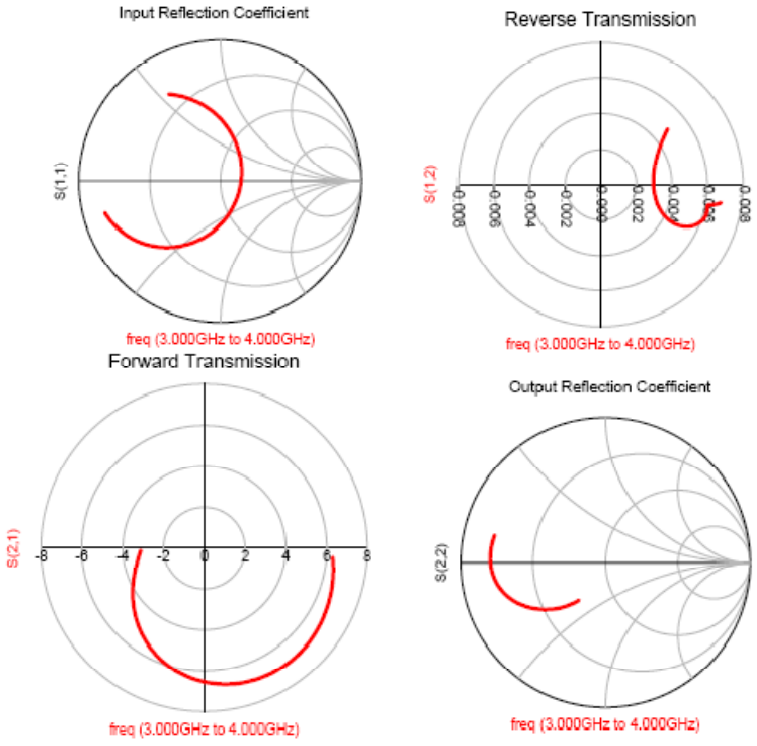


Figure 7.3: Simulated S-parameter for frequency range of 3GHz to 4GHz

freq	var("S")			
	(1,1)	(1,2)	(2,1)	(2,2)
3.410 GHz	0.215 / -67.825	0.006 / -21.963	6.383 / -96.035	0.724 / -162.129
3.420 GHz	0.235 / -73.925	0.006 / -22.595	6.315 / -98.211	0.728 / -162.741
3.430 GHz	0.255 / -79.257	0.006 / -23.212	6.245 / -100.360	0.732 / -163.348
3.440 GHz	0.276 / -83.970	0.006 / -23.810	6.172 / -102.480	0.736 / -163.947
3.450 GHz	0.297 / -88.185	0.006 / -24.385	6.097 / -104.571	0.740 / -164.541
3.460 GHz	0.318 / -91.993	0.006 / -24.933	6.021 / -106.630	0.744 / -165.129
3.470 GHz	0.339 / -95.466	0.006 / -25.450	5.943 / -108.657	0.747 / -165.711
3.480 GHz	0.360 / -98.661	0.005 / -25.933	5.864 / -110.651	0.750 / -166.288
3.490 GHz	0.380 / -101.621	0.005 / -26.378	5.784 / -112.612	0.753 / -166.858
3.500 GHz	0.400 / -104.381	0.005 / -26.781	5.703 / -114.538	0.755 / -167.424
3.510 GHz	0.419 / -106.968	0.005 / -27.139	5.622 / -116.429	0.759 / -167.984
3.520 GHz	0.438 / -109.404	0.005 / -27.449	5.541 / -118.286	0.762 / -168.539

Figure 7.4: S-parameter at 3.5GHz

7.1.5 Large Signal S-Parameter Simulation

Large signal s-parameter tests are used to obtain the s-parameters of nonlinear systems. LSSP test requires the use of a power source, because nonlinear systems may have different s-parameters at different power levels. For this test, a power level of 23dBm (200mW) was used to measure the s-parameters of the transistor at 3.5GHz. The transistor was also biased to the desired operating point as defined in the previous section. Table 7.2 shows large signal s-parameter for simulated LDMOS.

S(1,1)	S(1,2)	S(2,1)	S(2,2)
0.374 / -97.055	0.005 / -25.945	4.978 / -114.054	0.759 / -168.236

Table 7.2: Large signal S-parameter at 3.5GHz

It was not possible to directly compare the results obtained from these tests to the real transistor, because no s-parameter data had been recorded for the physical transistor. The LSSP simulation results were a good estimation of the transistor's s-parameters. However it was concluded that the model provided was not accurate enough to be the sole basis for a physical design.

7.1.6 Stability Analysis

The stability issue is very important for power amplifier design. If it's possible, we should make the power amplifier unconditional stable. But, the reality is we will lose a lot of gain if we make it unconditional stable. So, our strategy is to make the source and load stability circles outside the main area of the Smith chart and match the input and output outside the stability circles.

Figure 7.5 shows the load and source stability circles. The circles are plotted for supply voltage V_{DS} = 28V for frequency range of 3GHz to 4GHz. Red coloured contours represent source stability circles and red contours represent load stability circles.

It can be noticed that for the given range of frequency, both stability circles are outside the main smith chart region. This means that transistor in unconditional stable at given voltage for frequency region of interest.

Figure 7.6 shows curve for stability factor (K) and geometrically derived source stability factor (mu_source) and load stability factor (mu_load). The device is unconditionally stable if the stability factor is above 1 for frequency range of interest.

From graph in figure 7.6(b), it can be deduced that device is unconditionally stable for region of interest. But from figure 7.6(a) it can be concluded that there is need of stabilization network to be used at input to make the device unconditionally stable for whole frequency range.

Maximum available gain is gain that can be achieved when input and output are conjugately matched and there is no feedback. The value of MAG is real for all values where stability factor is greater than 1. For K<1, MAG becomes infinite. Infinite gain means Oscillation. The curve of MAG can be used to learn about oscillating behaviour of device.

Maximum available gain (MAG) is shown in figure 7.7 along with associated power gain and transducer gain.

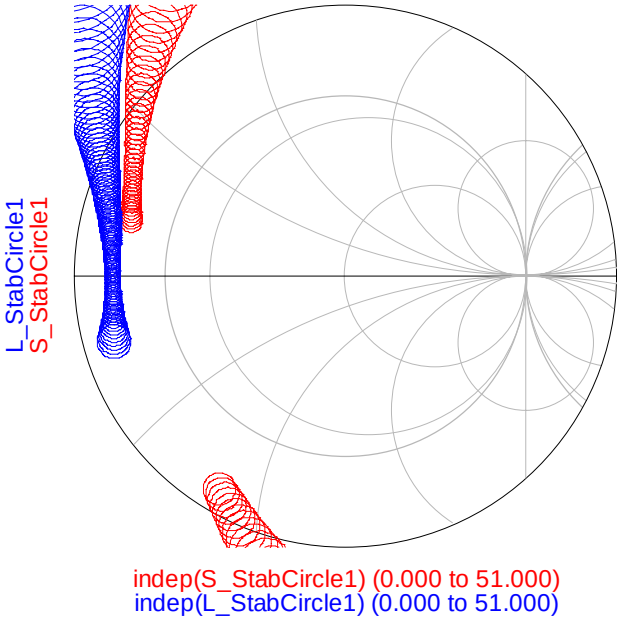


Figure 7.5 Source (Red) and load stability (blue) circle for V_{DS}=28V and frequency range of 3GHz to 4GHz

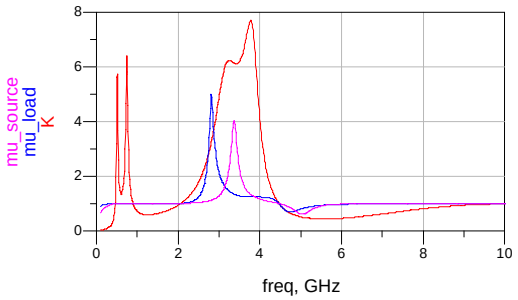


Figure 7.6(a): Stability factor from DC to 10GHz

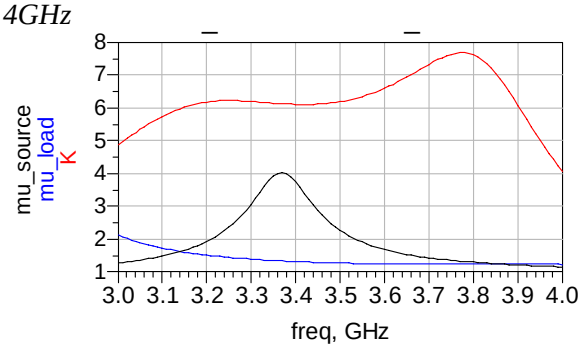


Figure 7.6(b): Zoomed graph of stability factor from 3GHz to 4GHz

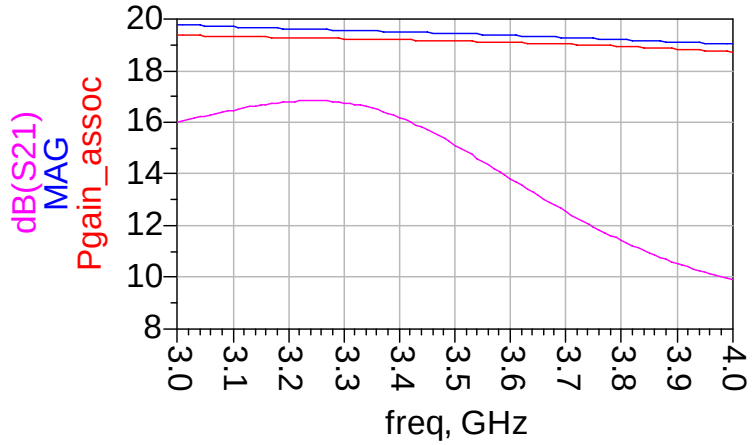


Figure 7.7: MAG (blue), associated power gain (red) and transducer gain (pink)

7.2 Input Network Design

7.2.1 Input Bias Network

If the transistor is to perform efficiently and consistently, it must be able to maintain its operating point throughout a variety of operating conditions. Therefore, an active bias network is designed to maintain a constant output voltage by compensating for fluctuations in input power and operating temperature. Input power quality is ensured by a 78L08 voltage regulator and temperature compensation is achieved with the use of a 2N2222

Bi-polar Junction Transistor (BJT) that is external from the LDMOS transistor but placed as close as possible to it. The voltage generated by this network can be tuned via a 200Ω potentiometer. The active bias network also features decoupling capacitors to minimize the RF interference from the adjacent input matching network.

The active bias network was modelled to be as accurate as possible in figure 7.8. A simple 8V source was used to represent the output of the voltage regulator, a SPICE model was used to represent the BJT and two variable resistors were used to model the potentiometer. Once the schematic was completed, another DC analysis was conducted. This time, the DC analysis was to study the circuit's behaviour and verify that the schematic can supply the required 2.3V to the transistor's gate. This was achieved by sweeping the potentiometer and reading the circuit's output voltage (labelled as VGS, as it represents the voltage applied to the transistor's gate). Since NXP's LDMOS model does not account for changes in temperature, thermal effects could not be studied. Therefore, operating temperature was kept to a constant 25^{o}C

As mentioned before, the potentiometer was modelled as two variable resistors (one resistor of variable value R1 and the other of value 200Ω minus R1). The graph in figure 7.9 indicates that with this 200Ω potentiometer, gate voltages between 1.5-2.9V can be achieved. This allows for quiescent drain currents between 3.5μA-2.3A. For the specifications of the project (IDQ = 319mA and VGS = 2.3V), this DC analysis indicates that the potentiometer should be somewhere in the middle of its range, with R1 roughly equal to 86.9Ω and R2 roughly equal to 113.1Ω.

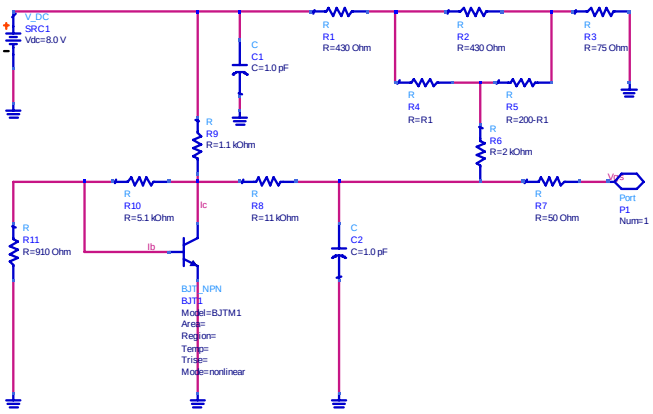


Figure 7.8: Input bias network design

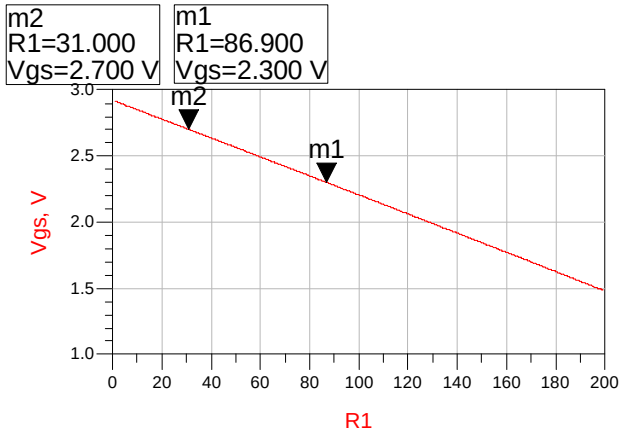


Figure 7.9: V_{GS} as function of potentiometer

7.2.2 Input Matching Network Design

While designing power amplifier, the most important thing in consideration is output power. The matching networks of this amplifier must be matched to give maximum power output with considerable efficiency. To transfer maximum power from source to transistor, source must be matched to conjugate of input impedance of transistor.

S-parameter simulations were used extensively for designing the input matching network. The networks were designed to match the impedance values obtained from calculation of input impedance using s-parameters.

From small signal s-parameter simulation, following values are obtained at 3.5GHz with drain bias voltage V_{DS}=28V and gate bias voltage V_{GS} = 2.3V.

S(1,1)	S(1,2)	S(2,1)	S(2,2)
0.400∠-104.381	0.005∠-26.781	5.703∠-114.538	0.756∠-167.424

Table 7.3: Small signal S-Parameter data for bias condition of V_{DS}=28V and V_{GS}=2.3V

By using these values, input impedance can be calculated which must be presented by input matching to gate of transistor to transfer maximum power from input source to transistor.

After mathematical calculations, the value comes out to be 34.58+j*29.15Ω.

Another way to verify these calculations is to do source pull simulation. Figure 7.10 shows result for source pull simulation.

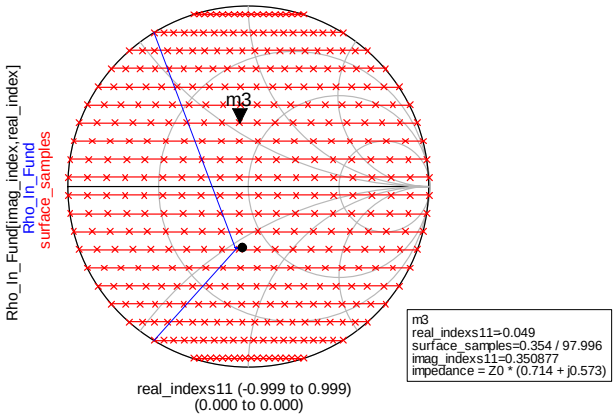


Figure 7.10: Source pull simulation (marker m3 shows source matching point)

Source pull gives source matching point impedance as 35.7+j*28.65Ω. By doing source pull for some fine surface samples, the results from source pull simulation and mathematical calculations are almost matched.

Next step is to design input matching network. Input matching network is designed using transmission line. A low pass network topology is used. Figure 7.11 shows the designed network.

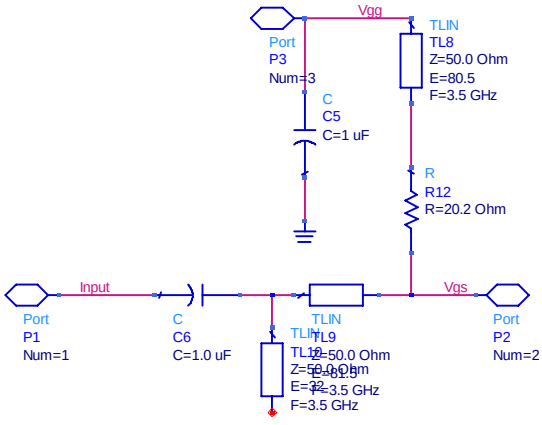


Figure 7.11 Input design network

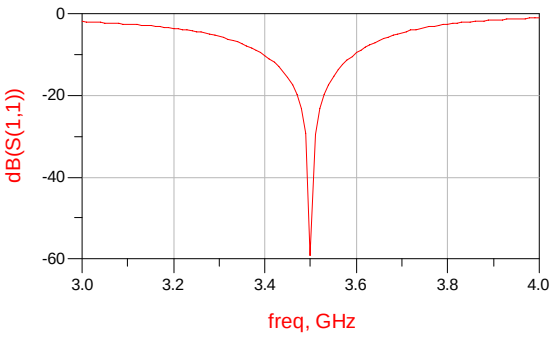


Figure 7.12 Return loss of network of figure 7.11

Resistance R_{12} and transmission line TL8 forms non ideal choke. TL9 and TL10 comprises low pass network which alongwith non ideal choke transfers 50Ω to required input source impedance. Capacitor C6 is used as d.c. blocking capacitor.

Figure 7.12 shows return loss presented by designed matching network. It has minimum at 3.5GHz. Figure 7.13 shows input matching network designed using micro-strip line.

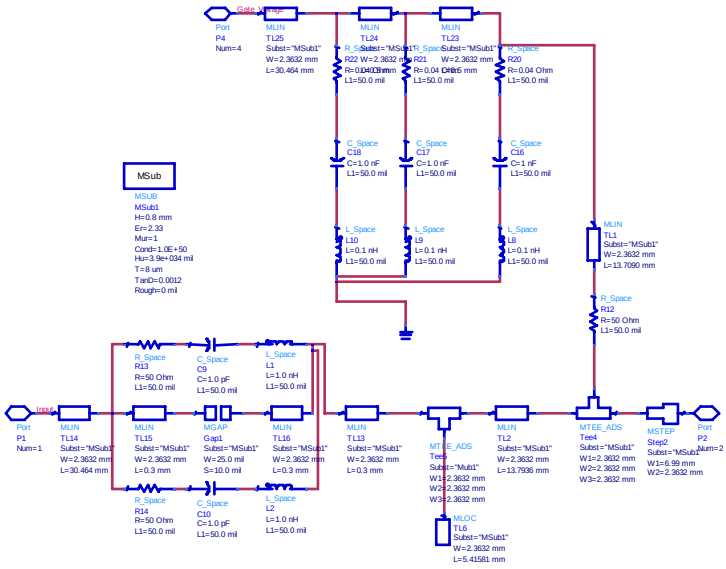


Figure 7.13: Input matching network implemented using microstrip line

DC block and AC short is implemented using parallel branch of lumped element. These blocks provide almost zero impedance effectively doing the work of DC block and AC short.

7.3 Design of Class AB Amplifier

7.3.1 Load Pull Analysis

Load Pull is a well-known measurement technique that is used to measure the power performance of a power amplifier/transistor vs. varying termination impedances. A typical load pull setup is comprised of a fundamental source and load tuner, biasing network attached to transistor. Load-pull simulation generates contours that indicate load impedances. These contours cause a certain power to be delivered to the load when they are presented to the output of a device along with the specified source impedances and available source power.

These simulations show the performance of the transistor under different load conditions using harmonic balance analysis. The load pull test templates in ADS were used to perform this test, because it would have been too complex of a task to write all the equations required to display the contour graphs. The results were relatively accurate for such a complex transistor model.

The load pull simulation is performed with V_{DS} = 28V, V_{GS}=2.3V with input power of 23dBm. The input power level is calculated for 1dB compression point. In order to get 44dBm (25W) output power with transistor having gain in range of 16dB to 20dB, 1dB compression point must be in range of 23dBm to 27dBm. We can choose lowest power since with increase in input power gain decreases. Therefore, input power level of 23dBm is selected for load pull simulation. The input frequency is set to 3.5GHz.

Figure 7.14 shows the result of load pull simulation. The estimated maximum efficiency is 63.14% and maximum output power is 45.74dBm. The points for maximum efficiency and for maximum power output are different. Since our main concern is efficiency, maximum efficiency point is considered as optimum load. The optimum load to be presented to output end of transistor comes out to be 5.870-j*1.566Ω. Corresponding efficiency is 63.14% and output power is 43.94dBm.

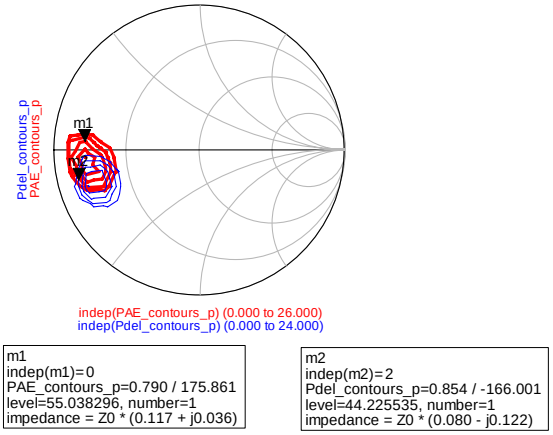


Figure 7.14(a): PAE (red) and power (blue) contours

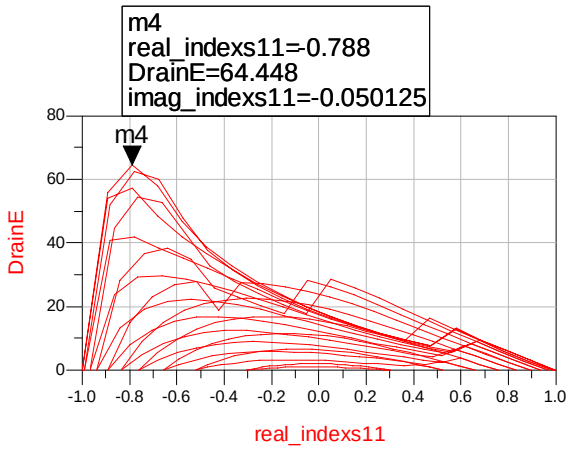


Figure 7.14(b): Drain efficiency

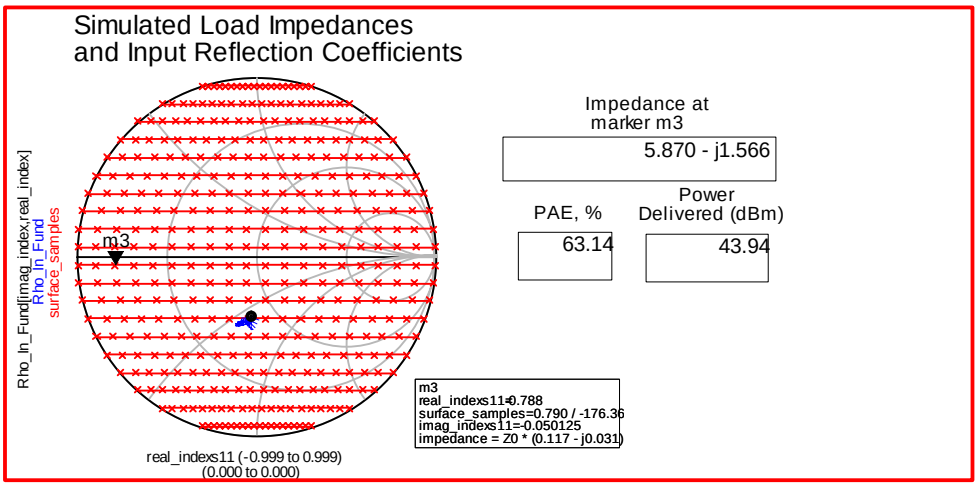


Figure 7.14(c): Simulated load impedance from fundamental load pull simulation

7.3.2 Output Matching Network

Using the simulated load pull results, load impedance to be presented to drain terminal is determined. Next step is to match the 50Ω termination to desired load. While designing class AB amplifier, the harmonic loads must be terminated with zero impedance. The output matching network must be designed in such way to present short at drain at second and higher harmonics.

Figure 7.15 shows designed output matching network. Transmission line TL13, TL14, TL15 and TL16 presents short at harmonic frequency up to fifth order. Next block is low pass network which shorts other higher harmonics and matches 50Ω load to desired load

impedance. Figure 7.16 shows simulated impedances up to fifth order on smith chart. Figure 7.17 shows output matching network implemented using microstrip line.

Table 7.4 shows impedance presented by output matching network to drain of transistor.

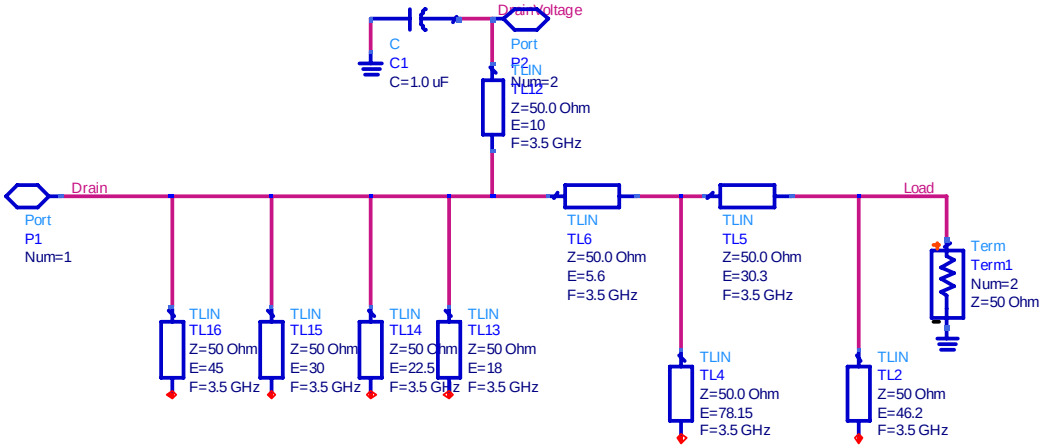


Figure 7.15 Output matching network

freq	Zin
3.500 GHz	6.067 / -14.701
7.000 GHz	2.500E-9 / -7.017E-5
10.50 GHz	2.500E-9 / -7.018E-5
14.00 GHz	2.500E-9 / -7.017E-5
17.50 GHz	2.500E-9 / -7.017E-5
21.00 GHz	2.500E-9 / -2.105E-4

Table 7.4: Impedance presented by output matching network

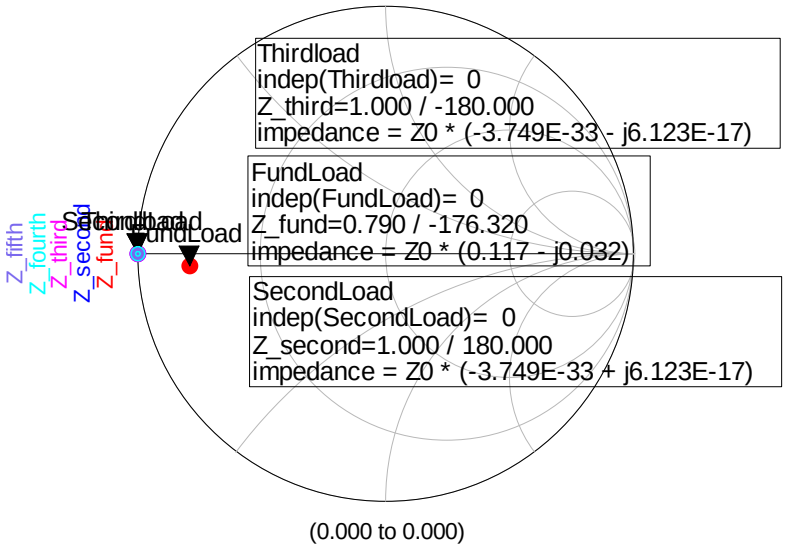


Figure 7.16: Simulated load impedance. Fundamental (red), second harmonic (blue)

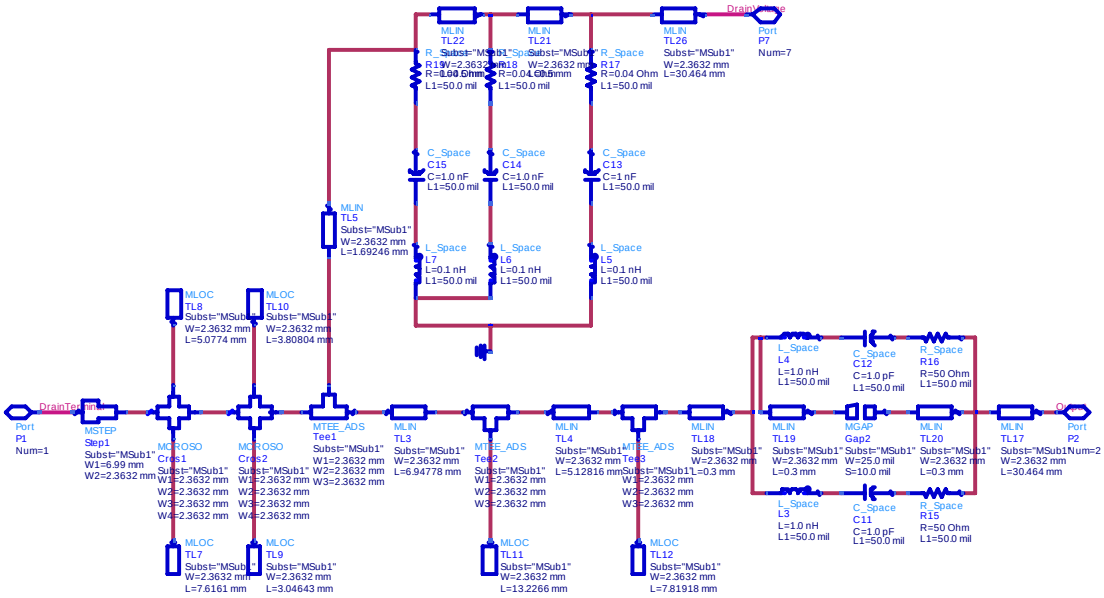


Figure 7.17: Output matching network using microstrip line

7.3.3 Overall Circuit and its Verification

7.3.3.1 Overall Circuit Design

Using networks designed above are assembled to generate overall circuit of Class AB amplifier. Figure 7.18 shows overall circuit of class AB amplifier and figure 7.19 shows design implemented using microstrip line. RT Duriod(5870) with ε_r=2.23 is used as substrate with height of substrate 0.8mm and thickness of conducting surface 8 μm.

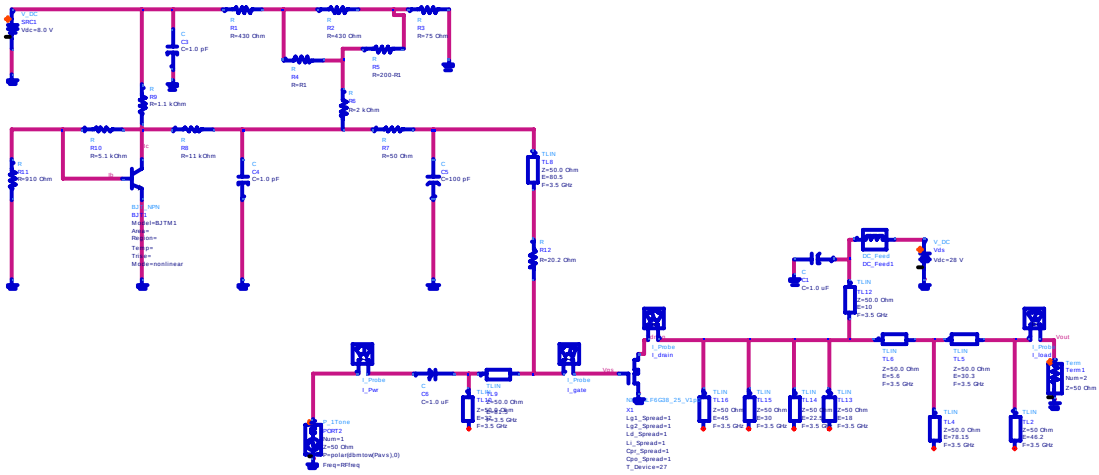


Figure 7.18: Overall circuit of Class AB amplifier

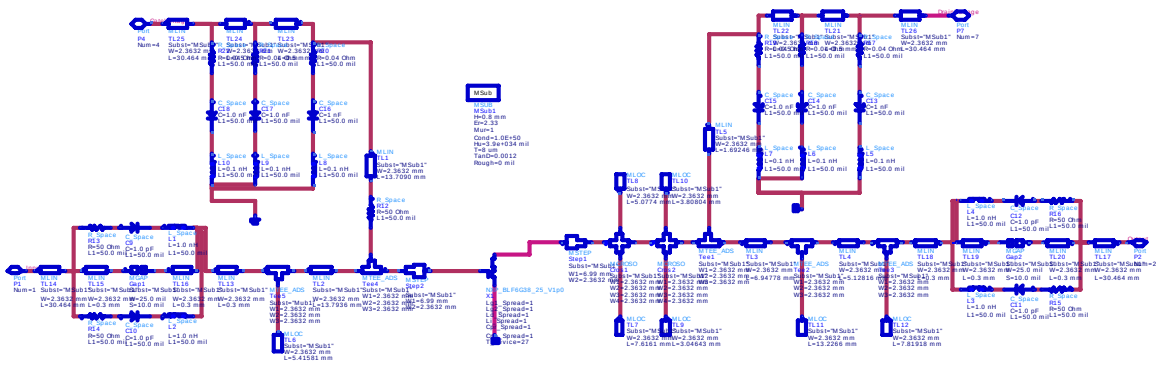


Figure 7.19: Circuit implemented using microstrip line

7.3.3.2 Verification

Next step is to verify the circuit for output power and efficiency. Harmonic balance simulation is dues for this purpose. 1-tone and 2-tone harmonic balance simulation is performed to find the output power and efficiency. In built ADS template is used for both simulation.

For one-tone simulation, power is swept from -10dBm to 38dBm with biasing condition described earlier. Following are the results for one-tone harmonic balance simulations.

Figure 7.21 shows the maximum achievable power added efficiency is 62.52% and drain efficiency 64.13% at fundamental output power of 44.8dBm.

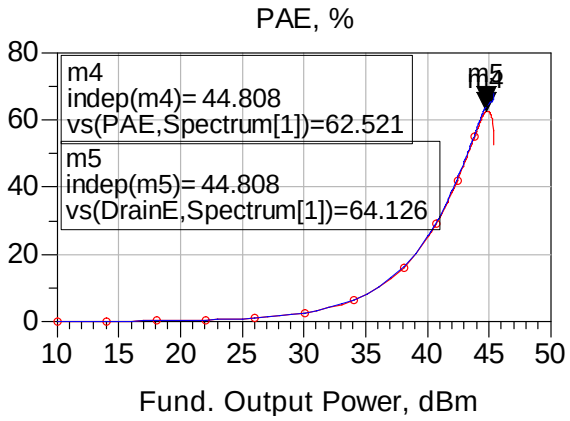


Figure 7.20: PAE and Drain efficiency

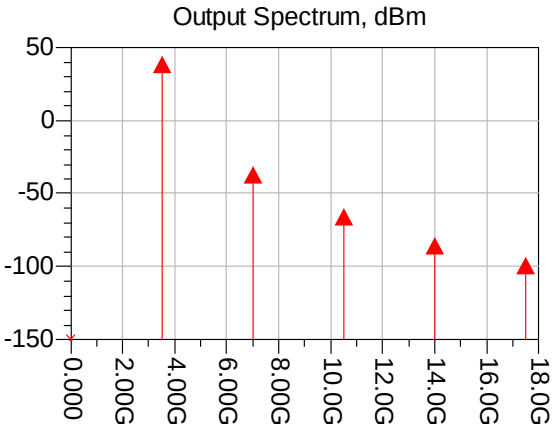


Figure 7.21: Output power spectrum

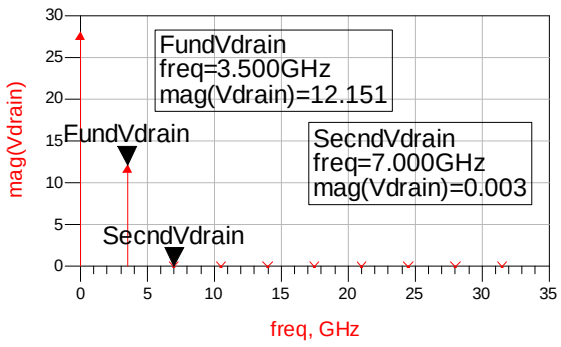


Figure 7.22: Drain voltage spectrum

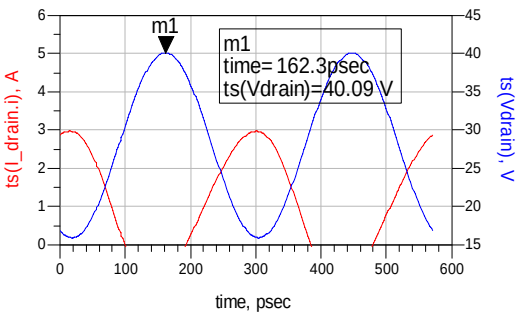


Figure 7.23: Drain current (red) and voltage (blue)

Figure 7.22 shows drain voltage spectrum. Harmonics are not present in the drain voltage spectrum of class AB amplifier as all harmonics are shorted.

Figure 7.23 depicts drain current and voltage waveform. Current and voltage are out of phase by 180^o due to the circuit topology. Since model is not giving access to the internal drain current, current waveform in figure 7.23 is truncated and only positive half is shown.

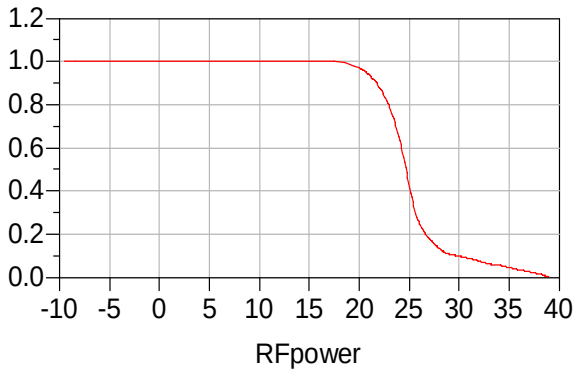


Figure 7.24: AM to AM conversion

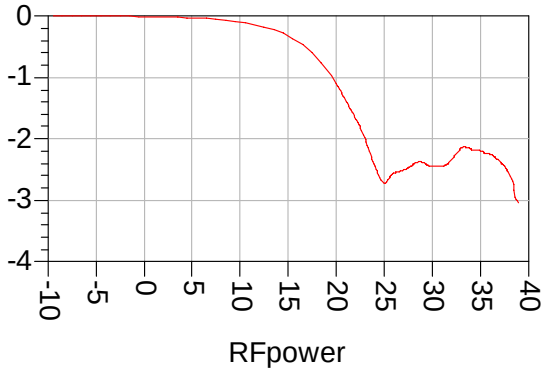


Figure 7.25: AM to PM conversion

Figure 7.24 and 7.25 shows effects of nonlinearity of internal components of transistor. Amplitude distortion (AM to AM conversion) can be accounted by using power input above 1dB compression point. The problem is due to phase distortion. The nonlinear components of transistor like output capacitance are the main culprit to cause phase distortion. The minimum the value of AM-PM conversion better is the linearity of designed amplifier. At input power level of 23dBm, phase distortion is around -2^o which is in range of acceptable level.

Next step is to perform two tone harmonic balance simulation. This is performed to evaluate the amplifier performance under two signals spaced vey near.

Two signal spaced apart by 100 kHz from each other are used as input in two tone simulation. ADS's built in template is used for data display. Following are results obtained from two-tone harmonic balance simulation.

Figure 7.26 shows maximum achievable efficiency is 50% under two tone condition which is under acceptable limit.

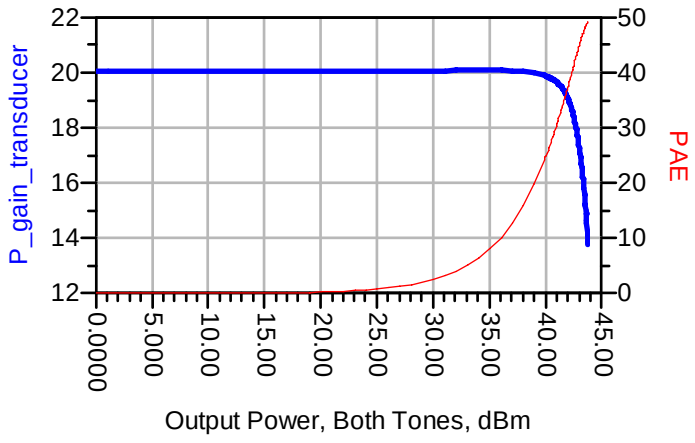


Figure 7.26: PAE (red) and gain (blue) for both tones

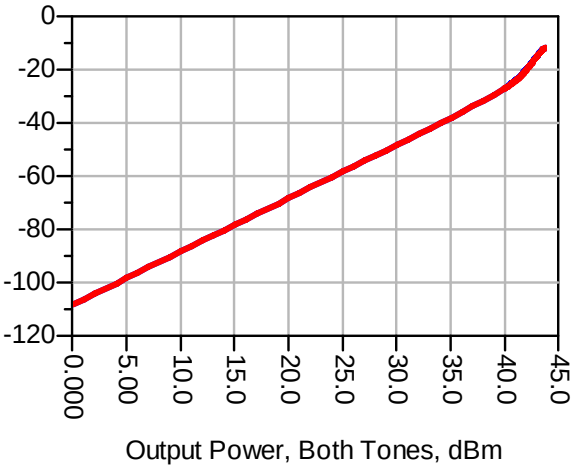


Figure 7.27: Third order IMD

Figure 7.28: Fifth order IMD

Third order harmonic and fifth order harmonic are -20dBc (figure 7.27) and -35dBc (figure 7.28) at output level of 42dBm which are bit larger than expected which shows the linearity decreased.

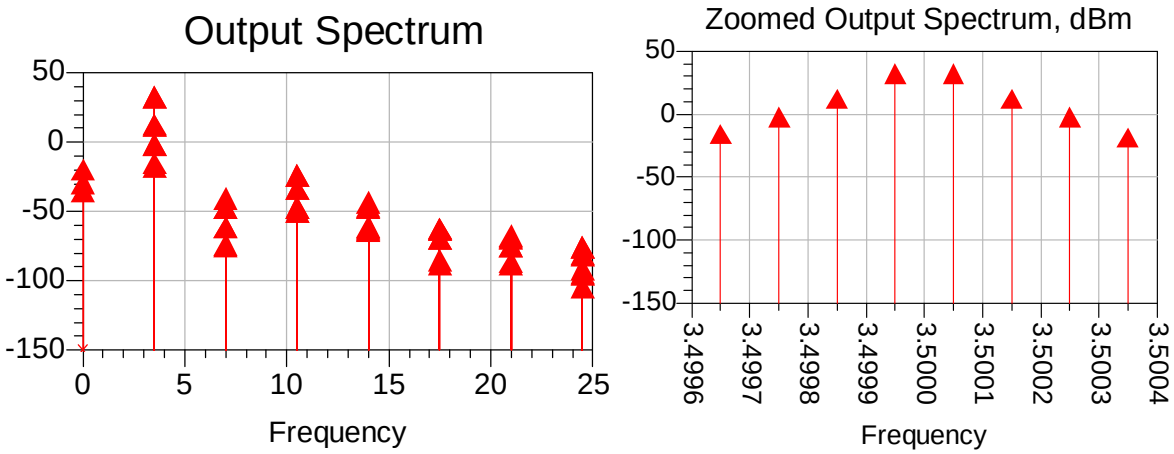


Figure 7.29: Output spectrum and zoomed spectra for centre frequency of 3.5 GHz

Class AB amplifier is designed is giving expected performance with efficiency of 62% and output power of 44 dBm. To implement above amplifier, physical layout is created. Physical layout is shown in appendix A.

7.4 Design of Class J Amplifier

7.4.1 Load Pull Analysis

7.4.1.1 Fundamental Load Pull Simulation

The load pull simulation is performed with V_{DS} = 28V, V_{GS}=2.3V with input power of 23dBm. The input power point is chosen as discussed in Class AB design. The input frequency is set to 3.5GHz.

Figure 7.30 shows the result of load pull simulation. The estimated maximum efficiency is 63.14% and maximum output power is 45.74dBm. The points for maximum efficiency and for maximum power output are different. Since our main concern is efficiency, maximum efficiency point is considered as optimum load. The optimum load to be presented to output end of transistor comes out to be 5.870-j*1.566Ω. Corresponding efficiency is 63.14% and output power is 43.94dBm.

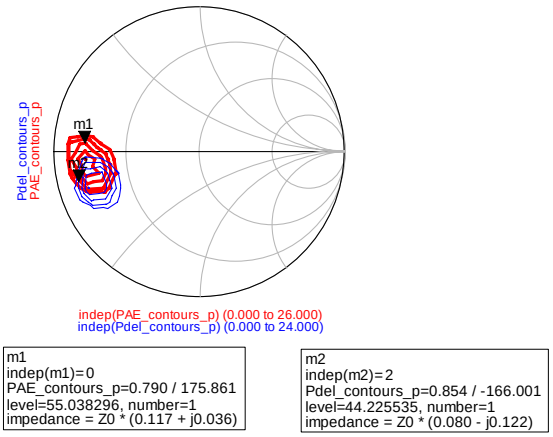


Figure 7.30(a): PAE (red) and power (blue) contours

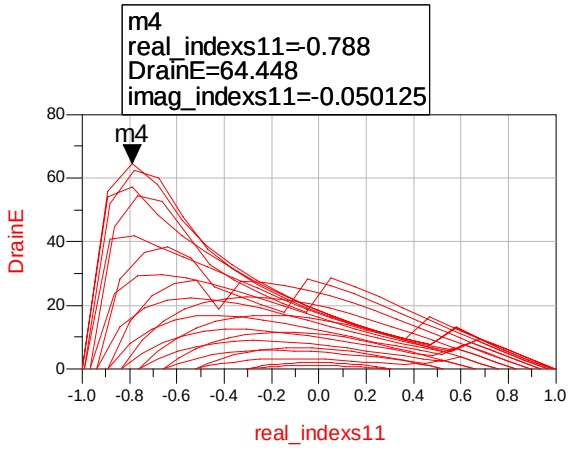


Figure 7.30(b): Drain efficiency

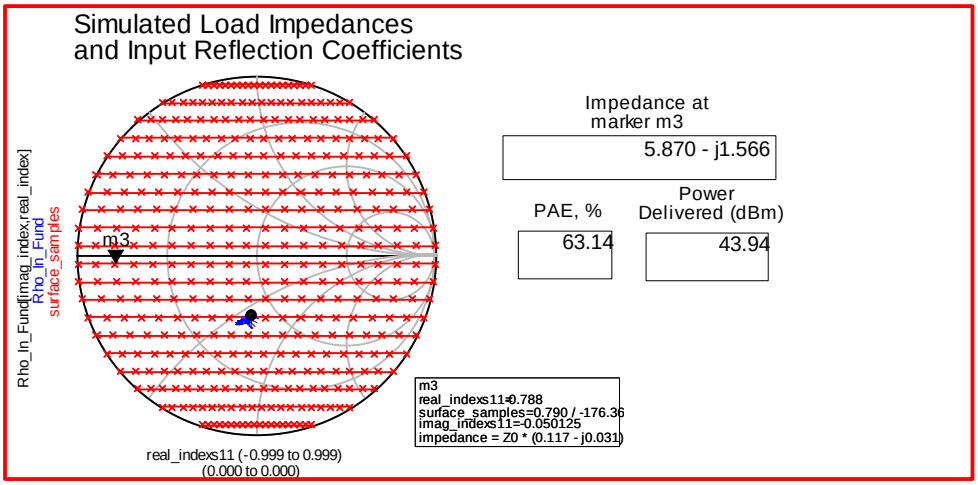


Figure 7.30(c): Simulated load impedance from fundamental load pull simulation

7.4.1.2 Second Harmonic Load Pull Simulation

The main requirement of Class J amplifier is tuning of second harmonic load. Second harmonic impedance must be set in such a way in order to increase the efficiency without any need to have a perfect short at higher harmonics as in case of class AB amplifier. Purpose of tuning second harmonic is to decrease power dissipation at second harmonic. Hence, as discussed earlier, second harmonic impedance must have real part zero while imaginary part inductive as fundamental load is capacitive.

Figure 7.31 shows imaginary part of second harmonic load swept for finding PAE and delivered output power. The highest achievable efficiency is 69% but output power also increases above the needed. So to compromise between efficiency and output power impedance of j*17.89Ω is used. Values of efficiency and output power are 67.15% and 44.8dBm respectively.

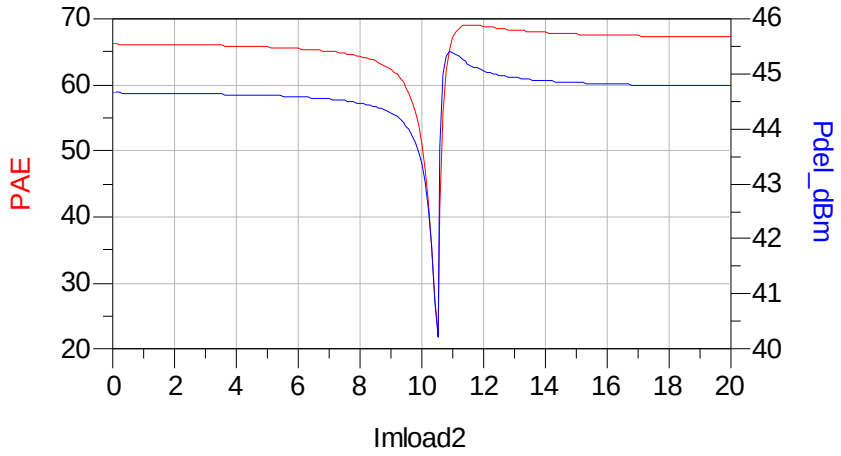


Figure 7.31: PAE and Pdel as function of imaginary part of second harmonic load

7.4.2 Output Matching Network

Using the simulated load pull results, load impedance to be presented to drain terminal is determined. Next step is to match the 50Ω termination to desired load. While designing class AB amplifier, the harmonic loads must be terminated with zero impedance. The output matching network must be designed in such way to present short at drain at second and higher harmonics.

Because we want to realize a class J power amplifier, we should choose a topology which allows easy tuning of the second harmonic load. Normally, the output of the power amplifier is connected to a 50 Ohms load and the optimum load for second harmonic load is purely inductive. So, we can use an inductive component and second harmonic short part to realize the second harmonic load.

TL3 is the second harmonic short part. It's a quarter-wave transmission line at 7 GHz. The input impedance of this transmission line is:

$$Z_{input} = \frac{Z_0^2}{Z_L}$$

Z_0 is the characteristic impedance of transmission line and Z_L is the load at the end of the transmission line. It's an open stub. So, Z_L is infinite and the input impedance of transmission line is 0. That means other components behind this transmission will not affect the second harmonic load. So, if we only use reactive components before this transmission line, we can get a pure reactive load for second harmonic load.

For the fundamental frequency (3.5 GHz), TL3 is like a capacitor:

$$Z_{input} = Z_0 \times \frac{1}{j \times \tan(\beta l)} = Z_0 \times \frac{1}{j \times tan45} = -j \times Z_0$$

So, we can use the characteristic impedance of TL2 to tune the fundamental load and don't affect the second harmonic load simultaneous.

TL 2 blocks the influence of other components behind TL2 for second harmonic load. We need other components to match the fundamental harmonic load. Normally, the output load of power amplifier is 50 Ohms and the load we need is smaller than 50 Ohms. So, we can use a low pass matching network to transform the 50 Ohms load to the load we need.

Since second harmonic tuning influences fundamental load, second harmonic load must be matched first and then fundamental load is tuned accordingly using low pass matching network.

Figure 7.32 shows designed output matching network. Transmission line TL12 and capacitor C7 along with TL11 are used to tune second harmonic impedance. Next block is low pass network which shorts other higher harmonics and matches 50Ω load to desired load impedance. Figure 7.33 shows simulated fundamental and second harmonic impedances on smith chart. Figure 7.34 shows output matching network implemented using microstrip line.

Table 7.5 shows impedance presented by output matching network to drain of transistor.

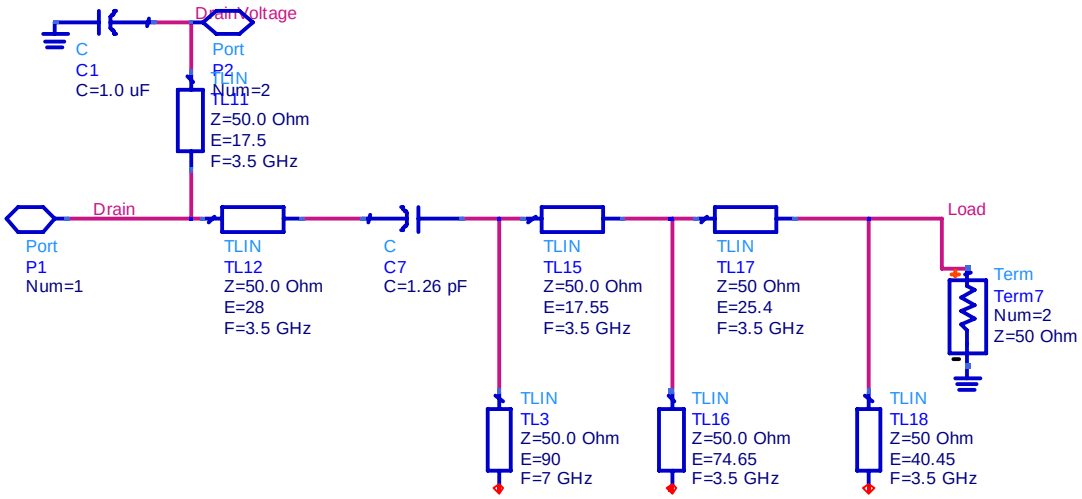


Figure 7.32: Output matching network

freq	Zin
3.500 GHz	6.093 / -14.965
7.000 GHz	17.878 / 90.000
10.50 GHz	53.720 / 85.668
14.00 GHz	25.125 / 64.078
17.50 GHz	84.913 / -22.891
21.00 GHz	15.647 / -90.000

Table 7.5: Impedance presented by output matching network

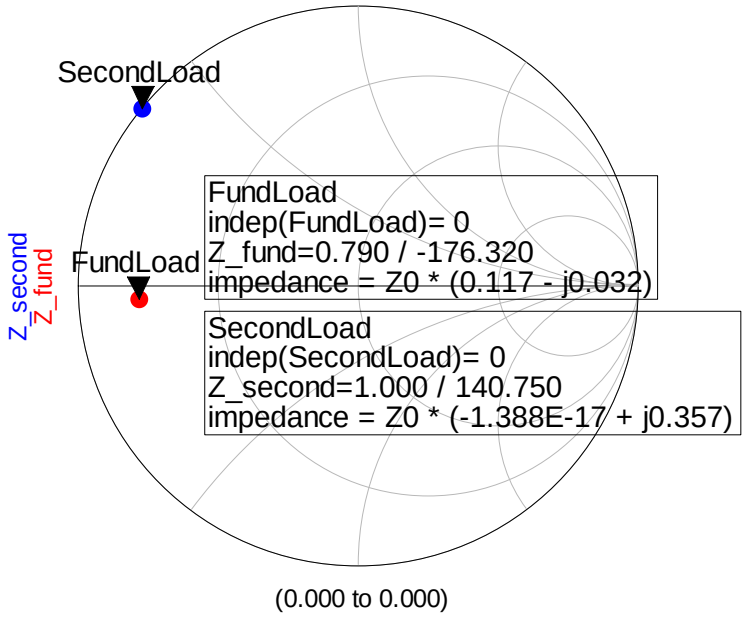


Figure 7.33: Simulated load impedance. Fundamental (red), second harmonic (blue)

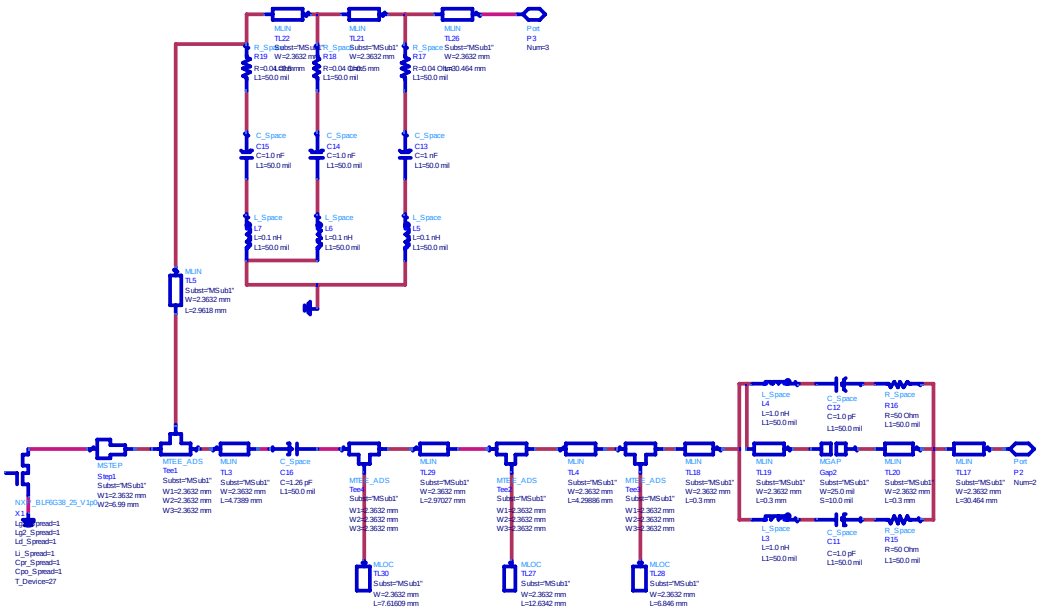


Figure 7.34: Output matching network using microstrip line

7.4.3 Overall Circuit and its Verification

7.4.3.1 Overall Circuit Design

Using networks designed above are assembled to generate overall circuit of Class J amplifier. Figure 7.35 shows overall circuit of class j amplifier and figure 7.36 shows design implemented using microstrip line. RT Duriod(5870) with ε_r=2.23 is used as substrate with height of substrate 0.8mm and thickness of conducting surface 8 µm.

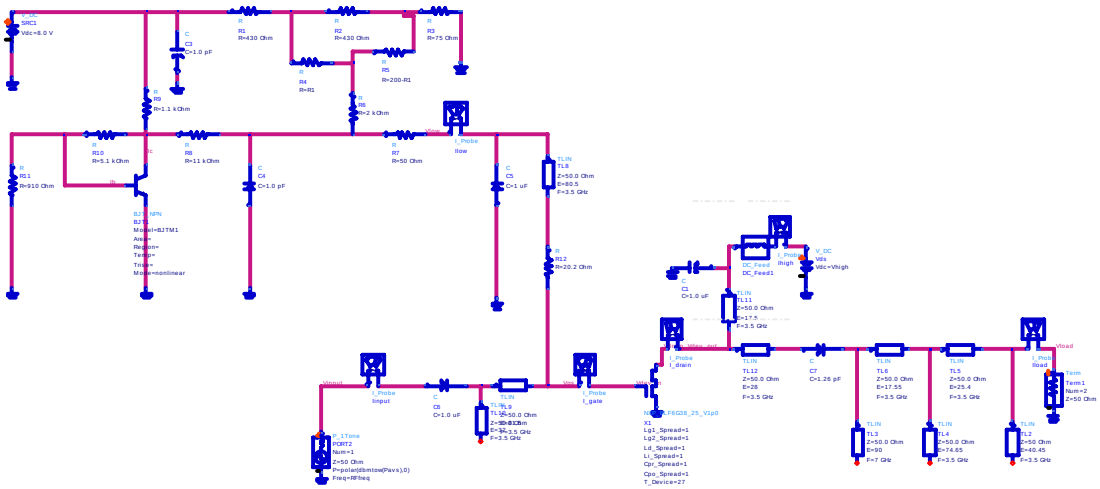


Figure 7.35: Overall circuit of Class J amplifier

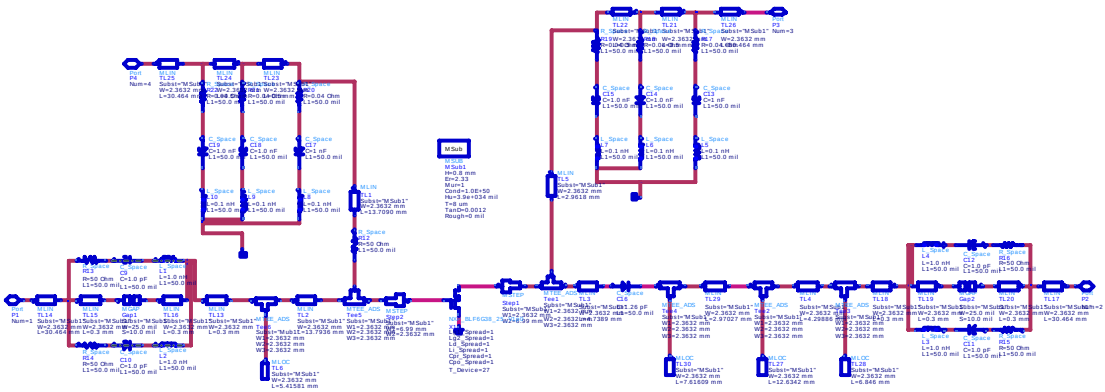


Figure 7.36: Circuit implemented using microstrip line

7.4.3.2 Verification

Next step is to verify the circuit for output power and efficiency. Harmonic balance simulation is dues for this purpose. 1-tone and 2-tone harmonic balance simulation is performed to find the output power and efficiency. In built ADS template is used for both simulation.

For one-tone simulation, power is swept from -10dBm to 38dBm with biasing condition described earlier. Following are the results for one-tone harmonic balance simulations.

Figure 7.27 shows the maximum achievable power added efficiency is 67.36% and drain efficiency 69.36% at fundamental output power of 44.74dBm.

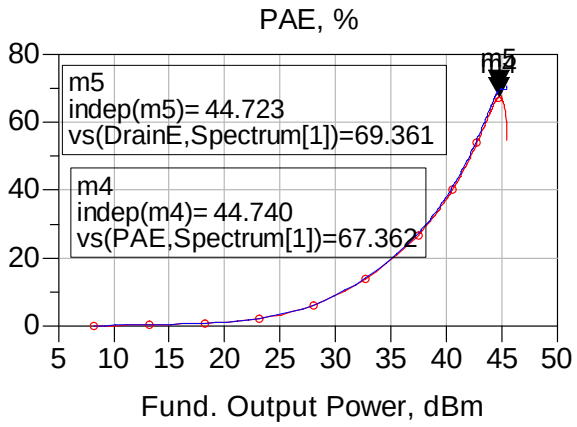


Figure 7.37: PAE and Drain efficiency

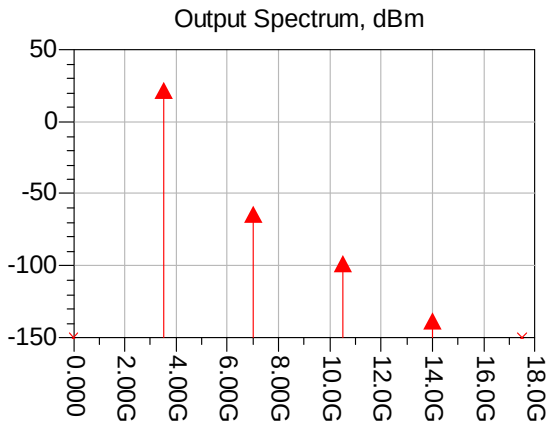


Figure 7.38: Output power spectrum

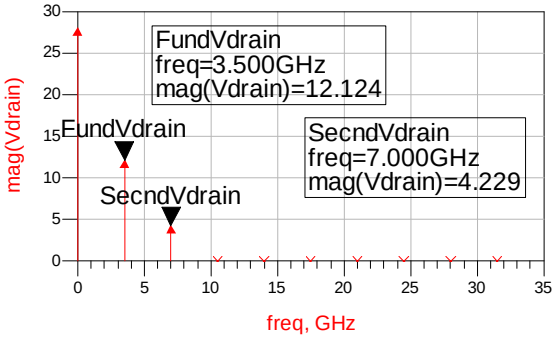


Figure 7.39: Drain voltage spectrum

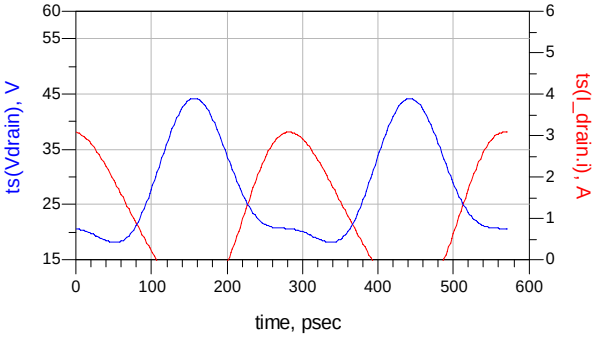


Figure 7.40: Drain current (red) and voltage (blue)

Figure 7.39 shows drain voltage spectrum. Second harmonic component is present at drain. The ratio of fundamental to second harmonic voltage is approximately equal to 3. This is one of the conditions for Class J amplifier which is satisfied.

Figure 7.40 depicts drain current and voltage waveform. Current and voltage are out of phase by 180^{o} due to the circuit topology. Since model is not giving access to the internal drain current, current waveform in figure 7.40 is truncated and only positive half is shown. Drain voltage waveform is half sinusoidal due to influence of second harmonic impedance.

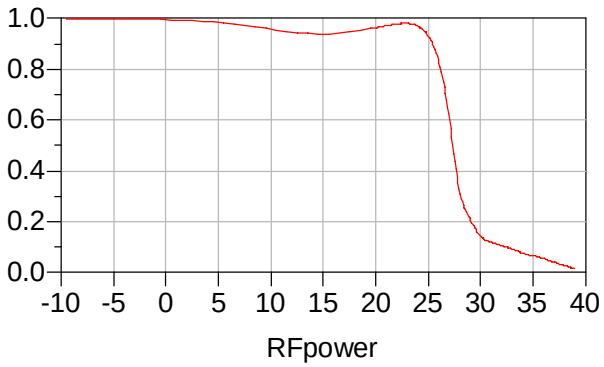


Figure 7.41: AM to AM conversion

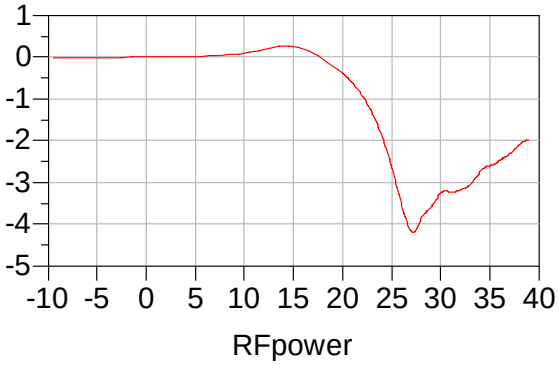


Figure 7.42: AM to PM conversion

Figure 7.41 and 7.42 shows effects of nonlinearity of internal components of transistor. Amplitude distortion (AM to AM conversion) can be accounted by using power input above 1dB compression point. The problem is due to phase distortion. The nonlinear components of transistor like output capacitance are the main culprit to cause phase distortion. The minimum the value of AM-PM conversion better is the linearity of designed amplifier. At input power level of 23dBm, phase distortion is around -2^{o} which is in range of acceptable level. In comparison with likely biased class AB amplifier, the linearity performance of Class J amplifier is upto mark and is in acceptable limits.

Next step is to perform two tone harmonic balance simulation. This is performed to evaluate the amplifier performance under two signals spaced vey near.

Two signal spaced apart by 100 kHz from each other are used as input in two tone simulation. ADS's built in template is used for data display. Following are results obtained from two-tone harmonic balance simulation.

Figure 7.26 shows maximum achievable efficiency increased to 56% under two tone condition as compared to Class AB amplifier.

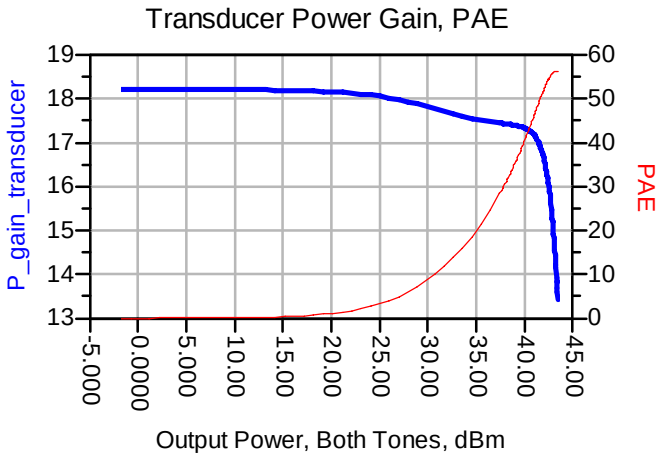


Figure 7.43: PAE (red) and gain (blue) for both tones

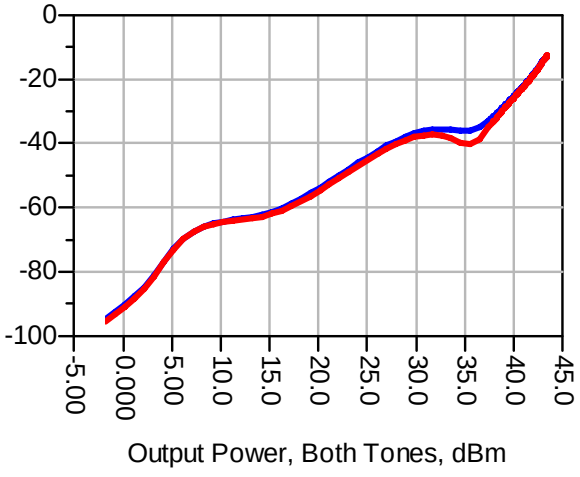


Figure 7.44: Third order IMD

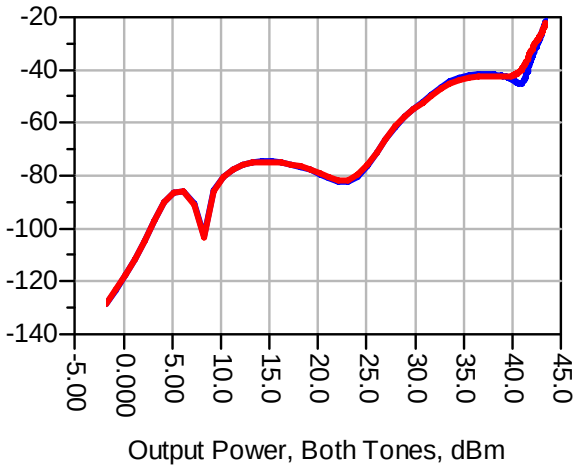


Figure 7.45: Fifth order IMD

Third order harmonic and fifth order harmonic are -17dBc (figure 7.44) and -32dBc (figure 7.45) at output level of 42dBm which are bit larger than corresponding Class AB amplifier. The non-linear component and intermodulation distortion is increased.

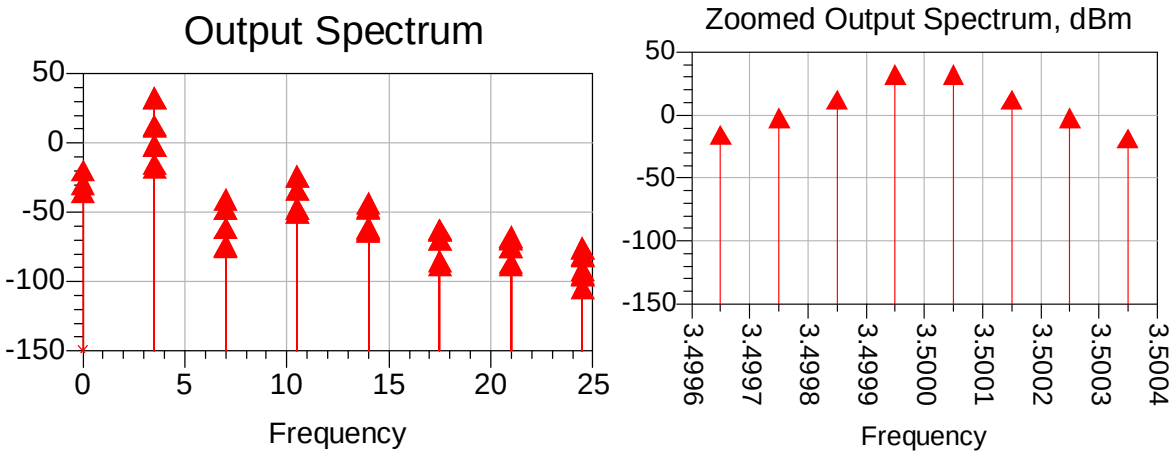


Figure 7.46: Output spectrum and zoomed spectra for centre frequency of 3.5 GHz

Class J amplifier is designed is giving performance superior to likely biased Class AB amplifier with efficiency of 67.36% and output power of 44 dBm. To implement above amplifier, physical layout is created. Physical layout is shown in appendix B.

Chapter 8
Conclusion and Future Work

8.1 Conclusion

The main objective of this project was to design a highly efficient power amplifier using LDMOS technology. Two amplifiers are designed and analysed using 25W LDMOS transistor BLF6G38S-25 from NXP semiconductors at working frequency of 3.5GHz.

First is class AB amplifier. The designed circuit gives efficiency of 62.5% with output power of 44.8 dBm. The linearity performance of this amplifier is within the limits to be accepted.

Another is Class J amplifier. This harmonic tuned version of deeply biased Class AB amplifier gives the performance as per the design goal established. The power added efficiency of Class J amplifier is 67.36% with corresponding drain efficiency of 69.36% with maximum power output of 44.8dBm.

As compared to likely biased Class AB amplifier, efficiency performance of Class J amplifier is more by nearly 5% at same output level.

8.2 Future Work

The layout developed using ADS momentum is not fabricated to develop physical circuit. In order to verify the designed circuit, physical circuit could be developed. Measurement taken form that circuit and simulation result will be compared.

Since the model obtained form NXP is not perfect and is not providing access to internal drain current, perfect characterization was not possible. One can model the transistor using mathematical models in order to characterize LDMOS technology for high frequency application,

References

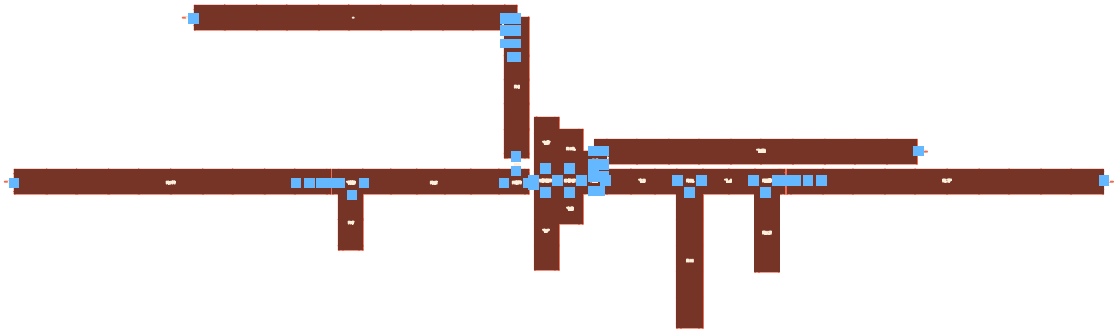
1. S. C. Cripps, "RF Power amplifier for wireless communication", *2nd ed, Artech House, 2006.*
2. S. C. Cripps, "Advanced techniques in RF power amplifier design", *2nd Edition , Artech House, 2006*
3. M. Albulet, RF Power Amplifiers, Noble Publishing, Atlanta, GA, 2001.
4. P. Wright, J. Lees, P. J. Tasker, J. Benedikt, and S. C. Cripps, "An efficient, linear, broadband class-J-mode PA realised using RF waveform engineering," in *IEEE 2009 MTT-S Int. Microwave Symposium Digest, June 2009, pp. 653–656.*
5. P. Wright, J. Lees, J. Benedikt, P. J. Tasker, and S. C. Cripps, "A Methodology for Realizing High Efficiency Class-J in a Linear and Broadband PA," *IEEE Transactions on Microwave Theory and Techniques, vol. 57, no. 12, pp. 3196–3204, 2009.*
6. S.M.lavi, M.Marchetti, L.C.N.de.Vreede, Fred van Rijs. "High-Efficiency Envelope Tracking operation through Second Harmonic Manipulation"
7. Frederick H. Raab, "Idealized Operation of the Class E Tuned Power Amplifier". IEEE Transactions on Circuits and Systems, VOL.CAS-24, no.12, pp.725-735, December 1977.
8. Frederick H. Raab, "Class-E, Class-C, and Class-F power amplifiers Based Upon a Finite Number of Harmonics". IEEE Transactions on Microwave Theory and Techniques, VOL.49, NO.8, pp.1462-1468, August 2001.
9. Adahl, H. Zirath, "An 1 GHz class E LDMOS power amplifier," 33rd European Microwave Conference, Vol. 1, Page(s):285 - 288, Oct. 2003.
10. K. Mimis, K.A. Morris and J.P. McGeehan. "A 2GHz GaN Class-J Power Amplifier for Base Station Applications", *IEEE Topical conference on Power Amplifiers for Wireless and Radio applications, 2011. pp.* 5-8
11. Intel Technology Journal: *RF System and Circuit Challenges for WiMax 198, Issue 3, Volume 08, August 20-2004.*
12. H. Sigg, G. Vendelin, T. Cauge, and J. Kocsis. "D-MOS Transistor for Microwave Applications." *IEEE Transaction on Electron Devices. Vol. ED-19, No. 1, Jan. 1972. pp 45-54.*
13. G. Ma, W. Burger, C. Dragon, and T. Gillenwater. "High Efficiency LDMOS Power FET for Low Voltage Wireless Communications." *Proceedings of IEDM. Dec. 1996. pp 91-94.*
14. A. Wood, C. Dragon, and W. Burger. "High Performance Silicon LDMOS Technology for 2GHz RF Power Amplifier Applications." *Proceeding of IEDM. Dec. 1996. pp 87-90.*
15. H. M. Nemati, C. Fager, M. Thorsell, and H. Zirath, "High-Efficiency LDMOS Power-Amplifier Design at 1 GHz Using an Optimized Transistor Model," *IEEE*

Transactions on Microwave Theory and Techniques, vol. 57, no. 7, pp. 1647–1654, 2009.

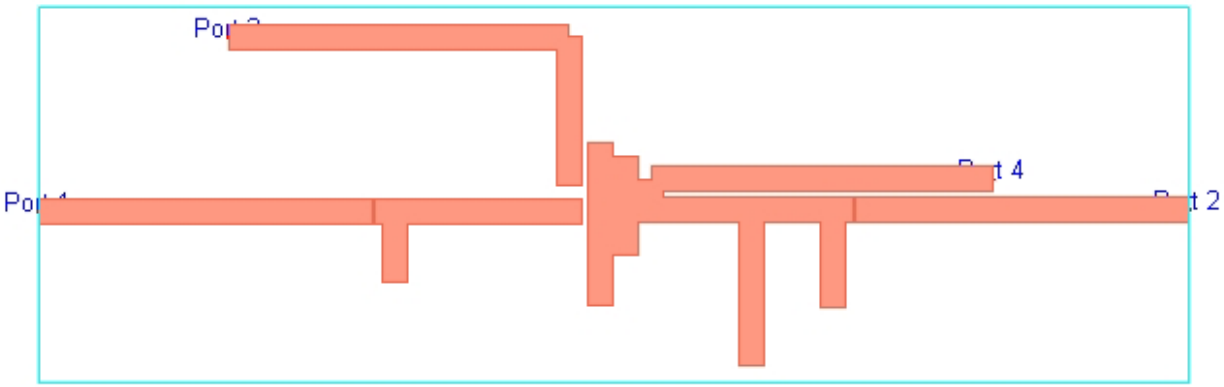
16. S. C. Cripps, P. Tasker, A. Clarke, J. Lees, and J. Benedikt, "On the Continuity of High Efficiency Modes in Linear RF Power Amplifiers," *IEEE Microwave and Wireless Components Letters,* vol. 19, no. 10, pp. 665–667, 2009.
17. M. M. Ebrahimi, M. Helaoui, and F. Ghannouchi, "Trading-off stability for efficiency in designing switching-mode GaN PAs for WiMAX applications," in *IEEE 2009 Asia Pacific Microwave Conference,* December 2009, pp. 2348–2351.
18. A. Sheikh, C. Roff, J. Benedikt, P. J. Tasker, B. Noori, J. Wood, and P. H. Aaen, "Peak Class F and Inverse Class F Drain Efficiencies Using Si LDMOS in a Limited Bandwidth Design," *IEEE Microwave and Wireless Components Letters, vol. 19, no. 7, pp. 473–475, 2009.*

Appendix

A: Layout of Class AB amplifier

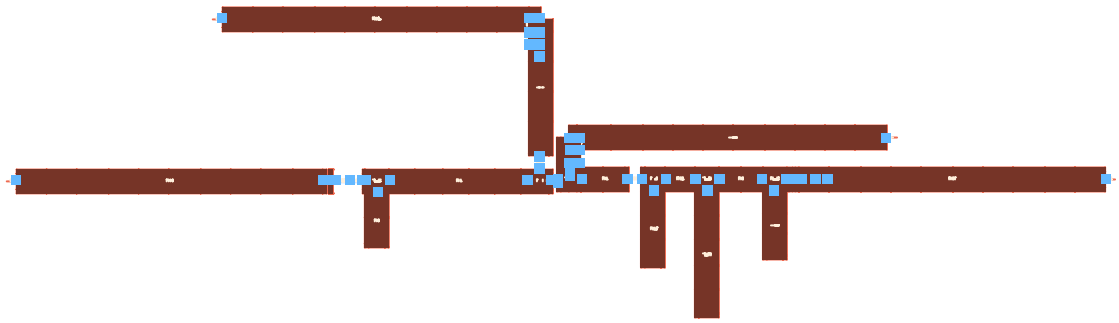


Momentum diagram of Class AB amplifier

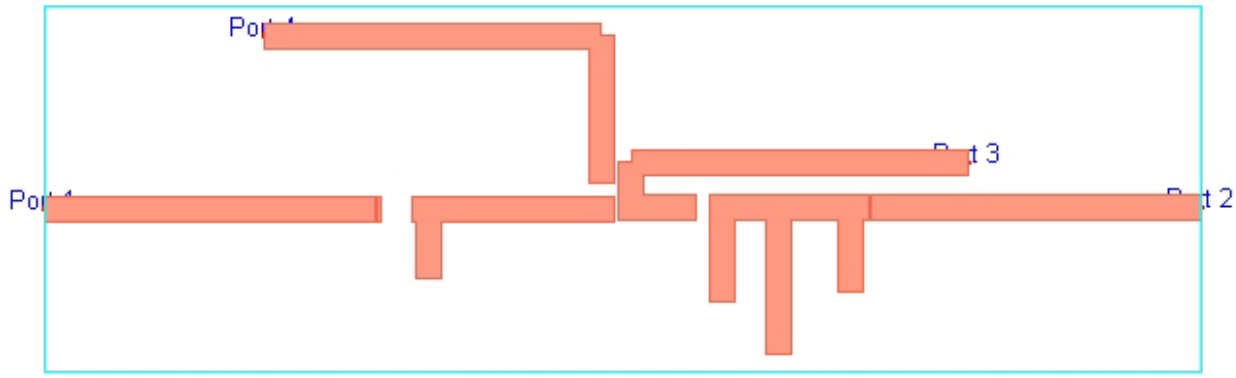


Visualization of above layout

B: Layout of Class J Amplifier



Momentum diagram of Class J amplifier



Visualization of above layout