

A  
Dissertation  
On

# DESIGN OF PARALLEL ARCHITECTURE USING MSP430 & VIRTEX-4

Submitted in Partial fulfillment of the requirement  
For the award of Degree of

**MASTER OF TECHNOLOGY  
(VLSI DESIGN & EMBEDDED SYSTEM)**

Submitted By:  
**PIYUSH GUPTA**  
12/VLSI/09

Under the Guidance of:  
**PROF. RAJIV KAPOOR**



DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING  
DELHI TECHNOLOGICAL UNIVERSITY, DELHI  
(FORMERLY DELHI COLLEGE OF ENGINEERING)  
2009-2011

**DELHI TECHNOLOGICAL UNIVERSITY, DELHI**  
Department of Electronics & Communication Engineering



## CERTIFICATE

---

---

This is certified that the dissertation entitled “**Design a parallel architecture using MSP430 and Virtex-4**” is a work of **Piyush Gupta** (University Roll No. 125/VLSI/09), a student of Delhi Technological University. This work was completed under my direct supervision and guidance and forms a part of the Master of Technology (VLSI Design and Embedded System) course and curriculum. He has completed his work with utmost sincerity and diligence.

The work embodied in this major project has not been submitted for the award of any other degree to the best of my knowledge.

Dr. Rajiv Kapoor  
Project Guide & Head of Dept.,  
Electronics & Communication Engg.  
Delhi Technological University, Delhi  
Date - 22/06/2011

# ACKNOWLEDGEMENT

---

It is distinct pleasure to express my deep sense of gratitude and indebtedness to my project guide **Prof. Rajiv Kapoor**, HOD, Department of Electronics and communication, Delhi Technological University, for his invaluable guidance, encouragement and patient reviews. His continuous inspiration only has made me complete this dissertation. Without his help and guidance, this dissertation would have been impossible. He remained a pillar of help throughout the project.

I am very thankful to the entire faculty and staff members of Electronics & Communication Engineering Department for their direct or indirect help, cooperation, love and affection.

I gratefully acknowledge for the best wishes and prayers of all my friends specially Saurabh Chitransi and Prateek Kabra.

I owe the most to my family for their love and support, who has given me enormous support. Lastly I like to remember the mercy and blessings of Almighty, on whose desire I have come to this level of career in my life.

**Piyush Gupta**  
(12/VLSI/09)

# ABSTRACT

---

---

The exponentially increasing demands for computationally intensive real-time signal processing applications outpace the performance improvements of each new generation of processors. With each passing year, more applications require tremendous computing capabilities that current processors cannot achieve. By coordinating the activities of individual processors, parallel processing offers the performance required by these applications. DSP applications are particularly suited for parallel processing because they are computationally intensive, highly parallel, highly structured, and often, periodic. Moreover, parallel multiprocessor systems have many benefits over single-processor systems. Parallel multiprocessor systems have virtually unlimited performance, better fault tolerance, scalability, flexibility, and upgradability. For these reasons, many high-end DSP applications, such as imaging, graphics, and data processing already benefit from parallel processing.

# TABLE OF CONTENTS

---

---

	<b>Page No.</b>
<b>Chapter 1: Introduction</b>	<b>1-3</b>
<b>1.1 On-Chip Parallel Processing</b>	<b>1</b>
<b>1.1.1 Superpipelining</b>	<b>2</b>
<b>1.1.2 Superscaling</b>	<b>2</b>
<b>1.1.3 Multi-CPU Integration</b>	<b>2</b>
<b>1.2 Off-Chip Parallel Processing</b>	<b>3</b>
<b>Chapter 2: Literature Survey</b>	<b>4-21</b>
<b>2.1 MSP430</b>	<b>4</b>
<b>2.1.1 Central Processing Unit</b>	<b>5</b>
<b>2.1.2 Program Memory</b>	<b>5</b>
<b>2.1.3 Data Memory</b>	<b>6</b>
<b>2.1.4 Operation Control</b>	<b>6</b>
<b>2.1.5 Peripherals</b>	<b>6</b>
<b>2.1.6 Oscillator and Clock Generator</b>	<b>7</b>
<b>2.1.7 Operating Modes</b>	<b>7</b>
<b>2.1.8 Interrupt Processing</b>	<b>10</b>
<b>2.1.9 Memory Mapping</b>	<b>11</b>
<b>2.1.10 16-Bit CPU</b>	<b>13</b>
<b>2.1.11 FLL Clock Module</b>	<b>14</b>
<b>2.1.12 Digital I/O Configuration</b>	<b>15</b>
<b>2.1.13 Timers</b>	<b>16</b>
<b>2.1.14 USART Peripheral Interface</b>	<b>17</b>
<b>2.1.15 ADC12+2 A-To-D Converters</b>	<b>17</b>
<b>2.1.16 Advantages of the MSP430 Concept</b>	<b>18</b>
<b>2.2 Virtex-4</b>	<b>20</b>
<b>2.2.1 Features</b>	<b>20</b>

<b>Chapter 3:</b>	<b>Hardware Design</b>	<b>22-28</b>
	3.1 Hardware Design of MSP430	22
	3.1.1 MSP-EXP430F5438 Experimenter Board	23
	3.1.2 User Interfaces	23
	3.1.3 Communication Peripherals	24
	3.2 Hardware Design of Virtex-4	26
	3.2.1 Features	27
<b>Chapter 4:</b>	<b>Parallel Architecture Design</b>	<b>29-31</b>
	4.1 Design Goal	30
	4.2 Design Consideration	30
	4.3 Asynchronous Communication	30
<b>Chapter 5:</b>	<b>Data Flow Design</b>	<b>32-36</b>
	5.1 Algorithm	33
<b>Chapter 6:</b>	<b>Implementation and Result</b>	<b>37-54</b>
<b>Chapter 6:</b>	<b>Conclusion</b>	<b>55</b>
<b>Chapter 6:</b>	<b>Future Scope of Work</b>	<b>56</b>
	<b>References</b>	<b>57</b>

## LIST OF FIGURES

---

<b>S.No.</b>	<b>Title</b>	<b>Page No.</b>
Figure 2.1	Functional Block Diagram of MSP430	5
Figure 2.2	Active and Low power Modes	10
Figure 2.3	Memory Mapping	12
Figure 2.4	Memory Address	12
Figure 2.5	CPU Registers	13
Figure 2.6	Status Register	14
Figure 2.7	FLL Clock Module	15
Figure 2.8	Virtex-4 FPGA Ordering Information	21
Figure 3.1	MSP430F5438A microcontroller	22
Figure 3.2	MSP-EXP430F5438 Experimenter Board	23
Figure 3.3	Virtex-4 ML401 evaluation platform	26
Figure 3.4	Block Diagram of ML401	27
Figure 4.1	Parallel architecture	28
Figure 4.2	USART	31
Figure 6.1	Transmitter and Receiver module	51