A
Dissertation
On

DESIGN OF PARALLEL ARCHITECTURE USING MSP430 & VIRTEX-4

Submitted in Partial fulfillment of the requirement
For the award of Degree of

MASTER OF TECHNOLOGY
(VLSI DESIGN & EMBEDDED SYSTEM)

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CERTIFICATE

This is certified that the dissertation entitled "**Design a parallel architecture using MSP430 and Virtex-4**" is a work of **Piyush Gupta (**University Roll No. 125/VLSI/09), a student of Delhi Technological University. This work was completed under my direct supervision and guidance and forms a part of the Master of Technology (VLSI Design and Embedded System) course and curriculum. He has completed his work with utmost sincerity and diligence.

The work embodied in this major project has not been submitted for the award of any other degree to the best of my knowledge.

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ABSTRACT

The exponentially increasing demands for computationally intensive real-time signal processing applications outpace the performance improvements of each new generation of processors. With each passing year, more applications require tremendous computing capabilities that current processors cannot achieve. By coordinating the activities of individual processors, parallel processing offers the performance required by these applications. DSP applications are particularly suited for parallel processing because they are computationally intensive, highly parallel, highly structured, and often, periodic. Moreover, parallel multiprocessor systems have many benefits over single-processor systems. Parallel multiprocessor systems have virtually unlimited performance, better fault tolerance, scalability, flexibility, and upgradability. For these reasons, many high-end DSP applications, such as imaging, graphics, and data processing already benefit from parallel processing.

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