REALIZATION OF SIGNAL PROCESSING & GENERATING CIRCUITS using OTRA

Project Report submitted in partial fulfillment of the requirements for the degree of

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Submitted by:

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(Session: 2009-2011)

CERTIFICATE

This is to certify that the project entitled, **"Realization of SIGNAL PROCESSING & GENERATING CIRCUITS using OTRA"** submitted by **RENU GUPTA, (15/EC/2K9)**, student of M.E. (Electronics and Communication Engg.) at Delhi Technological University (formerly Delhi College of Engineering) in partial fulfillment of requirement for the degree of Masters of Engineering in Electronics & Communication Engineering, is a bona fide work of the student mentioned above.

This project report is a record of the work carried out under my guidance and supervision and has not been submitted earlier in this institute to the best of my knowledge.

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I humbly extend my words of gratitude to my husband Mr. Sanjay Gupta for providing me his help, support and time for completing this project.

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ABSTRACT

With the evolution of submicron technologies such as 0.18 micron and 0.13 micron, the supply voltages have been reduced to 1.5 volts and lower. This makes it difficult to design a voltage mode CMOS circuit with high linearity and wide dynamic range. Also as signal processing extends to higher frequencies, the traditional design methods based on voltage operational amps are no longer adequate.

To overcome these problems circuits operating in current mode are preferred. Various analog building blocks operating in the current mode are available. Operational Trans-Resistance Amplifier (OTRA) is one of them. OTRA is a current controlled voltage source. Both its input and output terminals are characterized by low impedance, therefore eliminating response limitations incurred by capacitive time constants. Its bandwidth is independent of closed loop voltage gain. Thus using the OTRA as the active building block various signal processing and generating circuits can be realized with more flexibility in controlling the frequencies of waveforms.

The Operational Trans-Resistance Amplifier (OTRA) is though not available as a single IC but various CMOS circuit realizations are available in literature and can also be implemented using two standard CFOAs. One such CFOA that can be used is the commercially available AD844AN IC

manufactured by Analog Devices Inc., US. The AD844AN has current feedback architecture.

In this project Operational Trans-Resistance Amplifier (OTRA) based different analog signal processing and generating circuits such as Filters, Multiphase Sinusoidal Oscillators (MSO), Voltage Controlled Oscillator (VCO) and LC oscillator based on active realization of inductor have been realized. The theoretical results have been verified through PSPICE simulations and experimental work by assembling practical circuits of the above and testing them to give near theoretical results. For practical circuits the OTRA has been realized using the AD844AN CFOA ICs manufactured by Analog Devices.

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INTRODUCTION

In recent years, as the signal processing extends to the higher frequency, the circuit designers are finding that the traditional design methods which are based on the voltage operational amplifier are no longer adequate. It is well known that a voltage mode traditional operational amplifier has a bandwidth, which depends on the close-loop voltage gain [1]. The attempt to overcome this problem has led to a renewed interest in circuits, which operate in current mode.

The Analog IC design has historically been viewed as a voltage dominated form of signal processing. However, as new and more mature device technologies such as true complimentary silicon bipolar junction (BJT), and mixed silicon and bipolar and complimentary metal oxide semiconductor devices (Bi-CMOS), and Gallium Arsenide are becoming available, they bring with them the requirement of novel analog design, methods, techniques and CAD tools, necessary for the successful development of these technologies. Apart from these technological advances, the ever shrinking size of devices on ICs and the requirement to use low power supply voltages is resulting in new analog design techniques. Due to recent advances in integrated circuit (IC) technologies, analog IC Design is now able to exploit the potential of current mode processing, providing attractive and elegant solutions to a variety of circuit and system problems [2].

1.1 CURRENT MODE VS VOLTAGE MODE PROCESSING:

The evolution of submicron technologies such as 0.18 micron and 0.13 micron has resulted in the requirement to use low power supply voltages which makes it difficult to design voltage mode circuits with high linearity and wide dynamic range. Current mode circuits have become a viable alternative because of their inherent advantages over voltage mode circuits.

The main advantage of current mode circuits results from the nonlinear characteristic exhibited by field effect transistors. A small change in the input and or controlling voltage results in a much larger change in the output current. Thus for a fixed supply voltage the dynamic range of a current mode circuit is much larger than that of a voltage mode circuit.

A second advantage of current mode circuits is that they are much faster as compared to voltage mode circuits. The parasitic capacitances present in the analog circuits must be charged and discharged with the changing voltage levels. In a current mode circuit, a change in current level is not accompanied by a change in the voltage level. Hence the parasitic capacitances will not affect the operating speed of the circuit by a significant amount.

Due to the advantages offered by current mode processing early circuit design principles and techniques for current mode processing, such as the 'Trans-Linear Circuit' principle, are becoming powerful tools for the development of high performance analog circuits and systems. It has further

led to the emergence of new analog building blocks ranging from Operational Trans-Conductance Amplifiers (OTAs) [3] to Current Feedback Operational Amplifiers (CFOAs) [4] to various generations of current conveyors(CC) [5-11] to Operational Trans-Resistance Amplifiers (OTRAs) [12] etc.

The maturity of current mode signal processing is seen from the development of systems based on the current mode approach. A wide spectrum of applications includes important areas such as continuous-time and sampled-data filters through general analog interfacing, A/D and D/A converters to current-mode neural networks.

1.2 OPERATIONAL TRANS-RESISTANCE AMPLIFIERS (OTRAS)

The OTRA is a current-controlled voltage source. It is a three terminal device. The output voltage is proportional to the difference between the two input currents. The terminal equations of an ideal OTRA are characterized by equation (1) and its symbol is shown in Fig.1.1

$$\begin{bmatrix} V_+ \\ V_- \\ V_0 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_+ \\ I_- \\ I_0 \end{bmatrix} \quad (1)$$

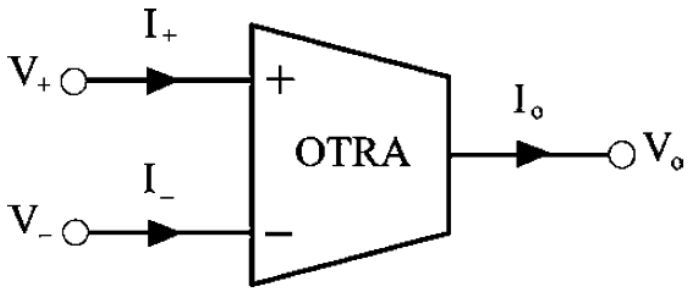


Fig.1.1

The trans-resistance gain is generally of the order of 100k V/I, which can be assumed to be tending towards ∞ for ideal case. Its input impedance is very low, which can be taken as zero for ideal analysis, and hence a virtual ground exists between the input terminals. The output impedance is also very low and hence results in very less gain loss.

The Operational Trans-Resistance Amplifier (OTRA) is one of the most important building blocks of analog integrated circuits and systems. Since the input terminals of OTRA are virtually grounded, most effects of parasitic capacitances and resistances disappear. Thus it possible to obtain very accurate and cascadable transfer functions by using this device in a negative feedback loop [12].

Although the OTRA is commercially available from several manufactures under the name of NORTON amplifier or current differencing amplifier, it has not gained attention until recently. These commercial realizations do not provide internal ground at the input port and they allow the input current to flow in one direction only. The former disadvantage limited the functionality of the OTRA whereas the latter forced to use

external DC bias current leading complex and unattractive design. Recently, current-mode analog integrated circuits in CMOS technology have received considerable interest. Current-mode techniques can achieve a considerable improvement in amplifier speed, accuracy and bandwidth, overcoming the finite gain bandwidth product associated with op-amp.

Chapter 2:

LITERATURE SURVEY

Traditionally, most analog signal processing operations have been accomplished employing the voltage as the signal variable, but due to the increasing demand for operation in the high frequency region and the finite gain-bandwidth product associated with operational amplifiers, a change from voltage mode circuits is required. Recently, current mode analog integrated circuits in CMOS technology have received considerable interest.

Recently Operational Trans-resistance Amplifier (OTRA) has emerged as an effective alternate analog building block which is a high gain current input, voltage output amplifier [12]. OTRA, being a current processing analog building block, inherits all the advantages of current mode technique and therefore is ideally suited for high frequency applications.

A variety of papers have been reported on OTRAs during the last one and a half decade. This includes various CMOS realization of OTRA and wide variety of signal processing and generation applications such as voltage and current mode filters.

2.1 OTRA REALIZATION:

Various implementations of OTRA are available in literature and are based on:

i.) Using commercially available analog integrated circuit AD844 (CFOA) OTRA can also be implemented using commercially available analog integrated circuit AD844 (CFOA). Two CFOAs are required for this implementation [13].

ii.) Using integrated circuit implementations.

This active element can be implemented by using a differential current controlled current source followed by a voltage buffer [12]. The OTRA described in [14] consists of a low voltage regulated cascade current mirror with a low voltage regulated cascade load as the core of the circuit, common source amplifiers gain boosting stage and level shifters followed by common source output stage. The OTRA described in [15] is based on cascaded connection of the modified differential current conveyor (MDCC) [16] and a common source amplifier. The OTRA structure available in [17] is similar to [15] but uses smaller number of current mirrors than [15]. This reduces the transistor mirror mismatch effect and also increases the frequency capabilities. Due to smaller number of transistors the power dissipation is also reduced. The CMOS OTRA realization in [18] uses same Input stage as in [17] while a differential gain stage is used instead of the single common source amplifier. This differential stage reduces the DC offset current and increases the DC open loop trans-resistance gain.

2.2 OTRA APPLICATIONS

A wide variety of system applications, ranging from filters, oscillators, multivibrators through general analog interfacing, have been developed using OTRA. The filter structures are broadly classified as voltage mode, current mode, trans-impedance type, multifunction or universal, single input single output or single input multiple output and all pass structures.

Voltage Mode structures [19] [20] [15] present MOSFET C integrators using OTRA. Structures available in [15] [19] [21] can be classified as universal single input single output structures. Tow Thomas and KHN bi-quad structures are presented in [15]. Linear transformation (LT) high- order active filters have the advantage that every section of the original LC ladder prototype can be realized by using active elements individually. Voltage mode high-order LT MOSFET – C filters using OTRAs are presented in [22-23]. A third order Chebyshev LPF is presented in [19]. Few first order all pass topology [24][26] and second order all pass structure [25][26] are also available.

OTRA based current mode MOSFET-C integrator and differentiator is presented in [27]. Two different universal bi-quad structures have also been discussed in [27]. Current mode first order all pass structure is presented in [28]. Current mode linear transformation MOSFET-C filters based on OTRAs and simplified MOSFET resistor circuits are available in [29].

Trans-impedance type first order all pass filter is available in [30] whereas [31] presents trans-impedance type fully integrated bi-quad using OTRA.

Ref [32] deals with positive inductance simulation using two OTRAs. Grounded parallel immitance simulator topology employing single OTRA is available in [33]. All forms of fully controllable negative inductance based on OTRA having control on both inductance value and the condition are available in [34].

A number of schemes have been described in the literature to realize OTRA based sinusoidal oscillators [32-36]. Quadrature oscillators are presented in [15] [24] [25] [26] [27] and multiphase sinusoidal oscillators have been described in [36]. OTRA based voltage mode square wave generator [14] and bistable multi vibrators [37] have been discussed. Ref.[38-39] present current mode monostable multi vibrators.

REALIZATION OF OTRA

The past decade has witnessed a continued scaling of CMOS technologies by an order of magnitude from 2µm in the early '90s to 0.18µm for the current processes. A further lowering of gate lengths to 0.07µm is envisioned in near future. The reduction in gate lengths is accompanied by reduction in supply voltages due to reliability issues. However the reduction in supply voltages is often not accompanied by reduction in the threshold voltages of transistors. The dissimilar scaling of supply and threshold has led to a loss of dynamic range in analog circuits as most of the supply voltage is used up to ensure that the transistors are in saturation. Consequently, the number of transistors that can be stacked between rails is limited.

Thus a pressing need exists for circuits that can operate at low voltages by avoiding the stacking of devices. OTRAs are attractive in this regard as they employ a shunt feedback, with the amplifier and the feedback network connected in parallel [12]. Various implementations of OTRA are available in literature and are based on:

I. Using integrated circuit implementations.

II. Using commercially available analog integrated circuit AD844 .

3.1 REALIZATION USING CMOS:

Several high performance CMOS OTRA realization are presented in literature. In this project the CMOS implementation of the OTRA [17] as given in Fig. 3.1 has been used for SPICE simulation using 0.5 µm CMOS process

parameters provided by MOSIS (AGILENT) and supply voltages taken are ±1.5 V. Aspect ratios used for different transistors are given in Table 3.1.

Transistor	W(µm)/L(µm)
M1-M3	100/2.5
M4	10/2.5
M5,M6	30/2.5
M7	10/2.5
M8-M11	50/2.5
M12,M13	100/2.5
M14	50/0.5

Table 3.1 Aspect ratio of the transistors

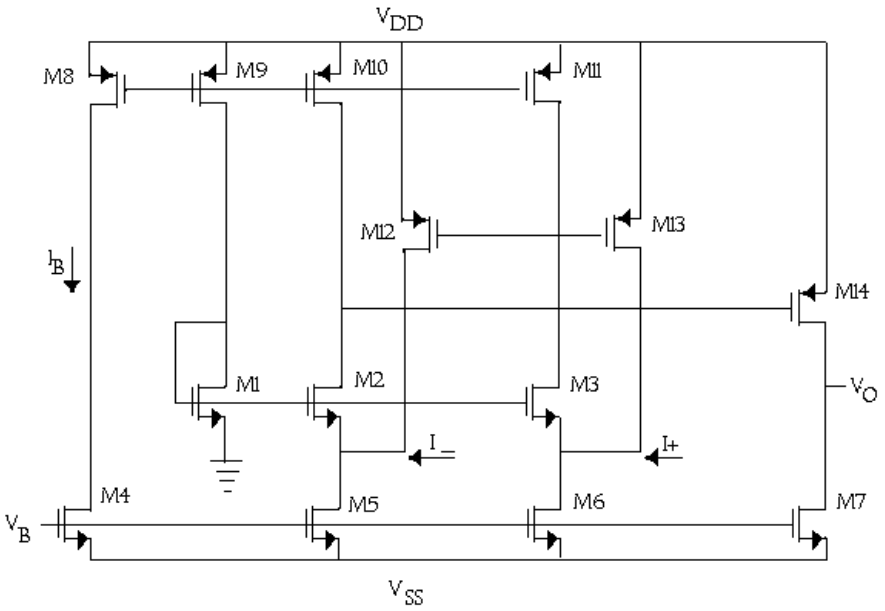


Fig. 3.1 CMOS Implementation of OTRA[17]

3.2 REALIZATION USING CFOA

CFOAs are commercially available in the form of IC as AD844AN. The terminal equations of a CFOA are given as:

$i_y = 0,$
$v_x = v_y,$
$i_z = i_x,$
$v_w = v_z$

Its symbolic notation and equivalent circuit is as given in Fig. 3.2

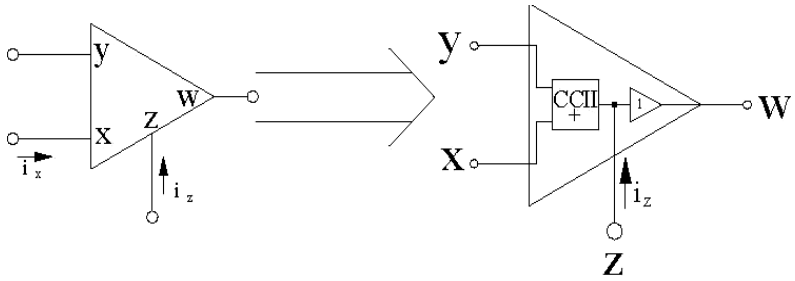


Fig. 3.2 CFOA Symbol and Equivalent Circuit

The practical realization of an OTRA using 2 nos. CFOAs is as shown Fig. 3.3. The ICs used are AD844AN manufactured by Analog Devices.

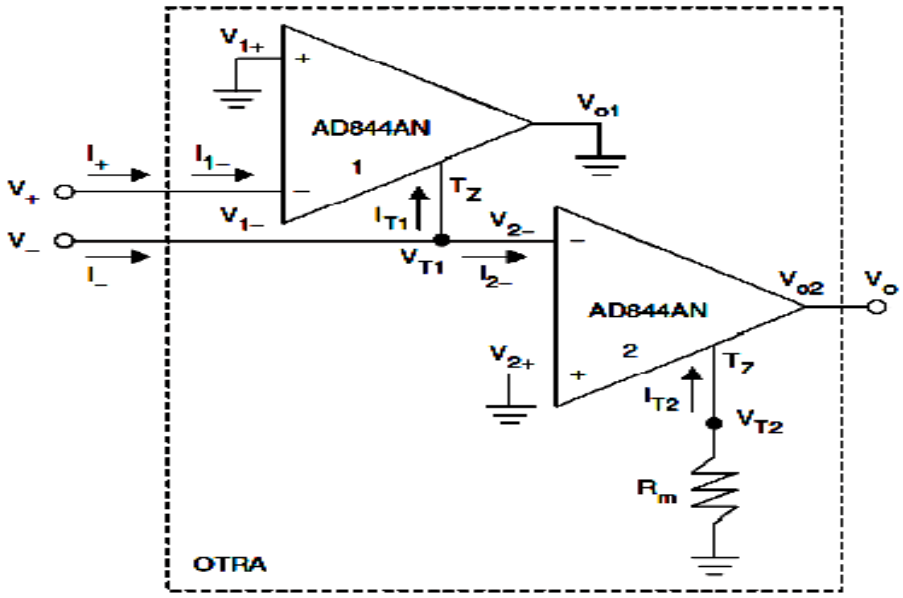


Fig. 3.3 Realization of an OTRA using CFOAs

Realization of an OTRA using CFOA

The above circuit can be analyzed as follows:

$$V_+ = V_{1-} = V_{1+} = 0$$

$$V_- = V_{2-} = V_{2+} = 0$$

$$V_{o1} = V_{T1} = V_{2-} = V_{2+} = 0$$

$$I_{T1} = I_{1-} = I_+$$

$$I_{T2} = I_{2-} = I_- - I_{T1} = I_- - I_+$$

$$V_o = V_{T2} = - R_m \times I_{T2} = R_m \times (I_+ - I_-)$$

$$Vo = Rm (I+ - I-)$$

Hence the terminal equations of OTRA are realized. Fig. 3.4 shows the schematic of CFOA based OTRA and its DC and AC characteristics are shown in Fig. 3.5a and Fig. 3.5b respectively.

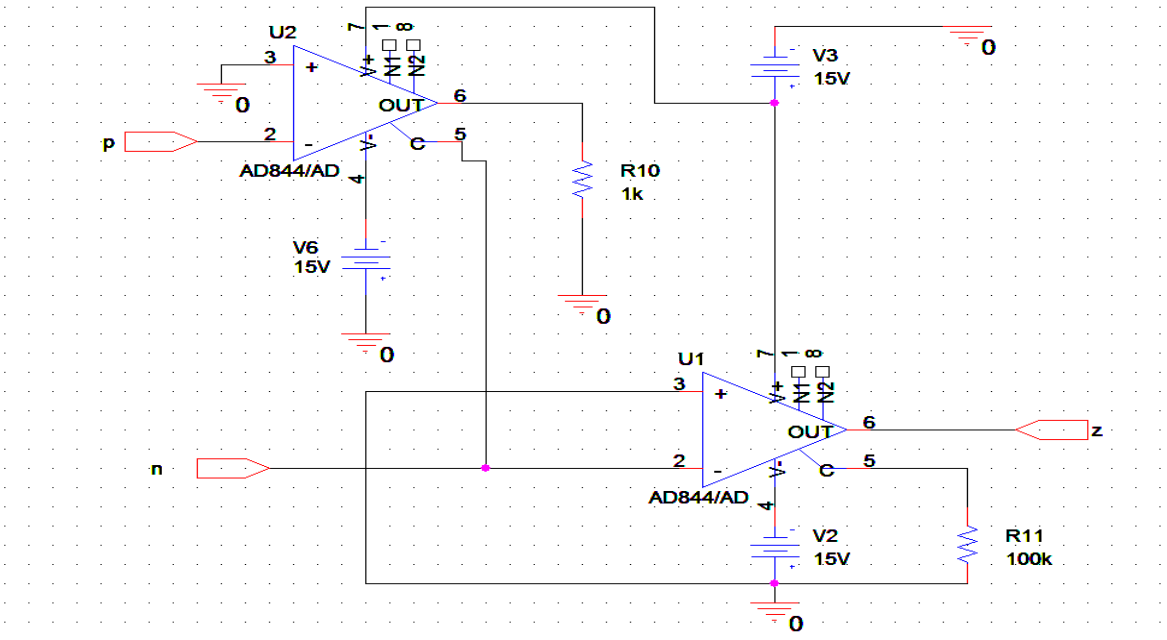


Fig. 3.4 Schematic realization of an OTRA using 2 nos. AD844AN ICs

Fig. 3.5a DC characteristics of OTRA realized using CFOA

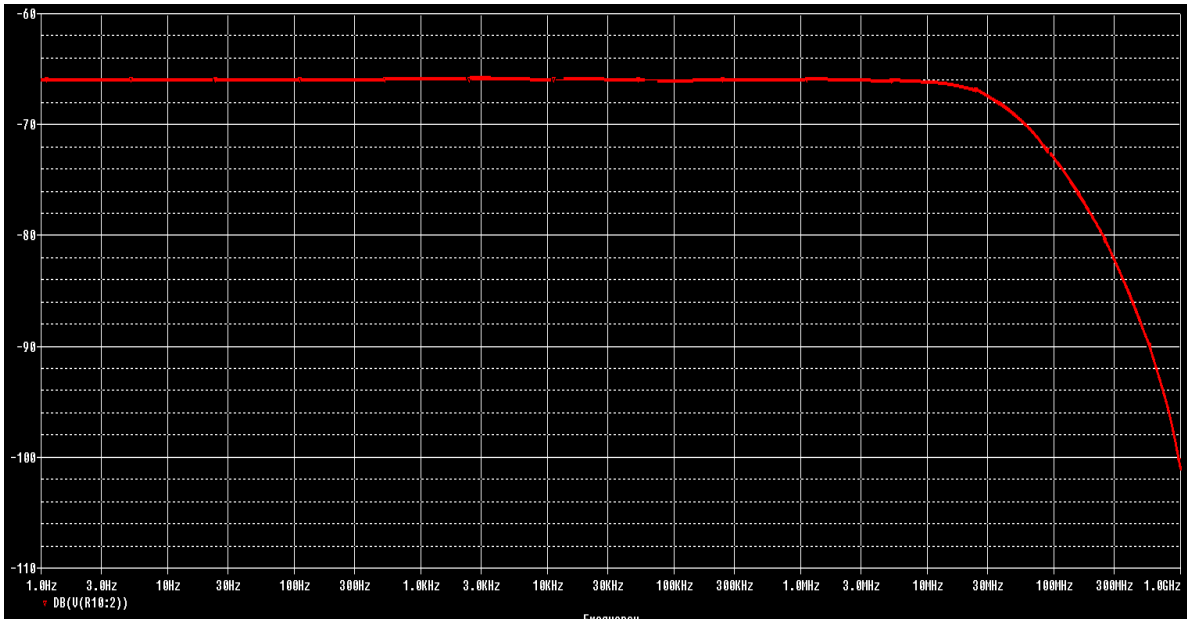


Fig. 3.5b Frequency response of OTRA realized using CFOA

SIGNAL PROCESSING CIRCUITS

Filters are common building blocks of Analog Signal Processing applications. Each signal requires some form of filtering before it could be applied to some use. Various filter functions using OTRA as the active element are available in literature. In this chapter two filter circuits are discussed and verified through simulations.

4.1 UNIVERSAL FILTER

In this section a voltage mode single input multi output (SIMO) bi-quadratic universal filter configuration is described. It exhibits the feature of orthogonal controllability of angular frequency and quality factor. The bi-quadratic universal filter is shown in Fig. 4.1. Routine analysis of the circuit of Fig. 4.1 results in the following transfer functions

$$\frac{V_{01}}{V_{in}} = \frac{s^2 G_1 C_1 C_2}{s^2 C_1 C_2 G_3 + s C_2 G_4 G_5 + G_2 G_4 G_6} \tag{1}$$

$$\frac{V_{02}}{V_{in}} = \frac{s C_2 G_1 G_4}{s^2 C_1 C_2 G_3 + s C_2 G_4 G_5 + G_2 G_4 G_6} \tag{2}$$

$$\frac{V_{03}}{V_{in}} = \frac{G_1 G_4 G_6}{s^2 C_1 C_2 G_3 + s C_2 G_4 G_5 + G_2 G_4 G_6} \tag{3}$$

$$\frac{V_{04}}{V_{in}} = \frac{\frac{G_7}{G_9} s^2 C_1 C_2 G_1 + \frac{G_8}{G_9} G_1 G_4 G_6}{s^2 C_1 C_2 G_3 + s C_2 G_4 G_5 + G_2 G_4 G_6} \tag{4}$$

$$\frac{V_{05}}{V_{in}} = \frac{\frac{G_7 G_{11}}{G_8 G_{12}} s^2 C_1 C_2 G_1 - \frac{G_{10}}{G_{11}} s C_2 G_1 G_4 + \frac{G_8 G_{11}}{G_9 G_{12}} G_1 G_4 G_6}{s^2 C_1 C_2 G_3 + s C_2 G_4 G_5 + G_2 G_4 G_6} \quad (5)$$

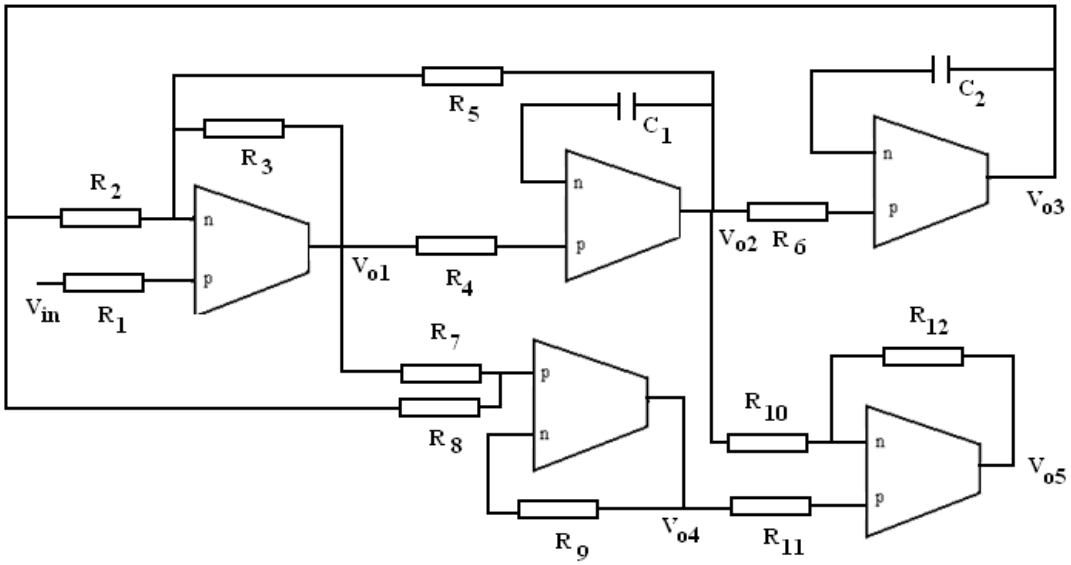


Fig. 4.1 Schematic of bi-quadratic universal filter

Equations (1) – (5) clearly indicate that high-pass, band-pass, low-pass responses are available at V_{o1}, V_{o2} and V_{o3} respectively.

Band reject response is available at V_{o4} , with BR gain (G_{BR}) =G_1/G_3, if

$G_7 = G_9$, $G_3G_8 = G_2G_9$ (6)

At V_{o5} all-pass response with all-pass gain (G_{AP}) = G_1/G_3 is available if

$G_3G_{10} = G_5G_{12}$, $G_7\,G_{11} = G_8G_{12}$, $G_3G_8\,G_{11} = G_2\,G_9G_{12}$ (7)

The high-pass gain (G_{HP}), band-pass gain (G_{BP}), and low-pass gain (G_{LP}) are given by

$$G_{HP}=\frac{G_1}{G_3}\ ,\ G_{BP}=\frac{G_1}{G_5}\ ,\ G_{LP}=\frac{G_1}{G_2} \tag{8}$$

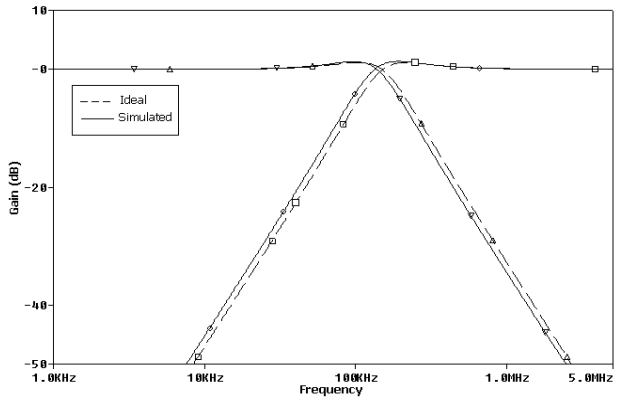
ω_0 and Q for the circuit is given by

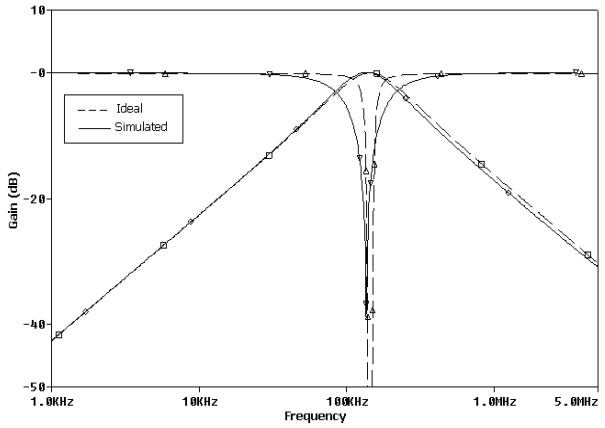
$$\omega_0 = \sqrt{\frac{G_2 G_4 G_6}{C_1 C_2 G_3}} \tag{9}$$

$$\mathrm{Q} = \frac{1}{G_5}\sqrt{\frac{C_1 G_2 G_3 G_6}{C_2 G_4}} \tag{10}$$

This suggests that the quality factor (Q) can be independently controlled by varying R_5 without affecting the resonant angular frequency ω_0. Also the filter gain can be controlled through R1 without affecting ω_0 and Q.

Workability of the universal filter is demonstrated through PSPICE simulations using 0.5 µm CMOS process parameters provided by MOSIS (AGILENT). The SIMO bi-quadratic universal filter was designed for the resonant frequency (f_0) of 120 KHz and Q_0 =1 with component values C1=C2=100pF and R_i =10.5KΩ for i = 1, 2, . . . 12. Fig 4.2 shows the simultaneously available magnitude responses for low-pass, high-pass, band-pass, notch and all pass filters. The simulated resonant frequency is found to be in close agreement to the theoretical value.





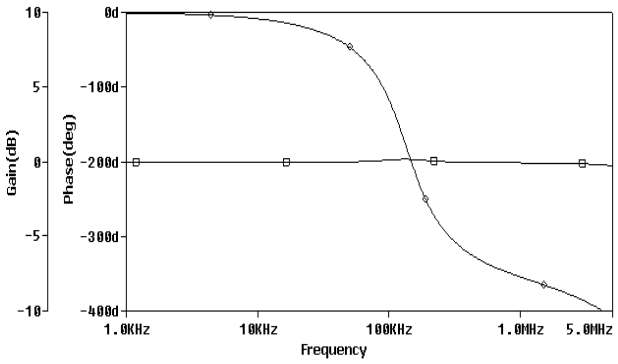


Fig. 4.2 Simulated responses of the circuit (a) low-pass and high-pass, (b) band-pass and notch, (c) all pass.

In Fig. 4.3 orthogonal tunability of Q_0 is demonstrated at f_0 =11.5 KHz. Selecting $C_1 = C_2 =$ 50pF, and R_i = 272 KΩ for i = 1,…,4,6,…,12, the values of Q_0 as obtained and R_5 are listed in Table 4.1.

Table 4.1

Sl.No.	R_5(KΩ)	Q_0
1	680	2.5
2	136	0.5
3	68	0.25
4	34	0.125

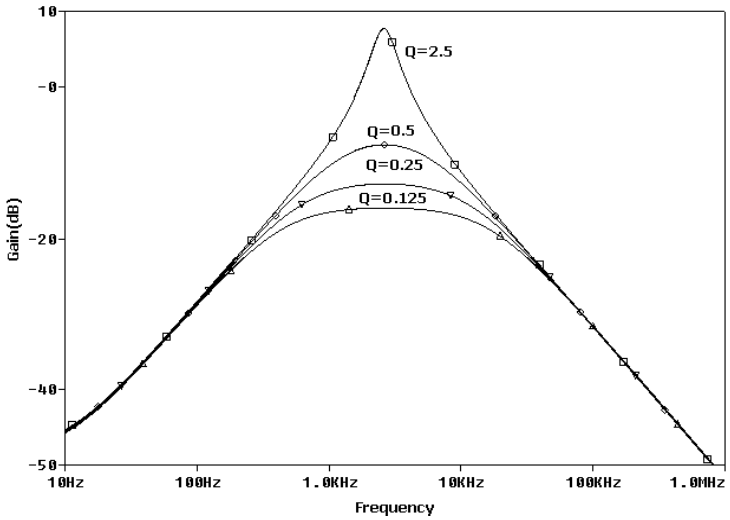


Fig. 4.3 Band-pass Response for different Q_0 values

The f_0 can be tuned by changing the R_4 and is verified through simulations as depicted in Fig. 4.4. Values of f_0, for $C_1 = C_2$ = 50pF and R_i= 23KΩ for i = 1,…3 , 5,. . . , 12, along with different values of R_4 are listed in Table 4.2.

Table 4.2

Sl.No.	R_4(KΩ)	f_0(KHz)
1	34	113.8
2	23	138.4
3	17	160
4	14	179

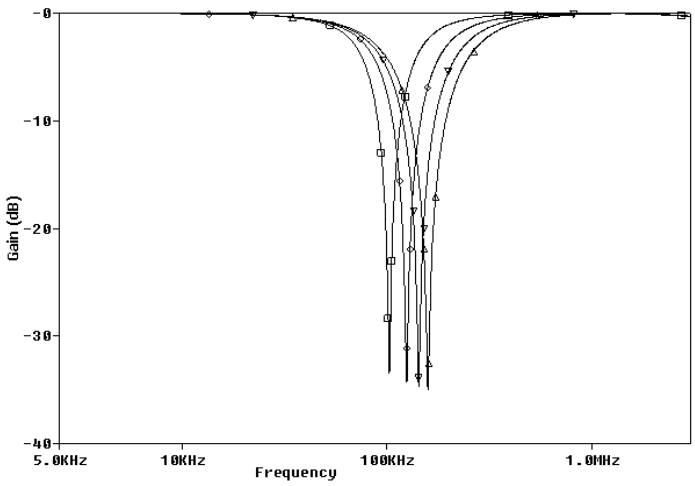


Fig. 4.4 Notch Response for different ω_0 values

4.2 GROUNDED IMMITANCE USING OTRA

Active immittance simulation has been an important research topic in active network synthesis for a long time. These simulators find application in areas such as oscillator design, filter design, phase shifters and parasitic element cancellation.

Here a method to realize a grounded immitance [41] based on single OTRA, two resistors and two virtually grounded capacitors is presented, which makes it further useful from IC fabrication viewpoint. The workability of the immittance simulator is verified through PSPICE simulations and two applications namely a current mode multiple output filter and an oscillator.

Circuit Description

The grounded immittance simulator [41] is shown in Fig.4.5. Routine analysis of the circuit results in the following expression for input admittance

$$Y_{in}(s) = G_1 + G_2 - \frac{G_1 G_2}{s(C_1 - C_2)} \tag{11}$$

which represents an impedance of type L_{eq}/ R_{eq} , where

$$R_{eq} = G_1 + G_2 \tag{12}$$

And the inductance value that results is

$$L_{eq} = \frac{(C_1 - C_2)}{G_1 G_2} \tag{13}$$

Proper choice of C_1 and C_2 may result in realization of inductance type (+L) parallel with R or inductance type (-L) parallel with R.

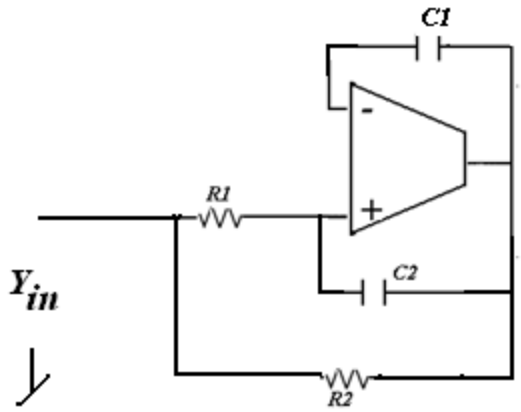


Fig.4.5 Grounded Immittance Simulator

OTRA Realization and Simulation Results

The functionality of this immittance simulator circuit is verified through CFOA based realization of OTRA as shown in Fig. 3.3.

Impedance magnitude and phase responses of the immittance simulator are given in Fig. 4.6a and Fig. 4.6b respectively.

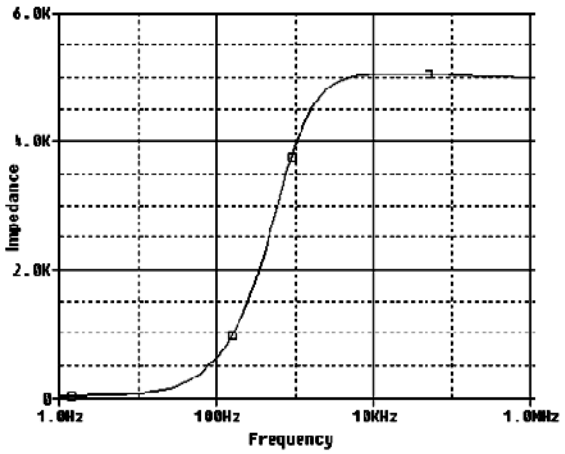


Fig. 4.6a Impedance Magnitude response

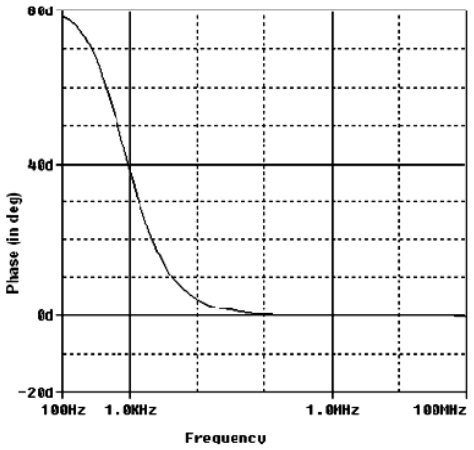


Fig. 4.6b Impedance phase response

Applications of Immitance Simulator

To show the application of the immittance simulator a current mode multiple output filter, giving high pass and band pass responses, and an LC oscillator are designed.

Current mode Multiple output Filter

The prototype of the filter is shown in Fig. 4.7. The immittance simulator replaces the parallel R-L circuit. The current transfer functions can be written as:

$$\frac{I_R}{I_i} = \frac{s\frac{(G_{eq}+G)}{C}}{s^2 + s\frac{(G_{eq}+G)}{C} + \frac{1}{CL_{eq}}} \quad (14)$$

$$\frac{I_c}{I_i} = \frac{s^2}{s^2 + s\frac{(G_{eq} + G)}{C} + \frac{1}{CL_{eq}}} \tag{15}$$

The band pass filter for center frequency f_0 =79.6 KHz is designed, for which the component values are calculated as R= 1kΩ, C = 1nF, and L_{eq} =4mH.For realizing $L_{eq=}$ 4mH, values of different components are chosen as R_1 = 2kΩ, R_2 = 2kΩ, C1 = 2nF and C_2 = 1nF. The simulated results, shown in Fig. 4.8, are found to be in close agreement with the theoretical predictions.

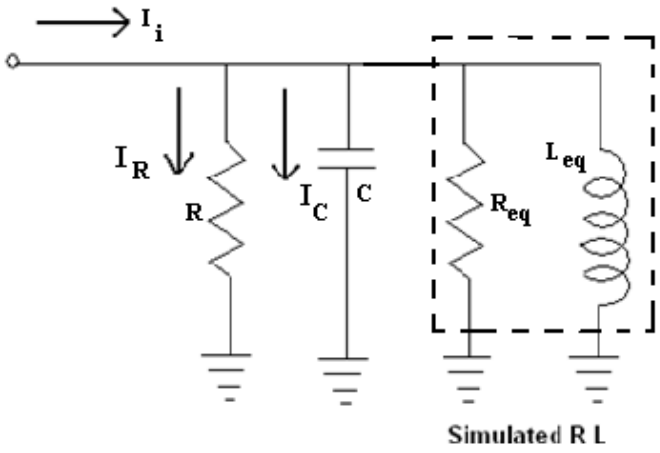


Fig. 4.7 Current Mode Filter

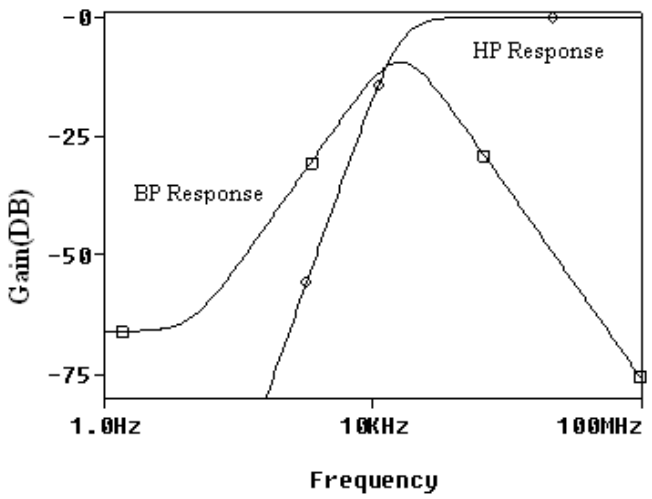


Fig. 4.8 Frequency Response

Realization of an LC oscillator using new immittance simulator

An LC oscillator is designed using new simulated inductor and is shown in Fig. 4.9. The condition of oscillation (C_O) and frequency of oscillation (F_O) for the oscillator are given by

C_O:

$$\frac{R_{eff}}{R + R_{eff}} = \frac{R_a}{R_b} \tag{16}$$

F_O:

$$\omega_0 = \frac{1}{\sqrt{L_{eq}C}} \tag{17}$$

where $R_{eff} = R_{eq}$ II R_a.

A typical simulation for element values R_a = 4kΩ, R_b = 8kΩ, R = 2kΩ, R_{eq} =16kΩ, L_{eq} = 0.64mH and C = 10pF is shown in Fig. 4.10. The circuit is found to work as per theoretical predictions**.**

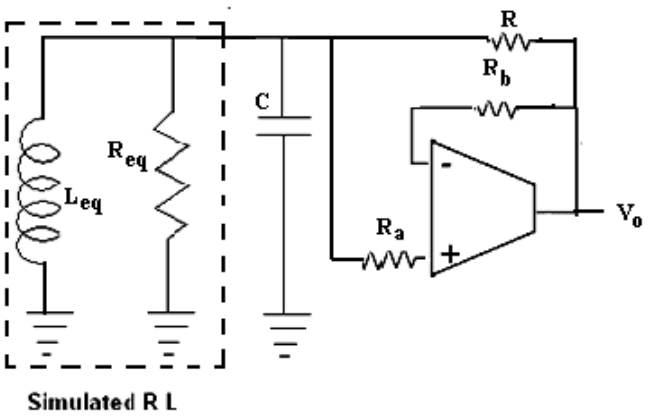


Fig. 4.9 LC oscillator using realized simulator

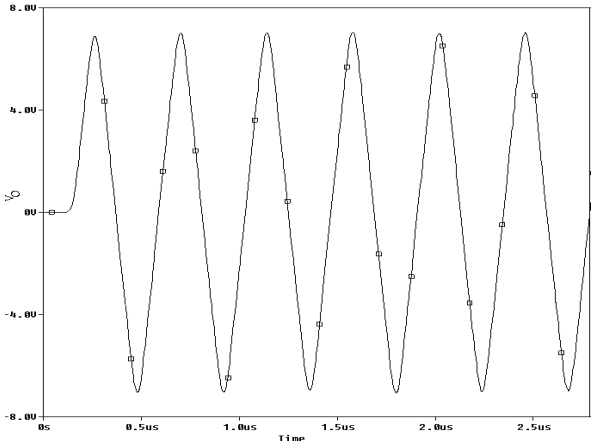


Fig. 4.10 Simulation Result of LC oscillator

4.3 BAND PASS FILTER

In this section a Band Pass Filter using Grounded inductor has been discussed and simulated. A practical circuit was also assembled and tested to give near theoretical results. The band pass filter circuit is shown in Fig. 4.11. The transfer function for band pass response is

$$\frac{V_0}{V_{in}} = \frac{\frac{s}{CR}}{s^2 + \frac{s}{CR} + \frac{1}{L_{eq}C}} \tag{18}$$

where $\omega_0 = \frac{1}{\sqrt{L_{eq}C}}$, $\frac{\omega_0}{Q} = \frac{1}{CR}$ and $Q = R\sqrt{\frac{C}{L_{eq}}}$ (19)

This suggests that the quality factor (Q) can be independently controlled by varying R without affecting the center frequency ω_o. Passive sensitivities are calculated as follows:

$$S_{R1}^{\omega_0} = S_{R2}^{\omega_0} = S_{C2}^{\omega_0} = S_C^{\omega_0} = -\frac{1}{2}, S_R^Q = 1, S_C^Q = \frac{1}{2}, S_{R1}^Q = S_{R3}^Q = S_{C2}^Q - \frac{1}{2} \tag{20}$$

To see the correctness of the theoretical proposition a BP filter is designed having 1.59 MHz center frequency. The component values are computed as R = 1KΩ, C = 1nF and L_{eq} = 10uH. For this value of L_{eq} component values are $R_1 = R_2 = R_3$ = 1K, C_1 = 30pF, C_2 = 10pF. The filter circuit is simulated using SPICE program and the frequency response of the filter is depicted in Fig. 4.12. The simulated results are in close agreement with the theoretical predictions.

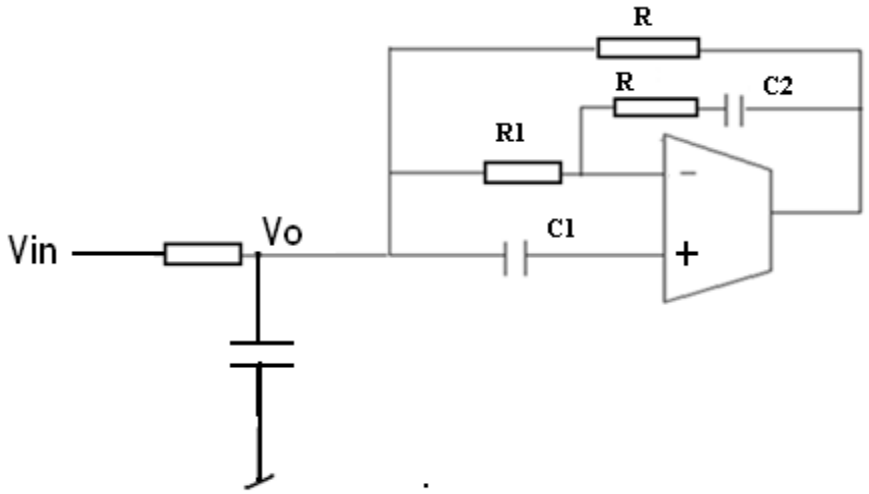


Fig. 4.11 Band Pass Filter

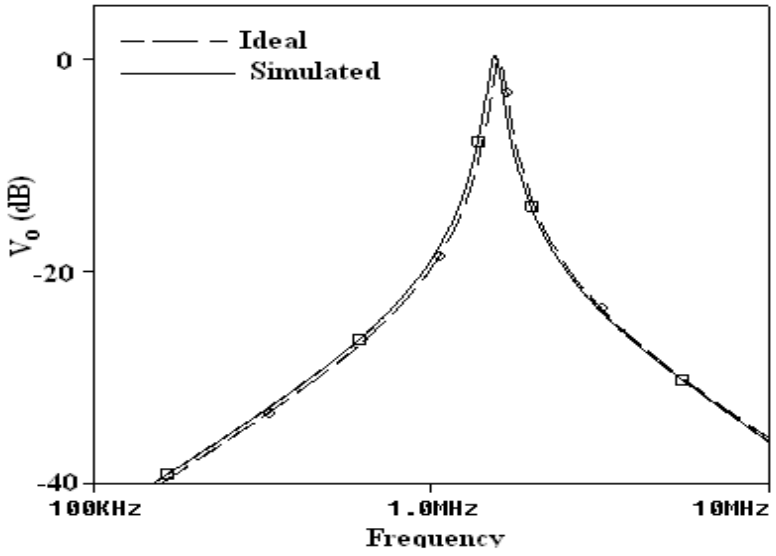


Fig. 4.12 Frequency Response

4.4 OBSERVATION OF PHYSICAL CIRCUIT

A practical circuit for the Band Pass Filter was also assembled. The component values are taken as R = 1KΩ, C = 1nF and L_{eq} = 100uH.

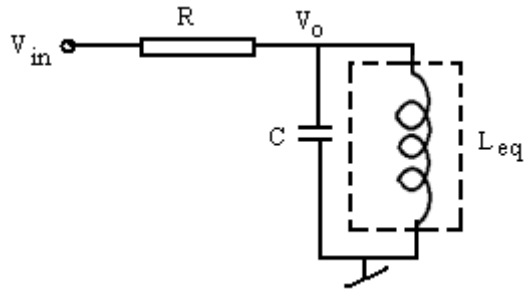


Fig 4.13 Band Pass Filter

For this value of L_{eq} component values are R = R_1 = 1K, C_1 = 330pF, C_2 = 100pF as shown below.

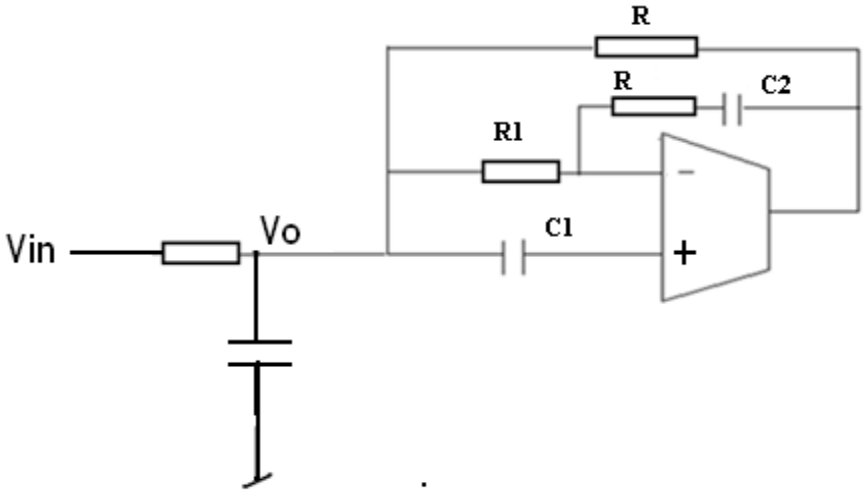


Fig. 4.14 Practical Circuit as assembled and tested

The circuit shown in fig 4.14 was tested in the Lab using the following

test equipment

a. Signal Generator – 1 Hz to 1 Mhz

b. Digital Storage Oscilloscope – Tektronics TDS 2014

c. Dual Power Supply – 0 to +/- 15 volts

d. Multimeter

The readings were taken and are tabulated below. A graph was plotted and the center frequency was found to be 450 KHz. This tallies well with the calculated theoretical value using the above component values

The Table 4.3 below is showing the readings taken

Frequency (KHz)	V in (Volts)	V out (Volts)	Gain (dB)
0.1	3.08	0.037	-38.45
0.5	3.08	0.038	-38.18
1.0	3.08	0.039	-37.91
10.0	3.12	0.045	-36.92
25.0	3.16	0.066	-33.55
50.0	3.16	0.116	-28.70
100.0	3.16	0.216	-23.30
150.0	3.24	0.352	-19.28
175.0	3.24	0.346	-19.43
200.0	3.24	0.540	-15.56
225.0	3.24	0.624	-14.31
250.0	3.24	0.746	-12.76
275.0	3.28	0.912	-11.12
300.0	3.36	1.060	-10.02
325.0	3.40	1.400	-7.71

350.0	3.48	1.660	-6.43
375.0	3.56	2.080	-4.67
400.0	3.76	2.520	-3.48
425.0	3.92	2.880	-2.68
450.0	3.88	2.960	-2.35
460.0	3.84	2.840	-2.62
475.0	3.72	2.680	-2.85
500.0	3.64	2.400	-3.62
525.0	3.56	2.080	-4.67
550.0	3.40	1.720	-5.92
575.0	3.28	1.520	-6.68
600.0	3.24	1.340	-7.67
625.0	3.16	1.220	-8.27
650.0	3.16	1.140	-8.86
675.0	3.16	1.080	-9.33
700.0	3.16	1.000	-9.99
725.0	3.16	0.940	-10.53
750.0	3.16	0.880	-11.10
775.0	3.16	0.760	-12.38
800.0	3.16	0.720	-12.85
825.0	3.12	0.688	-13.13
850.0	3.12	0.648	-13.65
875.0	3.12	0.620	-14.04
900.0	3.08	0.600	-14.21
925.0	3.08	0.570	-14.65
950.0	3.04	0.544	-14.95
975.0	3.04	0.520	-15.34
1,000.0	2.96	0.496	-15.52
1,025.0	2.96	0.480	-15.80

Table: 4.3 Readings taken on practical circuit

Frequency Response Curve of Band Pass Filter

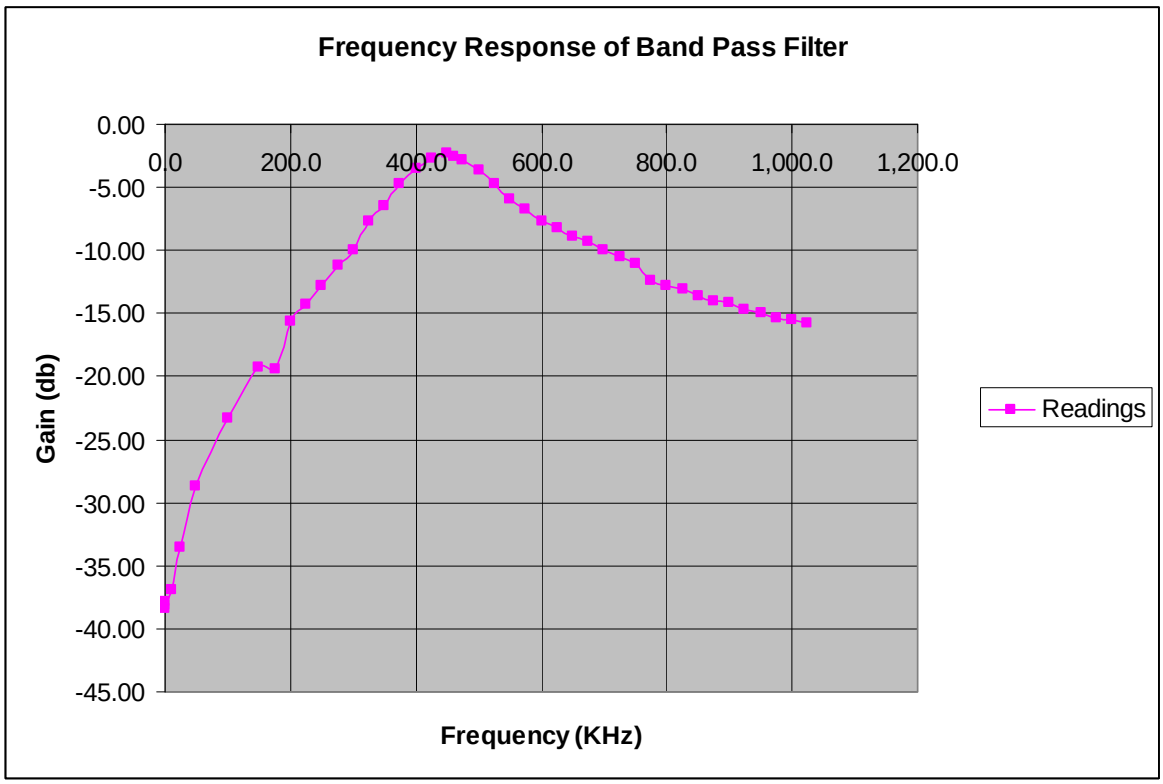
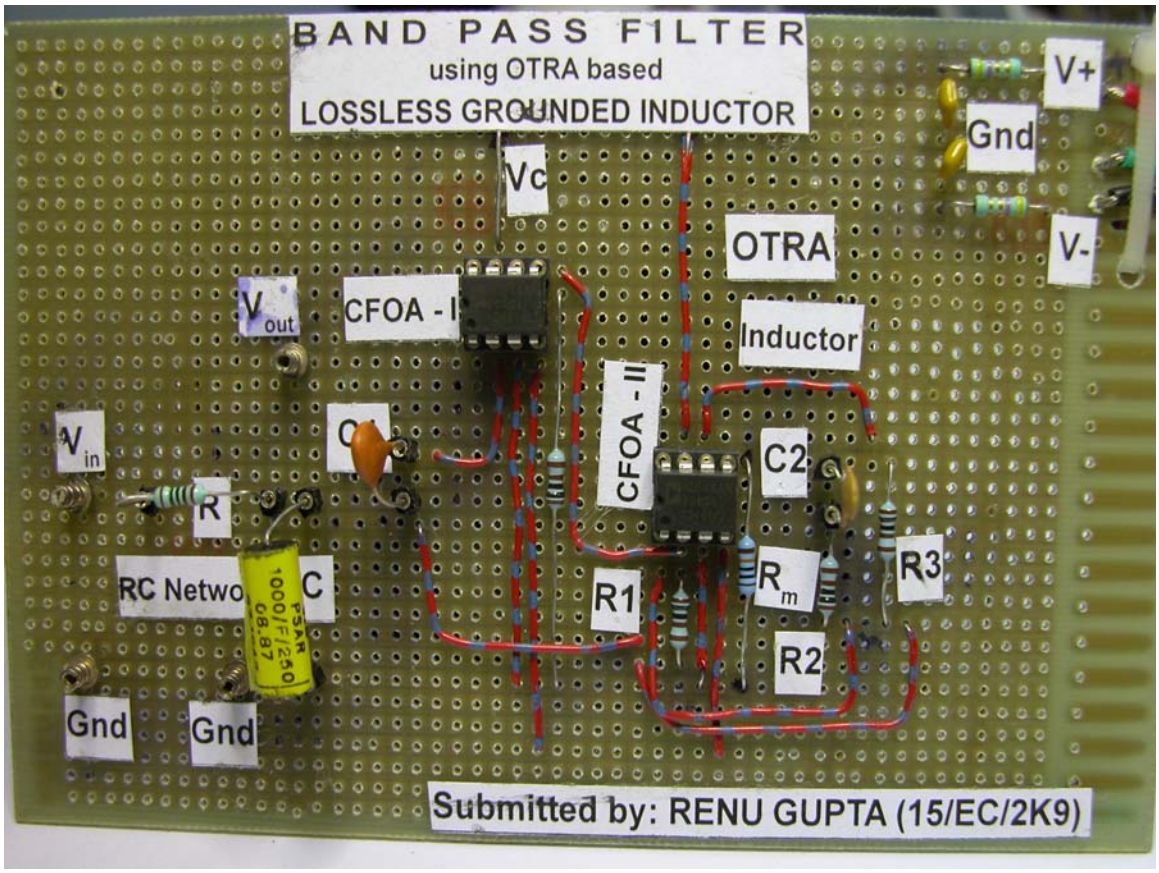


Fig. 4.15 Frequency Response Curve for the Band Pass Filter

The above curve has been plotted between the Gain calculated in dB and the Input frequency of the signal.

Picture of Physical Circuit Assembled for Band Pass Filter



Chapter 5:

SIGNAL GENERATION CIRCUITS

Signal generating circuits can be generally categorized into two groups based on the type of waveform produced: 1) Harmonic oscillators, and 2) Relaxation oscillators.

5.1 HARMONIC OSCILLATORS

Harmonic oscillators generate a sinusoidal waveform. They consist of an amplifier that provides adequate gain and a resonant circuit that feeds back signal to the input. Oscillation occurs at the resonant frequency where a positive gain arises around the loop. Some examples of harmonic oscillators are crystal oscillators and LC-tank oscillators and multiphase oscillators.

5.1.1 MULTIPHASE SINUSOIDAL OSCILLATOR

Multiphase sinusoidal oscillators (MSO) find extensive application in the field of power electronics and communications. In Communications MSO circuits are commonly used in single-sideband generators, phase modulators, and quadrature mixers.

Circuit Description

The circuit of MSO [36] is shown in Fig. 5.1 which produces **n** odd phase oscillations. The OTRAs have been connected in the inverting mode such that the gain G(s) of each block can be expressed as:

$$G(s) = \left(-\frac{K}{1+sCR}\right) \quad (1)$$

Where $R_2 = R_4 = \ldots = R_{2n} = R$; $R_1 = R_3 = \ldots = R_{2n-1} = R_x$; $K = (R/R_X)$ and $C_1 = C_2 = \ldots = C_n = C$

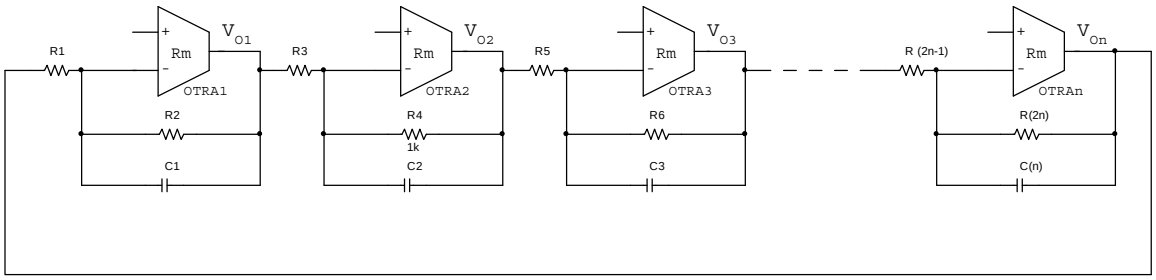


Fig. 5.1. Generalized scheme for producing n odd phase oscillation

From Fig. 5.1, the open loop gain L(s) can be expressed as:

$$L(s) = \left(-\frac{K}{1+sCR}\right)^n \tag{2}$$

For oscillations to occur, the Barkhausen criterion [18] must be satisfied, hence

$$\left(-\frac{K}{1+sCR}\right)^n = 1 \tag{3}$$

The above equation yields:

$$(1+sCR)^n + (-1)^{n+1}K^n = 0 \tag{4}$$

Equation (2) will converge only for odd values of n such that n≥3. Thus the circuit will give rise to equally spaced oscillations having a phase difference of (360/n)°.

Consider the case for n=3 then (1) reduces to

$$(1 + j\omega_0 CR)^3 + K^3 = 0 \tag{5}$$

Equating real and imaginary parts of (1) gives the frequency of oscillation (F_O) and condition of oscillation (C_O) as

Frequency of Oscillation (F_O):

$$f_0 = \frac{\sqrt{3}}{2\pi RC} \tag{6}$$

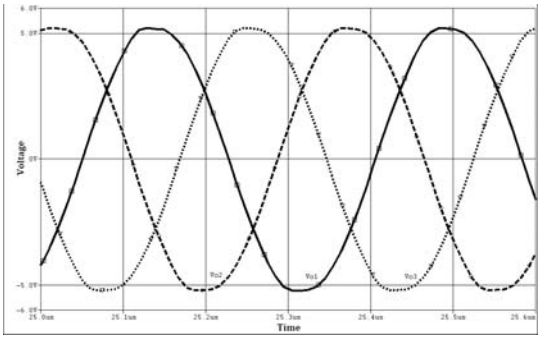
Condition of Oscillation (C_O):

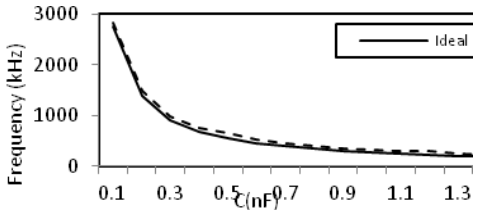
$$K = 2 \tag{7}$$

It is evident that C_O and F_O cannot be independently controlled for circuit. However the circuit is simple to realize and has a low component count. This circuit produces n odd-phase oscillations of equal amplitudes with a phase difference of $(360/n)^O$.

Simulation Results

The circuit has been simulated using PSPICE to validate the theoretical predictions. The OTRA is realized using IC AD 844 as shown in Fig. 3.3. Fig. 5.2a shows the simulation results of circuit as in Fig. 5.1 having n = 3 and component values $R_1 = R_3 = R_5 = 0.5k\Omega$, $R_2 = R_4 = R_6 = 1k\Omega$ and $C_1 = C_2 = C_3 = 100pF$. The frequency of oscillations achieved was 2.838MHz against the calculated value of 2.757 MHz having frequency error of 2.93%. Fig. 5.2b shows the simulated and theoretical frequency of oscillation as a function of capacitance (C). It shows that the simulated values deviate slightly from the ideal values at lower frequency range.





(a) Output waveform for n = 3, f = 2.838 MHz

(b) Frequency error curve

Fig.5.2 Simulation result for the circuit

5.1.2 OBSERVATIONS OF PHYSICAL CIRCUIT

The functionality of the MSO circuit is verified through hardware also. The commercial IC AD844AN is used to implement an OTRA. Supply voltages used are ±5 V. Fig. 5.3 shows the experimental results for circuit 5.1, having n = 3, for component values $R_1 = R_3 = R_5 = 2.7k\Omega$, $R_2 = R_4 = R_6 = 5.4\ k\Omega$, $R_8 = R_9 = R_{10} = 1k\Omega$ and $C_1 = C_2 = C_3 = 3.3nF$. Observed F_O is around 15.7 KHz and is in close agreement to calculated F_O of 15.469 KHz. The little variation in experimental values of F_O, as seen in Fig. 5.3, from phase to phase may be due to tolerance of the component values.

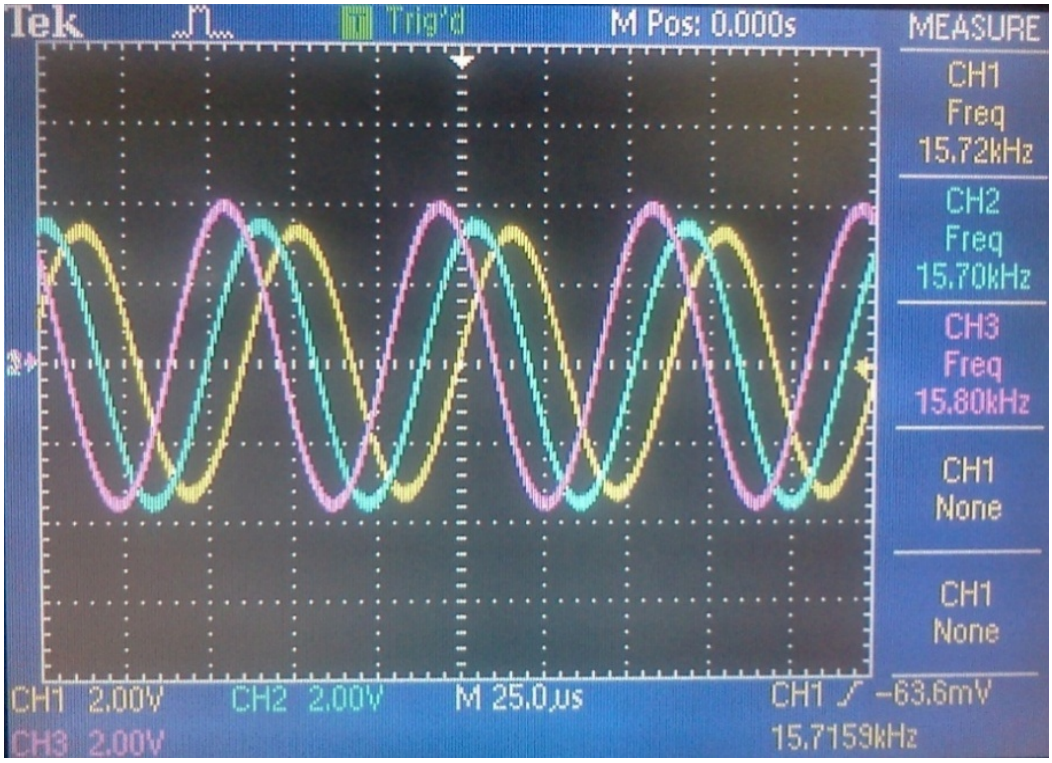


Fig 5.3 Waveform of Physical Circuit

5.2 RELAXATION OSCILLATORS

Relaxation oscillators can generate a sawtooth or triangular waveform. They can provide a wide range of operational frequencies with a minimal number of external components.

Voltage controlled oscillators

Voltage controlled oscillators are an important class of circuits and find application in function generators, frequency synthesizers and communications. The circuit presented here utilizes Operational Trans-Resistance Amplifier (OTRA) as the main active element. Conventional voltage mode op-amps aren't capable of operating at higher frequencies because of slew rate and fixed gain-bandwidth-product limitations [40].

Circuit Description

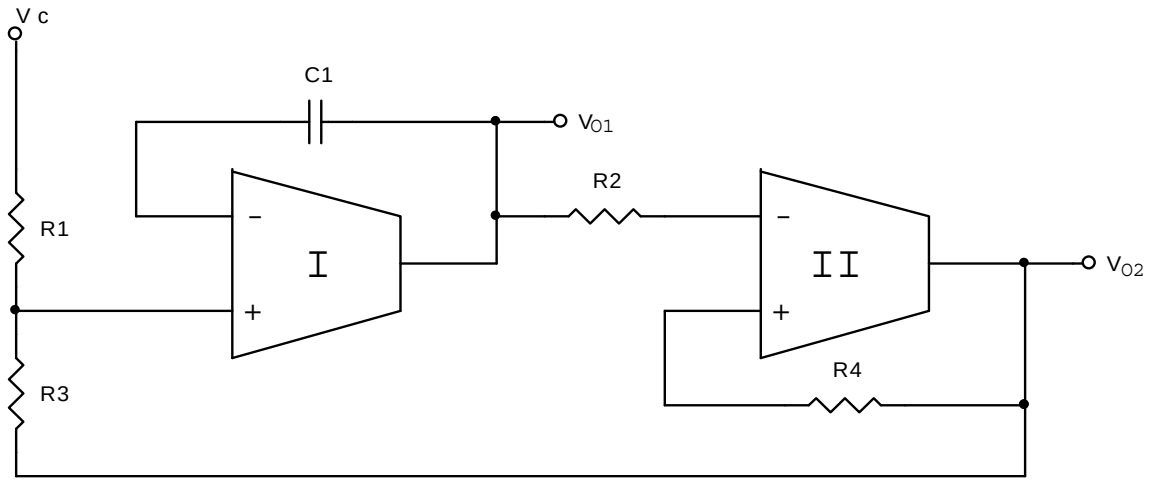


Fig. 5.4 - Voltage Controlled Relaxation Oscillator

The Fig. 5.4 shows the Voltage Controlled Relaxation Oscillator circuit. It consists of two OTRAs, four resistors and one capacitor. The circuit can be viewed as two cascaded blocks. The circuitry comprising OTRA I is a simple integrator, while the circuit comprising OTRA II, R_2 and R_4 is a Schmitt trigger working in the clockwise mode.

The threshold limits of the Schmitt trigger can be calculated as:

$$V_{TL} = \frac{R_2}{R_4} V_{02}^{+} \tag{8}$$

$$V_{TH} = \frac{R_2}{R_4} V_{02}^{-} \tag{9}$$

In the above equations, V_{02}^{+} and V_{02}^{-} signify the positive and negative saturation output levels respectively, and V_{TH} and V_{TL} signify the threshold levels for, V_{02}^{+} and V_{02}^{-} respectively of the Schmitt trigger.

For frequency calculation of the output signals, the time taken by the capacitors to charge and discharge to V_{TH} and V_{TL} must be calculated.

The time taken by the C_1 to charge to V_{TL} from level V_{TH} is given by:

$$T_{ON} = \frac{(V_{TL} - V_{TH}) C_1 R_1 R_3}{V_{02}^{+} R_1 + V_c R_3} \tag{10}$$

The time taken by the C_1 to charge to V_{TH} from level V_{TL} is given by:

$$T_{OFF} = \frac{(V_{TH} - V_{TL})C_1R_1R_3}{V_{02}^{-}R_1 + V_cR_3} \quad (11)$$

The range of tunability of this VCO circuit is dictated by (11) if V_C is positive or by (10) if V_C is negative. If V_C is positive then, since V_{TH} is negative and V_{TL} positive the numerator is negative and therefore, V_CR_3 must be less than $V^{-}_{O2}R_1$ such that denominator is also negative so that the expression on the whole is positive. The frequency of the signal can be given by:

$$F = \frac{1}{T_{ON} + T_{OFF}} \quad (12)$$

If V_{TH}, V_{TL} and V^{-}_{O2}, V^{+}_{O2} are assumed to be equal in magnitude to V_T and V_O respectively then the frequency can be calculated as:

$$F = \frac{(V_0R_1)^2 - ((V_cR_3)^2}{4V_0V_TR_1C_1{R_1}^2R_3} \quad (13)$$

The change in frequency with respect to control voltage V_C can be given by:

$$\frac{\partial F}{\partial V_c} = \frac{-V_cR_3}{2V_0V_TC_1{R_1}^2} \quad (14)$$

By controlling (12) the sensitivity of the output frequency to change in the input voltage level can be adjusted to the desired level. For example, if the value of R_3 is high the circuit will be more sensitive to the voltage changes at the input. The amplitude of the triangular wave is V_T which can be changed by using (8) and (9).

Simulation Results

To verify the workability of the VCO circuit, the circuit was simulated using the PSPICE program. Fig. 5.5a, b, and c show the simulation results achieved with the circuit given in Fig. 5.4

The components values used are

R_1, R_2 = 470Ω

R_3 = 1kΩ

R_4 = 750Ω

C_1 = 1nF

Fig. 5.6 shows the comparison between the calculated frequency and the achieved frequency of oscillations. The time taken by the OTRA to change its output level becomes comparable to T_{ON} and T_{OFF} at higher frequencies which results in slight variation in the calculated and the observed frequency in the higher frequency range.

Although, high frequencies are achievable there is a trade-off to be made between high frequency and accuracy as the gap between the predicted theoretical frequency and the achieved frequency in the simulations becomes larger as the frequency increases.

By using the Schmitt trigger connected in the counter clock wise mode and the integrator in the inverted mode, the circuit presented here can also be connected in a different configuration, giving outputs differing in phase as obtained from the configuration presented.

The presented circuit has two major drawbacks. Firstly, the non linearity of the output signal with respect to the control voltage and secondly, the non-uniform duty cycle of the output signal which changes with the frequency. The reason behind the non-uniform duty cycle is the increasing difference between T_{ON} and T_{OFF}. An alternate approach can be suggested to overcome these drawbacks.

Fig. 5.5 Simulation results of VCO

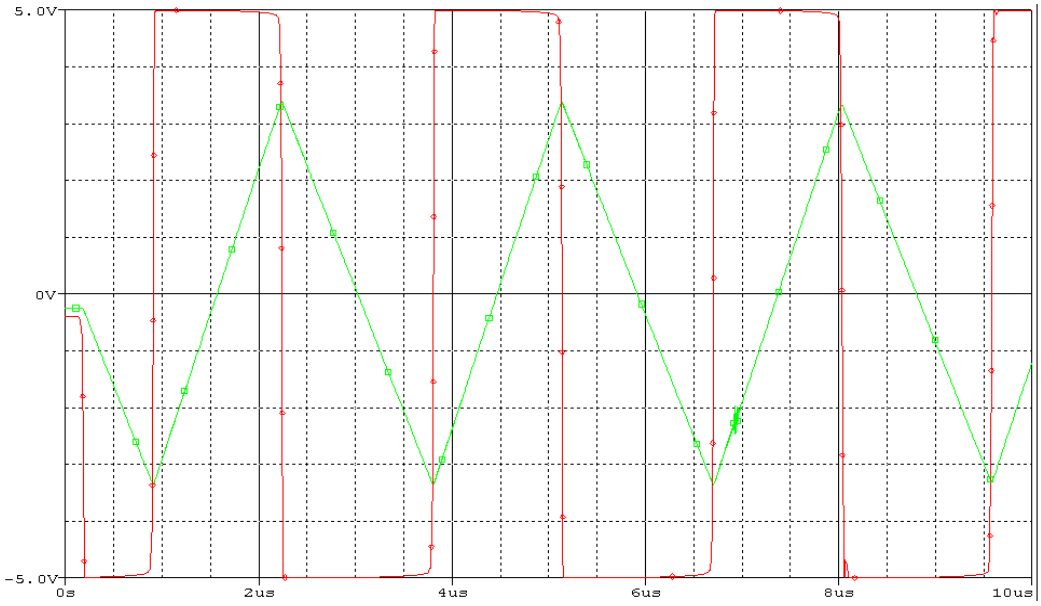


Fig. 5.5a - 345.185 KHz frequency against Vc of 0.2V

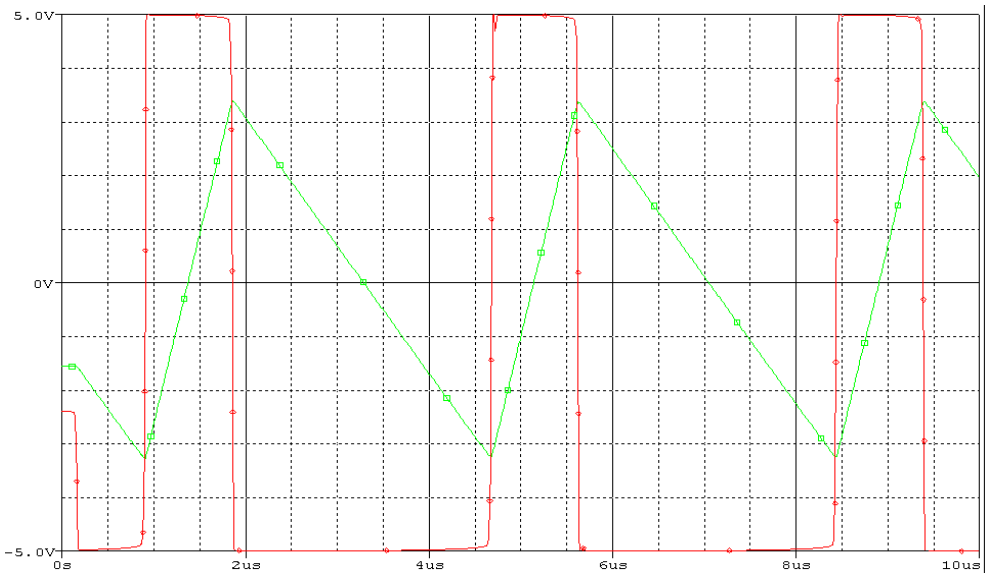


Fig. 5.5b - 265.182 KHz frequency against Vc of 1.2V

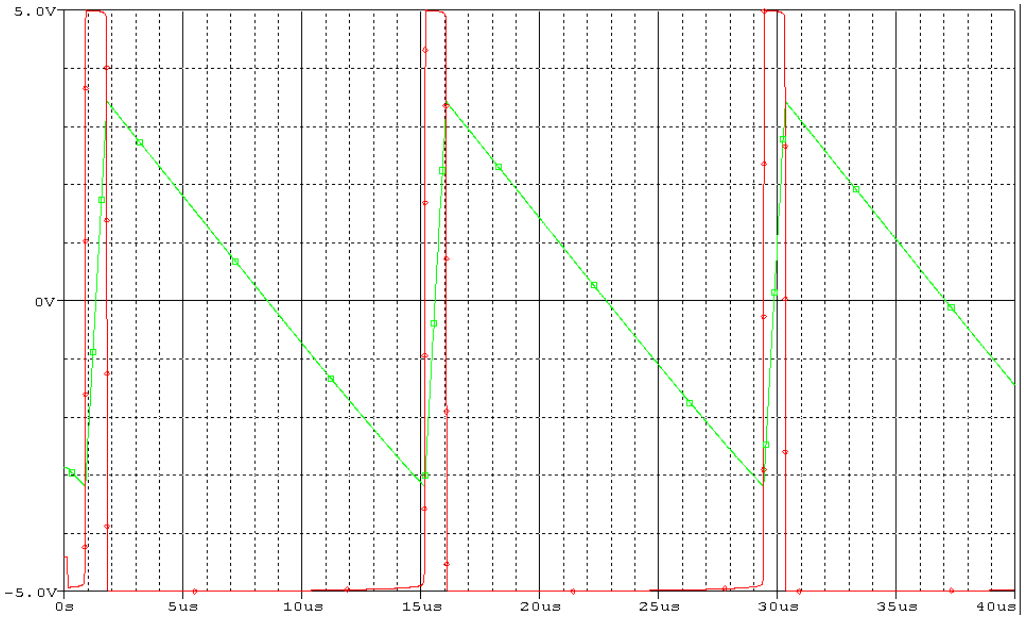


Fig. 5.5c - 70.028 KHz frequency against Vc of 2.2V

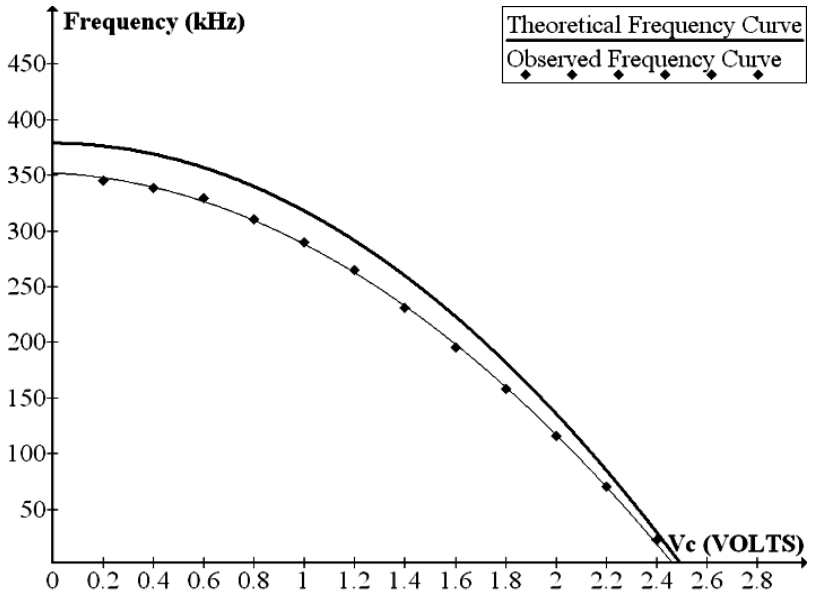
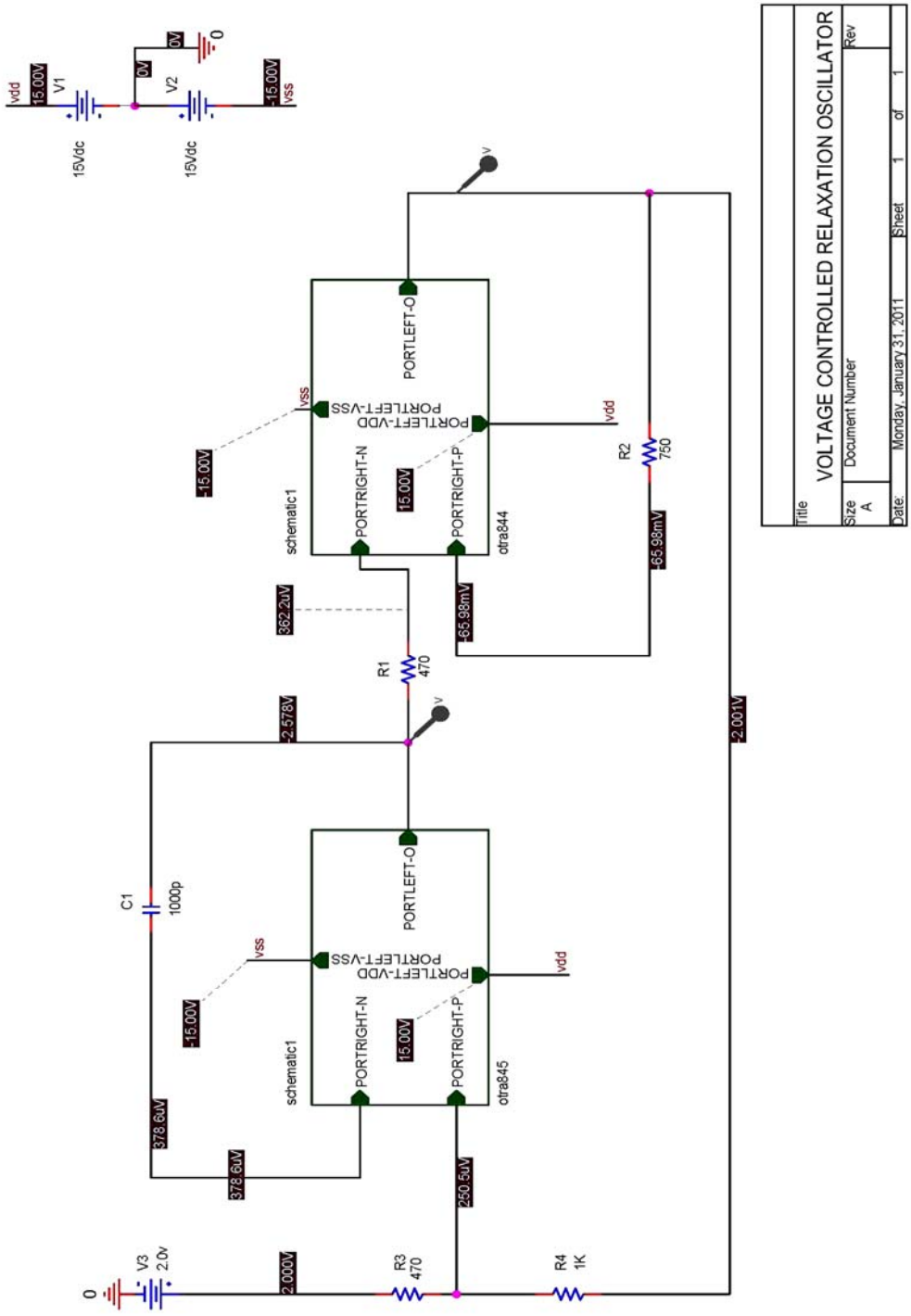


Fig. 5.6 - Comparison Curves

Schematic Circuit of the Voltage Controlled Relaxation Oscillator



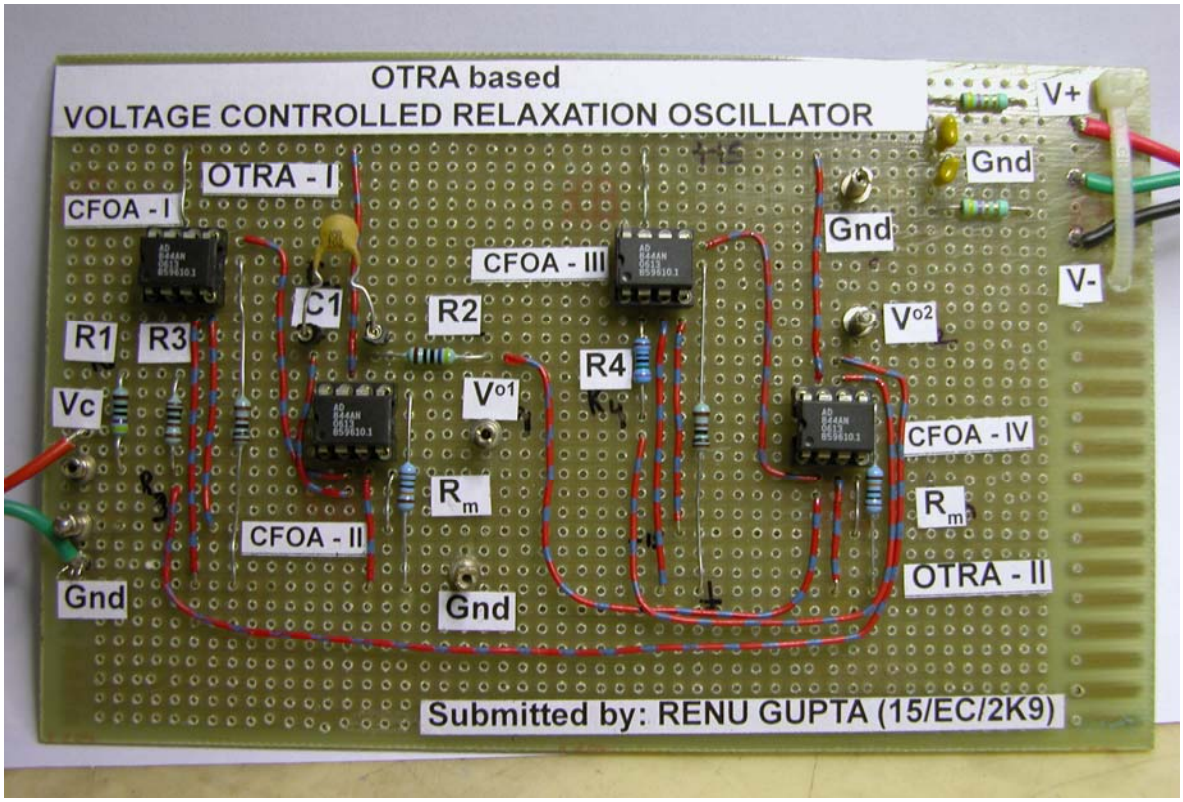
5.2.1 OBSERVATIONS OF PHYSICAL CIRCUIT

Voltage Controlled Relaxation Oscillator		
Observations Taken during Testing		
S.No.	**Vc**	**Frequency at Vo2**
1	0.2	575.16 KHz
2	0.4	547.90 KHz
3	0.5	536.89 KHz
4	1.0	526.29 KHz
5	1.5	506.45 KHz
6	2.0	503.66 KHz
7	2.5	432.94 KHz
8	2.7	387.20 KHz
9	3.0	276.39 KHz

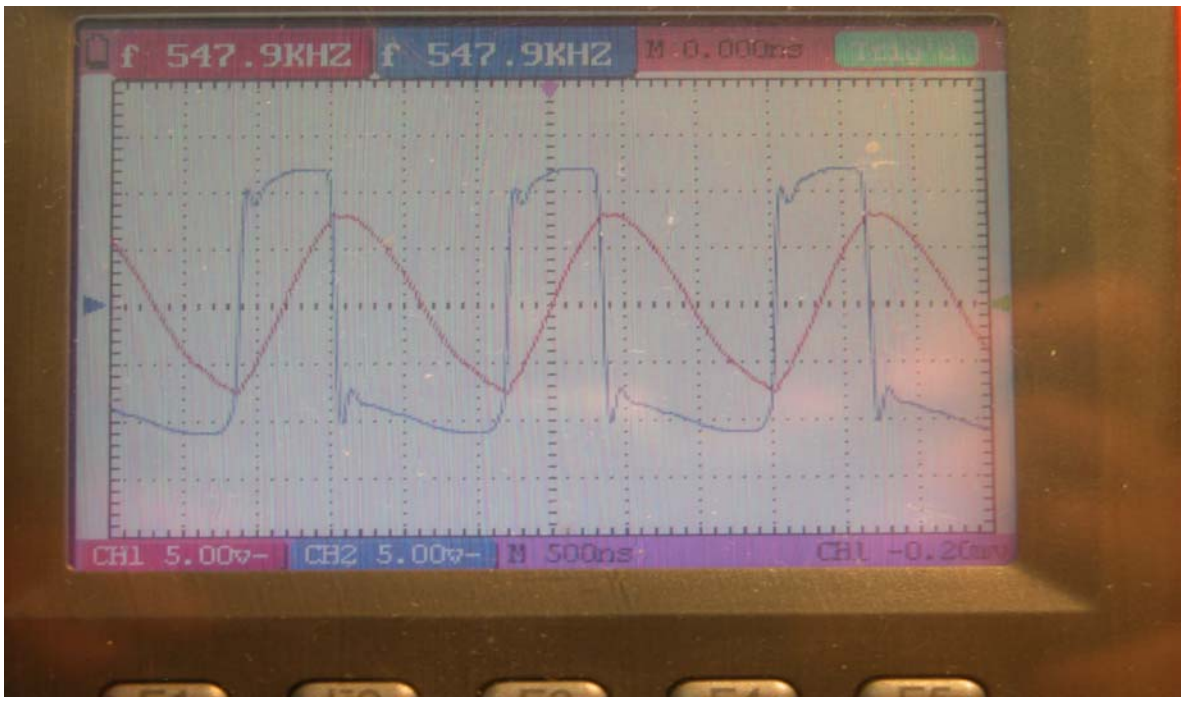
Table 5.1 Observations taken on Practical Circuit

The above observations were taken on the physical circuit assembled

Picture of Physical Circuit Assembled for Voltage Controlled Oscillator



Wave forms of VCO taken at respective Vin



CONCLUSION & FUTURE SCOPE OF WORK

Current-mode logic designs are attracting a lot of interest owing to their inherent advantages over conventional voltage-mode techniques. Its advantages can once again be summarized as follows:

- Higher bandwidth
- Low slew rates
- Low power consumption
- Lower supply voltages required
- Simplified circuit topologies

There are a number of new analog basic building blocks which are capable of Analog IC circuit designs each having some advantages/ disadvantages over others. These include Trans-linear circuits, current conveyors, current feedback amplifiers, OTAs, OTRAs, etc.

The main focus of this report has been on using OTRA as a basic building block in analog circuit design and circuits employing it to generate and process analog signals. First the realization of OTRAs has been discussed, both using CMOS technology, as well as using CFOA as the basic building block, and then its applications in various circuits has been discussed.

Working on the applications of OTRA, a block was developed which can simulate grounded inductor. The block has been tested for operation by assembling a band-pass filter. The results obtained conform to the theoretically expected results.

Some of the experimentally assembled and tested circuits include, Operational Trans-Resistance Amplifier (OTRA) based filters, multiphase sinusoidal oscillators, voltage controlled oscillator.

The VCO circuit using Operational Trans-Resistance Amplifier (OTRA) as the main active element has been presented in this project. As it is not slew limited and is free from fixed gain bandwidth product it is possible to operate the circuit at higher frequencies unlike conventional voltage mode op-amps .

Further Scope of Work :

It is clear that future of analog signal processing is very dynamic and current mode analog IC design would be catalytic in a decade where we are witnessing tremendous improvements in process technologies. It is only now becoming possible with such improvements in technology that with current mode analog techniques are providing dramatic benefits in practical circuits and systems.

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Appendix

Data Sheet of AD 844 AN (Analog Devices)

60 MHz 2000 V/µs Monolithic Op Amp

AD844

FEATURES

Wide bandwidth
60 MHz at gain of −1
33 MHz at gain of −10
Slew rate: 2000 V/µs
20 MHz full power bandwidth, 20 V p-p, R_L = 500 Ω
Fast settling: 100 ns to 0.1% (10 V step)
Differential gain error: 0.03% at 4.4 MHz
Differential phase error: 0.16° at 4.4 MHz
Low offset voltage: 150 µV maximum (B Grade)
Low quiescent current: 6.5 mA
Available in tape and reel in accordance with EIA-481-A standard

APPLICATIONS

Flash ADC input amplifiers
High speed current DAC interfaces
Video buffers and cable drivers
Pulse amplifiers

GENERAL DESCRIPTION

The AD844 is a high speed monolithic operational amplifier fabricated using the Analog Devices, Inc., junction isolated complementary bipolar (CB) process. It combines high bandwidth and very fast large signal response with excellent dc performance. Although optimized for use in current-to-voltage applications and as an inverting mode amplifier, it is also suitable for use in many noninverting applications.

The AD844 can be used in place of traditional op amps, but its current feedback architecture results in much better ac performance, high linearity, and an exceptionally clean pulse response.

This type of op amp provides a closed-loop bandwidth that is determined primarily by the feedback resistor and is almost independent of the closed-loop gain. The AD844 is free from the slew rate limitations inherent in traditional op amps and other current-feedback op amps. Peak output rate of change can be over 2000 V/µs for a full 20 V output step. Settling time is typically 100 ns to 0.1%, and essentially independent of gain. The AD844 can drive 50 Ω loads to ±2.5 V with low distortion and is short-circuit protected to 80 mA.

The AD844 is available in four performance grades and three package options. In the 16-lead SOIC (RW) package, the AD844J is specified for the commercial temperature range of 0°C to 70°C.

FUNCTIONAL BLOCK DIAGRAMS

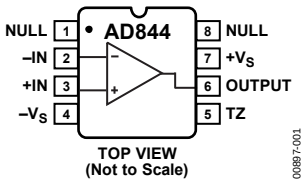

Figure 1. 8-Lead PDIP (N) and 8-Lead CERDIP (Q) Packages

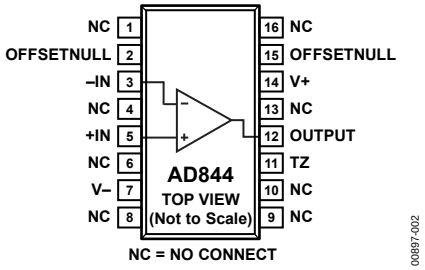

Figure 2. 16-Lead SOIC (R) Package

The AD844A and AD844B are specified for the industrial temperature range of −40°C to +85°C and are available in the CERDIP (Q) package. The AD844A is also available in an 8-lead PDIP (N). The AD844S is specified over the military temperature range of −55°C to +125°C. It is available in the 8-lead CERDIP (Q) package. A and S grade chips and devices processed to MIL-STD-883B, Rev. C are also available.

PRODUCT HIGHLIGHTS

1. The AD844 is a versatile, low cost component providing an excellent combination of ac and dc performance.
2. It is essentially free from slew rate limitations. Rise and fall times are essentially independent of output level.
3. The AD844 can be operated from ±4.5 V to ±18 V power supplies and is capable of driving loads down to 50 Ω, as well as driving very large capacitive loads using an external network.
4. The offset voltage and input bias currents of the AD844 are laser trimmed to minimize dc errors; V_{OS} drift is typically 1 µV/°C and bias current drift is typically 9 nA/°C.
5. The AD844 exhibits excellent differential gain and differential phase characteristics, making it suitable for a variety of video applications with bandwidths up to 60 MHz.
6. The AD844 combines low distortion, low noise, and low drift with wide bandwidth, making it outstanding as an input amplifier for flash analog-to-digital converters (ADCs).

Rev. F

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

SPECIFICATIONS

T_A = 25°C and V_S = ±15 V dc, unless otherwise noted.

Table 1.

		AD844J/AD844A			AD844B			AD844S			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
INPUT OFFSET VOLTAGE[1]			50	300		50	150		50	300	µV
T_{MIN} to T_{MAX}			75	500		75	200		125	500	µV
vs. Temperature			1			1	5		1	5	µV/°C
vs. Supply	5 V to 18 V										
Initial			4	20		4	10		4	20	µV/V
T_{MIN} to T_{MAX}			4			4	10		4	20	µV/V
vs. Common Mode	V_{CM} = ±10 V										
Initial			10	35		10	20		10	35	µV/V
T_{MIN} to T_{MAX}			10			10	20		10	35	µV/V
INPUT BIAS CURRENT											
Negative Input Bias Current[1]			200	450		150	250		200	450	nA
T_{MIN} to T_{MAX}			800	1500		750	1100		1900	2500	nA
vs. Temperature			9			9	15		20	30	nA/°C
vs. Supply	5 V to 18 V										
Initial			175	250		175	200		175	250	nA/V
T_{MIN} to T_{MAX}			220			220	240		220	300	nA/V
vs. Common Mode	V_{CM} = ±10 V										
Initial			90	160		90	110		90	160	nA/V
T_{MIN} to T_{MAX}			110			110	150		120	200	nA/V
Positive Input Bias Current[1]			150	400		100	200		100	400	nA
T_{MIN} to T_{MAX}			350	700		300	500		800	1300	nA
vs. Temperature			3			3	7		7	15	nA/°C
vs. Supply	5 V to 18 V										
Initial			80	150		80	100		80	150	nA/V
T_{MIN} to T_{MAX}			100			100	120		120	200	nA/V
vs. Common Mode	V_{CM} = ±10 V										
Initial			90	150		90	120		90	150	nA/V
T_{MIN} to T_{MAX}			130			130	190		140	200	nA/V
INPUT CHARACTERISTICS											
Input Resistance											
Negative Input			50	65		50	65		50	65	Ω
Positive Input		7	10		7	10		7	10		MΩ
Input Capacitance											
Negative Input			2			2			2		pF
Positive Input			2			2			2		pF
Input Common-Mode Voltage Range		±10			±10			±10			V
INPUT VOLTAGE NOISE	f ≥ 1 kHz		2			2			2		nV/√Hz
INPUT CURRENT NOISE											
Negative Input	f ≥ 1 kHz		10			10			10		pV/√Hz
Positive Input	f ≥ 1 kHz		12			12			12		pV/√Hz
OPEN-LOOP TRANSRESISTANCE	V_{OUT} = ±10 V										
	R_L = 500 Ω	2.2	3.0		2.8	3.0		2.2	3.0		MΩ
T_{MIN} to T_{MAX}		1.3	2.0		1.6	2.0		1.3	1.6		MΩ
Transcapacitance			4.5			4.5			4.5		pF
DIFFERENTIAL GAIN ERROR[2]	f = 4.4 MHz		0.03			0.03			0.03		%
DIFFERENTIAL PHASE ERROR[2]	f = 4.4 MHz		0.16			0.16			0.16		Degree

Parameter	Conditions	AD844J/AD844A Min	AD844J/AD844A Typ	AD844J/AD844A Max	AD844B Min	AD844B Typ	AD844B Max	AD844S Min	AD844S Typ	AD844S Max	Unit
FREQUENCY RESPONSE											
Small Signal Bandwidth[3, 4]											
Gain = −1			60			60			60		MHz
Gain = −10			33			33			33		MHz
TOTAL HARMONIC DISTORTION	f = 100 kHz, 2 V rms[5]		0.005			0.005			0.005		%
SETTLING TIME											
10 V Output Step	±15 V supplies										
Gain = −1, to 0.1%[5]			100			100			100		ns
Gain = −10, to 0.1%[6]			100			100			100		ns
2 V Output Step	±5 V supplies										
Gain = −1, to 0.1%[5]			110			110			110		ns
Gain = −10, to 0.1%[6]			100			100			100		ns
OUTPUT SLEW RATE	Overdriven input	1200	2000		1200	2000		1200	2000		V/µs
FULL POWER BANDWIDTH	THD = 3%										
V_{OUT} = 20 V p-p[5]	V_S = ±15 V		20			20			20		MHz
V_{OUT} = 2 V p-p[5]	V_S = ±5 V		20			20			20		MHz
OUTPUT CHARACTERISTICS											
Voltage	R_L = 500 Ω	±10	±11		±10	±11		±10	±11		V
Short-Circuit Current			80			80			80		mA
T_{MIN} to T_{MAX}			60			60			60		mA
Output Resistance	Open loop		15			15			15		Ω
POWER SUPPLY											
Operating Range		±4.5		±18	±4.5		±18	±4.5		±18	V
Quiescent Current			6.5	7.5		6.5	7.5		6.5	7.5	mA
T_{MIN} to T_{MAX}			7.5	8.5		7.5	8.5		7.5	8.5	mA

[1] Rated performance after a 5 minute warm-up at T_A = 25°C.
[2] Input signal 285 mV p-p carrier (40 IRE) riding on 0 mV to 642 mV (90 IRE) ramp. R_L = 100 Ω; R1, R2 = 300 Ω.
[3] For gain = −1, input signal = 0 dBm, C_L = 10 pF, R_L = 500 Ω, R1 = 500 Ω, and R2 = 500 Ω in Figure 29.
[4] For gain = −10, input signal = 0 dBm, C_L =10 pF, R_L = 500 Ω, R1 = 500 Ω, and R2 = 50 Ω in Figure 29.
[5] C_L = 10 pF, R_L = 500 Ω, R1 = 1 kΩ, R2 = 1 kΩ in Figure 29.
[6] C_L = 10 pF, R_L = 500 Ω, R1 = 500 Ω, R2 = 50 Ω in Figure 29.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C and V_S = ±15 V, unless otherwise noted.

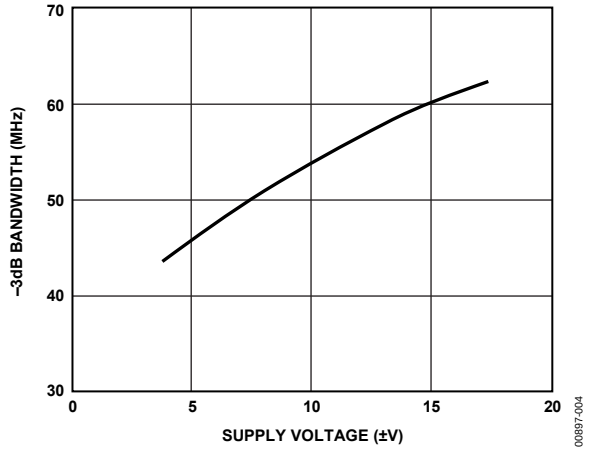

Figure 4. –3 dB Bandwidth vs. Supply Voltage, R1 = R2 = 500 Ω

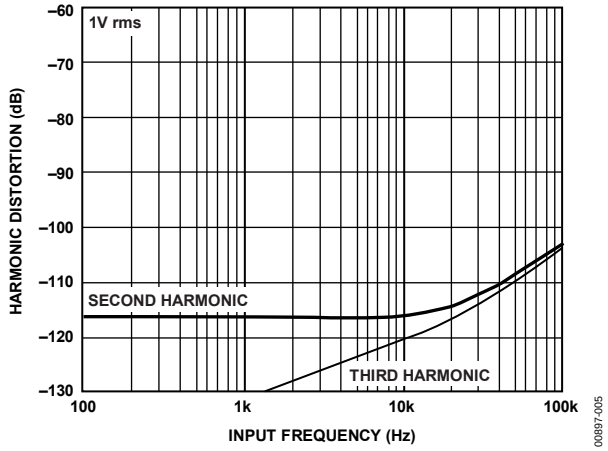

Figure 5. Harmonic Distortion vs. Input Frequency, R1 = R2 = 1 kΩ

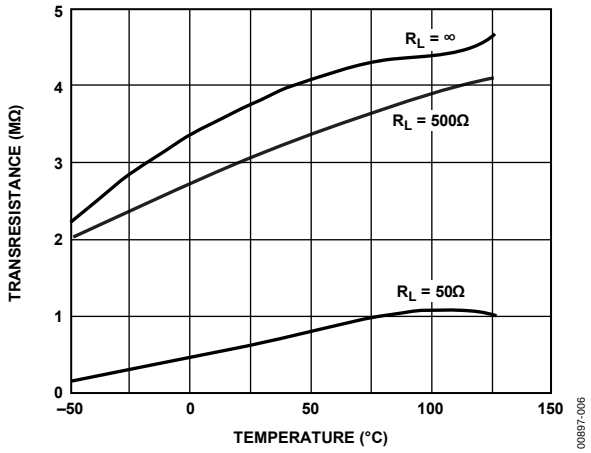

Figure 6. Transresistance vs. Temperature

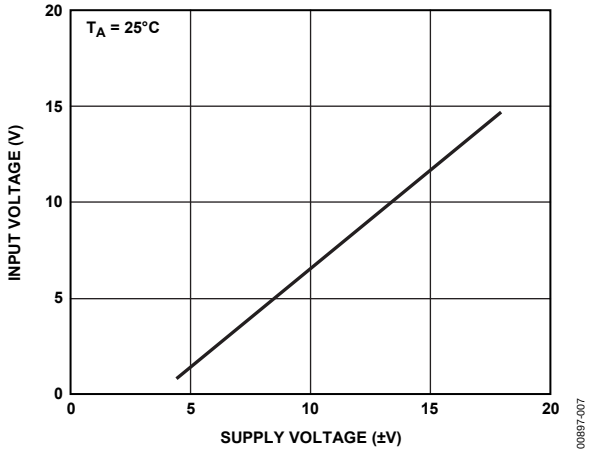

Figure 7. Noninverting Input Voltage Swing vs. Supply Voltage

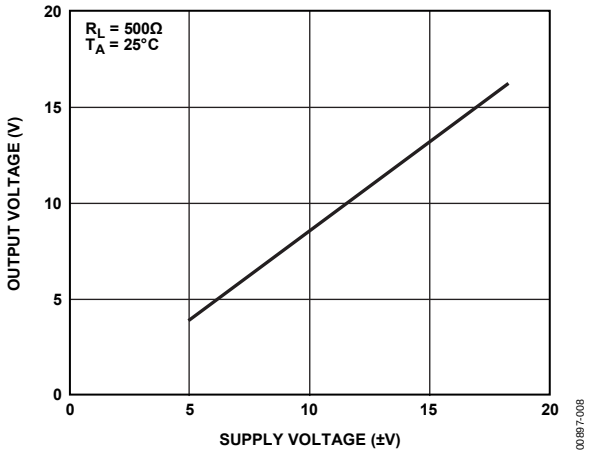

Figure 8. Output Voltage Swing vs. Supply Voltage

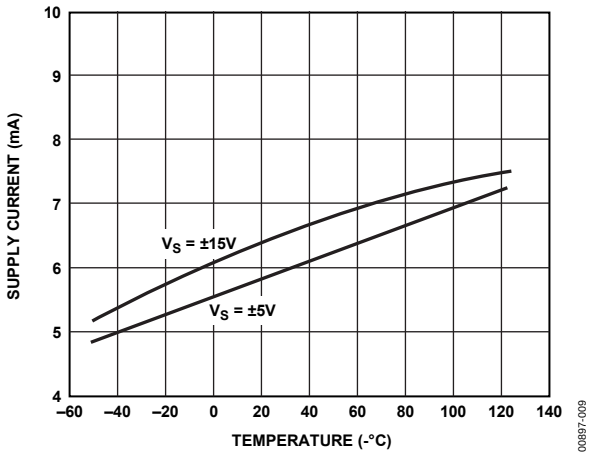

Figure 9. Quiescent Supply Current vs. Temperature and Supply Voltage

UNDERSTANDING THE AD844

The AD844 can be used in ways similar to a conventional op amp while providing performance advantages in wideband applications. However, there are important differences in the internal structure that need to be understood to optimize the performance of the AD844 op amp.

OPEN-LOOP BEHAVIOR

Figure 28 shows a current feedback amplifier reduced to essentials. Sources of fixed dc errors, such as the inverting node bias current and the offset voltage, are excluded from this model. The most important parameter limiting the dc gain is the transresistance, R_t, which is ideally infinite. A finite value of R_t is analogous to the finite open-loop voltage gain in a conventional op amp.

The current applied to the inverting input node is replicated by the current conveyor to flow in Resistor R_t. The voltage developed across R_t is buffered by the unity gain voltage follower. Voltage gain is the ratio R_t/R_{IN}. With typical values of R_t = 3 MΩ and R_{IN} = 50 Ω, the voltage gain is about 60,000. The open-loop current gain, another measure of gain that is determined by the beta product of the transistors in the voltage follower stage (see Figure 31), is typically 40,000.

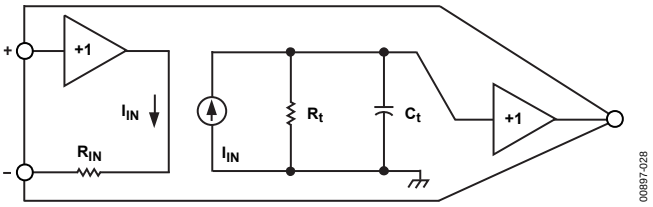

Figure 28. Equivalent Schematic

The important parameters defining ac behavior are the transcapacitance, C_t, and the external feedback resistor (not shown). The time constant formed by these components is analogous to the dominant pole of a conventional op amp and thus cannot be reduced below a critical value if the closed-loop system is to be stable. In practice, C_t is held to as low a value as possible (typically 4.5 pF) so that the feedback resistor can be maximized while maintaining a fast response. The finite R_{IN} also affects the closed-loop response in some applications.

The open-loop ac gain is also best understood in terms of the transimpedance rather than as an open-loop voltage gain. The open-loop pole is formed by R_t in parallel with C_t. Because C_t is typically 4.5 pF, the open-loop corner frequency occurs at about 12 kHz. However, this parameter is of little value in determining the closed-loop response.

RESPONSE AS AN INVERTING AMPLIFIER

Figure 29 shows the connections for an inverting amplifier. Unlike a conventional amplifier, the transient response and the small signal bandwidth are determined primarily by the value of the external feedback resistor, R1, rather than by the ratio of R1/R2 as is customarily the case in an op amp application. This is a direct result of the low impedance at the inverting input. As with conventional op amps, the closed-loop gain is –R1/R2.

The closed-loop transresistance is the parallel sum of R1 and R_t. Because R1 is generally in the range of 500 Ω to 2 kΩ and R_t is about 3 MΩ, the closed-loop transresistance is only 0.02% to 0.07% lower than R1. This small error is often less than the resistor tolerance.

When R1 is fairly large (above 5 kΩ) but still much less than R_t, the closed-loop HF response is dominated by the time constant R1 C_t. Under such conditions, the AD844 is overdamped and provides only a fraction of its bandwidth potential. Because of the absence of slew rate limitations under these conditions, the circuit exhibits a simple single-pole response even under large signal conditions.

In Figure 29, R3 is used to properly terminate the input if desired. R3 in parallel with R2 gives the terminated resistance. As R1 is lowered, the signal bandwidth increases, but the time constant R1 C_t becomes comparable to higher order poles in the closed-loop response. Therefore, the closed-loop response becomes complex, and the pulse response shows overshoot. When R2 is much larger than the input resistance, R_{IN}, at Pin 2, most of the feedback current in R1 is delivered to this input, but as R2 becomes comparable to R_{IN}, less of the feedback is absorbed at Pin 2, resulting in a more heavily damped response. Consequently, for low values of R2, it is possible to lower R1 without causing instability in the closed-loop response. Table 3 lists combinations of R1 and R2 and the resulting frequency response for the circuit of Figure 29. Figure 16 shows the very clean and fast ±10 V pulse response of the AD844.

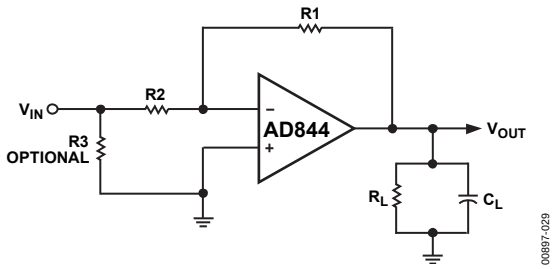

Figure 29. Inverting Amplifier

Table 3. Gain vs. Bandwidth

Gain	R1	R2	BW (MHz)	GBW (MHz)
–1	1 kΩ	1 kΩ	35	35
–1	500 Ω	500 Ω	60	60
–2	2 kΩ	1 kΩ	15	30
–2	1 kΩ	500 Ω	30	60
–5	5 kΩ	1 kΩ	5.2	26
–5	500 Ω	100 Ω	49	245
–10	1 kΩ	100 Ω	23	230
–10	500 Ω	50 Ω	33	330
–20	1 kΩ	50 Ω	21	420
–100	5 kΩ	50 Ω	3.2	320

RESPONSE AS AN I-V CONVERTER

The AD844 works well as the active element in an operational current-to-voltage converter, used in conjunction with an external scaling resistor, R1, in Figure 30. This analysis includes the stray capacitance, C_S, of the current source, which may be a high speed DAC. Using a conventional op amp, this capacitance forms a nuisance pole with R1 that destabilizes the closed-loop response of the system. Most op amps are internally compensated for the fastest response at unity gain, so the pole due to R1 and C_S reduces the already narrow phase margin of the system. For example, if R1 is 2.5 kΩ, a C_S of 15 pF places this pole at a frequency of about 4 MHz, well within the response range of even a medium speed operational amplifier. In a current feedback amp, this nuisance pole is no longer determined by R1 but by the input resistance, R_{IN}. Because this is about 50 Ω for the AD844, the same 15 pF forms a pole at 212 MHz and causes little trouble. It can be shown that the response of this system is:

$$V_{OUT} = I_{sig} \frac{K\,R1}{(1+s_{Td})(1+s_{Tn})}$$

where:
K is a factor very close to unity and represents the finite dc gain of the amplifier.
Td is the dominant pole.
Tn is the nuisance pole.

$$K = \frac{R_t}{R_t + R1}$$

$$Td = KR1C_t$$

$$Tn = R_{IN}C_S \text{ (assuming } R_{IN} << R1)$$

Using typical values of R1 = 1 kΩ and R_t = 3 MΩ, K = 0.9997; in other words, the gain error is only 0.03%. This is much less than the scaling error of virtually all DACs and can be absorbed, if necessary, by the trim needed in a precise system.

In the AD844, R_t is fairly stable with temperature and supply voltages, and consequently the effect of finite gain is negligible unless high value feedback resistors are used. Because that results in slower response times than are possible, the relatively low value of R_t in the AD844 is rarely a significant source of error.

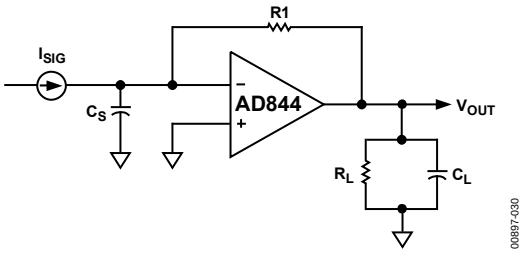

Figure 30. Current-to-Voltage Converter

CIRCUIT DESCRIPTION OF THE AD844

A simplified schematic is shown in Figure 31. The AD844 differs from a conventional op amp in that the signal inputs have radically different impedance. The noninverting input (Pin 3) presents the usual high impedance. The voltage on this input is transferred to the inverting input (Pin 2) with a low offset voltage, ensured by the close matching of like polarity transistors operating under essentially identical bias conditions. Laser trimming nulls the residual offset voltage, down to a few tens of microvolts. The inverting input is the common emitter node of a complementary pair of grounded base stages and behaves as a current summing node. In an ideal current feedback op amp, the input resistance is zero. In the AD844, it is about 50 Ω.

A current applied to the inverting input is transferred to a complementary pair of unity-gain current mirrors that deliver the same current to an internal node (Pin 5) at which the full output voltage is generated. The unity-gain complementary voltage follower then buffers this voltage and provides the load driving power. This buffer is designed to drive low impedance loads, such as terminated cables, and can deliver ±50 mA into a 50 Ω load while maintaining low distortion, even when operating at supply voltages of only ±6 V. Current limiting (not shown) ensures safe operation under short-circuited conditions.

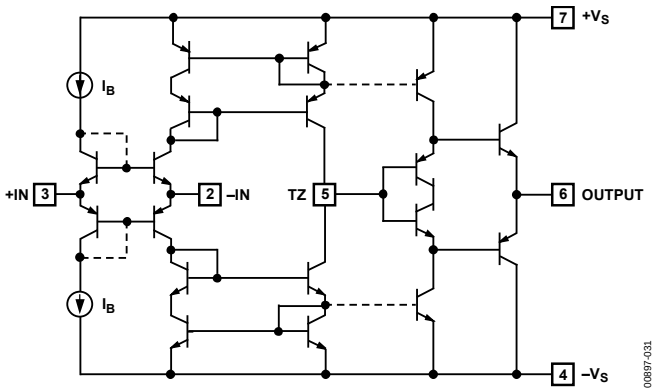

Figure 31. Simplified Schematic

It is important to understand that the low input impedance at the inverting input is locally generated and does not depend on feedback. This is very different from the virtual ground of a conventional operational amplifier used in the current summing mode, which is essentially an open circuit until the loop settles. In the AD844, transient current at the input does not cause voltage spikes at the summing node while the amplifier is settling. Furthermore, all of the transient current is delivered to the slewing (TZ) node (Pin 5) via a short signal path (the grounded base stages and the wideband current mirrors).

The current available to charge the capacitance (about 4.5 pF) at the TZ node is always proportional to the input error current, and the slew rate limitations associated with the large signal response of the op amps do not occur. For this reason, the rise and fall times are almost independent of signal level. In practice, the input current eventually causes the mirrors to saturate. When using ±15 V supplies, this occurs at about 10 mA (or ±2200 V/µs). Because signal currents are rarely this large, classical slew rate limitations are absent.

This inherent advantage is lost if the voltage follower used to buffer the output has slew rate limitations. The AD844 is designed to avoid this problem, and as a result, the output buffer exhibits a clean large signal transient response, free from anomalous effects arising from internal saturation.

RESPONSE AS A NONINVERTING AMPLIFIER

Because current feedback amplifiers are asymmetrical with regard to their two inputs, performance differs markedly in noninverting and inverting modes. In noninverting modes, the large signal high speed behavior of the AD844 deteriorates at low gains because the biasing circuitry for the input system (not shown in Figure 31) is not designed to provide high input voltage slew rates.

However, good results can be obtained with some care. The noninverting input does not tolerate a large transient input; it must be kept below ±1 V for best results. Consequently, this mode is better suited to high gain applications (greater than ×10). Figure 23 shows a noninverting amplifier with a gain of 10 and a bandwidth of 30 MHz. The transient response is shown in Figure 26 and Figure 27. To increase the bandwidth at higher gains, a capacitor can be added across R2 whose value is approximately (R1/R2) × C_t.

NONINVERTING GAIN OF 100

The AD844 provides very clean pulse response at high noninverting gains. Figure 32 shows a typical configuration providing a gain of 100 with high input resistance. The feedback resistor is kept as low as practicable to maximize bandwidth, and a peaking capacitor (C_{PK}) can optionally be added to further extend the bandwidth. Figure 33 shows the small signal response with C_{PK} = 3 nF, R_L = 500 Ω, and supply voltages of either ±5 V or ±15 V. Gain bandwidth products of up to 900 MHz can be achieved in this way.

The offset voltage of the AD844 is laser trimmed to the 50 µV level and exhibits very low drift. In practice, there is an additional offset term due to the bias current at the inverting input (I_{BN}), which flows in the feedback resistor (R1). This can optionally be nulled by the trimming potentiometer shown in Figure 32.

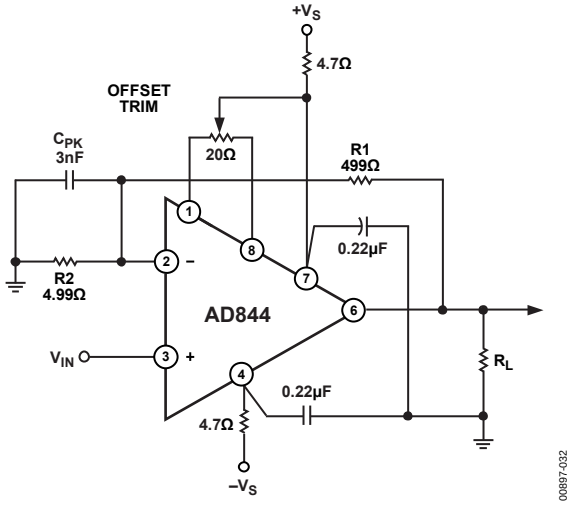

Figure 32. Noninverting Amplifier Gain = 100, Optional Offset Trim Is Shown

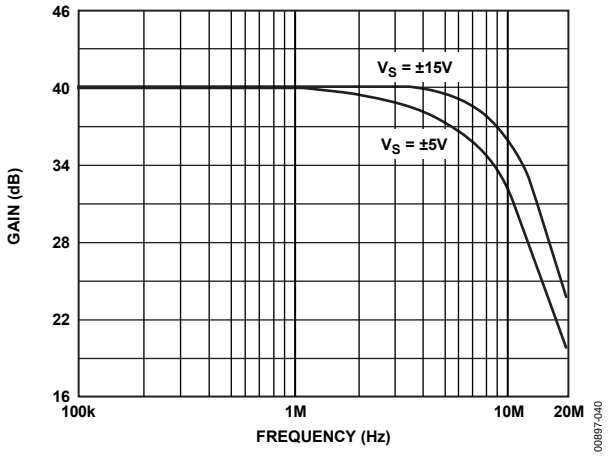

Figure 33. AC Response for Gain = 100, Configuration Shown in Figure 32

USING THE AD844

BOARD LAYOUT

As with all high frequency circuits considerable care must be used in the layout of the components surrounding the AD844. A ground plane, to which the power supply decoupling capacitors are connected by the shortest possible leads, is essential to achieving clean pulse response. Even a continuous ground plane exhibits finite voltage drops between points on the plane, and this must be kept in mind when selecting the grounding points. In general, decoupling capacitors should be taken to a point close to the load (or output connector) because the load currents flow in these capacitors at high frequencies. The +IN and −IN circuits (for example, a termination resistor and Pin 3) must be taken to a common point on the ground plane close to the amplifier package.

Use low impedance 0.22 µF capacitors (AVX SR305C224KAA or equivalent) wherever ac coupling is required. Include either ferrite beads and/or a small series resistance (approximately 4.7 Ω) in each supply line.

INPUT IMPEDANCE

At low frequencies, negative feedback keeps the resistance at the inverting input close to zero. As the frequency increases, the impedance looking into this input increases from near zero to the open-loop input resistance, due to bandwidth limitations, making the input seem inductive. If it is desired to keep the input impedance flatter, a series RC network can be inserted across the input. The resistor is chosen so that the parallel sum of it and R2 equals the desired termination resistance. The capacitance is set so that the pole determined by this RC network is about half the bandwidth of the op amp. This network is not important if the input resistor is much larger than the termination used, or if frequencies are relatively low. In some cases, the small peaking that occurs without the network can be of use in extending the −3 dB bandwidth.

DRIVING LARGE CAPACITIVE LOADS

Capacitive drive capability is 100 pF without an external network. With the addition of the network shown in Figure 34, the capacitive drive can be extended to over 10,000 pF, limited by internal power dissipation. With capacitive loads, the output speed becomes a function of the overdriven output current limit. Because this is roughly ±100 mA, under these conditions, the maximum slew rate into a 1000 pF load is ±100 V/µs. Figure 35 shows the transient response of an inverting amplifier (R1 = R2 = 1 kΩ) using the feedforward network shown in Figure 34, driving a load of 1000 pF.

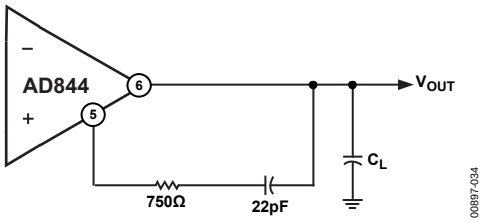

Figure 34. Feedforward Network for Large Capacitive Loads

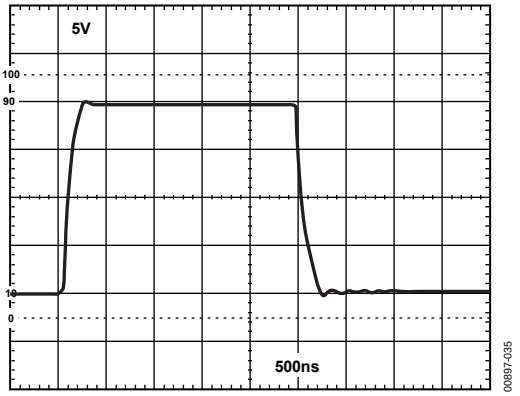

Figure 35. Driving 1000 pF C_L with Feedforward Network of Figure 34

SETTLING TIME

Settling time is measured with the circuit of Figure 36. This circuit employs a false summing node, clamped by the two Schottky diodes, to create the error signal and limit the input signal to the oscilloscope. For measuring settling time, the ratio of R6/R5 is equal to R1/R2. For unity gain, R6 = R5 = 1 kΩ, and R_L = 500 Ω. For the gain of −10, R5 = 50 Ω, R6 = 500 Ω, and R_L was not used because the summing network loads the output with approximately 275 Ω. Using this network in a unity-gain configuration, settling time is 100 ns to 0.1% for a −5 V to +5 V step with C_L = 10 pF.

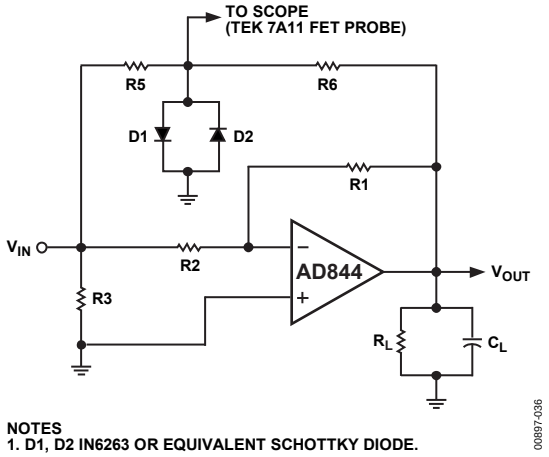

Figure 36. Settling Time Test Fixture