**Chapter 1 Introduction**

**1.1 Motivation**

Out surrounding world is analog in nature. Digital systems require analog to digital conversion at the front of the system and digital to analog conversion at its end. Analog computation and signal processing makes it simpler and faster [1]. Analog signal processing represents the signals as physical quantities like e.g. charge, current, voltage or frequency. These signals are continuous in value and continuous in time. Analog signal processing is most effective when precision is not the major criteria and when massive parallel collective processing of large number of signals that are continuous in time and amplitude is required [2]. Multiplication and division of analog signals are difficult operations in analog signal processing.

One of the fundamental building blocks in analog circuit design is the analog multiplier. Multipliers are particularly important in communication and signal processing circuit where they are commonly used for modulation, mixing, phase detection, adaptive filtering, function generators, frequency doubling, neural network and fuzzy logic applications. Voltage gain amplifier, signal squarer, RMS signal estimator and weight-input multiplication in neural networks are some application in signal processing. Phase detector is an essential element in phase locked loops. PLLs are widely used in frequency synthesizer, demodulators, clock generation circuits, clock recovery circuits and spread spectrum PLLs. Analog multipliers as a part of automatic gain control circuits used in AM radio receivers and radar system.

Most fundamental architectures were originally developed in bipolar technology, where the signal distortion can be kept low across the wide range of frequency [3]. As the digital design has improved, the ability to build analog and digital circuits with a single technology has become increasingly important. To meets mixed signal and low power needs, development of CMOS multiplier architecture has evolved. CMOS technology is better suited for digital circuits than bipolar due to its low processing cost and low power consumption.

Analog voltage multiplication can be performed either by using the square law characteristic of MOS transistors biased in saturation region [4] or by using Gilbert Cell [5-7]. The voltage multiplier presented in this work is based on second approach. Since the gain of this cell is a function of control voltage so the output is the multiplication of input voltage and control voltage and hence implements voltage multiplication.

Most multipliers can be classified as single-quadrant, two quadrant, or four quadrant multipliers, depending upon the possible polarities of the input signal. Single quadrant multipliers only allow positive input signals. Two quadrant multipliers allow one signal to swing both positive and negative. In four quadrant multipliers, both input signal can be positive or negative. The CMOS Gilbert cell multiplier architecture is a four quadrant multiplier. It is fully differential voltage multiplier. Multiplying voltage can offer better bandwidth performance, lower power operation.

The function of a multiplier is just as its name implies, it multiplies two signals together. Ideal multiplier satisfy the fundamental multiplication expression

Z= A0 XY ... [1.1]

Where output Z is the product of input signals X and Y and A0 is the multiplier constant. A key multiplier specification is linearity. The level of linearity that is allowed, depend on multiplier application. An example of this is in audio communication, where signal distortion is introduced by the multiplier is undesirable.

Low power and high performance hardware implementation of these circuits is a challenging task. In addition to these, the cost of circuits must be lowered as well. All these challenges of analog multiplier circuits are addressed in this thesis.

**1.2 Architecture of Phase locked loop**

Phased locked loop is a universal building block used in both analog and digital applications. The basic structure of Phase locked loop is shown in the Figure 1.1. Phase detector finds the phase difference between input and output signals of the controlled oscillator and locks the PLL on zero phase difference. Analog multiplier is most widely used as phase detector in PLLs with sine wave inputs and sine wave outputs [8]. Multiplier with two inputs having a phase difference of (inputs *Vx* sin*t* and Vy sin(*t* )) gives output *Vout*.

 [1.2]

The output of multiplier has DC term and double frequency term. Either by filtering the output or taking average of the output gives phase detection or phase error of the input signals.

 

**1.3 Architecture of Neural Network**

Analog VLSI implementation of artificial neural networks represents one of approaches to enhance the computational capabilities in real-time information processing. Character recognition, retrieval of data/image from fragments, pattern recognition and speech synthesis are some applications of artificial neural networks [9]. These neural networks consist of massive parallel layers of neurons interconnected with synapses as shown in Figure 1.2. The main function of the synapse cell is to achieve linear multiplication of input and a weight. These synaptic connections are implemented using Analog multipliers. Applications like multi layer feed forward networks require large number of interconnected neurons and synaptic connections (multipliers). Therefore careful design of multiplier is crucial in achieving compact silicon area, minimizing power consumption and improving input range.

 

 Figure 1.2 Architecture of Neural Network [10]

**1.4 Heterodyne Receiver Architectures**

A simplified block diagram of a conventional heterodyne receiver is shown in Figure 1.3. First, the antenna receives the RF incoming signal that is then fed into a band-select filter. The function of the band-select filter is to remove the out-of-band signals. Therefore, the RF signal at the output of the band-select filter contains only the amplifier (LNA), which is used to suppress the contribution of the noise from the succeeding stages along the receiving path. At the output of the LNA, the RF signal is passed through an image-reject filter. The function of the image-reject filter is to remove the image signal that has an offset of twice the intermediate frequency (IF) from the desired channel signal. Then the signal is down-converted to the intermediate frequency by a mixer that is followed by a channel-select filter. The channel-select filter performs channel selection at the IF, and the desired information is then retrieved by demodulation or detection.

 

 Figure 1.3 Simplified block diagram of heterodyne architecture [5]

**1.5 Research Goal**

Our research goal in this thesis is to design low voltage low power multiplier circuit. This design implements the multiplier circuit with MOS that operates in saturation region. In this thesis the special attention has been paid in improving the design characteristics like low power, input range and linearity.

Low power supply is directly related to the lower power consumption. Low supply voltage, low threshold voltage, low bias current is some methods by which the power consumption can be reduced.

One of the important characteristics of the multiplier is it’s linearity that is depend on the input range of the multiplier. The linearity of the multiplier is estimated in terms of either percentage of distortion in DC transfer characteristics or Total harmonic distortion (THD) of multiplier. A THD of less than 2% in the region of operation is sufficient for many analog VLSI signal and information processing applications [11].

**1.6 Thesis out Lines**

Chapter 1 shows the introduction about the multiplier circuit and the application of the multiplier.

Chapter 2 in this chapter, the basics about the Gilbert Cell and the multiplier circuit using Gilbert Cell is studied.

Chapter 3 presents background of multiplier circuits with the help of different multiplier architectures. The principle of operation of these multipliers is based on MOS operating region.

Chapter 4 in this chapter the proposed multiplier architecture design based on Gilbert Cell is analyzed.

Chapter 5 presents simulation results of four quadrant multiplier illustrating its characteristics and its applications.

Chapter 6 presents conclusions about my research work.

**Chapter 2 Background**

**2.1 Introduction**

Analog circuits are designed to implement some of mathematical operations. Addition, subtraction, integration and differentiation are some of the simple operations compared to multiplication and division of analog signals. If both the inputs of multiplier/divider can be either positive or negative, then it is called as four-quadrant multiplier/divider circuit. The inputs and outputs can be either voltage or current.

****

Fig.2.1Nonlinearity cancellations in four quadrant multiplier (a) using four single

 quadrant multipliers (b) using square devices

The ideal output of multiplier/divider is related to its inputs by

VOUT = k \*Vx \*Vy [2.1]

VOUT = k \*Vx /Vy  [2.2]

K is the multiplier/divider gain and Vx,Vy are voltage inputs of multiplier/divider circuits. In reality, the nonlinear characteristics of transistors results in offsets and nonlinearities. Non ideal output of multiplier can be written as [12]

Vout = k(Vx + Vosx)(Vy + Vosy)+ Vosout + Vnx + Vmy [2.3]

*Vosx, Vosy, Vosout* are the offset voltages and  *Vnx Vny* represent nonlinearities in the multiplier[13]. These nonlinearities in four-quadrant multipliers are cancelled by using four singlequadrant multipliers or four squared devices as shown in the Figure 2.1.

Barrie Gilbert designed one of successful four-quadrant multiplier in 1968 using the characteristics of bipolar transistor [14]. From Gilbert BJT multiplier to recently designed MOS transconductors based multipliers different topologies of multipliers are proposed. Multipliers are classified based on its MOS region of operation [15]. One type is analog multiplier circuit based on square-law characteristics of MOS transistor and the other type is based on linear characteristics of MOS transistor. Most of these transconductance multipliers are further categorized based on type of non linearity cancellation methods used in each multiplier. In transconductance multipliers, non linearities are cancelled either by single quadrant multipliers or squared devices as shown in Figure 2.1. In addition to these methods, voltage mode operation of multipliers is introduced.

Low voltage, low power, wide input range and linearity are the basic criteria in designing multipliers. CMOS multipliers are most widely used compared to BJT multipliers because CMOS multiplier gives low power and low voltage capabilities than BJT based multiplier. CMOS designs give low fabrication cost because of much widely used cmos digital technology.

**2.2 Gilbert Cell**

The Gilbert Cell was developed by B. Gilbert in 1968. Gilbert Cell can be made either by using BJT or by using MOS. To meets mixed signal and low power needs, development of CMOS multiplier architecture has evolved. CMOS technology is better suited for digital circuits than bipolar due to its low processing cost and low power consumption. The Gilbert Cell is made using differential amplifier. Gilbert Cell can be designed either by using single

differential amplifier, called single balanced Gilbert Cell or by using two differential amplifiers, called as double balanced Gilbert Cell.

Differential amplifier has two important characteristics [7] –

1. The small signal gain of the circuit is the function of the tail current.

2. The two transistors in the differential pair provide a simple means of steering the current to one of the two dimensions.

By combining these two properties we can develop versatile building block. The multiplier circuit is the result of these two properties.

**2.2.1 Differential Amplifier Using MOS**

The differential pair or differential amplifier configuration is most widely used building block in analog integrated- circuit design. For instance input stage of every op amp and in the Gilbert Cell.

 

 Fig.2.2 Differential amplifier circuit

The fig. 2.2 shows a MOS differential pair [16]. Here Q1 and Q2 are two matched transistors, whose sources are joined together and biased by a common current source I, with identical drain resistances Rd s. Vg1 and Vg2 are two input voltages applied at the gates G1 and G2. Both transistors operathes in saturation region. The Vg1 amd Vg2 can be written as:

Vg1 = Vgs1+Vss  [2.4]

Vg2 = Vgs2+Vss  [2.5]

Let Vid be the differential i/p voltage,

Vid = Vg 1- Vg2 = Vgs1 – Vgs2  [2.6]

The drain current of a MOSFET is given by the relation

[2.7]

Hence the currents id1 and id2 can be written as follows

 [2.8]

 [2.9]

Taking square root on both side of equation 2.8 and 2.9 we get,

Where K’n=

 Vid = Vid [2.10]

Where Vid = VGS1 – VGS2  and K = w/L \*n \*k’

Squaring equation (2.10)

 Vid

 Vid

Where I= Id1 + Id2

 Vid

 V2id [2.11]

 (Since I= Id1 + Id2)

Squaring equation (2.11)

4- 4=- V2id + V2id

Or, [2.12]

But we have Vid is positive, hence Id1 Id2, so

, [2.13]

, [2.14]

The transfer characteristics of equation (2.13) and (2.14) and fig.2.3 are non-linear. This due to the term involving (Vid )2 .



 Fig. 2.3 Plot of current in MOS differential pair.

**2.2.2 Differential Amplifier Using BJT**

 ****

 Fig.2.4 Differential amplifier using BJT

Fig.2.4 shows the differential amplifier using BJT. Both the transistors will operate in active region and both transistors are identical. To evaluate the linear multiplication the differential amplifier as shown in fir.2.4 is evaluated first. The I-V relationship applied to each transistor may be written as:

 [2.15]

Where Ic is the collector current, Is is the saturation current, VT is the thermal voltage, and VBE base to emitter voltage. I1 is the current flowing through the transistor T1 and I2 is the current through transistor T2. The sum of these two currents can be given as

 [2.16]

From equation 2.15 and 2.16, the I1 and I2 can be given as

 [2.17]

 [2.18]

For the differential input VID = Vb1 – Vb2, the differential output current can be written as

Iout = I1 – I2 [2.19]

Putting the value from equation 2.17 and 2.18 in equation 2.19

 [2.18]

 Fig. 2.4 shows the transfer characteristic plot for the differential amplifier. In this plot, there is a small linear range around the middle of each characteristic that is typically used for linear amplification of small signals.



 Fig.2.4 Transfer characteristic of bipolar differential amplifier.

**2.2.3 Gilbert Cell Multiplier Using BJT**

Gilbert Cell multiplier using BJT is shown in the fig. 2.5. This multiplier circuit uses two emitter coupled differential pair amplifier. All the transistors operate in the active region. The DC transfer characteristic shows that the emitter coupled pair exhibit tangential hyperbolic nature. This type of characteristic of emitter coupled pair is used for the implementation of Gilbert Cell multiplier. The collector current of emitter coupled pairs Q3, Q4 and Q5, Q6 can be given as

 [2.20]

 [2.21]

 [2.22]

 [2.23]

 

 Fig.2.5 BJT Gilbert multiplier

The collector currents of bottom emitter-coupled pair Q1, Q2 are given as

 [2.24]

 [2.24]

The output differential current can be given as

 [2.26]

The differential output current is product of the hyperbolic tangent of the two input voltages.

 [2.27]

For small values of x (x<<1) tanh *x* *x* , therefore equation (2.27) reduces to

 [2.28]

Where VT is thermal voltage with a value of 26mV at 300o K .

Multiplication of input signals is obtained by keeping the magnitude of input voltages ( *V1* and *V 2*) small relative to  *Vt* (Thermal voltage). This multiplier limits the input signal range to few tens of mill volts.



 Fig.2.6 Gilbert multiplier with predistortion circuit

In order to extend range of one of the input signals more than *Vt*, emitter degeneration is used in lower emitter-coupled pair. But this method cannot be used for cross coupled BJT pairs. As shown in Figure 2.6 an inverse hyperbolic tangent transfer characteristic circuit compensates nonlinearity in the BJT multiplier. This inverse hyperbolic tangent pre-distortion circuit before input voltages eliminates restriction on input voltage ranges. Input voltages are still limited by voltage current conversion capability of pre-distortion circuits.

**2.2.3 Gilbert Cell Multiplier Using MOS (Operating in Saturation Region)**

Fig.2.7 shows the basic Gilbert Cell multiplier circuit using MOS transistors. All the transistors M1, M2, M3 and M4 operate in saturation region. V is the supply voltage, I01 and I02. V1 and V4 is the input signal which multiplication have to be done. V2 and V3 is the source voltage.

When MOS transistor operates in saturation region then the current flowing through it can be given as

 [2.29]

Where K = , is mobility, is gate oxide capacitance, W is channel width and L is the channel length.is the gate to source voltage and is the threshold voltage.

The current flowing through the drain of transistor M1 - M4 is

 [2.30]

 [2.31]

 [2.32]

 [2.33]

The output current is the difference of I01 and I02

[2.34]

 [2.35]



 Fig.2.7 MOS multiplier circuit operating in saturation region

It is important to note that, the drain current of MOS transistor operating in saturation region is not controlled by drain voltage. Therefore drain voltages needn’t be equal for this multiplier configuration. Note that the above analysis neglects both channel length modulation and mobility reduction . Moreover multipliers operating in saturation region have much higher frequency response than multiplier operating in triode region [17]. Number of practical multiplier topologies is more in case of saturation region multipliers [18].

**2.3 Basics of Pspice**

The basic input file for PSpice is a text (ASCII) file that has the file type "CIR" [29].  In the beginning, this will be created by hand as the primary method of getting the circuit we want modeled into the PSpice program.  Later, when we use the schematic capture program, it will

create the \*.CIR file for us, along with several auxiliary file types.  Do not use a word processor to create these \*.CIR files unless you "Save as" text or as ASCII.  You can use Notepad to edit these files, but the best editor for this purpose is the one that is provided by MicroSim, called "TextEdit."

The output file always generated by PSpice is a text (ASCII) file that has the file type "OUT."  I.e., if you submit a data file to PSpice named "MYCIRKUT.CIR," it will create an output file named "MYCIRKUT.OUT."   This output file is created even if your run is unsuccessful due to input errors.   The cause for failure is reported in the \*.OUT file, so this is a good place to start looking when you need to debug your simulation model.  You examine the \*.OUT file with the TextEdit or Notepad programs.  When everything works properly, you will find the output results in this file if you are running a DC analysis.  If you are running a transient analysis or a frequency sweep analysis, there will be too much data for the \*.OUT file.  In these cases, we add a command to the \*.CIR file that tells PSpice to save the numerical data in a \*.DAT file.

The aforementioned \*.DAT file is by default a binary (i.e., non-ASCII) file that requires a MicroSim application called PROBE for you to see the data.  PROBE is installed with PSpice from the CD-ROM.  If you want, you can change the default storage format to ASCII.  This is not recommended because it requires more disk space to store the data in ASCII code.  Later, we will describe the procedure for invoking PROBE and creating the \*.DAT file.  A companion file to the \*.DAT file is the \*.PRB file which holds initializing information for the PROBE program.Another common method used by experienced PSpice users is the use of \*.INC (include) files.  These enable us to store frequently used subcircuits that have not yet been added to a library.  Then we access these \*.INC files with a single command line in the \*.CIR file.  very convenient.

Other files used with PSpice are \*.LIB files where the details of complex parts are saved; we may discuss this later, but it is unlikely that we will engage in LIB file alterations until you are taking advanced courses.

When we begin using the schematic capture program that is bundled with PSpice, we will encounter some additional file types.  These are the \*.SCH (the schematic data, itself), \*.ALS (alias files) and \*.NET (network connection files).

**2.3.1 Basic Rules About PSpice**

PSpice is not case sensitive.  This means that names such as *Vbus*, *VBUS*, *vbus* and even *vBuS* are equivalent in the program.

* All element names must be unique.  Therefore, you can't have two resistors that are both named "Rbias,"  for example.
* The first line in the data file is used as a title.  It is printed at the top of each page of output.  You should use this line to store your name, the assignment, the class and any other information appropriate for a title page.  PSpice will ignore this line as circuit data.  Do not place any actual circuit information in the first line.
* There must be a node designated "0." (Zero)  This is the reference node against which all voltages are calculated.
* Each node must have at least two elements attached to it.
* The last line in any data file must be ".END"  (a period followed by the word "end.")
* All lines that are not blank (except for the title line) must have a character in column 1, the leftmost position on the line.
	+ Use "\*" (an asterisk) in column 1 in order to create a comment line.
	+ Use "+" (plus sign) in column 1 in order to continue the previous line (for better readability of very long lines).
	+ Use "." (period) in column 1 followed by the rest of the "dot command" to pass special instructions to the program.
	+ Use the designated letter for a part in column 1 followed by the rest of the name for that part (no spaces in the part name).
* Use "whitespace" (spaces or tabs) to separate data fields on a line.
* Use ";" (semicolon) to terminate data on a line if you wish to add commentary information on that same line.

**Chapter 3 Related Works**

In this chapter the work related to multiplier circuit is studied. The multipliers can be made with the different technology. The multiplier circuit can be made using differential amplifier, using squaring circuit, using OTA circuit and can be made using Gilbert Cell.

**3.1 Multiplier Circuit Using Differential amplifier**

The multipliers are classified into two modes; voltage mode and current mode [19]. The analog circuit design using the current-mode approach has recently gained considerable attention. This stems from its inherent advantages of wide bandwidth, high slew rate, low power consumption, and simple circuitry [20, 21].

In this part a novel four-quadrant current-mode multiplier that mix between the voltage mode, in the form of two fully differential input voltages, and the current mode in terms of its fully differential output current. The most modern high performance analog integrated circuits incorporate fully differential signal paths. This is because fully differential circuit configurations have been widely used in high frequency analog signal applications like switched capacitor filters [22] and multi-standard wireless receivers [23]. Moreover, most modern systems employ both analog and digital parts on the same chip. A fully differential architecture of the analog part becomes more essential as it provides immunity to digital noise [24].

**3.1.1 Circuit Description**

The CMOS circuit of the fully differential four quadrant multiplier is shown in Fig.3.1.The proposed multiplier is consisting of four basic transistors *M*1 to *M*4 and two biasing circuits formed from transistors (*M*7 to *M*11) and (*M*12 to *M*16) and two biasing current sources formed from transistors *M*5 and *M*6. All transistors are assumed to be operating in the saturation. Transistors *M*1 to *M*4 are assumed to be matched transistors with transconductance parameter *K*, and their currents are linearized by using two biasing circuits



 Fig.3.1 CMOS Fully Differential Four Quadrant Multiplier [25 ]

formed from *M*7 to *M*16. First, expressions for the biasing voltages Va, Vb in terms of V4, V3, respectively, are obtained. Consider the biasing circuit formed from *M*7 to *M*11. The currents through *M*1 to *M*4 can be written as:

 [3.1]

 [3.2]

 [3.3]

 [3.4]

Where K = , is mobility, is gate oxide capacitance, W is channel width and L is the channel length and is the threshold voltage.

The differential voltage between the biasing voltages Va and Vb is given by:

 [3.5]

And the output differential current of the CMOS multiplier is given by:

=+) [3.6]

Assuming the two biasing current sources formed from M5 and M6 are equal. Then

 [3.7]

Therefore, the circuit operates as a four quadrant multiplier with two fully differential input voltages Vin1=(V1-V2) and Vin2=(V3-V4) and provide an output differential current Iod with a constant of proportionality K.

**3.2 Multiplier circuit using squaring circuit**

**3.2.1 Squaring Circuit**

Nowadays, the squarer circuit has been implemented by various techniques. One indirect method, by common the analog multiplier to obtain the squaring output. Although this is an easy way and can apply to proposed multiplier circuit, the large numbers of the transistors are required.

In this work low-voltage squarer circuit that uses the simple differential amplifier without any passive component. The circuit operates as source follower and all MOS transistors are in saturation region.

Considering the circuit in Fig. 1, while both transistor work in saturation region is expressed as,

 [3.8]

 [3.9]

For VGS > VTH, VDS > VGS - VTH

Where K =µ0 Cox W/L is the transconductance.

parameter of transistor, µO is the electron mobility, C0x is thegate oxide capacitance per unit area, W/L is the transistor aspect ratio, VGS is the gate-to-source voltage, VDS is the drain-to-source voltage and VTH is threshold voltage of the MOS transistor. If the transistors are homogeneous, as K1=K2=K and VTH1=VTH2=VTH, then the expression can be obtained as



 Fig.3.2 Squaring Circuit [26]

 [3.10]

Then the summation can be written as,

+ )2  [3.11]

Where Isum=II +I2 . Since Isum is also through M3, then it can be written as,

- VSS- )2

Or, = [3.12]

Substitution (3.11) into (3.12) get,

K()

Or, [3.13]

As small signal of Vin, assume that (Vin)0.Then, theoutput current can be expressed as the simple input signal squarer as follows,

 [3.14]

It can be derived from the small signal that

 or

 [3.15]

Equation (3.15) can be written as simple formula as

 [3.16]

Where a= and b=

**3.2.2 Multiplier circuit using squaring circuit**

The other approaches in CMOS technology are based on square-law characteristics of MOS transistor which are biased in saturation region [26] and that based on the current-voltage characteristics of MOS transistor in the non-saturation region [27]. However, all mention techniques require resistors to obtain the output signal in voltage form. The use of resistors may require external resistors, which occupy large chip area to implement in IC form and also cause of the multiplier frequency degradation.

This work presents a multiplier that use analog adder circuit with squaring circuits to get the quarter square algebraic identity.

**3.2.2.1 CIRCUIT DESCRIPTION**

The principle of the proposed multiplier is based on the quarter-square algebraic identity:

 [3.16]

In relation 9 VI and V2 are input voltages. Therefore, the circuit needs summing, and squarer circuits. The summation and subtraction between two input voltages are firstly performed, then, the results are squared. Finally, the multiplication is obtained by subtracting the square of the difference from the square of the sum.

(a) **SUBTRACTION CIRCUIT**

Fig.3.3 shows the subtraction circuit. All the transistor will operate in saturation region. V1 and V2 is the input signal. The current flowing through transistor M1 and M2 will be equal and current flowing through M3 and M4 will be equal, is given as:

= [3.17]

= [3.18]

****

 Fig.3.3 Subtraction Circuit

 [3.19]

 [3.18]

Vout1 is the output voltage at the drain of transistor M2 and Vout2 is the output voltage at the drain of M4. And can be given as:

 =- + [3.19]

 =+ + [3.20]

 =2(- ) [3.21]

 **(b) SUMATION CIRCUIT**

Fig.3.4 shows the subtraction circuit. All the transistor will operate in saturation region. V1 and V2 is the input signal. The current flowing through transistor M5 and M6 will be equal and current flowing through M7 and M8s will be equal, is given as:

= [3.22]

= [3.23]



 Fig.3.4 Summation circuit

 [3.24]

 [3.25]

Vout3 is the output voltage at the drain of transistor M6 and Vout4 is the output voltage at the drain of M8. And can be given as:

 =+ + [3.26]

 =- + [3.26]

- =2(+ ) [3.27]

 **(c) CALCULATION OF THE OUTPUT VOLTAGE**

The principle of the proposed multiplier is based on the quarter-square algebraic identity, that

Is:

 [3.28]

 Employ the squaring circuit of Fig. 3.2 and the summation-subtraction circuit of Fig 3.3 and Fig 3.4, the analog multiplier can be realized as shown in Fig 3.5. The sum and difference outputs from these stages are applied to the squarer circuits formed by M9, M10, M13 for summing and Mll, M12, MI4 for difference, and the squarer outputs are through M13 and M14 [3]. The subtraction between squarer summing and squarer difference gives the result of multiplier in voltage mode .

 [3.29]

 [3.30]

Where and



 Fig.3.5 Multiplier using squaring circuit [28]

**3.3 Multiplier Circuit Using Gilbert Cell**

The majority of popular CMOS mixer topologies are based on the traditional bipolar doubly balanced cross-coupled differential modulator stage introduced by Gilbert [29]. The core part of a CMOS Gilbert cell mixer resembles the Gilbert analog multiplier. All transistors are designed to operate in the saturation region. This type of mixer operates on a switched current principle. The output of the circuit depends on the transconductance of the cross couple pair and the bias current. Figure 3.5 shows the basic diagram of a CMOS Gilbert Cell multiplier. The small input signal is denoted by *Vx* and *Vy* respectively. The differential output current with respect to both Vx and Vy input is derived:

****

 Fig.3.6 Gilbert Cell Multiplier

 , [3.31]

 Where, Kx =µn Cox (W/L)1-4 , Ky =µn Cox (W/L)5-6

For a small input *Vx*, the gain is directly affected by the loading and the aspect ratio of all transistors. The differential output current is proportional to the amplitude of Vxand *Vy*.

The advantages of Gilbert Cell multiplier are high gain and low port-to-port feedthrough [7]. However, this type of multiplier requires staking of at least three transistors. This stacked-up structure poses a drawback for low voltage operation of the mixer.

**Chapter 4 Low Voltage Low Power Gilbert Cell Based Multiplier**

**4.1 Introduction**

In this work the multiplier using Gilbert Cell is presented. This multiplier can be used as a mixer, in modulation and in the neural networks. In this circuit the diode connected MOS resistance has been used rather simple resistance. The MOS resistance provides better frequency rather than simple resistance. Another advantage of the MOS resistance is they can be implemented on the integrated circuit in less area.

Analog voltage multiplication can be performed either by using the square law characteristic of MOS transistors biased in saturation region [4] or by using Gilbert Cell [5]. The property of the Gilbert cell is that the gain of the differential amplifier can be controlled by the tail current. Fig.3.1 shows the architecture of the proposed multiplier.

The voltage multiplier presented in this work is based on second approach. Since the gain of this cell is a function of control voltage so the output is the multiplication of input voltage and control voltage, and hence implements voltage multiplication.

Two kinds of multiplier is designed in this work. One multiplier circuit is designed using NMOS transistors and other by using CMOS. The characteristics of both kinds of multiplier are different in the way of frequency and power dissipation.

**4.2 Multiplier using CMOS**

Fig. 3.1 shows Gilbert Cell based multiplier using CMOS transistors. All the transistors operate in the saturation region. In this circuit, transistor MP1, MP2 and MP3 act as a current mirror. The current mirror is used to provide the active load. Transistor MP4 is a diode connect MOSFET act as a resistance. Transistor M1, M2, M3, M4, M5 and M6 form the Gilbert Cell architecture. M7 and M8 are the bias transistors, used to provide the constant current.



 Fig.4.1 Multiplier Circuit Using CMOS

**4.3 Multiplier using NMOS Transistor**

Fig. 3.2 shows Gilbert Cell based multiplier using NMOS transistors. All the transistors operates in the saturation region. In this circuit, transistor MN1, MN2 and MN3 and transistor MN4 is a diode connect MOSFET act as a resistance. Transistor M1, M2, M3, M4, M5 and M6 form the Gilbert Cell architecture. M7 and M8 are the bias transistors, used to provide the constant current.

Simulation results show that the frequency response of NMOS multiplier circuit is better than that of multiplier circuit using CMOS but the power dissipation of CMOS multiplier circuit is less than NMOS multiplier circuit.



 Fig.4.2 Multiplier Circuit using NMOS

**4.3 Analysis**

DC analysis of the both kind of multiplier is same. Since all the transistor operates in saturation region so the condition to keep the transistor in saturation is that:

 VDS ≥ VGS – VTH [4.1]

where VGS is gate to source voltage, VDS is drain to source voltage and VTH is threshold voltage. Current through the transistor in saturation is given by:

(VGS – VTH)2 [4.2]

where K = , is mobility, is gate oxide capacitance, W is channel width and L is the channel length.

From the fig.1 the following equation for transistor M5 & M6 can be written as

 VC1- VC2 = VGS5 - VGS6 [4.3]

When the transistor operates in saturation then from equation (1):

 (VGS – VTH)2 = = [4.4]

For transistor M1 & M2, M5 & M6:

 VGS1 =

 VGS2 = [4.6]

 VGS5 = [4.7]

 VGS6 =

 VC1- VC2 = [4.9]

 (VC1- VC2)2 =

Putting the value of VGS5 & VGS6 in eq. (4.3) and squaring. It gives

 = (VC1- VC2)2

Again squaring on both sides...

 = ( (VC1- VC2)2 )2

= (VC1- VC2)\* [4.10]

Similarly for transistor M1 & M2, M3 & M4:

 = (V1- V2) [4.11]

= (V1- V2) [4.12]

 Since the signal is applied in the complementary form, so:

 =-= & =

The input signal being very and can be approximated to zero.

Thus eq. (4.11) & (4.12) reduce to:

= V1 [4.13]

= V1 [4.14]

**4.3.1 The output voltage (Vout)**

Output is taken at the drain of transistor M1 &M3.So output VOUT can be written as:

 VOUT = RD ( +) [4.15]

 VOUT = RD V1 () [4.16]

Where RD is the resistance provided by the active load.

From eq. (4.9) putting the valve of () in eq. (14)

 VOUT = RD V1 (VC1- VC2) [4.16]

 since so from eq. (15)

 VOUT = C \*V1 \*VC [4.17]

Where C=2 RD K

This clearly shows that VOUT is multiplication of input voltage and control voltage.

**3.4 Performance Table**

**3.4.1 Performance table of NMOS multiplier**

|  |  |
| --- | --- |
| **Number of NMOS** | **12** |
| **Supply** | **±1.5** |
| **W/L** | **.18/.18** |
| **Input range** | **±10mV** |
| **Output range** | **60uV** |
| **-3dB freq response** | **39 GHz** |
| **Power Dissipation** | **.387mW** |

 **Fig.4.3 Performance table of NOS multiplier**

**4.4.2 Performance table of CMOS multiplier**

|  |  |
| --- | --- |
| **Number of NMOS** | **8** |
| **Number of PMOS** | **4** |
| **Supply** | **±1.5** |
| **(W/L)n** | **.18/.18** |
| **(W/L)p** | **25/.18** |
| **Input range** | **±10mV** |
| **Output range** | **0.25mV** |
| **-3dB freq response** | **26.73 GHz** |
| **Power Dissipation** | **.0755mW** |

 **Fig.4.4 Performance table of CMOS multiplier**

**Chapter 5 Simulation And Results**

The simulation of this Gilbert Cell based multiplier circuit is done on orcad pspice A/D using 180nm CMOS process parameter provided by Mosis. Supply voltage used was ±1.5V. In this thesis two multiplier is simulated. One is using all NMOS and another is using NMOS and PMOS. Number of transistors used in both circuits is same but both the circuits have different characteristics like power dissipation, linearity and cut off frequency.

**5.1 Simulation result of multiplier circuits**

**5.1.1 DC Response**

Fig.5(a) and fig.5(b) shows the input signal of peak voltage 10mV.V1 and Vc is the input signals. Here the frequency of the modulating (V1) and the career (Vc) signals are 500KHz and 0.1GHz sinusoidal with peak amplitude of 10mV.

Fig. 5.1 shows the DC response of the CMOS multiplier circuit. For ±10mV input signal voltage, the output voltage swing is ±250uV. Fig. 5.2 shows the DC response of the NMOS multiplier circuit. For ±10mV input signal voltage, the output voltage swing is ±60uV.

****

 Fig. 5(a) input modulating signal



 Fig. 5(b) input career signal

****

 **Fig.5.1 DC response of CMOS**



 **Fig.5.2 DC response of NMOS**

**5.1.2 AC Response**

Fig.5.3 shows the AC response of the multiplier circuit. The -3dB bandwidth of this CMOS multiplier is 26.73GHz. Fig.5.4 shows the AC response of the multiplier circuit. The -3dB bandwidth of this multiplier is 38.99GHz.

****

 Fig.5.3 AC response CMOS multiplier

****

Fig.5.4 AC response of all NMOS multiplier

**5.1.3 Transient Response**

 Fig.3.5 and fig.3.6 shows the transient response of both for the input as shown in fig. And fig. multiplier circuit as an amplitude modulator. Here the frequency of the modulating (V1) and the career (Vc) signals are 500KHz and 0.1GHz sinusoidal with peak amplitude of 10mV.



 Fig.5.5 Transient response as a amplitude modulator of CMOS.



 Fig.5.6 Transient response as a amplitude modulator of all NMOS.

**5.2 Comparison Table**

|  |  |  |
| --- | --- | --- |
| **Parameter** | **CMOS** | **NMOS** |
| **Input supply** | **±1.5V** | **±1.5V** |
| **Signal voltage** | **±10mV** | **±10mV** |
| **Output range** | **0.25mV** | **60uV** |
| **Power dissipation** | **.0755mW** | **.387mW** |
| **-3dB frequency** | **26.73 GHz** | **39GHz** |

**Fig. 5.7 comparison table of NMOS and CMOS multiplier circuit**

**Chapter 5 Conclusion**

In this work two kinds of multiplier, based on Gilbert Cell, have been designed and simulated. This work is done to design two four quadrant multiplier circuit using NMOS and CMOS. The power supply of both the circuit is same that is ±1.5v for ±10mv input signal range. This designed circuit is simulated on PSPICE simulator on 180nm technology using level 7 provided by Mosis.

 The simulation result shows that the CMOS multiplier circuit has better power dissipation but lower -3dB frequency as compared to NMOS multiplier while NMOS multiplier circuit has better -3dB frequency but poor power dissipation as compared to CMOS multiplier of both the multipliers are 26.73GHz and 38.99 GHz. Both multipliers have the better linearity for ±10mv input signal range.

**References**

[1] Bogdan M. Wilamowski, “VLSI Analog Multiplier/divider Circuit,” *International Symposium on Industrial Electronics,* July, 7-10, 1998, Pretoria, South Africa,pp. 493-496.

[2] Eric A. Vittoz, “Analog VLSI signal processing: Why, where and how?”, *International Journal on Analog Integrated Circuits and Signal Processing,* Vol. 6, No. 1, July 1994, pp. 27-44.

[3]B. Gilbert, “A Precise Four-Quadrant Multiplier with Subnanosecond Response”, IEEE Journal of Solid-State Circuit, Vol. SC-3 No.4 pp.365, Dec 1968

[4] A Low Voltage High Frequency Four Quadrant Analog Multiplier, 2010 International Conference on Mechanical and Electrical Technology (ICMET 2010).

[5] Design of Gilbert Cell mixer in .18um CMOS technology and IF filter For FM receiver, IEEE 2009.

[6] A MOS Four-Quadrant Analog Multiplier Based on the Multitail Technique Using Quadritail Cell as a Multiplier Core, IEEE transactions on circuits and systems-i: fundamental theory and applications, vol. 42, no. 8, august 1995.

[7] Behzad Razavi. *RF Microelectronics*, Prentice Hall, Inc. (1998).

[8] Thomas H. Lee, *The Design of CMOS Radio Frequency Integrated Circuits,* Cambridge University Press, United Kingdom, 1998.

[9] M. Ismail, T. Fiez, Analog VLSI Signal and Information Processing, McGraw-Hill, Inc., United States, 1994.

[10] Dominique Coue and George Wilson, “A four quadrant sub-threshold mode multiplier for analog neural-network applications”, *IEEE Transactions on Neural* *Networks,* Vol. 7, No. 5, September 1996, pp. 1212-1219.

[11] K. T. Lau, S.T. Lee, V.K.S. Ong, “Four-quadrant analog CMOS multiplier cell for VLSI signal and information processing”, *IEE Proceedings on Circuits, Devices and* *Systems,* Vol. 145, No. 2, April, 1998, pp. 132-134.

[12] S. Soclof, *Applications of Analog Integrated Circuits,* Prentice Hall, 1985.

[13] R. Jacob Baker, Harry W. Li and David E. Boyce, *CMOS Circuit Design, Layout and Simulation,* Prentice Hall, 1998.

[14] B. Gilbert, “A precise four-quadrant multiplier with sub nanosecond response,” *IEEE Journal of Solid State Circuits,* Vol. 3, No. 4, December 1968, pp. 365-373.

[15] Gunhee Han and Edgar Sanchez Sinencio, “CMOS transconductance amplifiers: A Tutorial”, *IEEE Transactions on Circuits and Systems-II,* Vol. 45, No. 12, December 1998, pp. 1550-1563.

[16] Ref: Micro Electronic Circuits; Sedra/Smith. 5th Edition

[17] S. Szczepanski and S. Koziel, “1.2V Low-power four-quadrant CMOS transconductance multiplier operating in saturation region”, *International* *Symposium on Circuits and Systems,* Vol. 1, 2004, pp. 1016-1019.

[18] Gunhee Han and Edgar Sanchez Sinencio, “CMOS transconductance amplifiers: A Tutorial”, *IEEE Transactions on Circuits and Systems-II,* Vol. 45, No. 12, December 1998, pp. 1550-1563.

[19] M. A. Hashiesh, S. A. Mahmoud, and A. M. Soliman, “New Four- Quadrant CMOS Current Mode and Voltage Mode Multiplier,” Analog Integrated Circuits and Signal Processing, Vol.45, pp. 295- 307, Dec.2005.

[20] Toumazou, C., Lidgey, J., and Haigh, D. Analogue IC Design: The Current Mode Approach. Peregrinus, London, U.K., 1990.

[21] Alzaher, H.A., Elwan, H., and Ismail, M. “ACMOSfully balanced second-generation current conveyor.” IEEE Trans. Circuit Syst. II,vol. 50, pp. 278–287, 2003.

[22] T. Choi, R. Kaneshiro, R. Bodersen, P. Gray, W. Jett, and M. Wilcox, “High-frequency CMOS switched-capacitor filters

[23] J. Rudell, J.-J. Ou, T. Cho, G. Chien, F. Brianti, J. Weldon, and P. Gray, “A 1.9 GHz wide-band If double conversion CMOS receiver for cordless telephone applications,” *IEEE J. Solid-State Circuits*, vol. 32, pp. 2071–2088, 1997.

[24] S. A. Mahmoud**,**” Fully Differential CMOS CCII based on differential difference transconductor” Analog Integrated Circuits and Signal Processing, Vol. 50, pp. 195-203, March 2007.

[25] Soliman A. Mahmoud “Low Voltage Low Power Wide Range Fully Differential CMOS Four-Quadrant Analog Multiplier” [Circuits and Systems, 2009. MWSCAS '09. 52nd IEEE International Midwest Symposium on](http://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=5230480) Aug. 2009 **pp.** 130 - 133

[26] Risanuri Hidayat, Kobchai Dejhan, Phichet Moungnoul, Yoshikazu Miyanaga ” Simple CMOS Squarer Circuit” 2008 International Symposium on Communications and Information Technologies (ISCIT 2008)

[27] Risanuri hidayat,kobchai dejhan,phichetmoungnoul,yashikazu miyanaga "ota based high frequency CMOS and squaring circuit" King Mongkut's Institute of Technology Ladkrabang, Bangkok 10520, Thailand.

[28] Alireza Mallahzadeh , Milad Kaboli , Behzad Ghanavati” A Low Voltage High Frequency Four Quadrant Analoge Multiplier” 201O International Conference on Mechanical and Electrical Technology (ICMET 2010)

[29] G. Kathiresan and C. Toumazou, “A Low Voltage Bulk Driven Downconversion Mixer Core”, *Proceedings of IEEE International Symposium on Circuits and* *Systems*, vol 2, pp.598-601, 1999

[30] *SPICE for Circuits and Electronics Using PSpice*; Rashid, Muhammad H.; © 1990 by Prentice-Hall, Inc.; ISBN: 0-13-834672; (supports electronics well)