Chapter 1

Introduction

In the modern era of VLSI, with the shrinking sizes of electronic circuits, the voltage supply and consequently the power consumption is also reduced in the same ratio to maintain the appropriate power dissipation per area. However, designing of electronic circuits with low supply voltages and power consumption become the limiting factor in the design, particularly when extreme speed or accurate signal processing are required. The simultaneous fulfilment of seemingly contradictory requirement has led to the evolution of various trends in the analog signal processing applications. In the last two decades, the evolution of analog signal processing applications has followed the trends of so-called current mode [1], where signals, representing the information, are in the form of electric currents.

The current mode approach for analog signal processing circuits and systems has emerged as an alternate method besides the traditional voltage mode circuits [2] due to their potential performance features like wide bandwidth, less circuit complexity, wide dynamic range, low power consumption and high operating speed. The current mode active elements are appropriate to operate with signals in current or voltage or mixed mode, and are gaining acceptance as building blocks in high performance circuit designs which is clear from the availability of wide variety of current mode active elements such as operational transconductance amplifier (OTA) [3], current feedback operational amplifier (CFOA) [4], current conveyors (CC) [5]-[6], current controlled conveyor [7], differential voltage current conveyor (DVCC) [8]-[12] etc.

Recently, some analog building blocks in open literature are obtained by cascading of various current conveyor blocks with transconductance amplifier (TA) block in monolithic chip for compact implementation of signal processing circuits and systems. Current conveyor transconductance amplifier (CCTA) [13]-[14], current controlled current conveyor (CCCCTA) [15]-[16], differential voltage current conveyor transconductance amplifier (DVCCTA) [17]-[19], differential voltage current controlled conveyor transconductance amplifier (DVCCCTA) [20] are example of such building blocks.

In this thesis the implementation of higher order filter using DVCCCTA as an active building block has been presented. The use of DVCCCTA in filter design gives the resistorless implementation due to internal parasitic resistance and transconductance of DVCCCTA. The DVCCCTA based filters also possess electronic tunability because the value of parasitic resistance and transconductance depends on bias current.

For implementing higher order filter, there are mainly three approach- operational simulation or leapfrog approach, topological simulation or element replacement and wave active approach. In leapfrog approach [21] the voltage and current relationships of an LC ladder are written that are used for the construction of the corresponding Signal Flow Graph (SFG). The number of the required equations for deriving the corresponding SFG increases according to the order of the filter. The resulted SFG is realized by employing lossy and loss less integrator configurations [22]. In practice, the realization of lossless integrators is not easy due to the imperfections imposed by the used active and passive elements.

In the topological simulation approach, the inductors of the passive prototype filters are replaced by appropriate configured active elements. The drawback of this configuration is that a floating capacitor is generally required and this degrades the performance of the derived filter topology in high frequency application.

An attractive approach for designing high-order filters is the wave method [23]-[24]. According to this method, the corresponding LC ladder filter is split into two-port subnetworks which are fully described using the wave variables, defined as incident and reflected waves. By choosing an inductor in a series branch as the elementary building block, its wave equivalent includes an appropriately configured lossy integrator. The wave equivalents of the other passive elements are derived by interchanging the terminals of the appropriate wave signals and signal inversion. Then each element of the passive prototype filter is substituted by its wave equivalent. The advantages of this approach are - the derived filter structures are modular and it use only lossy integrator.

Several implementations are available in the literature for wave active filters that use variety of active building blocks [25]-[27]. In this thesis the implementation of DVCCCTA based wave active filter is presented.

This thesis is organised in 6 chapters.

Chapter-2 explains the operation of the DVCCCTA. In chapter-3, the theory of wave active filter is explained. Chapter-4 presents the DVCCCTA based wave equivalent of an inductor

in a series branch, which is chosen to be the elementary building block. The wave equivalents of the other reactive elements are also presented in this chapter. To demonstrate the wave active approach the 4^{th} order low pass filter is also realized. Chapter 5 shows the operational simulation or leapfrog approach of higher order filter. The thesis is concluded in Chapter 6.

All the results have been verified through SPICE simulation using 0.25 μm TSMC CMOS technology parameters.

Chapter 2

DVCCCTA: Current Mode Building Block

The Differential Voltage Current Controlled Conveyor Transconductance Amplifier (DVCCCTA) is an attractive active building block for analog signal processing. The applications based on DVCCCTA are resistor less as it has one parasitic resistance and transconductance element each which can be tuned electronically by adjusting the input bias current of DVCCCTA. This chapter discusses the DVCCCTA that consists of Differential Voltage Current Conveyor (DVCC), Translinear loop and Transconductance amplifier (TA).

2.1 Differential Voltage Current Conveyor

The differential voltage current conveyor (DVCC) is an extension of the second-generation current conveyor (CCII). The second-generation current conveyor (CCII) is a versatile analog building block that can be used to implement various high frequency analog signal applications, like filters and current-mode oscillators. But for the application which require two high input impedance terminals (differential or floating inputs) like impedance converters and current-mode instrumentation amplifiers, a single CCII block is not sufficient. In addition, most of these applications employ floating elements in order to minimize the number of used CCII blocks. For this reason and in order to provide two high input impedance terminals, the differential voltage current conveyor (DVCC) is used.

The CCII has a disadvantage that only one of the input terminals has high input impedance (the Y terminal). This disadvantage becomes evident when the CCII is required to handle differential signals, as in the case of an instrumentation amplifier.

The block diagram of the DVCC is shown in Fig. 2.1.

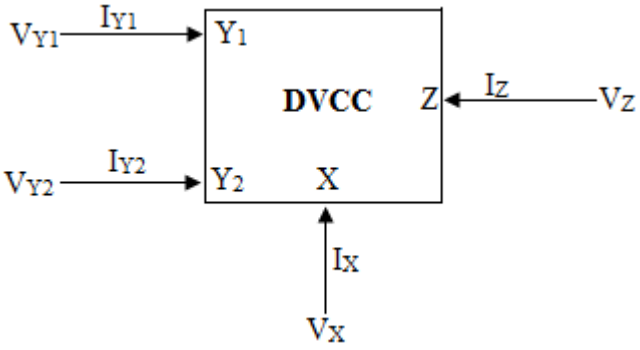


Fig. 2.1 Block diagram of DVCC

And its terminal relations are given by following matrix

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_X \\ V_Z \end{bmatrix}$$

From above matrix we find following relation

$$V_X = V_{Y1} - V_{Y2}, \quad I_{Y1} = I_{Y2} = 0, \quad I_Z = I_X \tag{2.1}$$

The voltage at X terminal is equal to the voltage difference of terminals Y_1 and Y_2; a current injected at the X terminal is being replicated to the Z terminal. An ideal DVCC exhibits zero input resistance at terminal X, and infinite resistance at both Y terminals as well as the Z terminal. Since the DVCC has two high input impedance terminals, it is suitable for handling differential input signals. The CMOS implementation of DVCC is shown in Fig. 2.2.

The differential voltage conveying action of the circuit is based on the differential pairs M_1-M_2 and M_3-M_4. The current mirror formed by transistors M_5 and M_6 forces the sum of the drain currents of M_1 and M_4 to be equal to the sum of the drain currents of M_2 and M_3.

Hence

$$I_{D1} + I_{D4} = I_{D2} + I_{D3} \tag{2.2}$$

$$\Rightarrow I_{D1} - I_{D2} = I_{D3} - I_{D4}$$

$$\textit{hence} \quad V_{G1} - V_{G2} = V_{G3} - V_{G4}$$

$$\Rightarrow V_{Y2} - 0 = V_{Y1} - V_X$$

$$\Rightarrow V_X = V_{Y1} - V_{Y2} \tag{2.3}$$

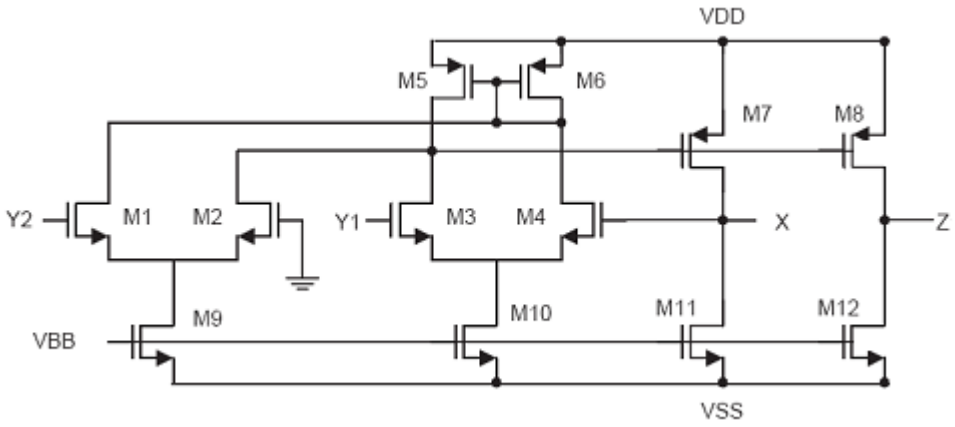


Fig. 2.2 CMOS Implementation of DVCC

Transistors M_7 and M_{11} provide the necessary feedback action to make the voltage V_X independent of the current drawn from the terminal X. The current through terminal X is conveyed to the Z terminal by the current mirrors consisting of transistors M_7-M_8 and M_{11}-M_{12}. The operation of this circuit is insensitive to the threshold voltage variation caused by the body effect. All the PMOS transistors have sources which are connected to the positive supply rail, while all NMOS transistors, except M_1, M_2, M_3 and M_4, have sources connected to the negative supply rail. This causes no variation in the threshold voltage because the source to body voltage is maintained equal to zero at all times. Although the sources of transistors M_1 and M_2 are not connected to the body, their operation is still unaffected by the body effect because they form a differential pair, and, hence, have the same source voltage. This causes equal variation in the threshold voltage of M_1 and M_2, and, hence, the two threshold voltages cancel out. The same is true for the differential pair transistors M_3 and M_4.

2.2 Translinear loop

This block is used to provide parasitic resistance in DVCCCTA and is shown in Fig. 2.3. The parasitic resistance is controlled by bias current.

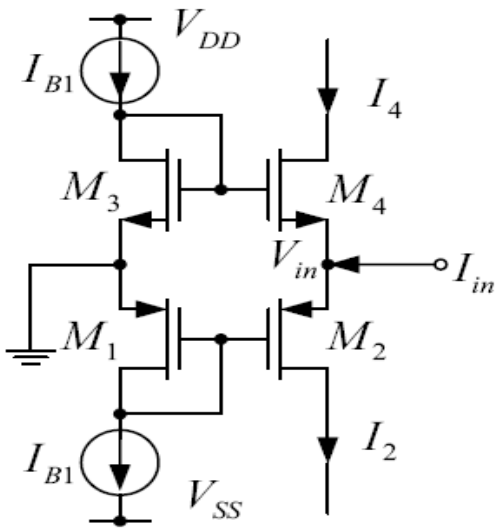


Fig. 2.3 Class AB Translinear loop

Calculation of parasitic resistance:

Apply KCL at input node

$$I_{in} = I_2 - I_4 \tag{2.4}$$

For small signal model the diode connected transistors M_1 and M_3 will be replaced by resistance of $1/g_{m1}$ and $1/g_{m3}$ where g_{mi} (i=1,3) is transconductance of i^{th} transistor. The currents I_2 and I_4 may be expressed as

$$I_2 = g_{m2} V_{SG2}, \qquad I_4 = g_{m4} V_{GS4} \tag{2.5}$$

$$\text{But} \quad V_{SG2} = V_{S2} - V_{G2} \quad \Rightarrow \quad V_{in} - \left(- \frac{I_{B1}}{g_{m1}} \right)$$

$$\text{And} \quad V_{GS4} = V_{G4} - V_{S4} \quad \Rightarrow \quad \frac{I_{B1}}{g_{m3}} - V_{in} \tag{2.6}$$

On putting the value of V_{SG2} and V_{GS4} in equation (2.5), we have

$$I_2 = g_{m2} \left(V_{in} + \frac{I_{B1}}{g_{m1}} \right) \quad \text{And} \quad I_4 = g_{m4} \left(\frac{I_{B1}}{g_{m3}} - V_{in} \right) \tag{2.7}$$

Now put I_2 and I_4 in equation (2.4),

$$I_{in} = g_{m2}\left(V_{in} + \frac{I_{B1}}{g_{m1}}\right) - g_{m4}\left(\frac{I_{B1}}{g_{m3}} - V_{in}\right)$$

$$\Rightarrow I_{in} = V_{in}\left(g_{m2} + g_{m4}\right) + I_{B1}\left(\frac{g_{m2}}{g_{m1}} - \frac{g_{m4}}{g_{m3}}\right)$$

$$\Rightarrow 1 = R_X\left(g_{m2} + g_{m4}\right) + \frac{I_{B1}}{I_{in}}\left(\frac{g_{m2}}{g_{m1}} - \frac{g_{m4}}{g_{m3}}\right) \qquad \text{Where } R_X = \frac{V_{in}}{I_{in}}$$

On rearranging

$$R_X = \frac{1}{g_{m2} + g_{m4}} - \frac{I_{B1}}{I_{in}\left(g_{m2} + g_{m4}\right)}\left(\frac{g_{m2}}{g_{m1}} - \frac{g_{m4}}{g_{m3}}\right) \tag{2.8}$$

If $g_{m1} = g_{m3}$ and $g_{m2} = g_{m4} = g_m$, then

$$R_X = \frac{1}{g_{m2} + g_{m4}} = \frac{1}{2g_m} = \frac{1}{\sqrt{8kI_{B1}}} \tag{2.9}$$

Where transistors are assumed to be in saturation region and

$$k = \mu_n C_{OX}\left(\frac{W}{L}\right)_4 = \mu_p C_{OX}\left(\frac{W}{L}\right)_2 \tag{2.10}$$

2.3 Transconductance Amplifier

The operational transconductance amplifier is a differential amplifier whose differential input voltage produces an output current. Thus, it is a voltage controlled current source (VCCS). The transconductance of the amplifier is proportional to the square root of bias current. This feature makes it useful for electronic control of amplifier gain. The block diagram and CMOS implementation of transconductance amplifier is shown in Fig. 2.4 and Fig. 2.5.

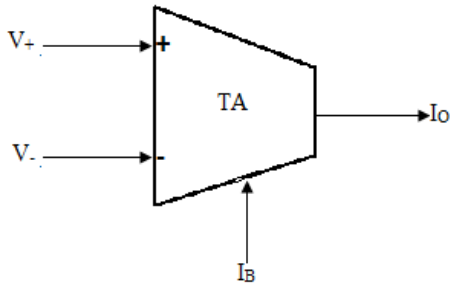


Fig. 2.4 Block diagram of Transconductance Amplifier

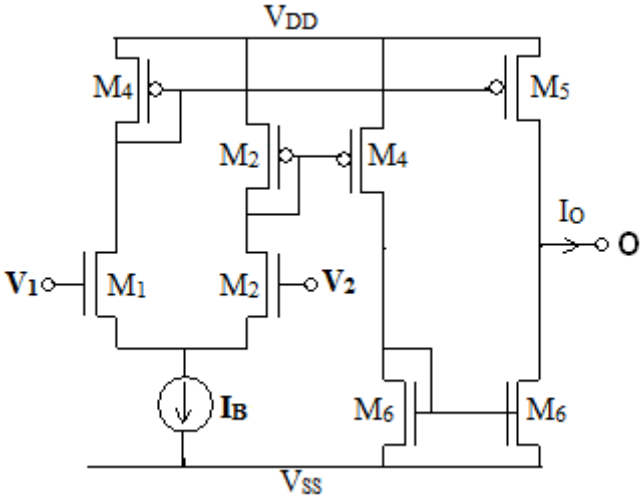


Fig. 2.5 CMOS Implementation of Transconductance Amplifier

The output current I_O may be given as

$$I_O = g_m (V_1 - V_2) \tag{2.11}$$

$$\text{Where} \quad g_m = \sqrt{\mu_n C_{Ox} \left(\frac{W}{L}\right)_{1,2} I_B} \tag{2.12}$$

2.4 DVCCCTA

Since DVCCCTA is consist of DVCC, translinear loop and Transconductance amplifier, so on combining the circuit diagram of Fig. 2.2, Fig. 2.3 and Fig. 2.5, the block diagram and CMOS implementation of DVCCCTA is shown in Fig. 2.6 and Fig. 2.7

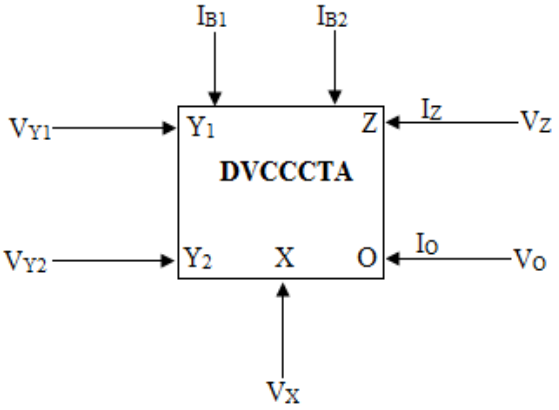


Fig. 2.6 Block diagram of DVCCCTA

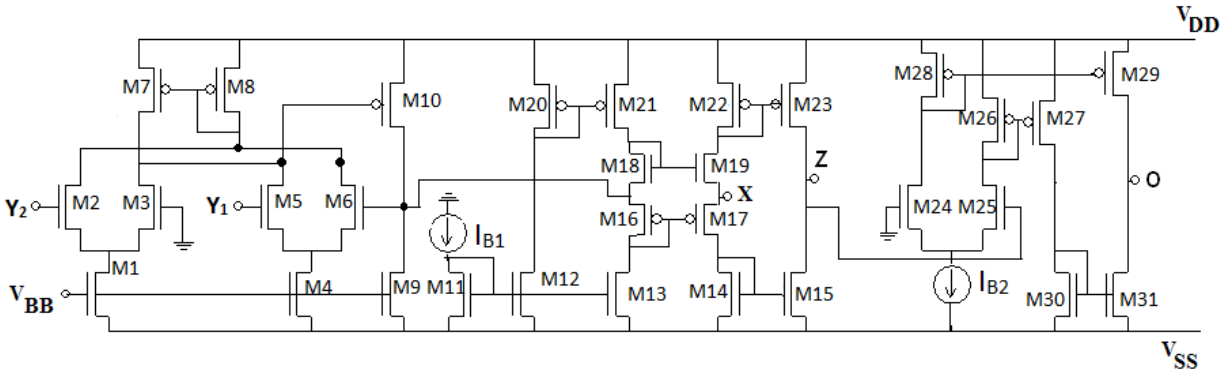


Fig. 2.7 CMOS Implementation of DVCCCTA

In the Fig. 2.7, the transistors from M_1 to M_{10} forms DVCC, the transistors from M_{11} to M_{23} form translinear loop, while transistors from M_{24} to M_{31} form transconductance amplifier. The port relationships of the DVCCCTA can be characterized by the following matrix

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_Z \\ I_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & R_x & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & -g_m & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_X \\ V_Z \\ V_O \end{bmatrix}$$

And in equation form

$$I_{Y1} = I_{Y2} = 0, \quad V_X = V_{Y1} - V_{Y2} + I_X R_X, \quad I_Z = I_X, \quad I_O = -g_m V_Z \tag{2.13}$$

Where R_x is the intrinsic resistance at X terminal and g_m is the transconductance from Z terminal to O terminal of the DVCCCTA. The values of R_x and g_m depend on bias currents I_{B1} and I_{B2} respectively, which may be expressed as

$$R_x = 1/\left(\sqrt{2\mu_n C_{ox} (W/L)_{18,19} I_{B1}} + \sqrt{2\mu_p C_{ox} (W/L)_{16,17} I_{B1}}\right) \tag{2.14}$$

And

$$g_m = \sqrt{2\mu_n C_{ox} (W/L)_{24,25} I_{B2}} \tag{2.15}$$

2.4.1 Simulation for the Verification of port relationship

The performance of the DVCCCTA has verified by performing SPICE simulations with supply voltages ±1.25V using 0.25μm TSMC CMOS technology. Simulations are carried out with I_{B1} = 25µA, I_{B2} = 200µA and transistor aspect ratios given in Appendix-A.

a) DC Analysis:

Fig. 2.8 shows the port relationship between X and Y port voltages. To verify $I_Z = I_X$, we take $V_{Y1} = V_{Y2}$ =0 and I_X=100µA. The Fig. 2.9 shows the graph for Z terminal output current versus X-terminal current. Fig.2.10 shows the plot for output current at O terminal Versus Z terminal voltage, for this we take the input setting as V_{Y1}=V_{Y2}=0 and V_Z=100mV.

b) AC Analysis:

The various simulation results are shown in from Fig. 2.11 to Fig. 2.15. The value of parasitic resistance at X terminal is 1454.3Ω (at the bias current of 25µA) from the graph shown in Fig. 2.14. And the value of transconductance g_m is 698.78µS (at the bias current I_{B2} of 200µA) from the graph shown in Fig. 2.15.

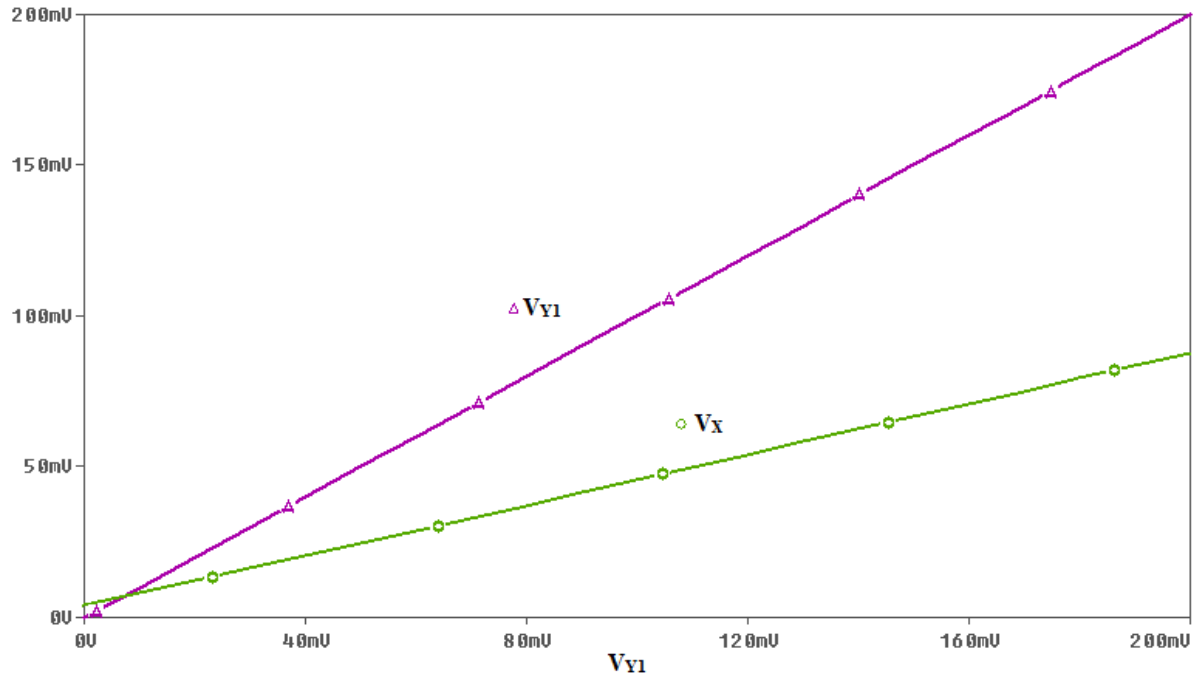


Fig. 2.8 Simulated port relationship $V_X = V_{Y1} - V_{Y2} + I_X R_X$ in DC analysis

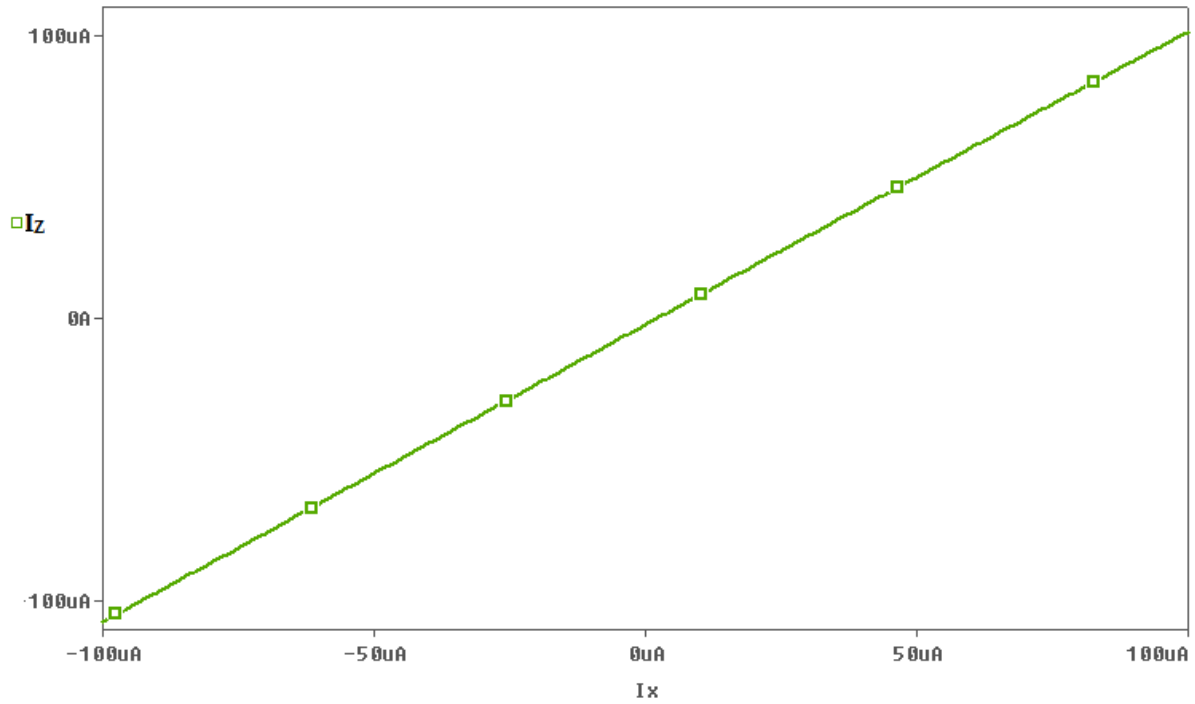


Fig. 2.9 Simulated port relationship $I_Z = I_X$ in DC analysis

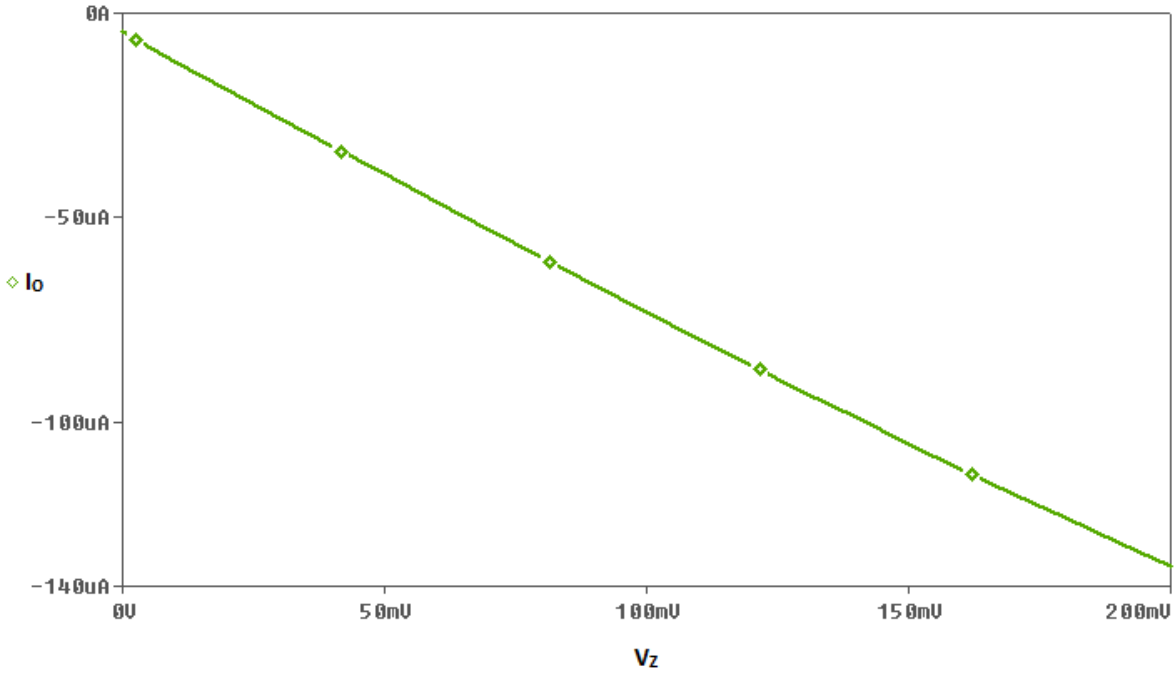


Fig. 2.10 Simulated port relationship $I_O = -g_m V_Z$ in DC analysis

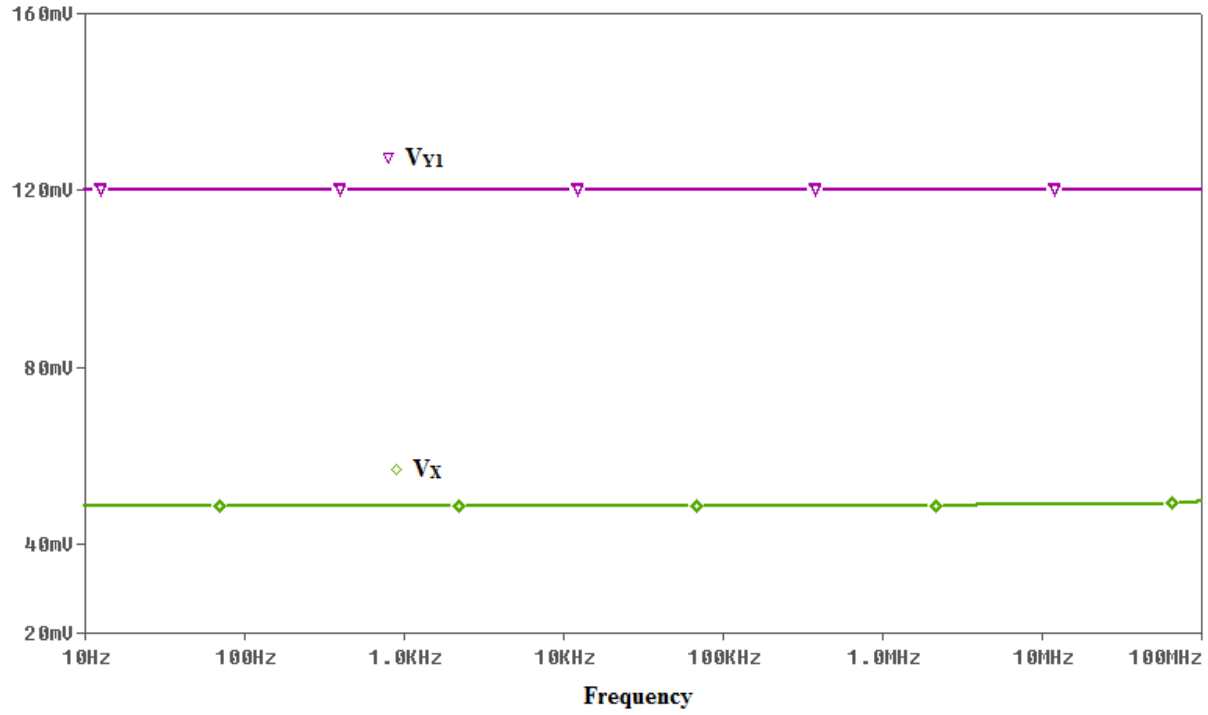


Fig. 2.11 Simulated port relationship $V_X = V_{Y1} - V_{Y2} + I_X R_X$ in AC analysis

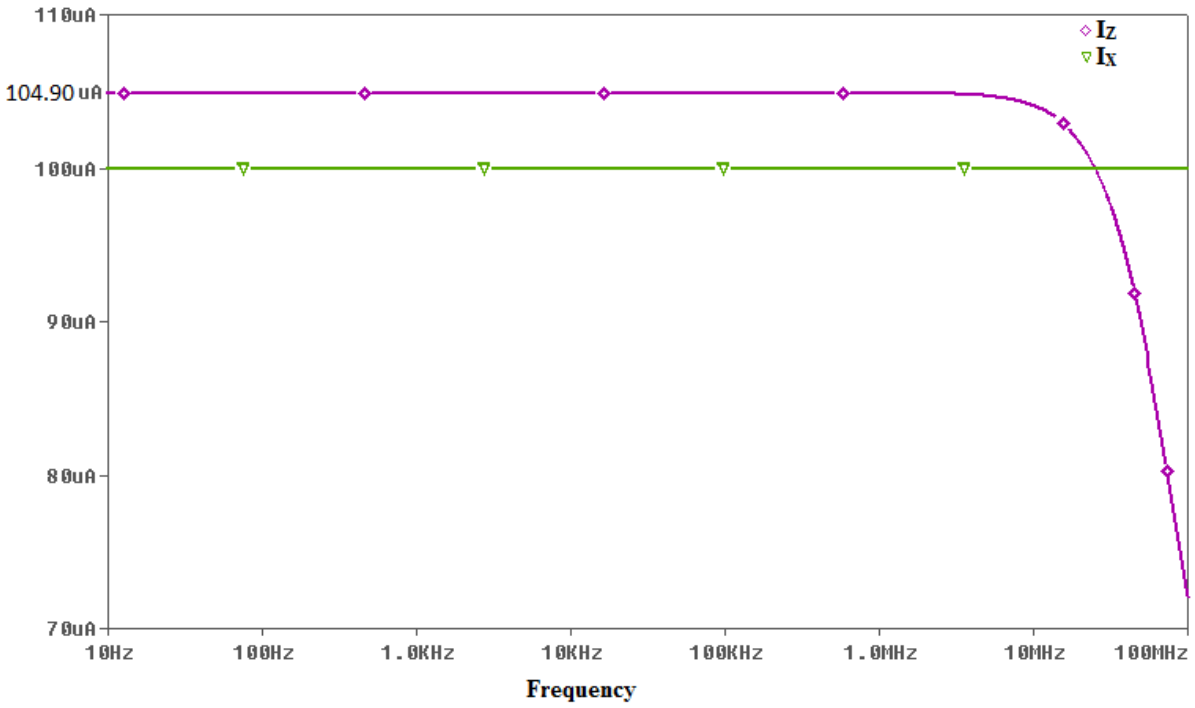


Fig. 2.12 Simulated port relationship $I_Z = I_X$ in AC analysis

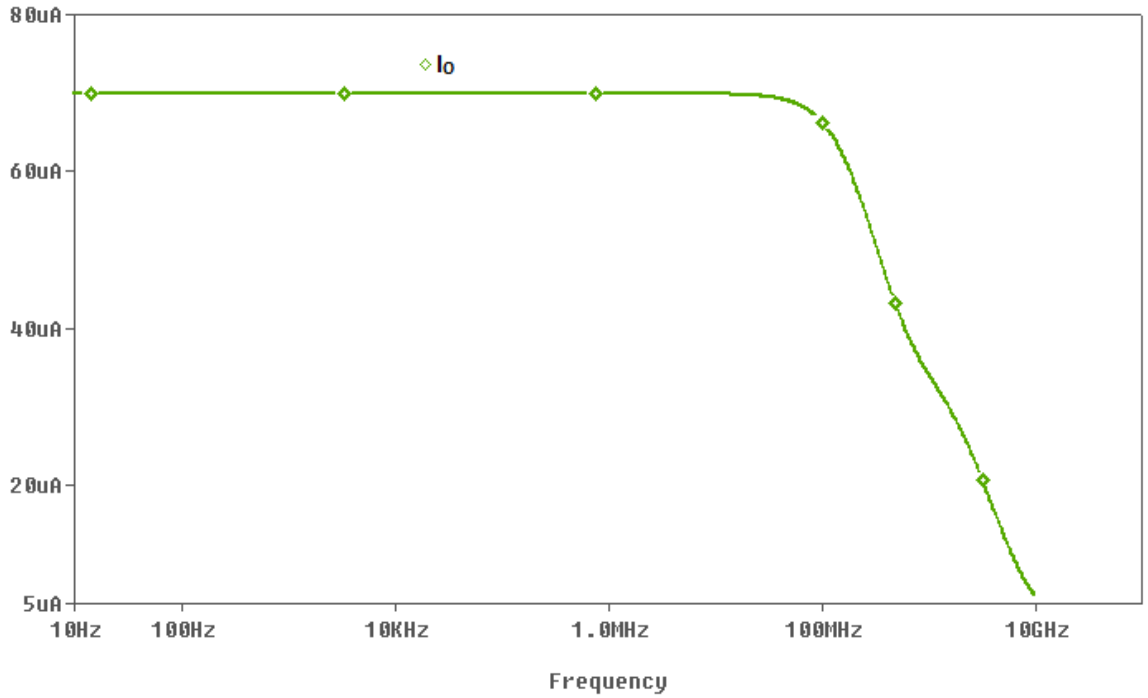


Fig. 2.13 Simulated port relationship $I_O = -g_m V_Z$ in AC analysis

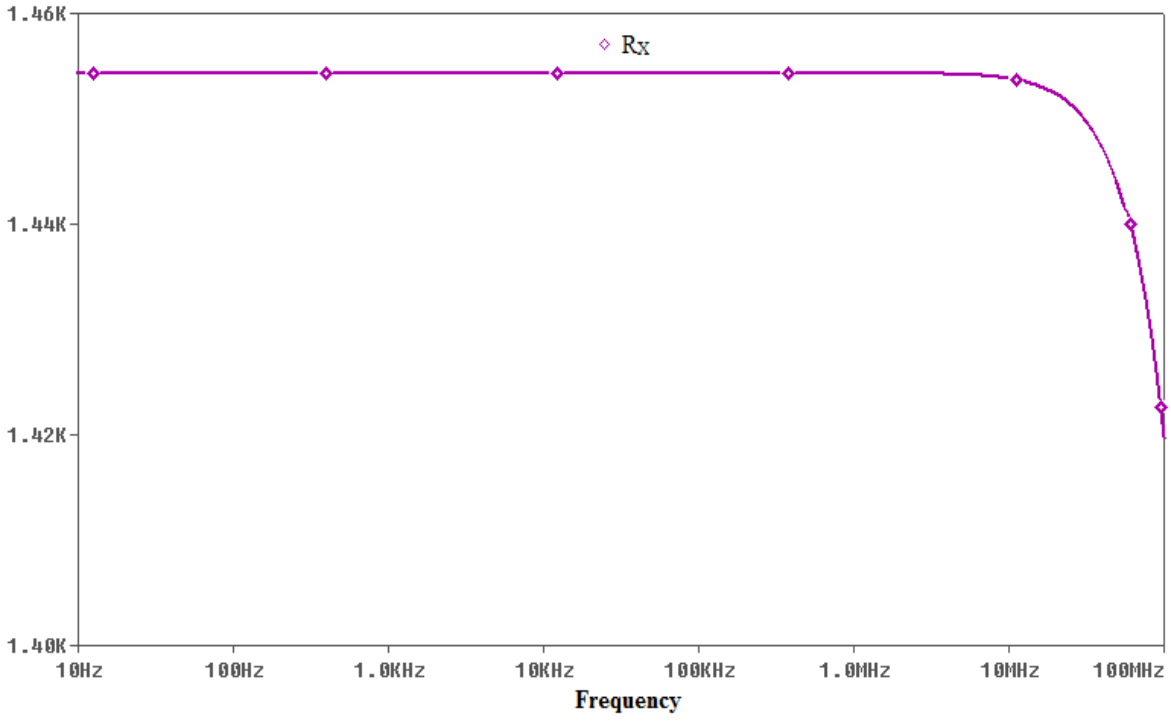


Fig. 2.14 Frequency response of parasitic Resistance of DVCCCTA at I_{B1} =25µA

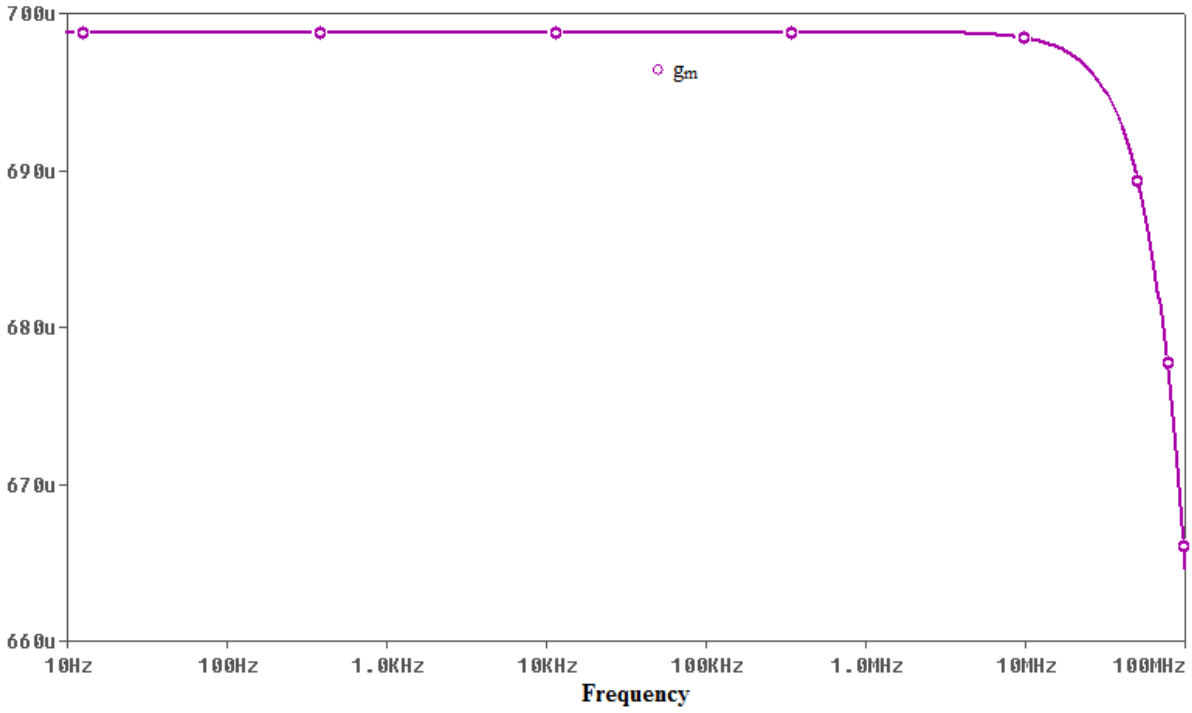


Fig. 2.15 frequency response of transconductance of DVCCCTA at I_{B2} =200µA

c) Non- ideality in DVCCCTA:

Taking into consideration the DVCCCTA non-idealities due to voltage and current tracking error, the terminal relation in equation (2.13) can be expressed as

$$V_X = \beta_1 V_{Y1} - \beta_2 V_{Y2} + I_X R_X, \quad I_Z = \alpha I_X, \quad I_O = -\gamma g_m V_Z$$

β_1 and β_2 represents the voltage tracking error from Y_1 and Y_2 terminal to the X terminal respectively. α and γ represents the current tracking error from X to Z terminal and Z to O terminal respectively.

To calculate β_1, put $V_{Y2} = 0$ and $I_X = 0$. The calculated value of β_1 from the graph shown in Fig. 2.16 is .9875 and to calculate β_2, put $V_{Y1} = 0$ and $I_X = 0$. The calculated value of β_2 from the graph shown in Fig. 2.17 is .9865. From the graph shown in Fig. 2.12, the measured value of α is 1.049

d) Parasitic at Z and O terminal:

From the graph shown in Fig. 2.18, the parasitic resistance and capacitance at Z terminal is 241.804 KΩ and 32.98 ff respectively and the measured value of parasitic

resistance and capacitance at O terminal from the graph of Fig. 2.19 are 67.931 KΩ and 8.7ff respectively.

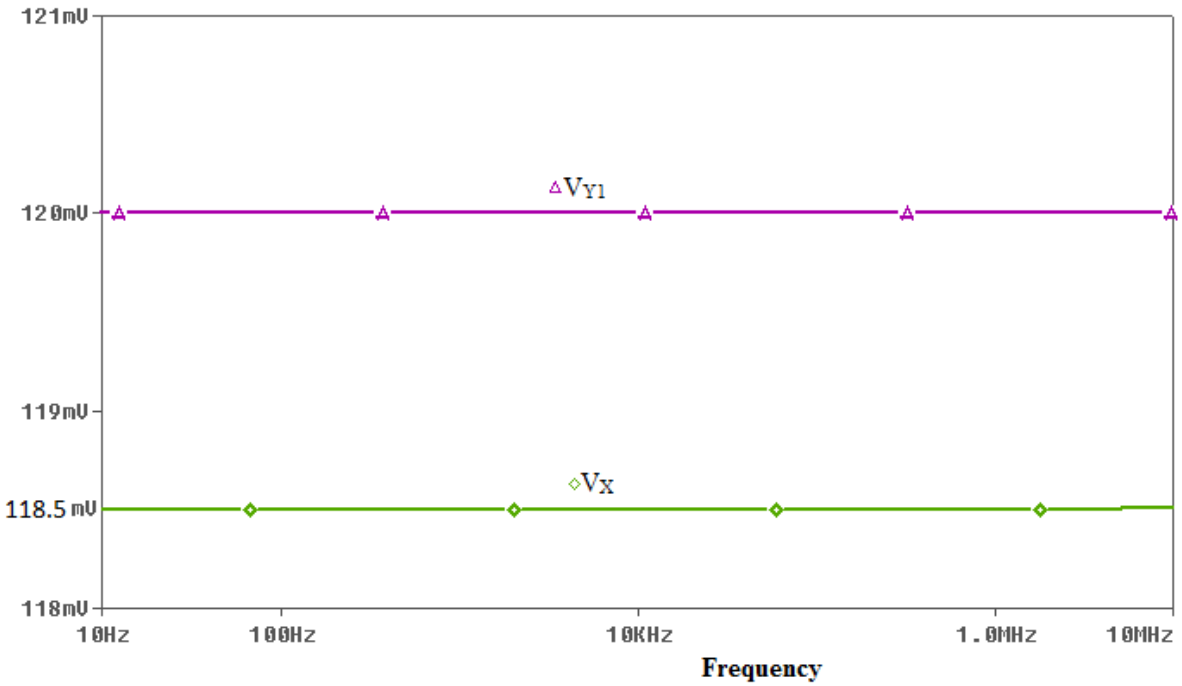


Fig. 2.16 graph for calculation of β_1

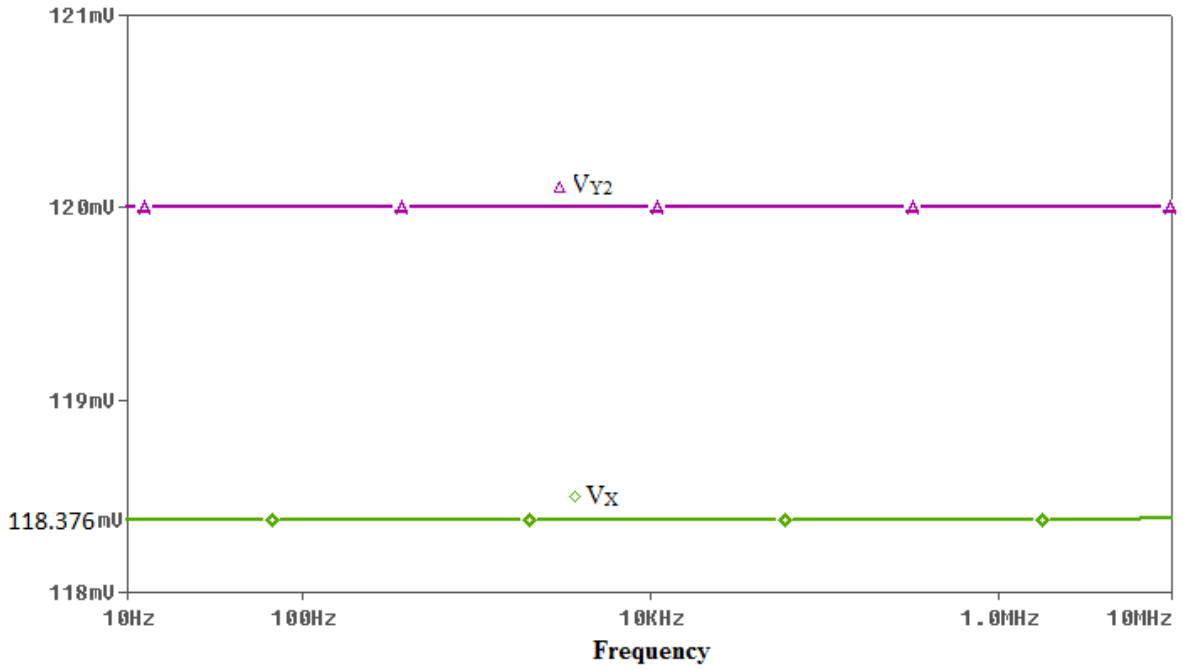


Fig. 2.17 graph for calculation of β_2

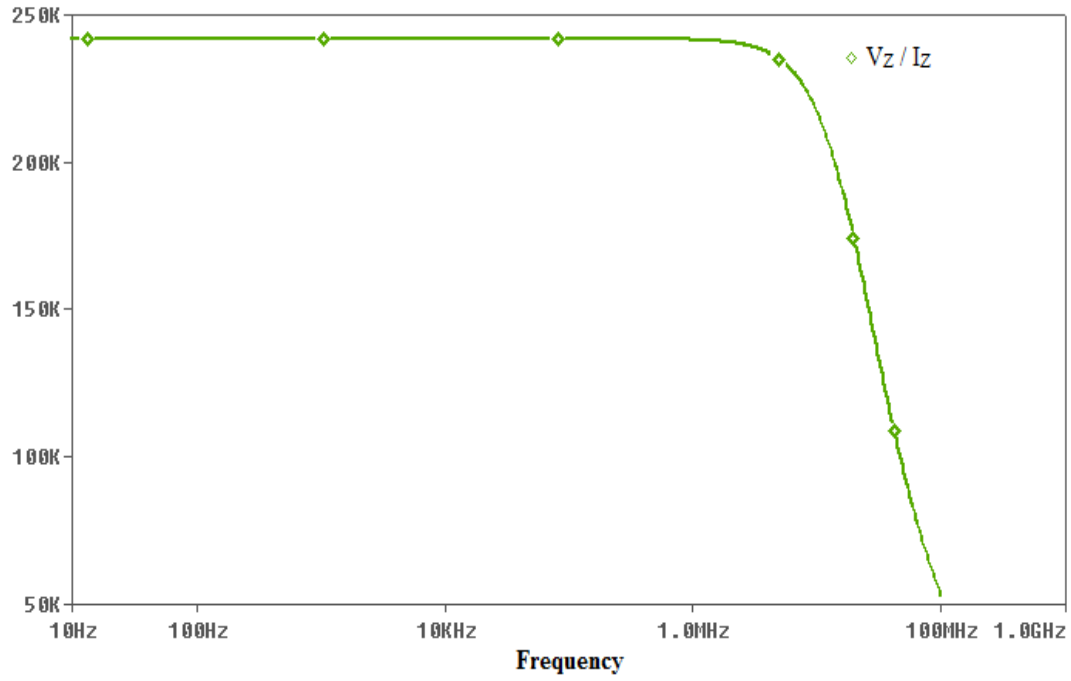


Fig. 2.18 graph for calculation of parasitic at Z terminal

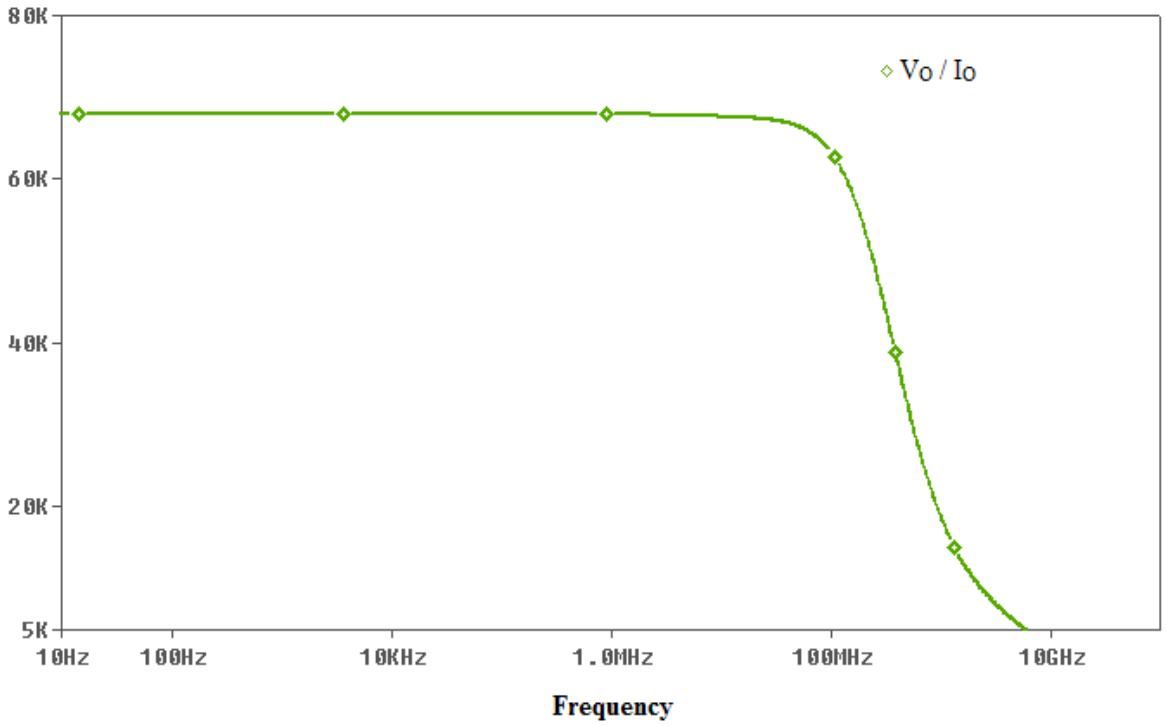


Fig. 2.19 graph for calculation of parasitic at O terminal

Chapter 3

Wave Active Filter

3.1 Introduction

Higher order filter may be designed by mainly three approaches- topological simulation, operational simulation and wave active.

In topological simulation or element replacement approach, the objective is to eliminate the inductor from the ladder filter. So the inductors of the LC ladder filters are replaced by appropriate configured active elements. The disadvantage of this approach is that a floating capacitor is used in active element and the floating passive elements are not good from the IC point of view as the parasitic are involve at high frequency.

In the operational simulation or leapfrog approach, the voltage and current relationships for each element of LC ladder filter are written. Then a Signal Flow Graph (SFG) is drawn using these equations and the resulted SFG is realized by lossy or lossless integrator. The drawback of this approach is that as we increase the order of filter, the number of the required equations for deriving the corresponding SFG increases. Another drawback is that, the realization of lossless integrators is not practically easy due to the imperfections imposed by the used active and passive elements.

An alternative approach for designing high-order filters is the wave method [21]-[27]. In this approach, we split the given filter into two port subnetworks. We draw the wave equivalent of the element of each subnetwork. For this first we draw the basic wave equivalent of series inductor, then the wave equivalent of other passive component can be drawn by interchanging the terminal and signal inversion. By interconnecting the wave equivalents of each passive component we get the complete wave equivalent of the given filter. Wave active approach offers the following attractive feature.

a) The derived filter structures are modular, as the equivalents of the other passive components can be obtained from the wave equivalent of the elementary building block

b) In wave active approach there is no mathematical relationships related to the SFG representation as in the case of operational simulation approach. So the design procedure of high-order filters is much easier in compare to operational simulation approach

c) Realization of only lossy integrators using only grounded capacitors are required, instead of lossless integrators employed in the operational simulation or floating capacitors employed in the topological simulation.

3.2 Wave Active Filter

Wave active filter (WAF) design is an alternative approach to the simulation of resistively terminated LC ladder filter. According to this method, the corresponding passive prototype filter is split into two-port subnetworks which are fully described using the wave variables, defined as incident and reflected waves. The method to obtain wave equivalents of the two-port subnetworks is by using the scattering parameters matrix description. By choosing an inductor in a series branch as the elementary building block, its wave equivalent includes an appropriately configured lossy integrator. The wave equivalents of the other passive elements are derived by interchanging the terminals of the appropriate wave signals and signal inversion.

As already mentioned, our approach to the synthesis of RC-active networks is based on the use of wave quantities rather than voltage-current quantities, hence the scattering matrix will play an important role in our concept. Usually, if scattering parameters are being used, as e.g., in microwave theory, they are derived for power waves; we could adopt this concept for our aim, too, but the use of voltage or current waves seems more convenient for our approach, since it leads sometimes to simpler circuits and, in addition, it simplifies the notation. For the approach presented in this report, we have decided to use voltage waves, which shall be introduced now.

Consider the two-port N shown in Fig. 3.1, where the A_1, A_2 and B_1, B_2 denote the incident and reflected voltage waves at port one and two, respectively. To either port we assign a port resistance (characteristic resistance) R_1 and R_2 respectively; the port resistances are assumed to be real positive constants.

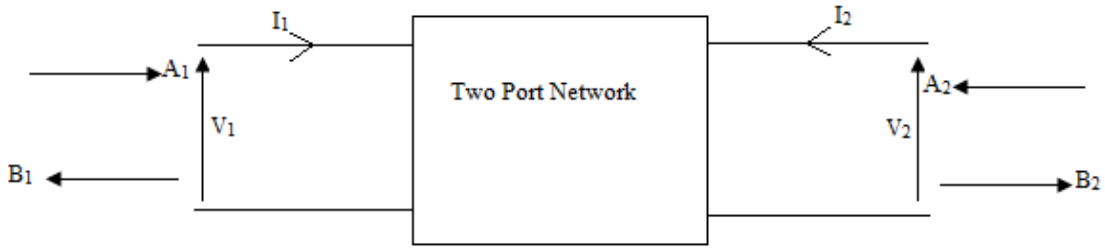


Fig. 3.1 Two port network

The V, I port variables are related by means of a transmission matrix A as:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \tag{3.1}$$

The incident and reflected voltage waves are depicted as A_j (j=1,2) and B_j (j=1,2) respectively for two port network of Fig. 3.1 and are related with port resistance R_j (j=1,2) by the following relation:

$$A_j = V_j + I_j R_j \quad \text{and} \quad B_j = V_j - I_j R_j \tag{3.2}$$

On combining equation (3.1) and (3.2) we have the following relationship for incident and reflected wave in the form of scattering matrix as:

$$\begin{bmatrix} B_1 \\ B_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{21} \end{bmatrix} \begin{bmatrix} A_1 \\ A_2 \end{bmatrix} \tag{3.3}$$

Where

$$S_{11} = (A - CR_1 - BG_2 + DR_1G_2) / \Delta$$

$$S_{12} = R_1G_2 / \Delta$$

$$S_{21} = 1/ \Delta$$

$$S_{22} = (A + CR_1 + BG_2 + DR_1G_2) / \Delta$$

And here

$$G_2 = 1/R_2$$

$$\Delta = A + CR_1 - BG_2 - DR_1G_2 \tag{3.4}$$

Since the aim of the procedure is the realization of ladder filters, we need only consider subnetworks for equation (3.2), which are either impedances in the series arms or admittances in the shunt arms. From these subnetworks, we can derive the overall ladder by suitable interconnections.

The transmission parameter for a series-arm impedance Z and a parallel-arm admittance Y, are as follows:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & -Z \\ 0 & -1 \end{bmatrix} \tag{3.5}$$

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ Y & -1 \end{bmatrix} \tag{3.6}$$

Substituting in equation (3.4) and subsequently in equation (3.3) we get the following equations relating the wave variables for the two cases:

For series arm impedance

$$S_{11} = \frac{R_2 - R_1 + Z}{R_1 + R_2 + Z} \qquad S_{12} = \frac{2R_1}{R_1 + R_2 + Z}$$

$$S_{21} = \frac{2R_2}{R_1 + R_2 + Z} \qquad S_{22} = \frac{R_1 - R_2 + Z}{R_1 + R_2 + Z} \tag{3.7}$$

And for shunt arm admittance

$$S_{11} = \frac{G_1 - G_2 - Y}{G_1 + G_2 + Y} \qquad S_{12} = \frac{2G_2}{G_1 + G_2 + Y}$$

$$S_{21} = \frac{2G_1}{G_1 + G_2 + Y} \qquad S_{22} = \frac{G_2 - G_1 - Y}{G_1 + G_2 + Y} \tag{3.8}$$

Substituting these values in equation (3.3), we have the following relation for incident and reflected wave form for series arm impedance

$$\begin{bmatrix} B_1 \\ B_2 \end{bmatrix} = \begin{bmatrix} \frac{R_2 - R_1 + Z}{R_2 + R_1 + Z} & \frac{2R_1}{R_2 + R_1 + Z} \\ \frac{2R_2}{R_2 + R_1 + Z} & \frac{R_1 - R_2 + Z}{R_2 + R_1 + Z} \end{bmatrix} \begin{bmatrix} A_1 \\ A_2 \end{bmatrix} \tag{3.9}$$

And for shunt arm admittance is

$$\begin{bmatrix} B_1 \\ B_2 \end{bmatrix} = \begin{bmatrix} \frac{G_1 - G_2 + Y}{G_1 + G_2 + Y} & \frac{2G_2}{G_1 + G_2 + Y} \\ \frac{2G_1}{G_1 + G_2 + Y} & \frac{G_2 - G_1 + Y}{G_1 + G_2 + Y} \end{bmatrix} \begin{bmatrix} A_1 \\ A_2 \end{bmatrix} \tag{3.10}$$

Here $G_i = 1/R_i$

We shall restrict the port resistances to be equal, i.e. $R_1 = R_2 = R$, and hence we shall have the relation between reflected and incident waves for series arm impedance is

$$B_1 = \frac{Z}{2R + Z} A_1 + \frac{2R}{2R + Z} A_2 \tag{3.11}$$

$$B_2 = \frac{2R}{R_2 + R_1 + Z} A_1 + \frac{Z}{R_2 + R_1 + Z} A_2 \tag{3.12}$$

And for shunt arm admittance, the relation between reflected and incident wave are

$$B_1 = \frac{-Y}{2G + Y} A_1 + \frac{2G}{2G + Y} A_2 \tag{3.13}$$

$$B_2 = \frac{2G}{2G + Y} A_1 + \frac{-Y}{2G + Y} A_2 \tag{3.14}$$

We note that the reflected waves arise as linear combinations of incident waves. For example, in the series-arm impedance, we see that B_1 is formed by linearly combining A_1 and A_2, and the constants of such a linear combination are themselves transfer ratios of the form $\frac{Z}{2R + Z}$ and $\frac{2R}{2R + Z}$. Thus, we no longer treat the incident voltage waves as waves, but rather as voltages impressed on an appropriate RC active network conceived so that

the reflected voltage waves appear as voltages resulting from such an excitation across some other pairs of terminals. By this means, the relationships can be satisfied.

Equations (3.10) to (3.11) are the basic equation for series arm impedance and equation (3.12) and (3.14) are for shunt arm admittance. For example to obtain wave equation for series inductor put, Z = sL in equation (3.10) and (3.11).

Chapter 4

Realization of wave active filter using DVCCCTA

This chapter presents systematic design approach for realization of DVCCCTA based wave active filter. As described in the chapter 3, in wave method, the corresponding passive prototype filter is split into two-port subnetworks which are fully described using the wave variables, defined as incident and reflected waves. We use series inductor as a basic element for developing the wave active filter. The wave equivalent of an inductor in series branch is developed using differential voltage current controlled conveyor transconductance amplifier (DVCCCTA), then this basic wave equivalent can be used for other passive element realization by making appropriate connection. The results are verified through SPICE simulation using 0.25µm TSMC CMOS technology parameters.

4.1 Basic Wave Equivalent (Series Inductor)

The wave equivalent of series branch inductor is used as a basic wave equivalent. For series inductor put Z= sL, in the equation (3.11) and (3.12) and rearranging them we have the following equation

$$B_1 = A_1 - \frac{1}{1+s\tau}\left(A_1 - A_2\right) \tag{4.1}$$

$$B_2 = A_2 + \frac{1}{1+s\tau}\left(A_1 - A_2\right) \tag{4.2}$$

Where $\tau = \frac{L}{2R}$, time constant and R is is represents port resistance.

The implementation of wave equations (4.1) and (4.2) require three operations - lossy integration subtraction, summation and subtraction. These operations can easily be realized using DVCCCTA and are explained in the following section.

4.1.1 Lossy Integration Subtraction

The structure to implement lossy integration subtraction is depicted in Fig. 4.1. It uses a single DVCCCTA and a grounded capacitor.

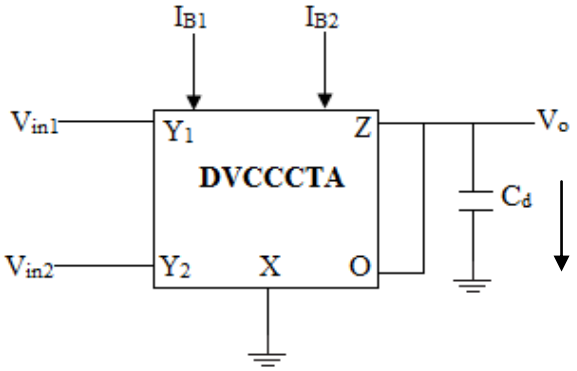


Fig. 4.1 Block diagram of lossy integration subtraction using DVCCCTA

Apply KCL at output node, the current through capacitor is

$$I_C = -(I_Z + I_O) \tag{4.3}$$

Then

$$V_O = -\left(\frac{I_Z + I_O}{sC}\right) \tag{4.4}$$

$$I_Z = I_X, \quad I_O = g_m V_O \tag{4.5}$$

Put the value of eqn. (4.5) into eqn. (4.4)

$$V_O = -\left(\frac{I_X + g_m V_O}{sC}\right)$$

$$V_O\left(g_m + sC\right) = -I_X \tag{4.6}$$

From the port relation of DVCCCTA

$$V_X = V_{in1} - V_{in2} + I_X R_X \tag{4.7}$$

From the block diagram of Fig. 4.1, put $V_X = 0$

Then

$$I_X = -\left(\frac{V_{in1} - V_{in2}}{R_X}\right) \tag{4.8}$$

Put the value of I_X in equation (4.6)

$$V_O = \left(\frac{V_{in1} - V_{in2}}{1 + \tau s}\right) \tag{4.9}$$

Where $\tau = R_X C_d$ is time constant and $g_m R_X = 1$. Using (4.1), (4.2) and (4.9), the value of C_d may be computed as

$$R_X C_d = \frac{L}{2R} \tag{4.10}$$

Assuming $R_X = R$, the value of capacitor C_d may be expressed as

$$C_d = \frac{L}{2R^2} \tag{4.11}$$

4.1.2 Subtraction

The subtraction operation can be easily performed with DVCCCTA as it has two high input impedance terminals. Fig. 4.2 shows the topology that can be used for voltage subtraction. To calculate the output voltage output $V_{O,}$ apply KCL at output node

$$I_Z + I_O = 0$$

Put the value of I_Z and I_O from equation (4.5)

$$I_X + g_m V_O = 0$$

$$V_o = -\frac{I_X}{g_m}$$

Put the value of I_X from equation (4.8)

$$V_o = V_{in1} - V_{in2} \quad \text{With} \quad g_m R_X = 1 \tag{4.12}$$

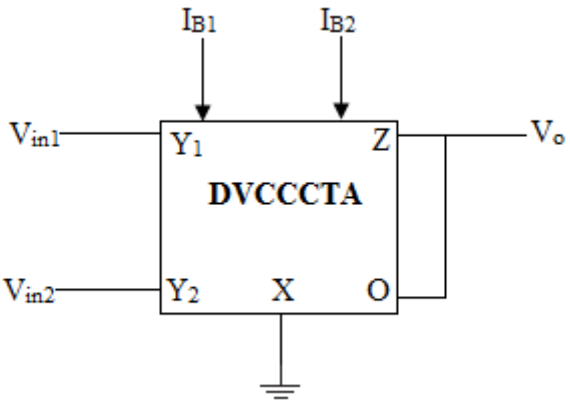


Fig. 4.2 Block diagram of subtraction using DVCCCTA

4.1.3 Summation

The circuit for summation is shown in Fig. 4.3. The first DVCCCTA inverts the inputs V_{in2} which is then subtracted from input V_{in1} by second DVCCCTA to provide output as

$V_o = V_{in1} - (-V_{in2})$

$V_o = V_{in1} + V_{in2}$ With $g_m R_X = 1$ (4.13)

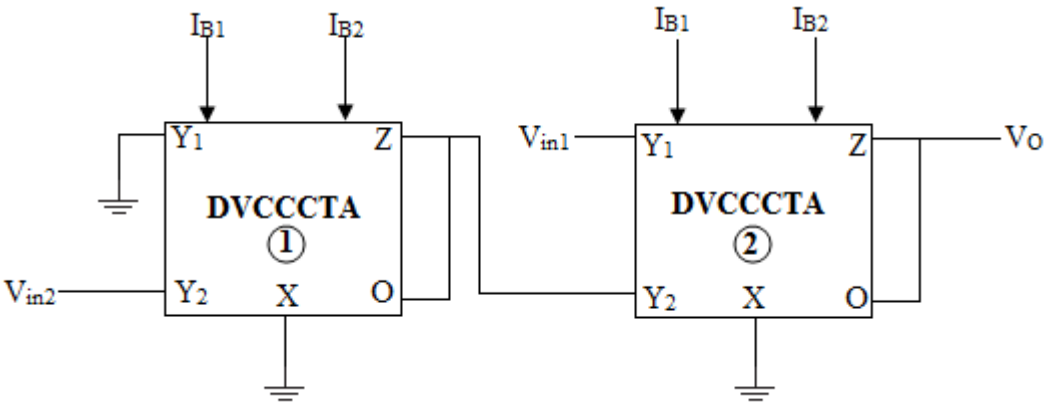
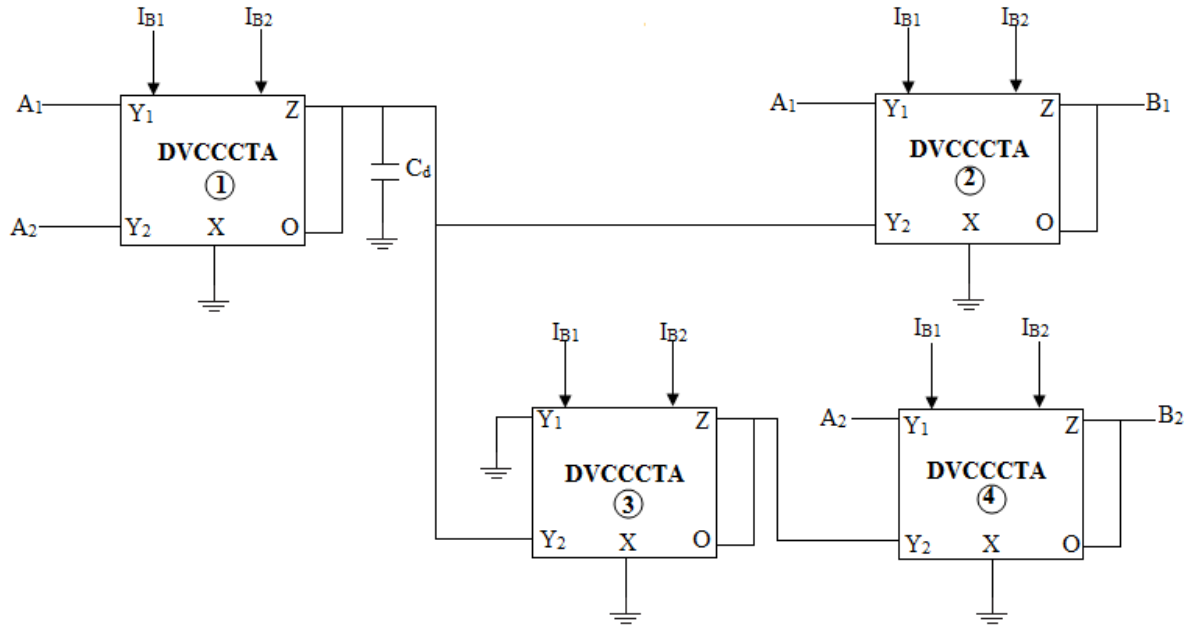


Fig. 4.3 Block diagram of summation using DVCCCTA

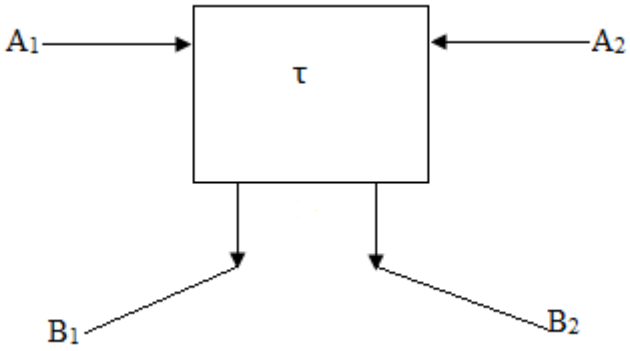
4.1.4 Complete Realization of series Inductor

The complete schematic of wave equivalent for series inductor as given by (4.1) and (4.2) can be obtained by cascading the blocks of Fig. 4.1 to 4.3. The arrangement is shown in Fig.

4.4(a) and its symbolic representation is shown in Fig. 4.4(b).



(a)



(b)

Fig. 4.4 (a) Complete schematic of DVCCCTA based wave equivalent of series inductor and (b) its symbolic representation

With the help of this basic wave equivalent, the wave equivalent of other passive component can be obtained by swapping outputs and using signal inversion as shown in table1 and table2.

Table1

Wave equivalent of Elementary Two Port consisting of series branch element

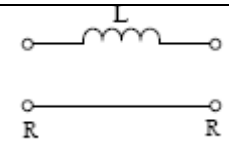
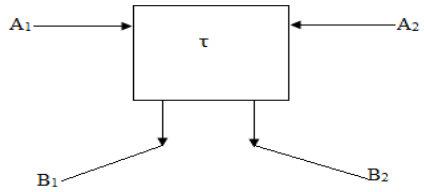
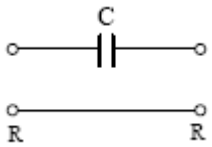
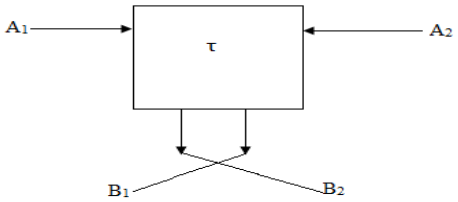
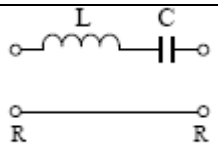
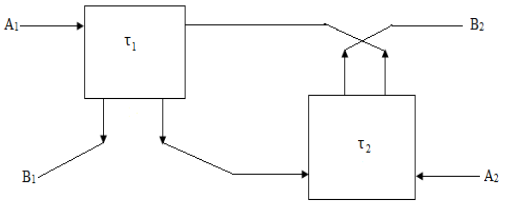
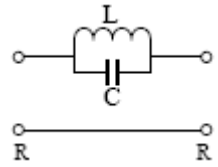
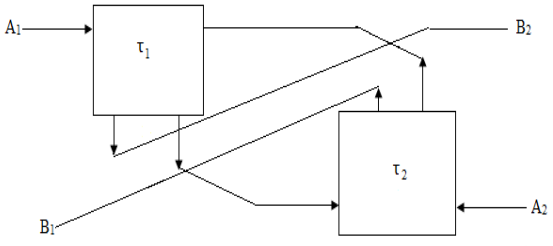
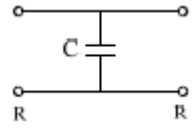
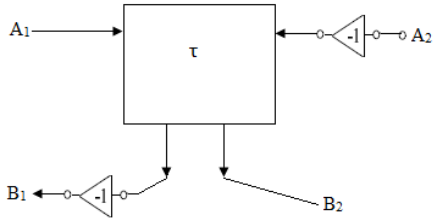
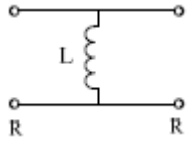
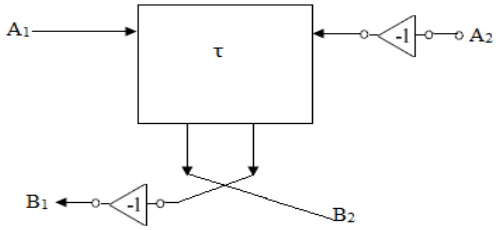
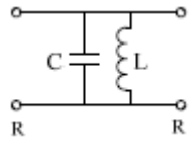
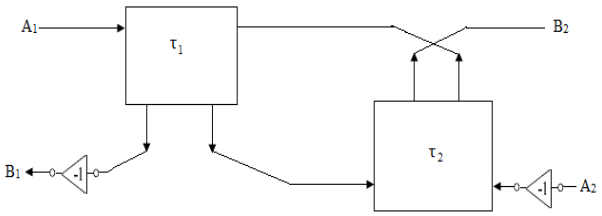
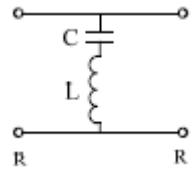
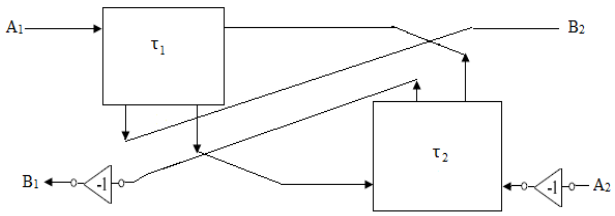
Elementary two port	Wave flow diagram	Time Constant	Capacitor in DVCCCTA Integrator
		$\tau = L/2R$	$C_d=L/2R^2$
		$\tau = 2RC$	$C_d=2C$
		$\tau_1= L/2R$ $\tau_2= 2RC$	$C_{1d}=L/2R^2$ $C_{2d}=2C$
		$\tau_2= 2RC$ $\tau_1= L/2R$	$C_{1d}=2C$ $C_{2d}=L/2R^2$

Table2

Wave equivalent of Elementary Two Port consisting of shunt branch element

Elementary two port	Wave flow diagram	Time Constant	Capacitor in DVCCCTA Integrator
		$\tau = RC/2$	$C_d=C/2$
		$\tau = 2L/R$	$C_d=2L/R^2$
		$\tau_1 = RC/2$ $\tau_2 = 2L/R$	$C_{1d}=C/2$ $C_{2d}=2L/R^2$
		$\tau_1 = 2L/R$ $\tau_2 = RC/2$	$C_{1d}=2L/R^2$ $C_{2d}=C/2$

4.2 Wave equivalent of two port sub network in floating Branch

4.2.1 Inductor in series branch

Here we take L = 1mH.

For L = 1mH, and R = R_X =1454.3Ω the value of cut-off frequency is 463 KHz. The value of capacitor used in its wave equivalent is C_d=L/$2R^2$ = 236.4pf. The value of cut-off frequency from the simulated result shown in Fig. 4.5(c) is 462 KHz.

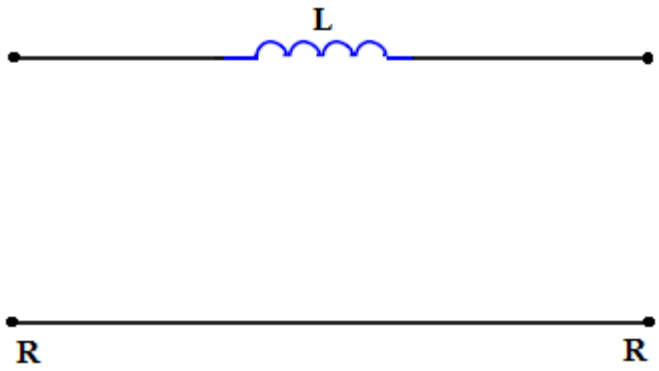


Fig. 4.5(a) two port network of floating inductor

The wave equivalent of floating inductor is shown in Fig. 4.5(b).

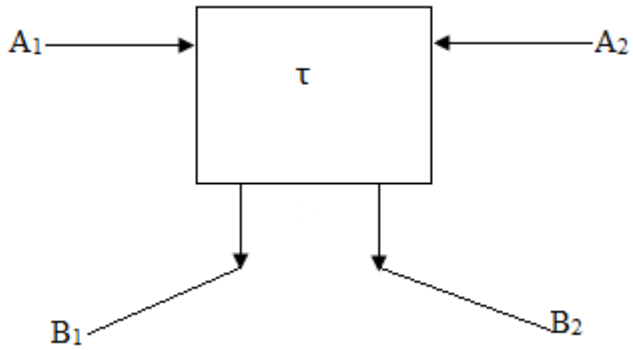


Fig. 4.5(b) wave equivalent of floating inductor

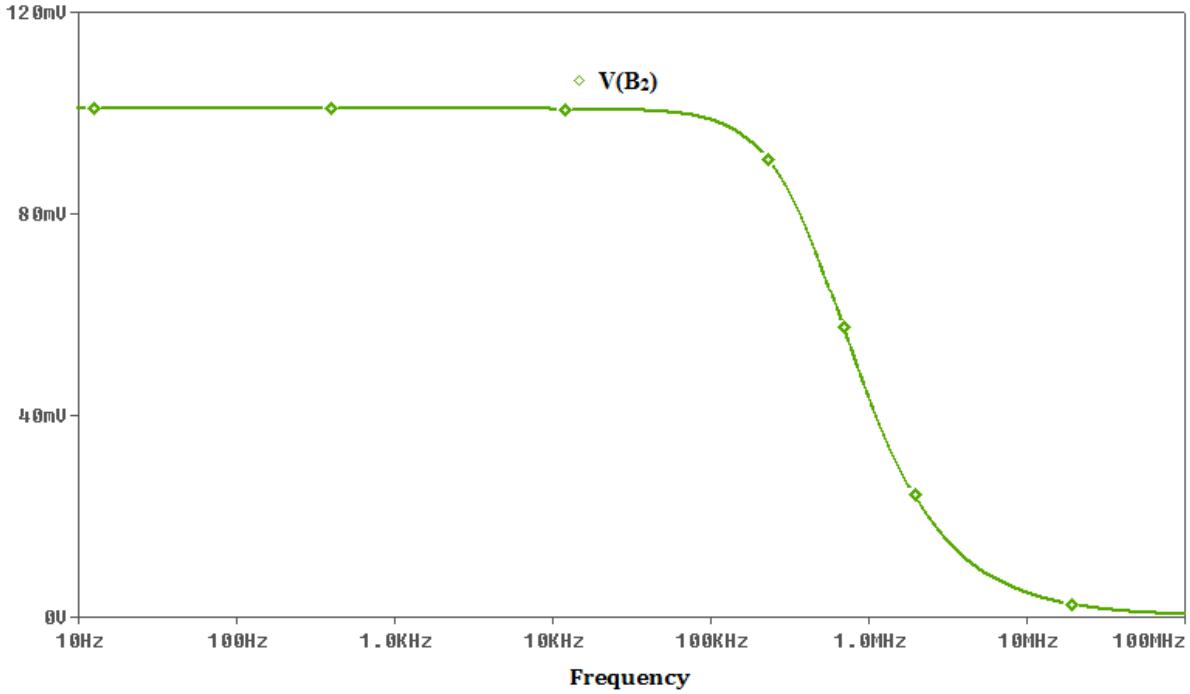


Fig. 4.5(c) Frequency response of floating inductor

4.2.2 Capacitor in series branch

Here we take C = 100pf. For C = 100pf, and R = R_X =1454.3Ω, the value of cut-off frequency is 547.18 KHz. The value of capacitor used in its wave equivalent is C_d=2C = 200pf. The value of cut-off frequency from the simulated result shown in Fig. 4.6(c) is 596 KHz.

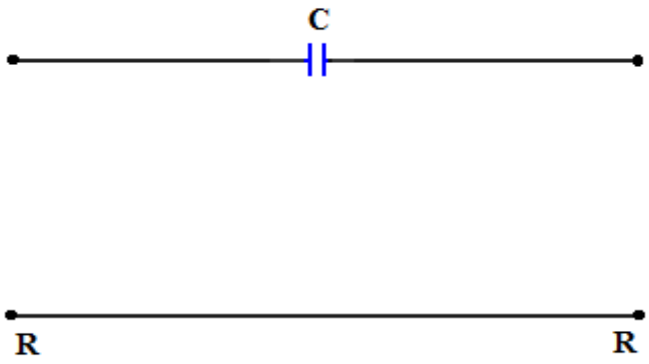


Fig. 4.6(a) two port network of floating capacitor

The wave equivalent of floating capacitor is shown in Fig. 4.6(b).

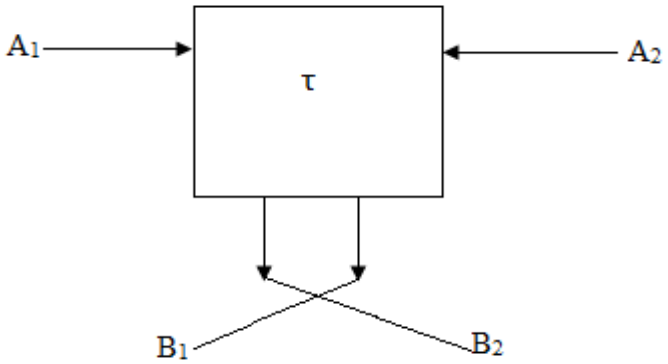


Fig. 4.6(b) wave equivalent of floating capacitor

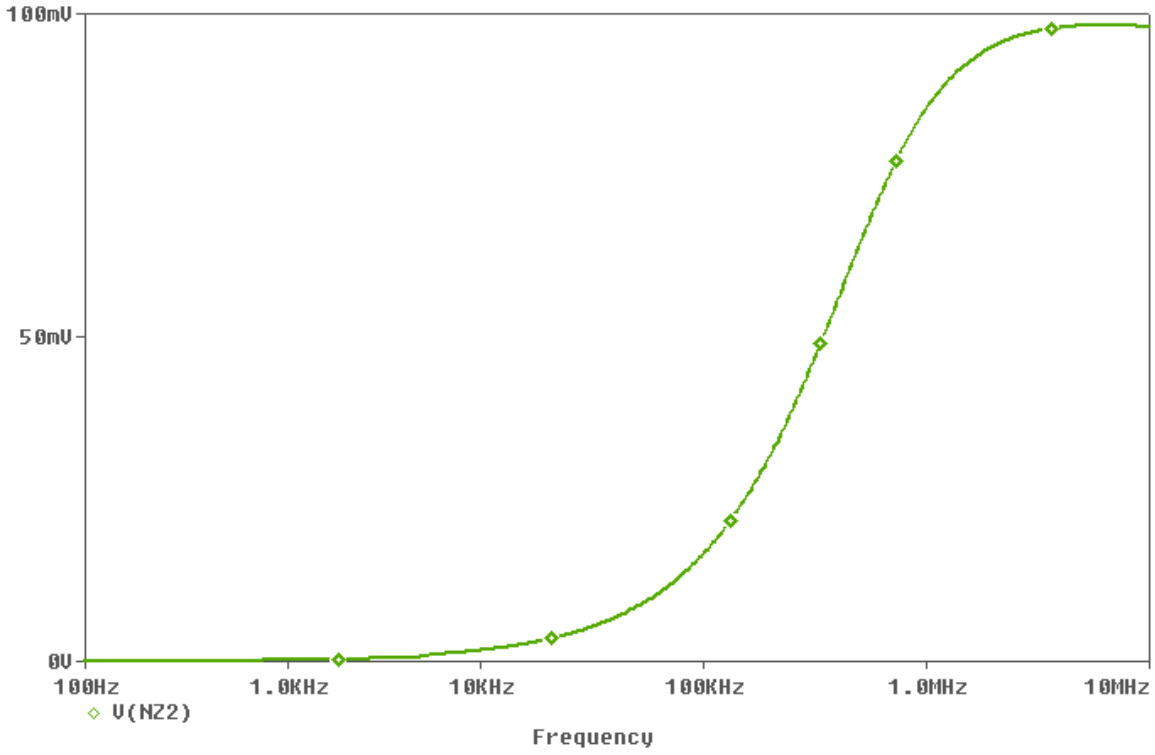


Fig. 4.6(c) Frequency response of floating capacitor

4.2.3 LC series in floating fashion

Here we take L = 1mH and C = 5nf and R = R_X =1454.3Ω. The value of capacitor used in its wave equivalent is C_{1d}=L/$2R^2$ = 236.4pf and C_2 = 2C = 10nf.

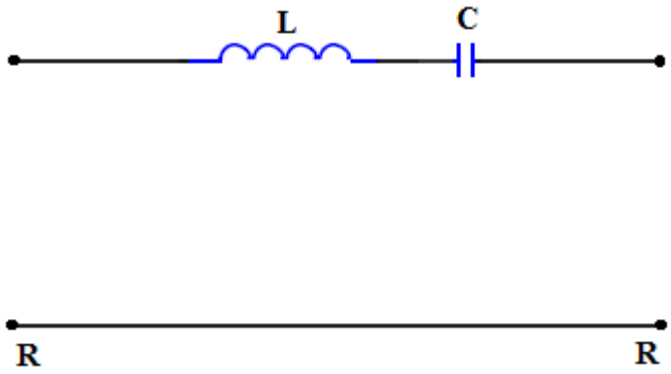


Fig. 4.7(a) two port network of floating LC series

The wave equivalent and the frequency response of floating LC series is shown in Fig. 4.7(b) and Fig. 4.7(c)

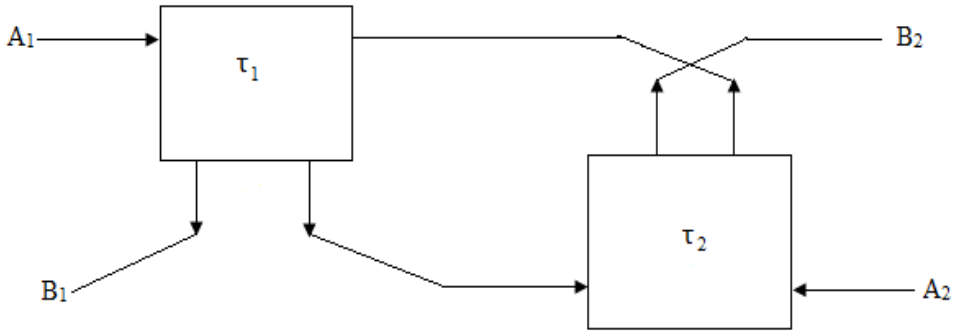


Fig. 4.7(b) wave equivalent of floating LC series

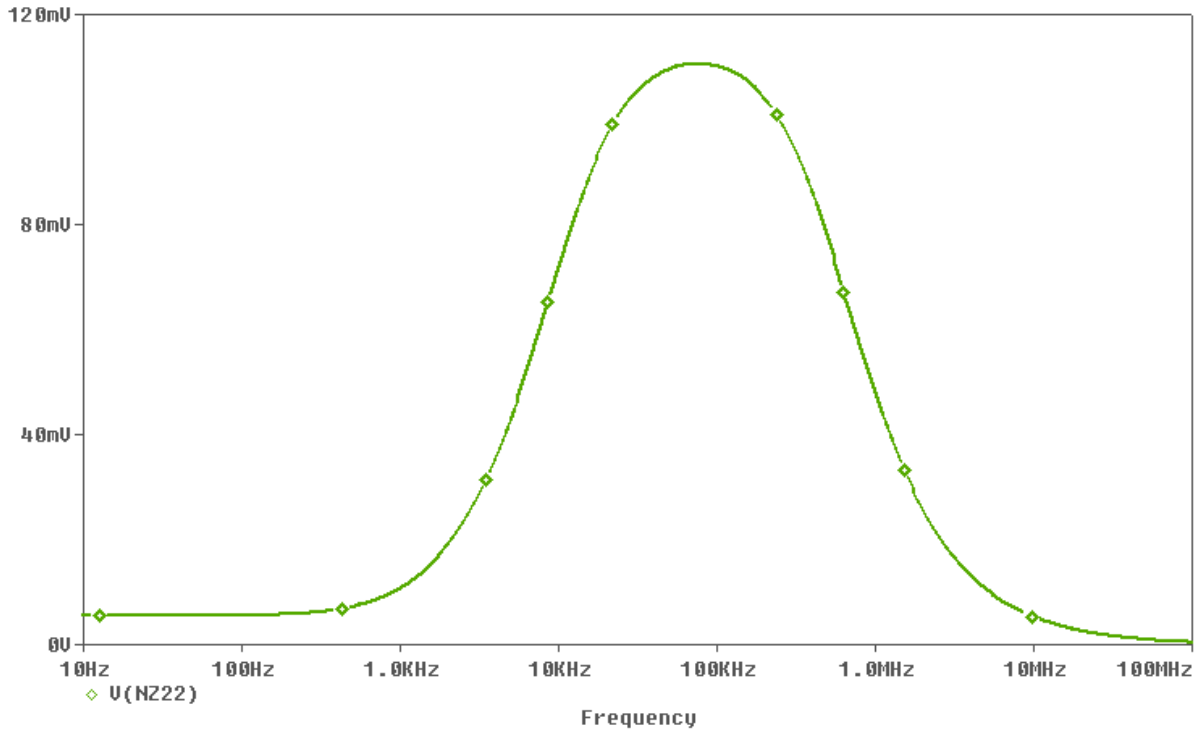


Fig. 4.7(c) Frequency response of floating LC series

4.2.4 LC parallel in floating fashion

For simulation we take L = 10mH and C = 200pf and R = R_X =1454.3Ω. The value of capacitor used in its wave equivalent is C_{2d}=L/$2R^2$ = 2364pf and C_1 = 2C = 400f.

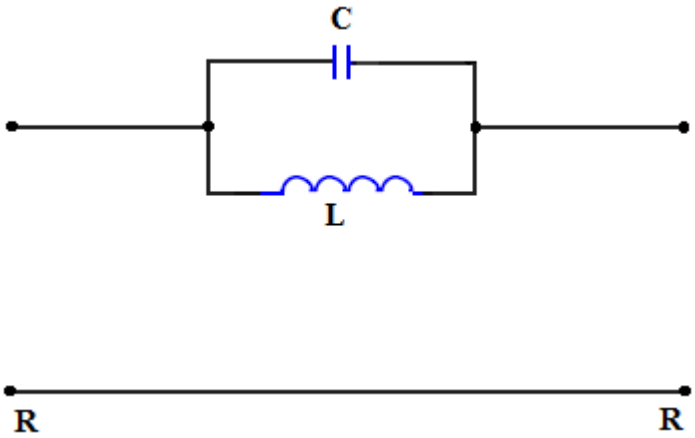


Fig. 4.8(a) two port network of floating LC parallel

The wave equivalent of floating LC parallel is shown in Fig. 4.8(b)

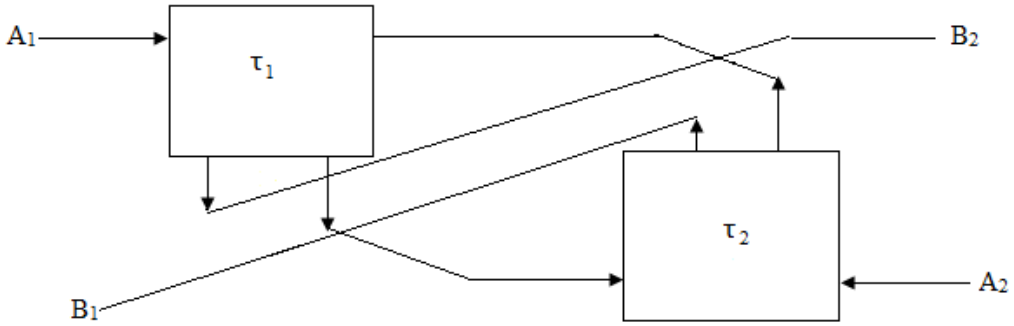


Fig. 4.8(b) wave equivalent of floating LC parallel

The frequency response of floating LC parallel is band reject as shown in Fig. 4.8(c)

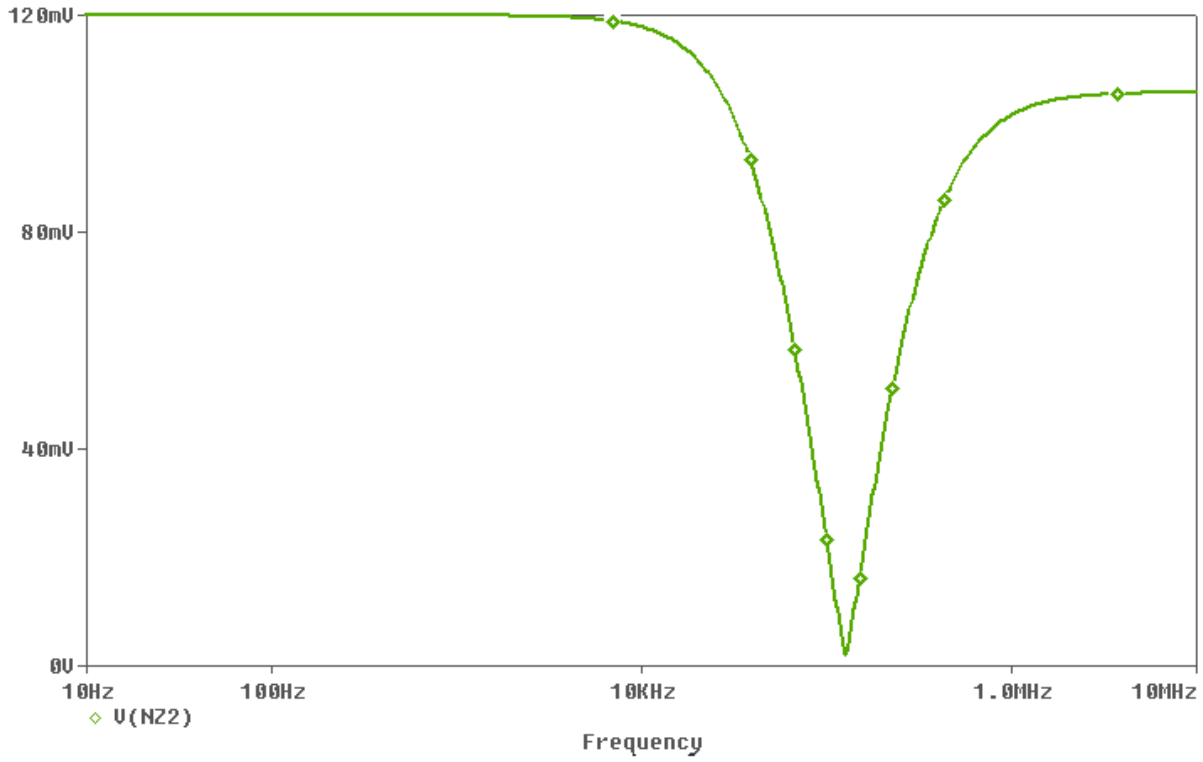


Fig. 4.8(c) Frequency response of floating LC parallel

4.3 Wave equivalent of two port sub network in shunt (grounded) Branch

4.3.1 Inductor in shunt branch

Here we take L = 1mH.

For L = 1mH, and R = R_X =1454.3Ω the value of cut-off frequency is 115.73 KHz. The value of capacitor used in its wave equivalent is C_d=2L/R^2 = 945.63pf. The value of cut-off frequency from the simulated result shown in Fig. 4.9(c) is 134 KHz.

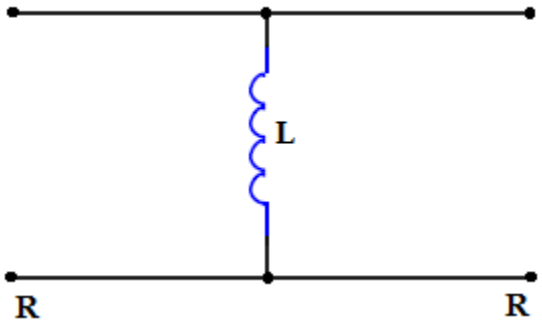


Fig. 4.9(a) two port network of grounded inductor

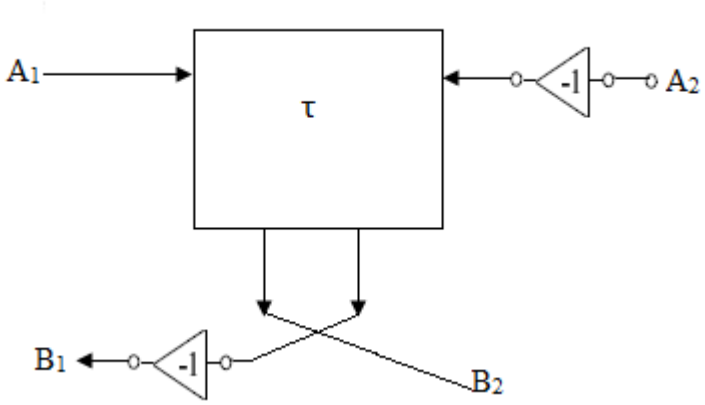


Fig. 4.9(b) wave equivalent of grounded inductor

The frequency response of grounded inductor is high pass as shown in Fig. 4.9(c)

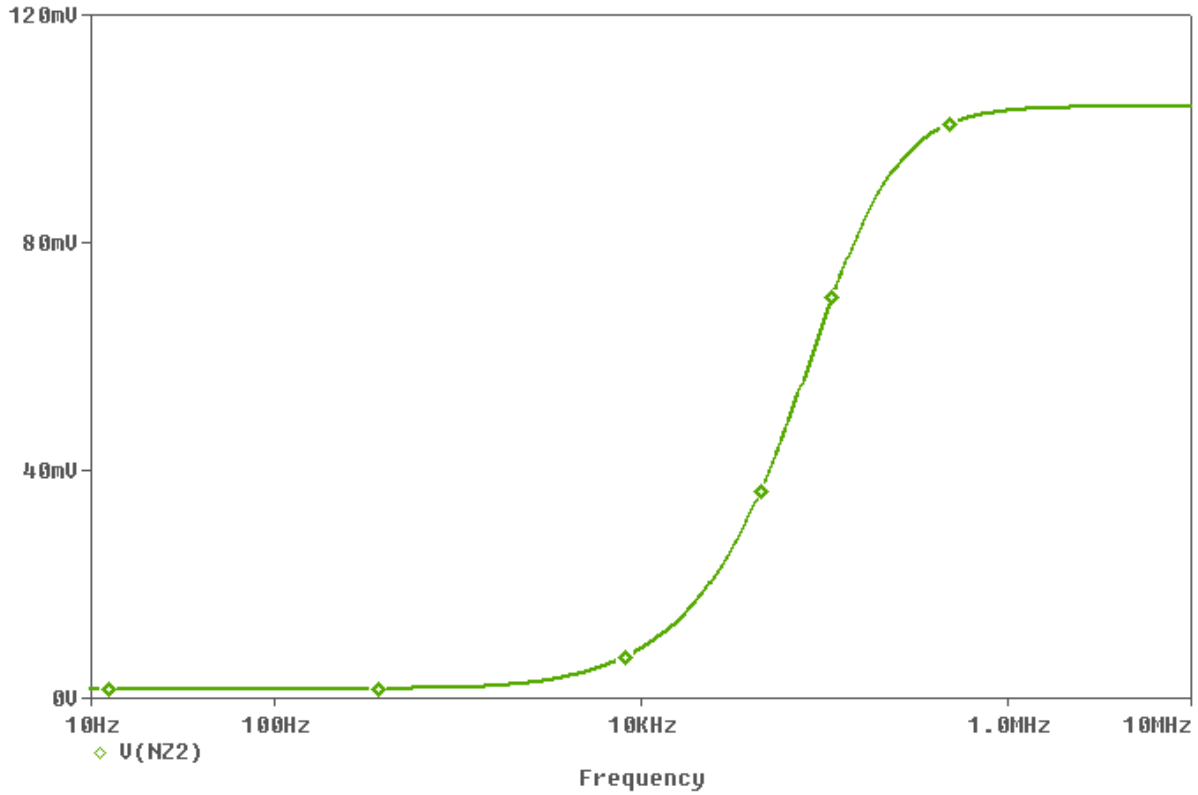


Fig. 4.9(c) Frequency response of grounded inductor

4.3.2 Capacitor in shunt branch

Here we take C = 400pf.

For C = 400pf, and R = R_X =1454.3Ω the value of cut-off frequency is 547.18 KHz. The value of capacitor used in its wave equivalent is C_d = C/2 = 200pf. The value of cut-off frequency from the simulated result shown in Fig. 4.10(c) is 587.74 KHz.

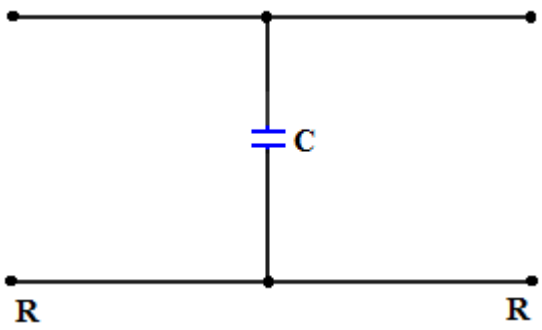


Fig. 4.10(a) two port network of grounded capacitor

The wave equivalent of grounded capacitor is shown in Fig. 4.10 (b).

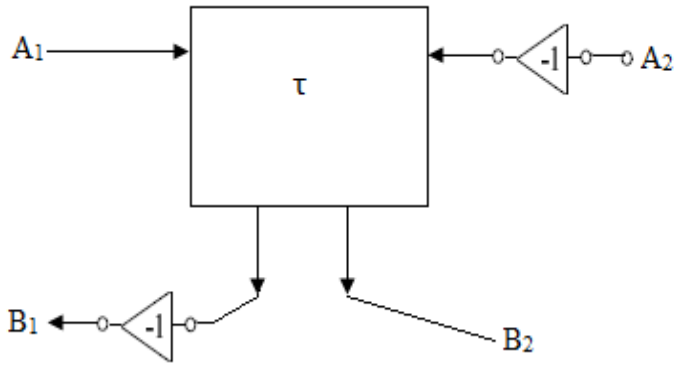


Fig. 4.10(b) wave equivalent of grounded capacitor

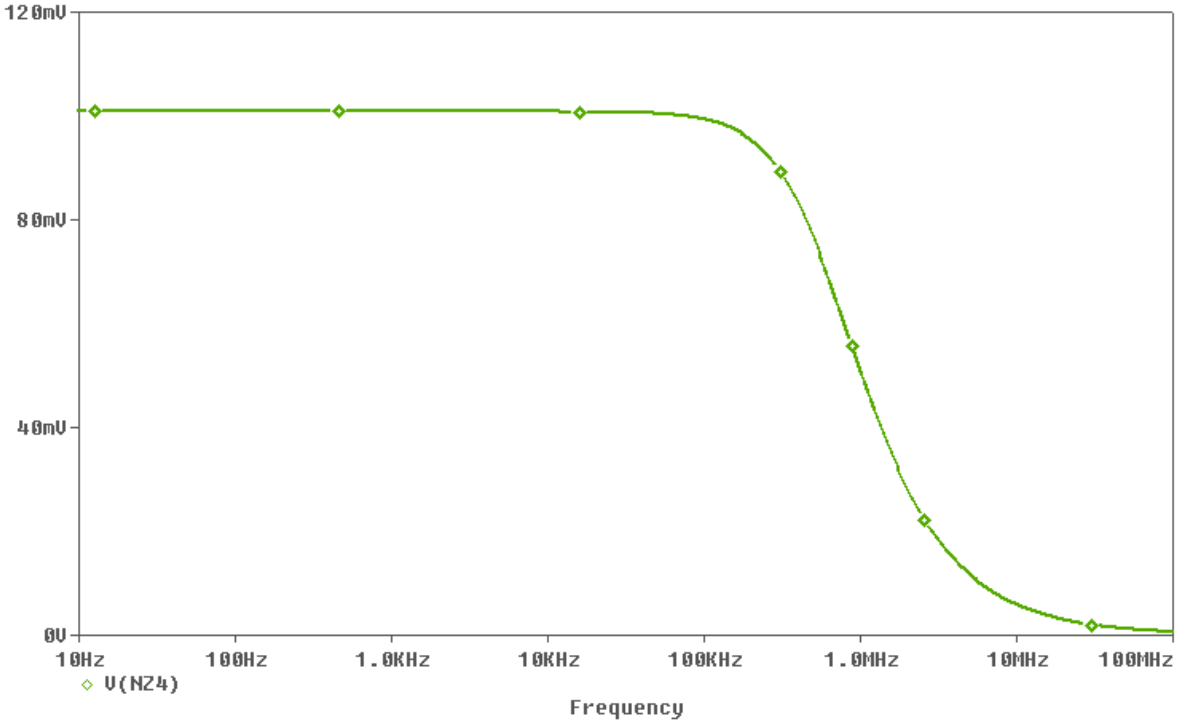


Fig. 4.10(c) Frequency response of grounded capacitor

4.3.3 LC series in grounded fashion

For simulation we take L = 100μH and C = 1nf and R = R_X =1454.3Ω. The value of capacitor used in its wave equivalent is C_{1d}=L/R^2 = 94.56pf and C_2 = C/2 = 500pf.

The frequency response of grounded LC series is band reject as shown in Fig. 4.11(c)

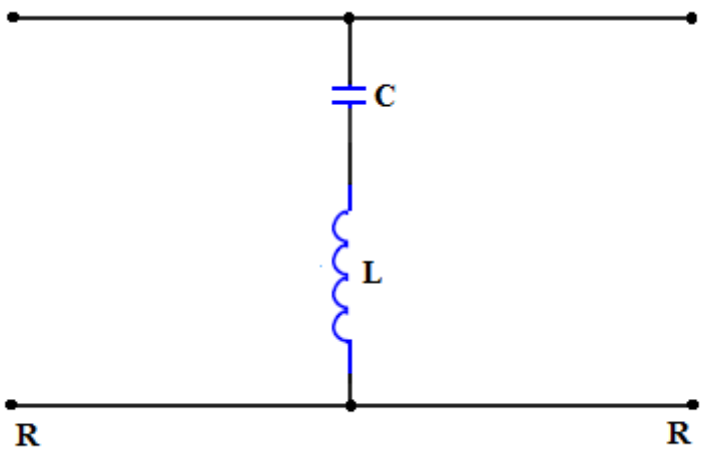


Fig. 4.11(a) two port network of grounded LC series

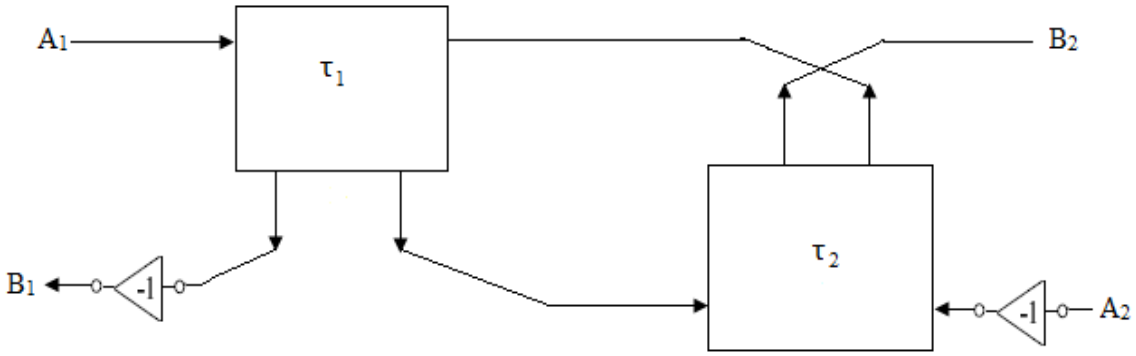


Fig. 4.11(b) wave equivalent of grounded LC series

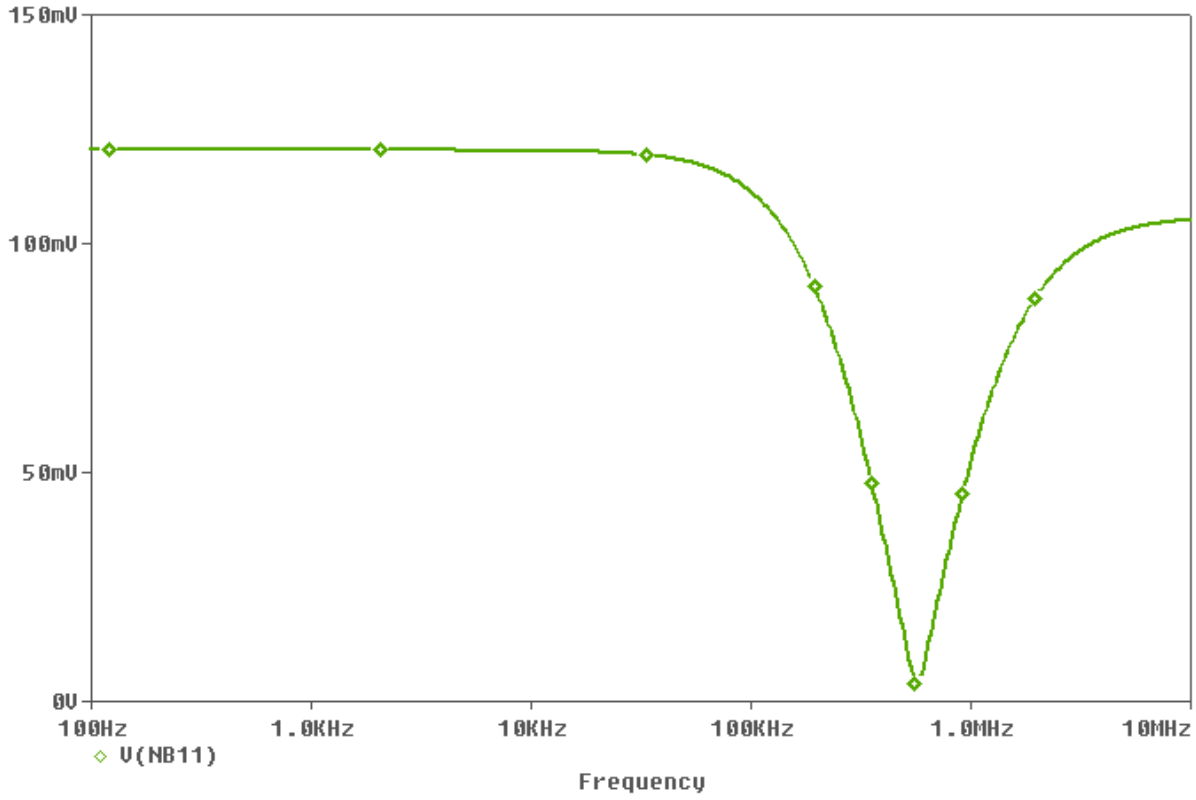


Fig. 4.11(c) Frequency response of grounded LC series

4.3.4 LC parallel in Capacitor in grounded fashion

For simulation we take L = 1mH and C = 200pf and R = R_X =1454.3Ω. The value of capacitor used in its wave equivalent is C_{2d}=L/R^2 = 945.63pf and C_1 = C/2 = 100pf.

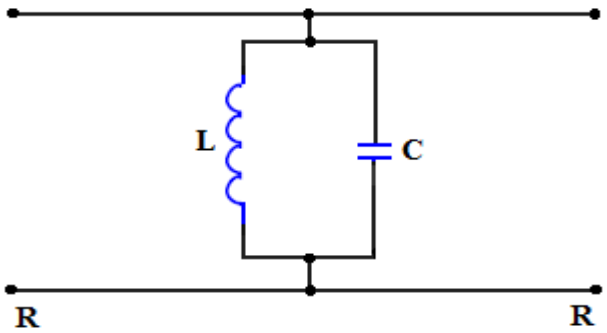


Fig. 4.12(a) two port network of grounded LC parallel

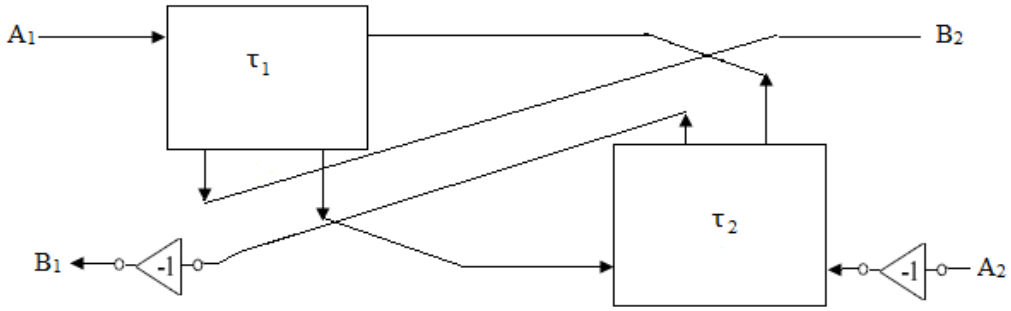


Fig. 4.12(b) wave equivalent of grounded LC parallel

The frequency response of grounded LC parallel is band pass as shown in Fig. 4.12(c)

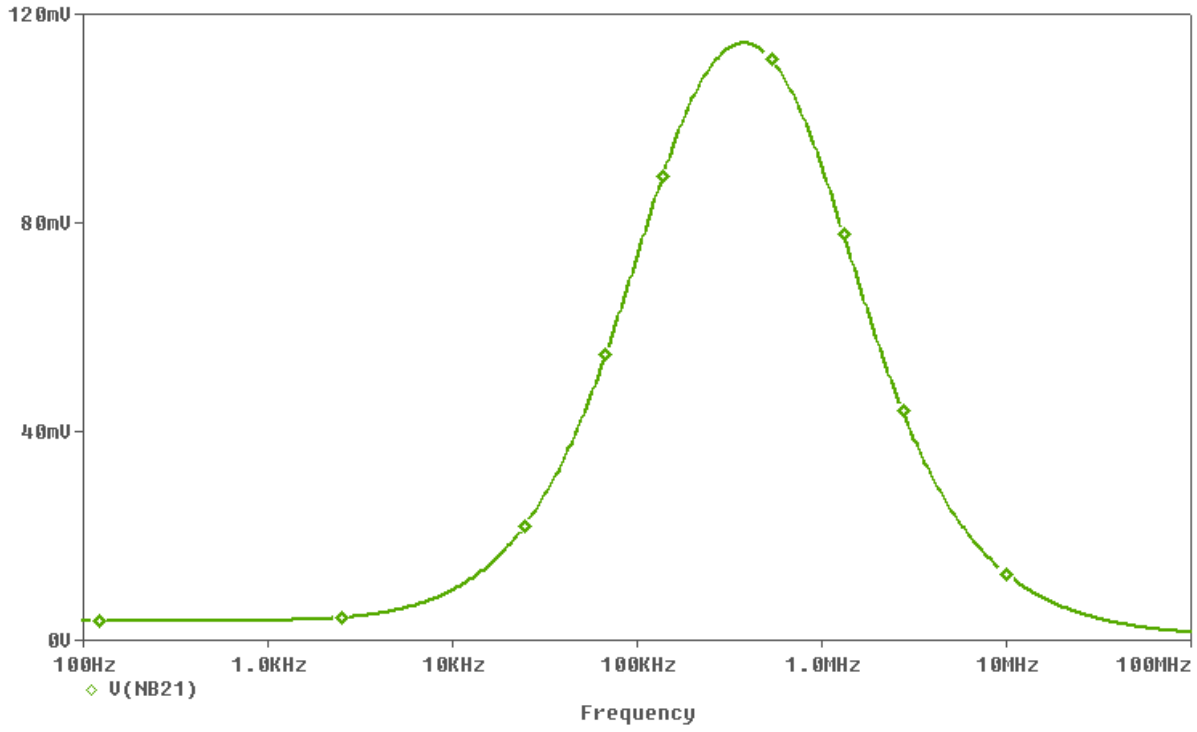


Fig. 4.12(c) Frequency response of grounded LC parallel

4.4 Realization of 4th order filter using wave active method

To demonstrate the wave active filter described in chapter 3, a fourth order low pass butterworth filter of Fig. 4.13 has been taken as prototype. The normalized component values are R_s = 1, L_1 = .7654, L_2 = 1.8485, C_1 = 1.8485, C_2 = .7654and R_L = 1 for maximally flat response. The wave equivalent topology of Fig. 4.13 may be constructed by replacing series inductor and shunt capacitor by wave equivalent of Table 1 and table 2 and is shown in Fig. 4.14. For cut-off frequency f_o = 200 KHz, the bias currents I_{B1} and I_{B2} are taken as 25µA and 200µA respectively. The capacitor values for wave equivalent of series inductors (L_1, L_2) and shunt capacitors (C_1, C_2) are 209.4 pF, 505.67 pF and 505.67 pF, 209.4 pF respectively. The topology of Fig. 4.13 has been simulated using DVCCCTA based wave equivalent and inverter as discussed in section 4.2 and 4.3 using 0.25µm TSMC CMOS technology parameters and power supply of ±1.25V. Fig. 4.15 and 4.16 show the simulated low pass responses (V_{out}) and its complementary high pass response ($V_{out,c}$) respectively. The achieved cut-off frequency is 213KHz. The tunability of the filter response by varying bias current I_{B1} from 25 µA to 35 µA and I_{B2} from 200 µA to 280 µA (I_{B2}= 8I_{B1} for g_mR_x=1) is also studied through simulations and the results are shown in Fig. 4.17.

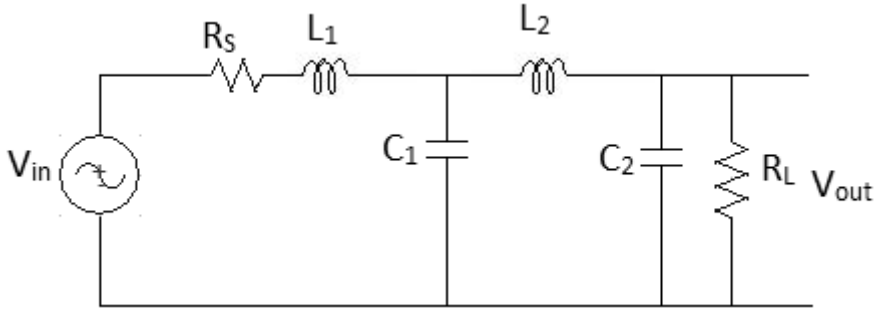


Fig. 4.13 4th order low pass butterworth filter

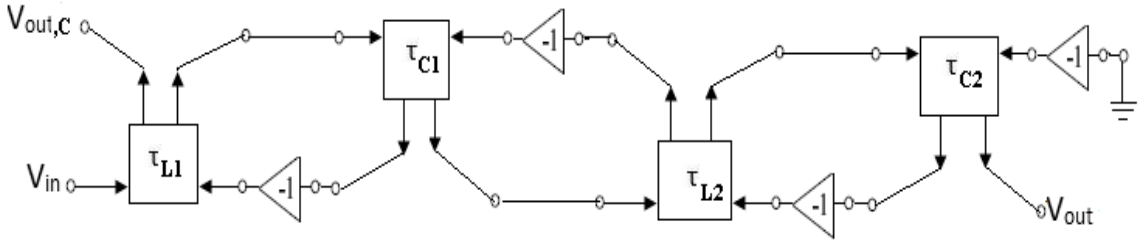


Fig. 4.14 Wave equivalent of 4th order low pass butterworth filter

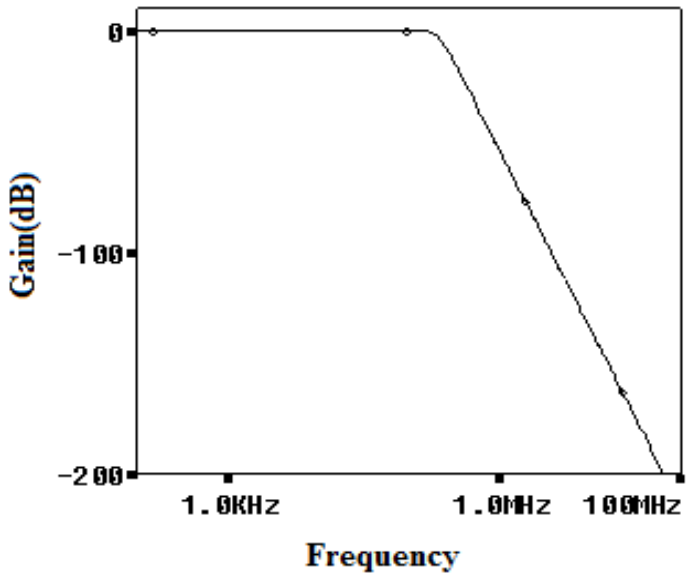


Fig. 4.15 low pass response of 4th order filter

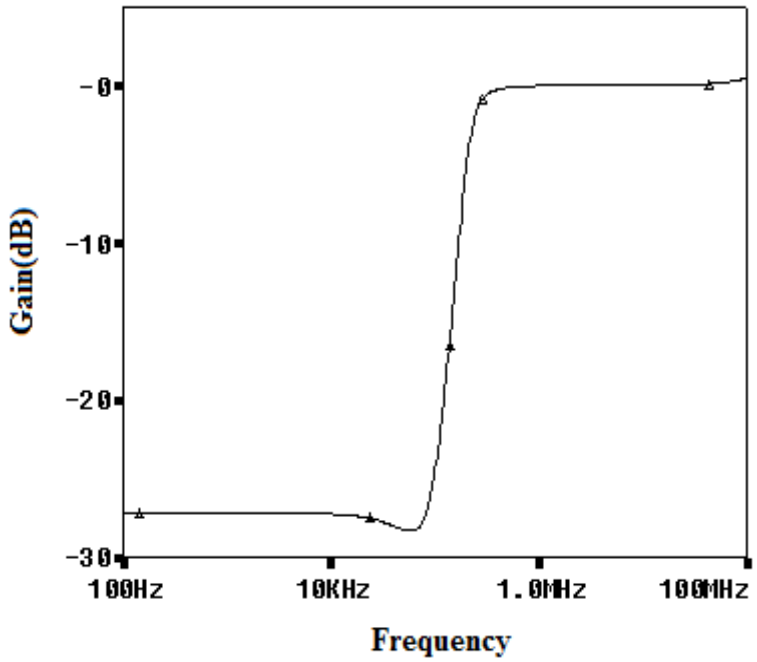


Fig. 4.16 complementary high pass response of 4th order filter

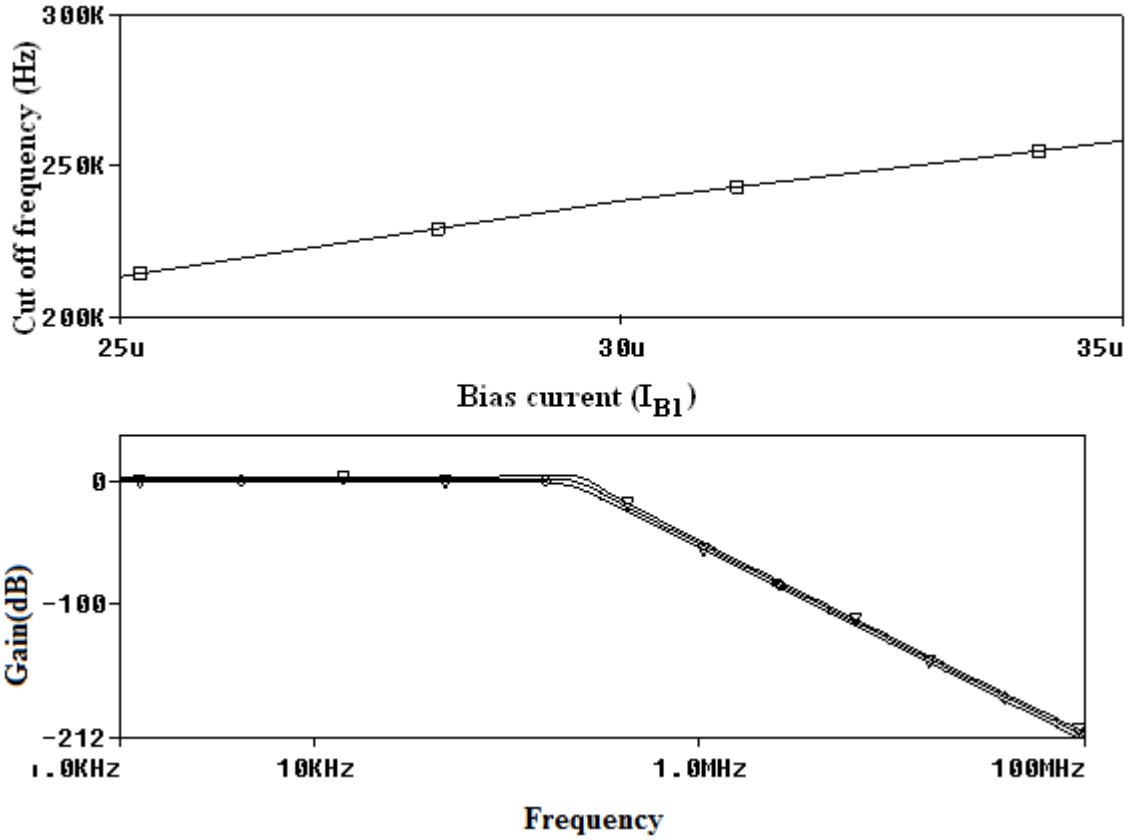


Fig. 4.17 Demonstration of electronic tunability of 4th order low pass filter

Chapter 5

Operational Simulation of LC Ladder Filter

5.1 Introduction

The operational simulation method takes a different approach than topological simulation or wave active method, as in this approach we simulate operation of ladder rather than its component [21]. The circuit equations and voltage- current relationship of each element are written. Then these equations are represented by block diagrams or signal flow graph. Each block represents some analog operation, such as summation, integration etc.

The process of simulating the operation of LC ladder is best explained by the following example from which the general design procedure become clear.

5.2 Operational simulation of 4th order low pass filter

To clarify the previous statement, consider the 4th order low pass filter as shown in Fig. 5.1

Apply Kirchhoff‟s law in his circuit

$$V_1 = V_{in} - V_2 \qquad V_3 = V_2 - V_O \tag{5.1}$$

$$I_2 = I_1 - I_3 \qquad I_4 = I_3 - I_5 = I_3 \tag{5.2}$$

Here we assumed that $I_5 = 0$

The V-I relationship for the series and shunt branch for the ladder

$$I_1 = \frac{V_1}{sL_1 + R_S} \qquad I_3 = \frac{V_3}{sL_2} \tag{5.3}$$

$$V_2 = \frac{I_2}{sC_1} \qquad V_O = \frac{I_4}{sC_2 + G_L} \tag{5.4}$$

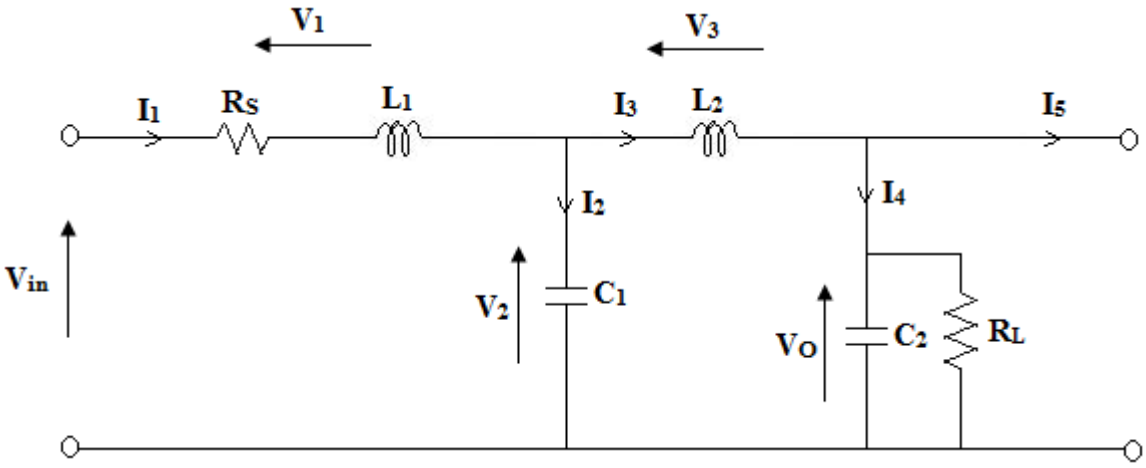


Fig. 5.1 4th order low pass butterworth filter

To simulate the equations from (5.1) to (5.4), we need the circuit which perform the differences of two voltage or currents, and those that perform the lossy and lossless integration. If we take these circuits and connect them appropriately, all the equation will be realized and the resulting structure will realized the given LC filter.

To develop this process in a mathematical manner so that the results become generally valid, consider the general ladder of Fig. 5.2. The series branch element are labelled by admittance Y_i and the shunt branch by impedance Z_i

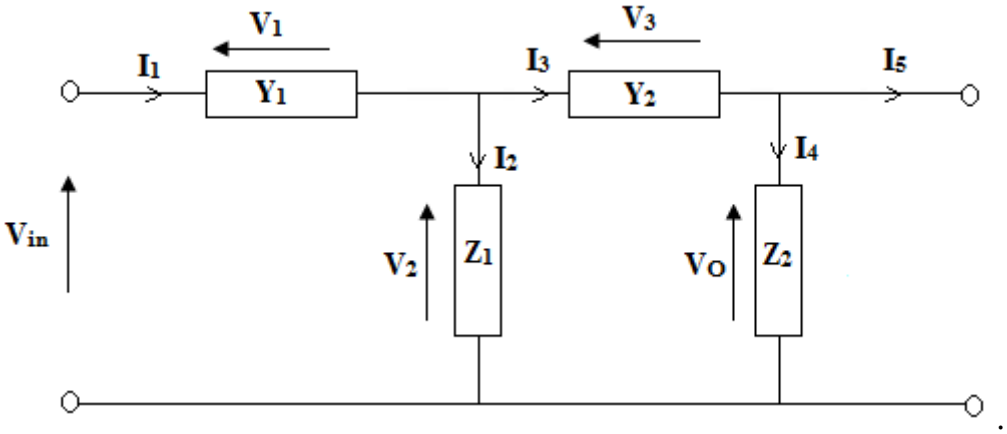


Fig. 5.2 The ladder of Fig. 5.1

The ladder is described by the equations

$$I_1 = Y_1 \left(V_{in} - V_2 \right) \tag{5.5}$$

$$V_2 = Z_1\left(I_1 - I_3\right) \tag{5.6}$$

$$I_3 = Y_2\left(V_2 - V_O\right) \tag{5.7}$$

$$V_O = Z_2\left(I_3 - I_5\right) = Z_2 I_3 \tag{5.8}$$

In the above equations both the voltage and current terms are present. This problem can be solved by scaling the equation by a resistor $R_{p.}$ Then we get the following equations

$$R_P I_1 = R_P Y_1\left(V_{in} - V_2\right) \rightarrow v_{I1} = t_{Y1}\left(V_{in} - V_2\right) \tag{5.9}$$

In the above equation we labelled R_pI_1 by the lower case symbol v_{I1} and retained the subscript to I to indicate that this voltage was derived from a current in a circuit. We labelled all voltage in the normalized circuit by lower-case v. The dimensionless quantity R_pY_1 is labelled by t_{Y1}because it is now transfer function. In the same way we obtain from equation (5.6) to (5.8)

$$V_2 = \frac{Z_1}{R_P}\left(R_P I_1 - R_P I_3\right) \rightarrow V_2 = t_{Z1}\left(v_{I1} - v_{I3}\right) \tag{5.10}$$

$$R_P I_3 = R_P Y_2\left(V_2 - V_O\right) \rightarrow v_{I3} = t_{Y2}\left(V_2 - V_O\right) \tag{5.11}$$

$$V_O = \frac{Z_2}{R_P} R_P I_3 \rightarrow V_O = t_{Z2} v_{I3} \tag{5.12}$$

Where $t_{Y1} = \frac{1}{sL_1 + R_S}$, $t_{Z2} = \frac{1}{sC_1}$, $t_{Y2} = \frac{1}{sL_2}$, $t_{Z2} = \frac{1}{sC_2 + \frac{1}{R_L}}$

To implement the 4th order low pass filter we have to implement the above equations using DVCCCTA.

5.3 Realization using DVCCCTA

To realize the given filter using DVCCCTA we have to realize the equation from (5.9) to (5.12).

To realize equation (5.9) using DVCCCTA, it can be rewritten as

$$v_{I1} = \frac{R_P}{s L_1 + R_S}\left(V_{in} - V_2\right) \quad \text{Or}$$

$$v_{I1} = \frac{1}{s\frac{L_1}{R_P} + \frac{R_S}{R_P}}\left(V_{in} - V_2\right) \tag{5.13}$$

This is an equation of lossy integration. To implement this equation we can use the structure of Fig. 4.1.

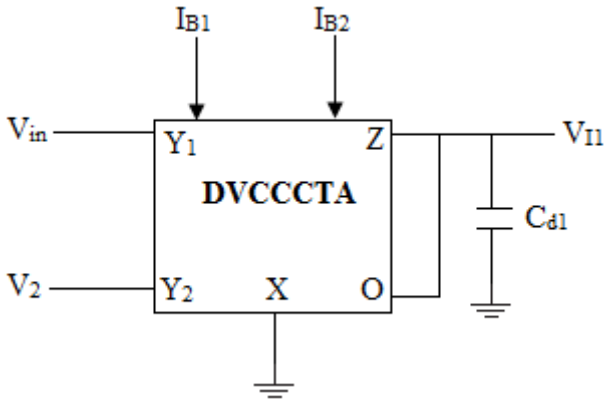


Fig. 5.3 Block diagram of lossy integrator using DVCCCTA

From equation (4.9) its output voltage is

$$v_{I1} = \frac{1}{s\tau + 1}\left(V_{in} - V_2\right) \tag{5.14}$$

On comparing equation (5.13) and (5.14)

$$\frac{R_S}{R_P} = 1 \quad and \quad \tau = R_X C_d = \frac{L_1}{R_P} \tag{5.15}$$

Hence $R_S = R_P$

If we assume $R_S = R_L = R_X$

Then from equation (5.15)

$$R_P = R_X \quad and \quad C_{d1} = \frac{L_1}{R_X{}^2} \tag{5.16}$$

For realizing equation (5.10) using DVCCCTA, it can be rewritten as

$$V_2 = \frac{Z_1}{R_P}\left(v_{I1} - v_{I3}\right) \quad \rightarrow \quad V_2 = \frac{1}{s\,C_1\,R_P}\left(V_{I1} - V_{I3}\right) \tag{5.17}$$

This is an equation of lossless integrator; it can be implemented by the block diagram of Fig. 5.4 as

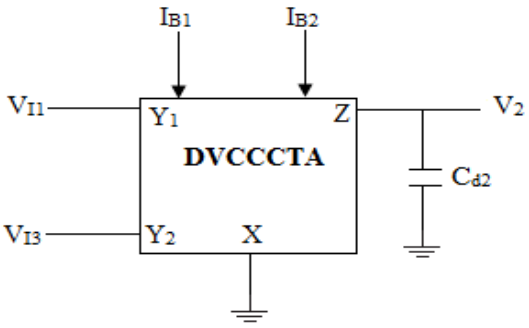


Fig. 5.4 Block diagram lossless integrator sing DVCCCTA

Its output voltage is

$$V_2 = \frac{1}{s\,\tau}\left(V_{I1} - V_{I2}\right) \qquad where \quad \tau = R_X\,C_{d2} \tag{5.18}$$

On comparing equation (5.17) and (5.18)

$$R_X\,C_{d2} = R_P\,C_1 \quad \rightarrow \quad C_{d2} = C_1 \qquad since \quad R_P = R_X \tag{5.19}$$

For the realization of equation (5.11), it can be written as

$$v_{I3} = \frac{R_P}{s\,L_2}\left(V_2 - V_O\right) \quad \rightarrow \quad v_{I3} = \frac{1}{s\,\frac{L_2}{R_P}}\left(V_2 - V_O\right) \tag{5.20}$$

This is again lossless integrator; the block diagram of Fig. 5.4 can be used to implement this equation. Comparing equation (5.17) and (5.20), the value of capacitor can be calculated as

$$C_{d3} = \frac{L_2}{R_X{}^2} \tag{5.21}$$

Similarly to realize equation (5.12) using DVCCCTA, it can be written as

$$V_O = \frac{1}{s C_2 R_P + \frac{R_P}{R_L}} v_{I3} \qquad (5.22)$$

This is lossy integrator, the block diagram of Fig. 5.3 can be used to implement this equation and on comparing equation (5.14) and (5.22), the value of capacitor used in lossless integrator can be calculated as (assuming $R_S = R_L = R_X = R_P$)

$$C_{d4} = C_2 \qquad (5.23)$$

Complete Realization of 4th order low pass filter

The normalized component values of the filter shown in Fig. 5.1, are $R_s = 1$, $L_1 = .7654$, $L_2 = 1.8485$, $C_1 = 1.8485$, $C_2 = .7654$ and $R_L = 1$. For cut-off frequency $f_o = 200$ KHz, the bias currents I_{B1} and I_{B2} are taken as 25µA ($R_X = 1454.3\Omega$) and 200µA respectively.

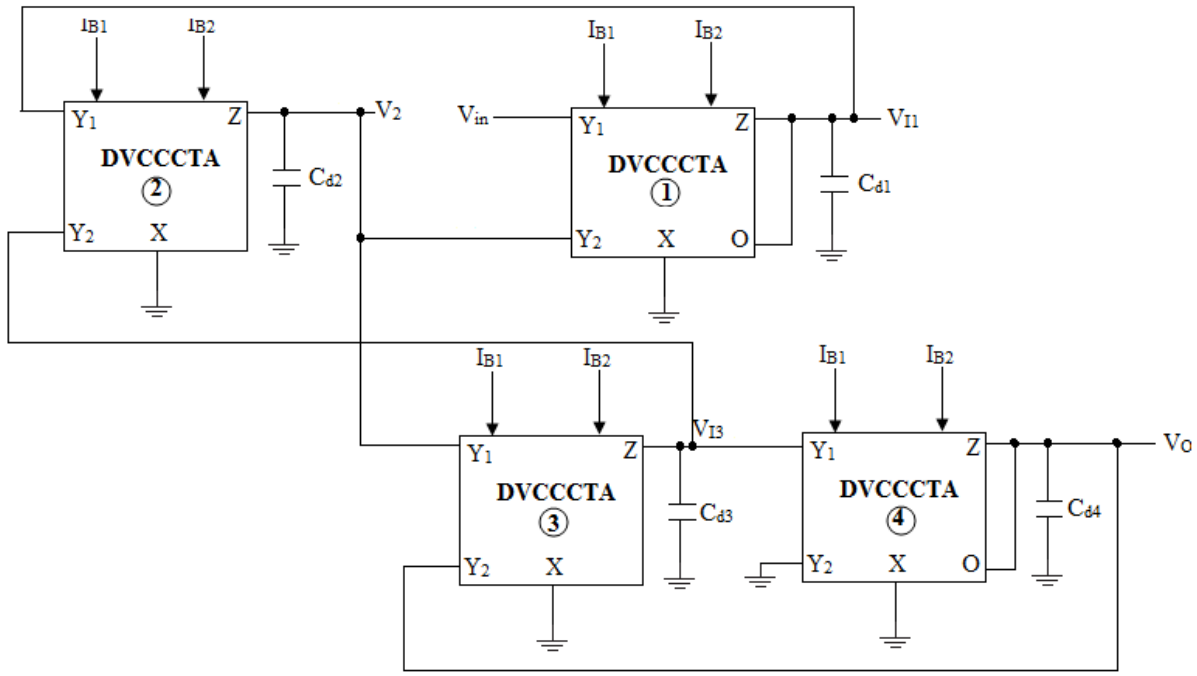


Fig. 5.5 Complete realization of 4th order low pass filter using DVCCCTA

The value of used capacitor in DVCCCTA block can be calculated by the equation (5.16), (5.19), (5.21), (5.23) and the value of C_{d1}, C_{d2}, C_{d3}, C_{d4} are 418.817pf 1011.47pf, 1011.47pf, 418.817pf respectively.

The simulation is carried out through 0.25µm TSMC CMOS technology parameters and power supply of ±1.25V. The low pass filter response is shown in Fig. 5.6. The achieved cut-off frequency is 196.88 KHz.

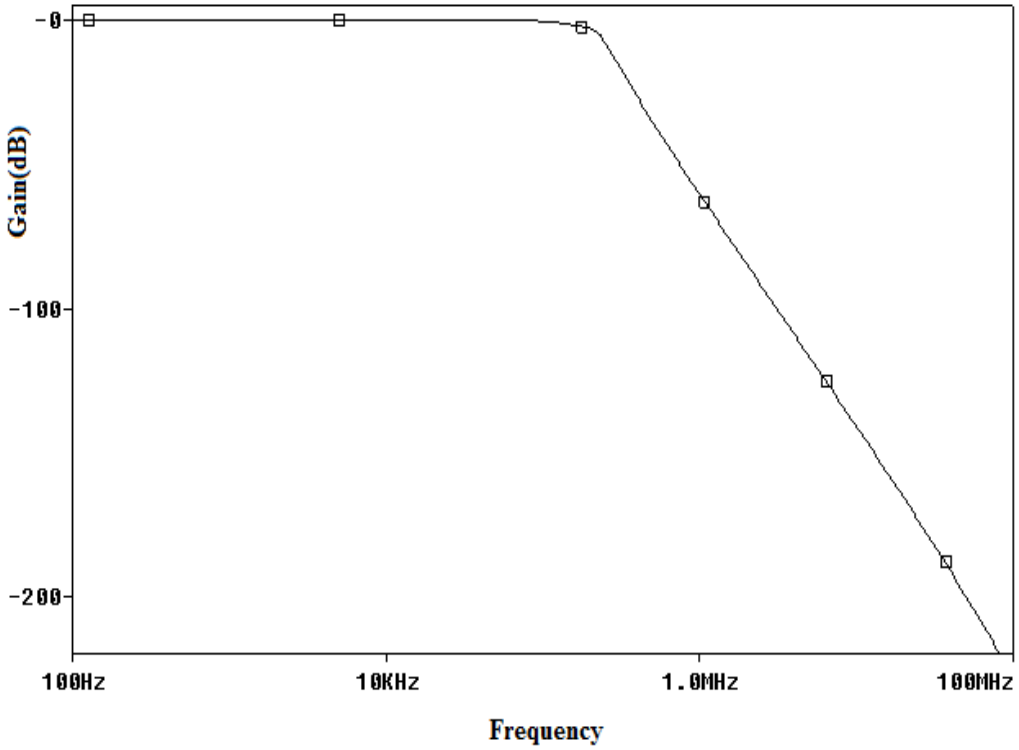


Fig. 5.6 Low pass response of 4th order filter

Chapter 6

Conclusion

In this thesis a detail study of differential voltage current controlled conveyor transconductance amplifier (DVCCCTA) is presented in Chapter 2.

Higher order filters can be easily designed using the wave method and operational simulation (leapfrog) method. DVCCCTA based high order voltage mode filter based on wave method is presented in chapter 4 and based on operational simulation is presented in chapter 5. In wave method DVCCCTA based series inductor wave equivalent is realized as it is basic building block which is then configured for other passive element realization by making appropriate connections. This structure uses grounded capacitors and possesses electronic tunability of cut-off frequency.

The proposed approach is verified for a 4^{th} order low pass filter through SPICE simulation using 0.25µm CMOS technology parameters.

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Appendix-A

Aspect ratio of transistors used in DVCCCTA

Transistors	**Aspect ratio (W(μm)/L(μm))**
M_1, M_4, M_9, M_{11}- M_{15}, M_{30} – M_{31}	3/0.25
M_2, M_3, M_5, M_6	1/0.25
M_7 - M_8, M_{20} – M_{23}, M_{26}, M_{28} – M_{29}	5/0.25
M_{10}	12.5/0.25
M_{16} – M_{17}	8/0.25
M_{18} – M_{19},	5/0.25
M_{24} – M_{25},	5/0.25
M_{27}	4.35/0.25

Appendix-B

.25µm TSMC CMOS Technology Parameter

```
.MODEL NMOS NMOS  (LEVEL = 3

+ TOX = 5.7E-9              NSUB = 1E17             GAMMA = 0.4317311
+ PHI = 0.7                 VTO = 0.4238252         DELTA = 0
+ UO = 425.6466519          ETA = 0                 THETA = 0.1754054
+ KP = 2.501048E-4          VMAX = 8.287851E4       KAPPA = 0.1686779
+ RSH = 4.062439E-3         NFS = 1E12              TPG = 1
+ XJ = 3E-7                 LD = 3.162278E-11       WD = 1.232881E-8
+ CGDO = 6.2E-10            CGSO = 6.2E-10          CGBO = 1E-10
+ CJ = 1.81211E-3           PB = 0.5                MJ = 0.3282553
+ CJSW = 5.341337E-10       MJSW = 0.5 )

.MODEL PMOS PMOS (LEVEL = 3
+ TOX = 5.7E-9              NSUB = 1E17             GAMMA = 0.6348369
+ PHI = 0.7                 VTO = -0.5536085        DELTA = 0
+ UO = 250                  ETA = 0                 THETA = 0.1573195
+ KP = 5.194153E-5          VMAX = 2.295325E5       KAPPA = 0.7448494
+ RSH = 30.0776952          NFS = 1E12              TPG = -1
+ XJ = 2E-7                 LD = 9.968346E-13       WD = 5.475113E-9
+ CGDO = 6.66E-10           CGSO = 6.66E-10         CGBO = 1E-10
+ CJ = 1.893569E-3          PB = 0.9906013          MJ = 0.4664287
+ CJSW = 3.625544E-10       MJSW = 0.5 )
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