

A
Dissertation
On

**STUDY AND IMPLEMENTATION OF DIFFERENTIAL
VOLTAGE CURRENT CONTROLLED CONVEYOR
TRANSCONDUCTANCE AMPLIFIER BASED FILTERS**

Submitted in Partial fulfillment of the requirement
For the award of Degree of

**MASTER OF TECHNOLOGY
(VLSI DESIGN & EMBEDDED SYSTEM)**

Submitted By:

PRAVEEN KUMAR

University Roll No: 15/VLSI/09

Under the Guidance of:

Dr. NEETA PANDEY

(ASSISTANT PROFESSOR)

Department of Electronics & Communication Engineering
Delhi Technological University, Delhi.



**DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
DELHI TECHNOLOGICAL UNIVERSITY
(FORMERLY DELHI COLLEGE OF ENGINEERING)
2009-2011**

DELHI TECHNOLOGICAL UNIVERSITY, DELHI

Department of Electronics & Communication Engineering



CERTIFICATE

This is certified that the dissertation entitled “**Study and Implementation of Differential Voltage Current Controlled Conveyor Transconductance Amplifier based Filters**” is a work of **Praveen Kumar** (University Roll No. 15/VLSI/09), a student of Delhi Technological University. This work was completed under my direct supervision and guidance and forms a part of the Master of Technology (VLSI Design and Embedded System) course and curriculum. He has completed his work with utmost sincerity and diligence.

The work embodied in this major project has not been submitted for the award of any other degree to the best of my knowledge.

Dr. Neeta Pandey
Assistant Professor
ECE department
Delhi Technological University
Delhi-110042

ACKNOWLEDGEMENT

It is distinct pleasure to express my deep sense of gratitude and indebtedness to my project guide **Dr. Neeta Pandey**, Assistant Professor, Department of Electronics and communication Engineering, Delhi Technological University, for her invaluable guidance, encouragement and patient reviews. Her continuous inspiration only has made me complete this dissertation. Without her help and guidance, this dissertation would have been impossible. She remained a pillar of help throughout the project.

I am deeply thankful to **Prof. Rajiv Kapoor**, H.O.D., Electronics and Communication Engineering and **Prof. Asok Bhattacharyya** (former H.O.D.) for their motivation and inspiration, at the same time I am very thankful to the entire faculty and staff members of Electronics & Communication Engineering Department for their direct or indirect help, cooperation, love and affection.

I wish to express thanks to *Mrs. Kirti Gupta* and all persons, who with their encouraging, caring words, constructive criticism and suggestions have contributed directly or indirectly in a significant way towards completion of this work. I gratefully acknowledge for the best wishes and prayers of all my friends. .

At last, I am grateful to my parents and my wife *Mrs. Neha* for their moral support all the time. They have been always around to cheer me up in the odd times of this work.

Praveen Kumar
(15/VLSI/09)

ABSTRACT

In this thesis differential voltage current controlled conveyor transconductance amplifier (DVCCCCTA), a current mode building block and its application as higher order voltage mode filter has been studied. The higher order filter may be realized using operational simulation (or leapfrog approach), topological simulation or wave active method. A detailed discussion of wave active method and operational simulation method has been given. The wave method is used for simulating reflected and incident wave for basic building block i.e. series inductor and configuring it for other passive element realization by making appropriate connection. DVCCCCTA gives the resistorless realization of wave active filter and leap-frog filter. This structure also possesses electronic tunability of cutoff frequency. A 4th order lowpass filters has been realized using DVCCCCTA based wave equivalents and its performance is evaluated through SPICE simulations using 0.25 μ m TSMC CMOS technology parameters.

TABLE OF CONTENTS

	<i>Page No.</i>
Chapter 1: Introduction	1-3
Chapter 2: DVCCCTA: Current Mode Building Block	4-18
2.1 Differential Voltage Current Conveyor	4
2.2 Translinear loop	6
2.3 Transconductance Amplifier	8
2.4 DVCCCTA	9
2.4.1 Simulation for the Verification of port relationship	11
Chapter 3: Wave Active Filter	18-23
3.1 Introduction	18
3.2 Wave Active Filter	19
Chapter 4: Realization of Wave Active Filter using DVCCCTA	24-45
4.1 Basic Wave Equivalent (Series Inductor)	24
4.1.1 Lossy Integration Subtraction	25
4.1.2 Subtraction	26
4.1.3 Summation	27
4.1.4 Complete realization of series Inductor	27
4.2 Wave equivalent of two port sub network in series branch	31
4.2.1 Inductor in series branch	31
4.2.2 Capacitor in series branch	32
4.2.3 LC series in floating fashion	33
4.2.4 LC parallel in floating fashion	35
4.3 Wave equivalent of two port network in shunt branch	32
4.3.1 Inductor in shunt branch	37

4.3.2 Capacitor in shunt branch	38
4.3.3 LC series in grounded fashion	39
4.3.4 LC parallel in grounded fashion	41
4.4 Realization of 4 th order filter using Wave Active method	43
Chapter 5: Operational Simulation of LC Ladder Filter	46-52
5.1 Introduction	46
5.2 Operational Simulation of 4 th order lowpass filter	46
5.3 Realization using DVCCCTA	48
Chapter 6: Conclusion	53
References	54-56
APPENDIX	57-58

LIST OF FIGURES

<i>S.No.</i>	<i>Title</i>	<i>Page No.</i>
Table 1	Wave equivalent of elementary two port consisting of series branch element	29
Table 2	Wave equivalent of elementary two ports consisting of series shunt element	30
Figure 2.1	Block diagram of DVCC	5
Figure 2.2	CMOS Implementation of DVCC	6
Figure 2.3	Class AB Translinear loop	7
Figure 2.4	Block diagram of Transconductance Amplifier	8
Figure 2.5	CMOS Implementation of Transconductance Amplifier	9
Figure 2.6	Block diagram of DVCCCTA	9
Figure 2.7	CMOS Implementation of DVCCCTA	10
Figure 2.8	Simulated port relationship $V_x = V_{Y1} - V_{Y2} + I_x R_x$ in DC analysis	11
Figure 2.9	Simulated port relationship $I_z = I_x$ in DC analysis	12
Figure 2.10	Simulated port relationship $I_o = -g_m V_z$ in DC analysis	12
Figure 2.11	Simulated port relationship $V_x = V_{Y1} - V_{Y2} + I_x R_x$ in AC analysis	13
Figure 2.12	Simulated port relationship $I_z = I_x$ in AC analysis	13
Figure 2.13	Simulated port relationship $I_o = -g_m V_z$ in AC analysis	14
Figure 2.14	Frequency response of parasitic Resistance of DVCCCTA	14
Figure 2.15	Frequency response of transconductance of DVCCCTA	15
Figure 2.16	Graph for calculation of β_1	16
Figure 2.17	Graph for calculation of β_2	16
Figure 2.18	Graph for calculation of parasitic at Z terminal	17
Figure 2.19	Graph for calculation of parasitic at O terminal	17
Figure 3.1	Two port network	20

Figure 4.1	Block diagram of lossy integration subtraction using DVCCCTA	25
Figure 4.2	Block diagram of Subtraction using DVCCCTA	27
Figure 4.3	Block diagram of Summation using DVCCCTA	27
Figure 4.4(a),(b)	Complete schematic and wave equivalent of series Inductor	28
Figure 4.5(a)	Two port network of floating Inductor	31
Figure 4.5(b)	Wave equivalent of floating Inductor	31
Figure 4.5(c)	Frequency response of floating inductor	32
Figure 4.6(a)	Two port network of floating Capacitor	32
Figure 4.6(b)	Wave equivalent of floating Capacitor	33
Figure 4.6(c)	Frequency response floating Capacitor	33
Figure 4.7(a)	Two port network of floating LC series	34
Figure 4.7(b)	Wave equivalent of floating LC series	34
Figure 4.7(c)	Frequency response of floating LC series	35
Figure 4.8(a)	Two port network of floating LC parallel	35
Figure 4.8(b)	Wave equivalent of floating LC parallel	36
Figure 4.8(c)	Frequency response of floating LC parallel	36
Figure 4.9(a)	Two port network of grounded Inductor	37
Figure 4.9(b)	Wave equivalent of grounded Inductor	37
Figure 4.9(c)	Frequency response of grounded inductor	38
Figure 4.10(a)	Two port network of grounded Capacitor	38
Figure 4.10(b)	Wave equivalent of grounded Capacitor	39
Figure 4.10(c)	Frequency response of grounded Capacitor	39
Figure 4.11(a)	Two port network of grounded LC series	40
Figure 4.11(b)	Wave equivalent of grounded LC series	40
Figure 4.11(c)	Frequency response of grounded LC series	41
Figure 4.12(a)	Two port network of grounded LC parallel	41
Figure 4.12(b)	Wave equivalent of grounded LC parallel	42
Figure 4.12(c)	Frequency response of grounded LC parallel	42
Figure 4.13	4 th order low pass butterworth filter	43

Figure 4.14	Wave equivalent of 4 th order low pass butterworth filter	43
Figure 4.15	Low response of low pass filter	44
Figure 4.16	Complementary high pass response of 4 th order filter	44
Figure 4.17	Demonstration of electronic tunability of low pass response	45
Figure 5.1	4 th order low pass butterworth filter	47
Figure 5.2	The ladder of fig.5.1	47
Figure 5.3	Block diagram of lossy Integrator using DVCCCTA	49
Figure 5.4	Block diagram of lossless Integrator DVCCCTA	50
Figure 5.5	Complete realization of 4 th order low pass filter using DVCCCTA	51
Figure 5.6	Low pass response of 4 th order filter	52