A Major Project Report submitted in partial fulfillment for the requirement of the degree of

Masters of Engineering

In

Electronics and Communication Engineering

Titled

Improving Signal Processing in ADCs

By-

Veepsa Bhatia

13/E&C/02

Univ. Roll. No. 4071

Guided By-

Prof. (Dr.) A. Bhattacharyya

Head, Department of Electronics and Communication Engineering

Delhi College of Engineering

Delhi University

Certificate

Certified that for Major Project work titled **"Improving Signal Processing in ADCs"** which is submitted by **Ms. Veepsa Bhatia** in partial fulfillment of the requirement for the award of degree of **Masters of Engineering** of University of Delhi is a record of the student's own work for the collection of information and was carried out by her under my supervision and guidance at this institution.

Prof. Dr. A. Bhattacharyya
H.O.D., Electronics & Communication Department
Delhi College of Engineering, Delhi

Acknowledgement

The author wishes to express sincere appreciation of the guidance given by the guide of the project Dr. A. Bhattacharyya, H.O.D., Dept. of Electronics and Communication Engineering, Delhi College of Engineering, without whose invaluable guidance and support this project would not have been successfully completed. The author would further express heartfelt gratitude to colleague and mentor Mrs. Neeta Pandey, Assistant Professor, Bharati Vidyapeeth's College of Engineering, for her continuous help and guidance. The author would further like to thank all the faculty members and lab technicians of Dept. of Electronics and Communication Engineering, Delhi College of Engineering for their support from time to time.

Veepsa Bhatia

Table of Contents

Abstract

A current-mode technique for the design of algorithmic ADCs is presented. The current mode technique allows the necessary voltage swing for a given dynamic range to be reduced while at the same time eliminating the need of large capacitors on which to store charge. Consequently the resulting ADC can be made very small and yet still capable of providing high sampling rates. In this thesis the advantages and disadvantages of various current mirror structures used in the ADCs are discussed. Also, the ADCs have been implemented by using different current comparators.

For the current-mode ADC, the algorithmic ADC was selected because presently this style of converter occupies the smallest amount of silicon chip area. This architecture also takes the advantage of relatively simple hardware to produce either a Gray-code output or a binary-code output.

Chapter 1: Introduction

The growth of analog IC design has been impeded by the process technologies which are mostly optimized for digital applications only. With the evolution of sub-micron technologies such as 0.18 micron and 0.13 micron, the supply voltages have been reduced to 3.3 Volts and lower. This makes it difficult to design a voltage mode CMOS circuits with high linearity and dynamic range. Recently, current mode circuits have become a viable alternative for future applications because of their inherent advantages over voltage mode circuits.

The main advantage of using current mode technique is because the non-linear characteristics exhibited by most field effect transistors. A small change in the input or controlling voltage results in a much larger change in the input or the controlling voltage results in a much larger change in the output current. Thus for a fixed supply voltage, the dynamic range of a current mode circuit is much larger than that of a voltage mode circuit. If a supply voltage is lowered, one can still get the required signals represented by the current.

A second disadvantage of current mode circuits is that they are much faster as compared to voltage mode circuits. The parasitic capacitances present in the analog circuits must be charged and discharged with the changing voltage levels. In a current mode circuits, a change in current level is not necessarily accompanied by a change in the voltage level. Hence, the parasitic capacitances will not affect the operating speed of the circuit by a significant amount.

Other advantages of using current mode circuits are that they do not require specially processed capacitors or resistors; they are more compatible with digital CMOS technology making integration of mixed signal circuits more feasible.

Chapter 2: ANALOG TO DIGITAL CONVERTERS

An analog-to-digital converter takes an analog input voltage and after a certain amount of time, produces a digital output code, which represents the analog output.

Fig. 21 shows the general block diagram of an analog-to-digital converter. Many analog-to-digital converters require a digital -to- analog converter as a part of their circuitry.

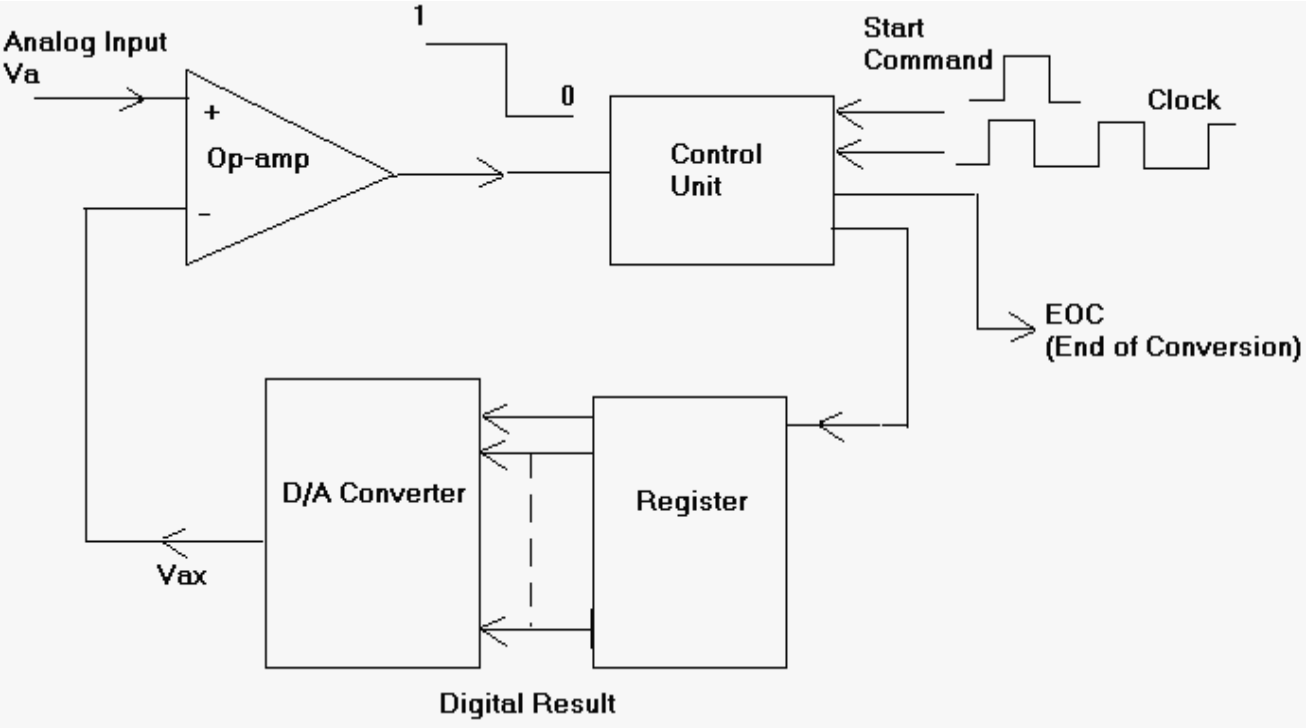


Fig. 2.1 General Block Diagram of an A/D converter

The input clock provides the timing for the operation. The Control Unit contains the logic circuitry for generating the proper sequence of operations in response to the START command, which initiates the conversion process.

The op-amp comparator has two analog inputs and a digital output that switches states depending on which analog input is greater.

The basic operation of the A/D converter of this type consists of the following steps-

1. The START command pulse initiates the operation.
2. At a rate determined by the clock, the control unit continuously modifies the binary number stored in the register.
3. The binary number in the register is converted to an analog voltage V_{AX} by the D/A converter.
4. The comparator compares V_{AX} with analog input V_A. As long as $V_{AX} < V_A$, the comparator output stays HIGH. When $V_{AX} > V_A$ by at least an amount equal to V_T (threshold voltage), the comparator output goes LOW and stops the process of modifying the register number. At this point, V_{AX} is a close approximation to V_A. The digital number in the register, which is the digital equivalent of V_{AX} is also the approximate digital equivalent of V_A, within the resolution and accuracy of the system.
5. The control logic activates the end-of-conversion signal, EOC, when the conversion is complete.

The several variations of this A/D conversion scheme differ mainly in the manner in which the control section continually modifies the number in the

register. Otherwise the basic idea is the same, with the register holding the required digital output when the conversion process is complete.

2.1 Characteristics of A/D Converters

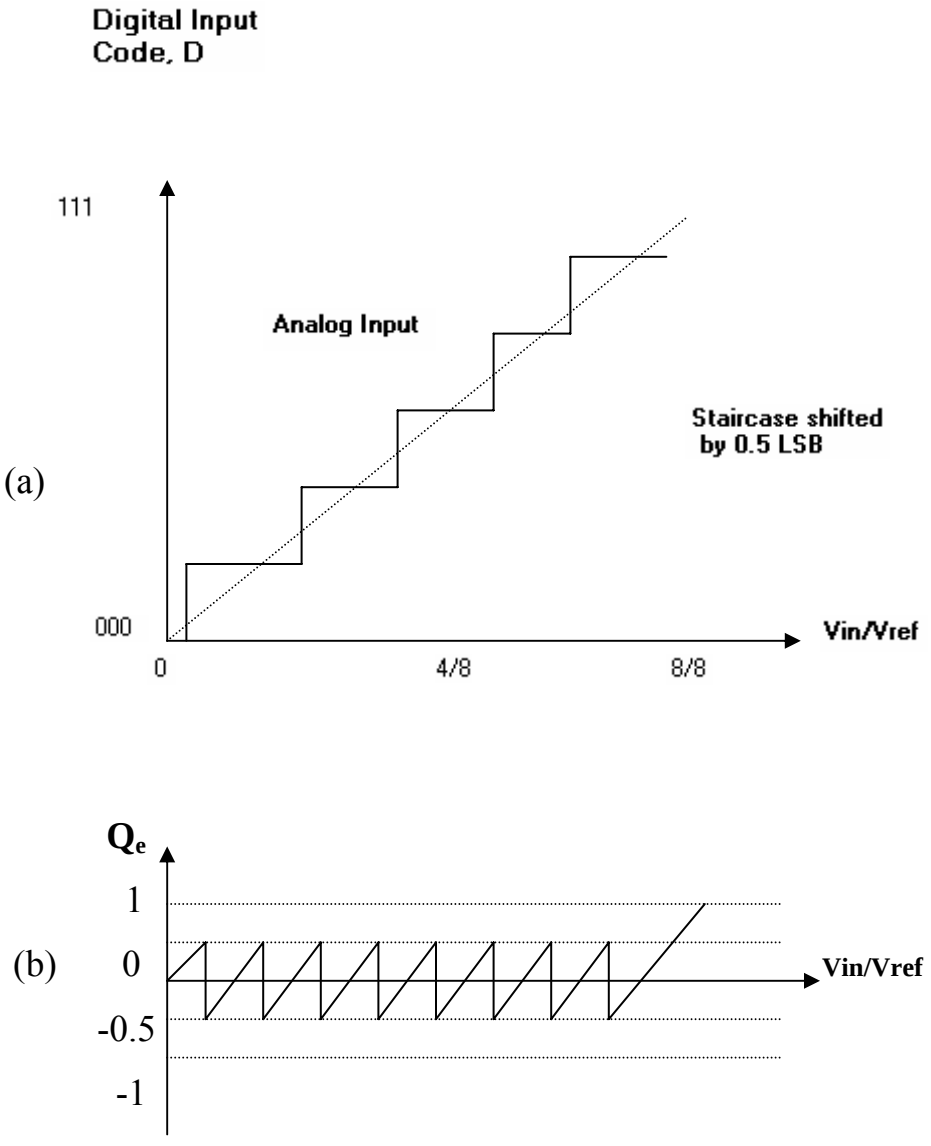


Fig.2.2 (a) Transfer curve for an ideal 3-bit A/D Converter with (b) quantization error centered about zero.

Fig.2.2 shows the digital output D of a 3-bit A/D converter plotted against the analog input V_{in}. Since the input signal is a continuous signal and the output is discrete, the transfer curve of the A/D converter resembles that of a staircase. Another fact to observe is that the 2^N quantization levels correspond to the digital output codes 0 to7. Thus, the maximum output of the A/D converter will be 111 (2^N-1), corresponding to the value for which $V_{in}/V_{ref} \geq 7/8$. Fig 2.2(b) corresponds to the error caused by the quantization. The value of 1 LSB for this A/D converter can be calculated using the following equation-

$$1LSB = \frac{V_{REF}}{2^N} \quad (1)$$

Quantization Error

Since the analog input is an infinite valued quantity and the output is a discrete value, an error will be produced as a result of the quantization. This error, known as **quantization error**, Q_e, is defined as **the difference between the actual analog input and the value of the output (staircase) given in voltage.** It is calculated as-

$$Qe = V_{in} - S_{taircase} \quad (2)$$

where the value of the staircase output, $S_{taircase}$ can be calculated by

$$V_{Staircase} = D.\frac{V_{REF}}{2^N} = D.V_{LSB} \quad (3)$$

where D is the value of the digital output code and V_{LSB} is the value of 1LSB in volts.

Differential Nonlinearity (DNL)

Differential nonlinearity for an ADC is the difference between the actual code width of a non-ideal converter and the ideal case. Fig.2.3 shows the transfer curve for a non-ideal 3-bit ADC.

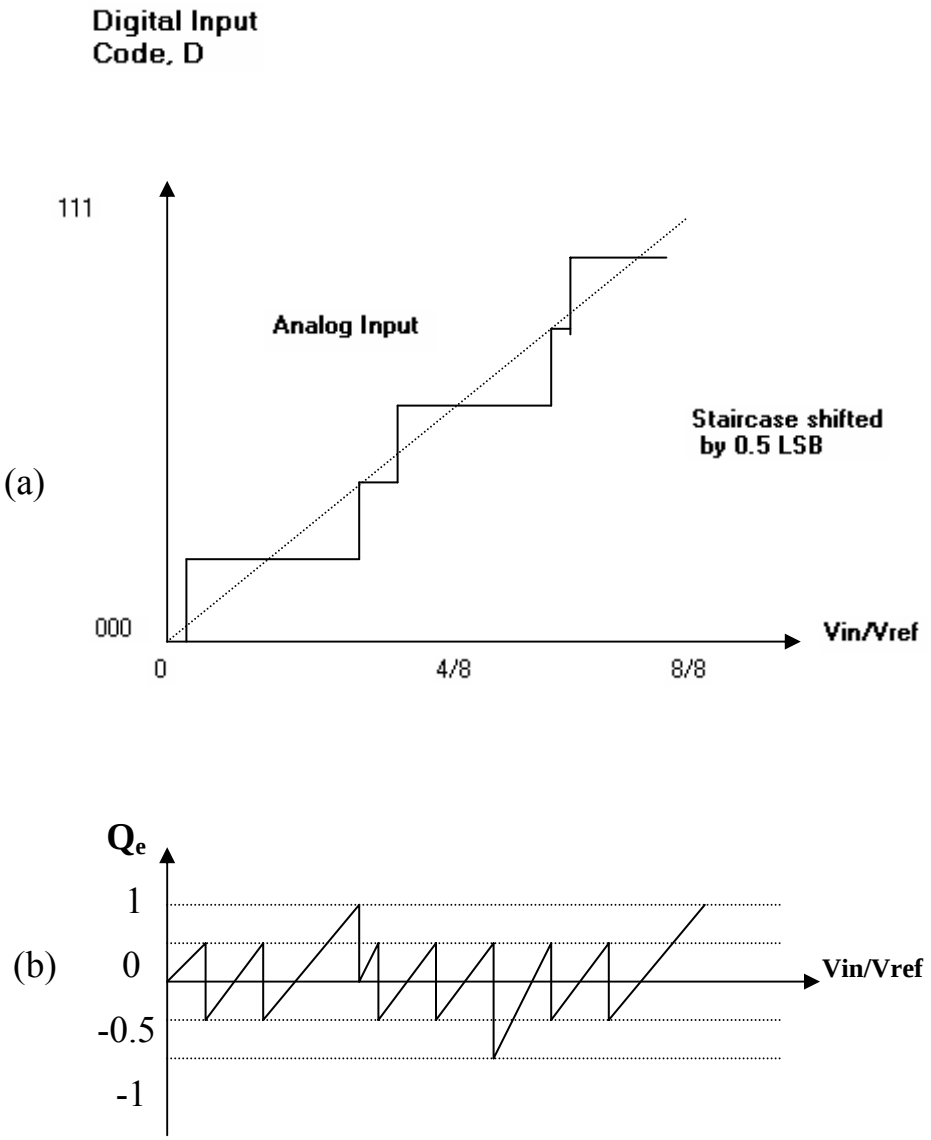


Fig.2.3 (a) Transfer curve for a non-ideal 3-bit A/D Converter with (b) quantization error illustrating differential nonlinearity.

The values for the DNL can be solved as follows-

DNL = Actual step width- Ideal step width. (4)

Since the step widths can be converted into either volts for LSBs, DNL can be defined using either units. The value of ideal step is 1/8.

Integral Nonlinearity (INL)

INL is defined as the difference between data converter output and the reference straight line drawn through the first and last output line. INL defines the linearity of the overall transfer curve and can be defined as-

INL= Output value for input code- Output value of the reference line at that point. (5)

Offset and Gain error

Offset error occurs when there is a difference between the value of first code transition and the ideal value of ½LSB.

Gain error or scale factor error is the difference in the slope of a straight line drawn through the transfer characteristics and the slope of an ideal A/D converter.

Aliasing

The sampling of the input signal should be done at such a rate that is determined by the ***Nyquist Criterion***. Nyquist criterion defines how fast the sampling rate needs to represent an analog signal accurately. This criterion requires that the sampling rate be at least twice the highest frequency contained in the analog signal.

$F_{Sampling} = 2.F_{MAX}$ (6)

where $F_{Sampling}$ is the sampling frequency required to accurately represent the analog signal and F_{MAX} is the highest frequency of the sampled signal.
If the sampling is done at a rate less than that specified by the Nyquist Criterion, a phenomenon called **aliasing** would occur.
Aliasing can be eliminated either by sampling at higher frequencies or by filtering the analog signal before sampling and removing any frequencies that are greater than one half the sampling frequency. A pre-alias filter can be used to eliminate any unknown harmonics that could result in aliasing.

Signal-to-noise Ratio

Signal-to-noise ratios (SNR) of ADCs represent the value of the largest RMS input signal into the converter over the RMS value of the noise. It is expressed as-

$$SNR = 20\log\left(\frac{V_{in(\max)}}{V_{noise}}\right) \tag{7}$$

If it is assumed that the input signal is a sinewave with a peak-to-peak value equal to the full scale reference voltage of the converter, then the RMS value for $V_{in(max)}$ becomes

$$V_{in(\max)} = \frac{V_{REF}}{2\sqrt{2}} = \frac{2^N(V_{LSB})}{2\sqrt{2}} \tag{8}$$

2.2 ADC Architectures

There are five main types of ADC architectures- pipeline, **flash-type**, **pipeline**, **integrating**, **successive approximation**, **oversampled** and **algorithmic** ADCs. Each has benefits that are the unique to that architecture and span the spectrum high speed and resolution.

2.2.1 Flash

Flash or the parallel converters have the highest speed of any type of ADC. They utilize one comparator per quantization level(2^N - 1) and 2^N resistors.

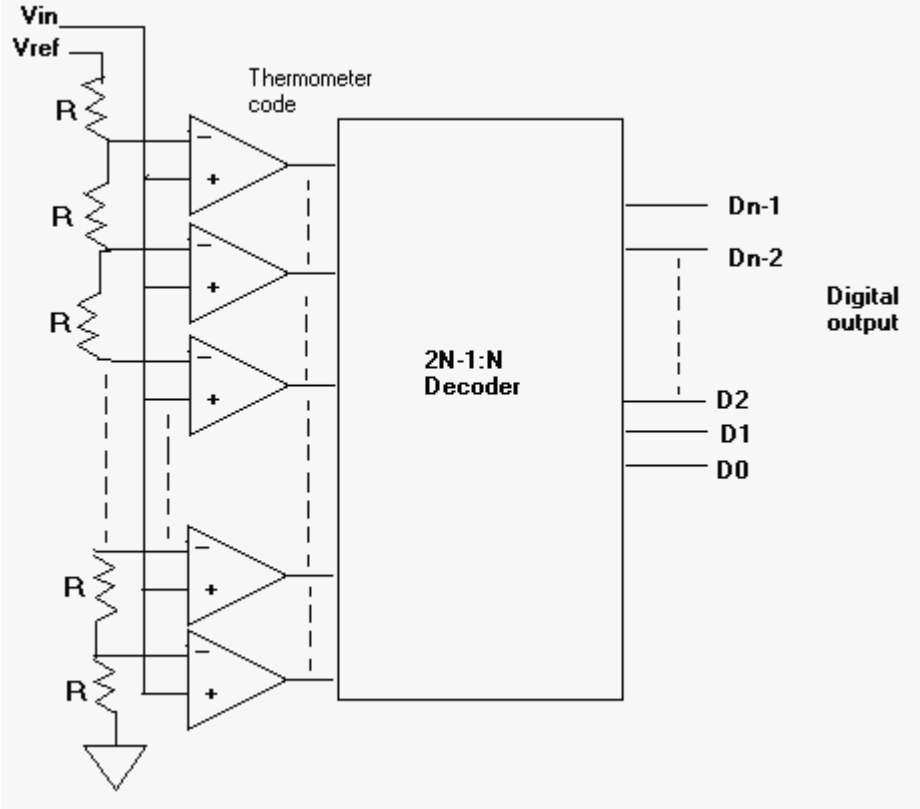


Fig. 2.4 Block Diagram of a Flash ADC

The reference voltage is divided into 2^N values, each of which is fed into comparator. The input voltage is compared with each reference value and results in a thermometer code at the output of the comparators. A thermometer code will exhibit all zeroes for each resistor level if the value of v_{in} is less than the value on resistor string and ones if v_{in} is greater than or equal to voltage on the resistor string. A simple 2^N-1: N digital thermometer decoder circuit coveters the compared data into an N-bit digital word.

The obvious advantage of this circuit is the speed with which one conversion can take place. Each clock pulse generates an output digital word.

The advantage of having high speed is however counterbalanced by the doubling of area with each bit of increased resolution. He disadvantages of Flash ADC are the area and power requirements of the 2^N-1 comparators. The speed is limited by the switching of the comparator and the digital logic.

2.2.2 Pipeline ADC

The pipeline ADC is an N-step converter, with 1-bit being converted per stage. Able to achieve high resolution (10-13 bits) at relatively fast speeds, the pipeline ADC consists of N-stages connected in series.

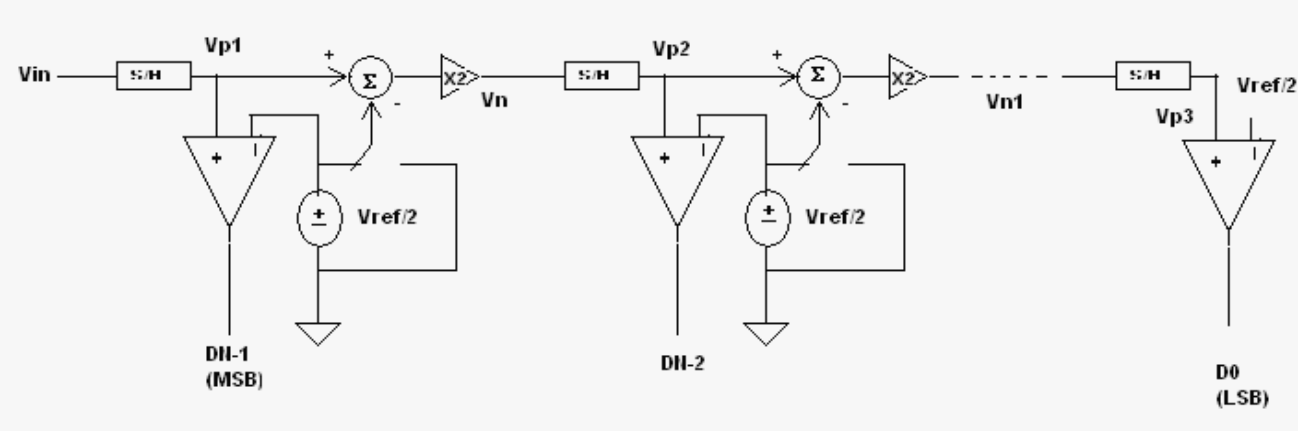


Fig. 2.5 Block diagram of Pipeline ADC

Each stage contains a 1-bit ADC (a comparator), a sample and hold, a summer and a gain of two amplifier.

Each stage of converter performs the following operations-

1. After the input signal has been sampled, it is compared to Vref/2. The output of each comparator is the bit conversion for that stage.
2. If Vin>Vref/2 (comparator output is 1), Vref/2 is subtracted from the held signal and result is passed to the amplifier. If Vin<Vref/2 (comparator output is 0), then the original input signal is passed to the

amplifier. The output of each stage in the converter is referred to as the *residue*.

3. Multiply the result of the summation by 2 and pass the result to the sample and hold of the next stage.

A main advantage of the pipeline converter is its high throughput. After an initial delay of N clock cycles, one conversion will be completed per clock cycle. While the residue of the first stage is being operated on by the second stage, the first stage is free to operate on next samples. Each stage operates on the residue passed down from the previous stage, thereby allowing for fast conversions.

The disadvantage is having initial N clock cycle delay before the first digital output appears. The severity of disadvantage is, of course, dependent on the application.

One interesting aspect of this conversion is its dependency on the most significant stages for accuracy. A slight error in the first stage propagates through the converter and results in a much larger error at the end of the conversion. Each succeeding stage requires less accuracy than the one before, so special care must be taken when considering the first several stages.

2.2.3 Integrating ADCs

Another type of ADC performs the conversion by the input signal and correlating the integrating time with a digital counter. Known as single and dual-slope ADCs, these types of converters are used in high resolution applications but have relatively slow conversions. However, they are very inexpensive to produce and are commonly found in slow-speed, cost conscious applications.

Single-slope Architecture

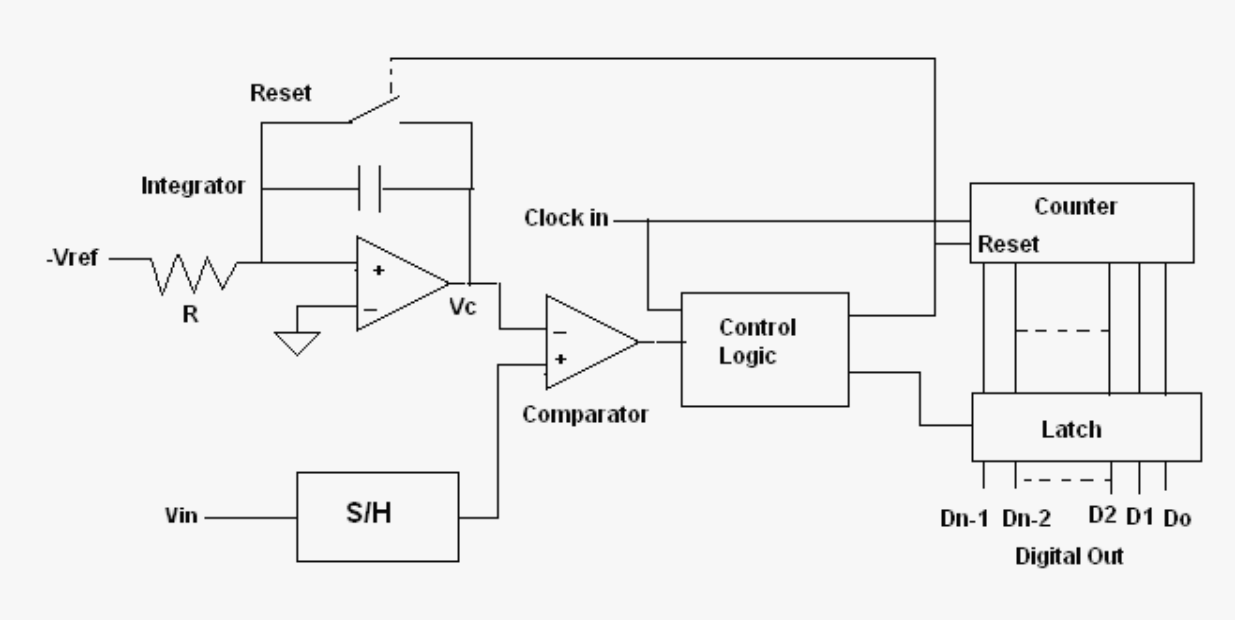


Fig. 2.6 Block diagram of single-slope ADC

Fig. 2.6 shows the single-slope converter in the block diagram form. A counter determines the number of clock pulses that are required before the integrated value of a reference voltage is equal to the sampled input signal. The number of clock pulses is proportional to the actual value of the input, and the output of the counter is the actual digital representation of analog voltage.

Since the reference is a DC voltage, the output of the integrator should start at zero and linearly increase with the slope that is dependent on the gain of the integrator. The reference voltage is defined as negative so that the output of the inverting integrator is positive. At the time when the output of the integrator surpasses the value of S/H output, the comparator switches states, thus triggering the control logic to latch the value of the counter. The control logic also resets the system for the next sample. Fig. 2.7 illustrates the behavior of the integrator output and the clock.

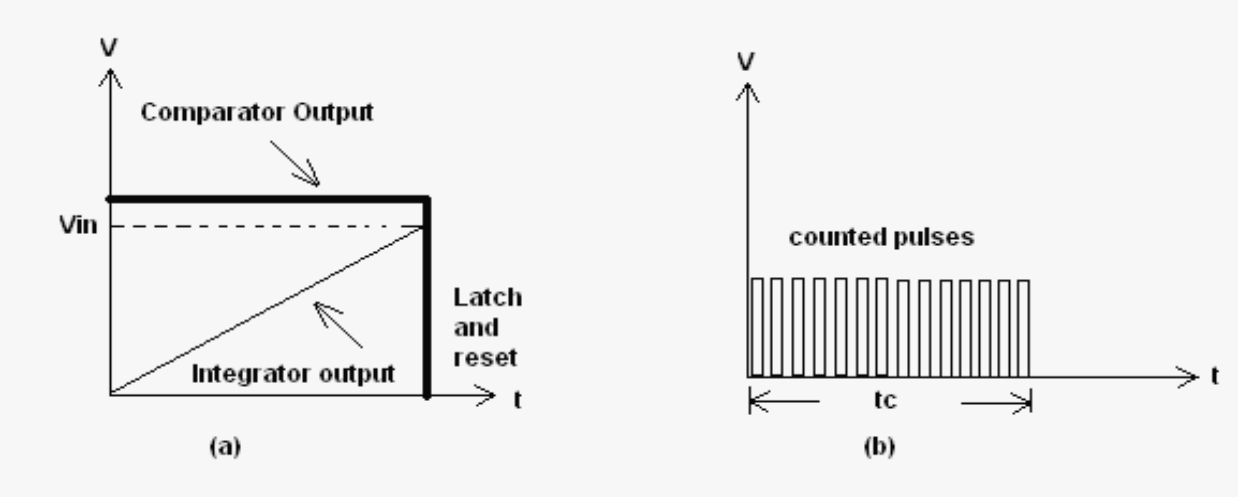


Fig. 2.7 Single slope ADC timing diagrams for (a) the comparator inputs and outputs (b) the resulting counted pulses

If the input voltage is very small, the conversion time is very short, since the counter has to increment only a few times before the comparator latches the data. However, if the input voltage is at its full-scale value, the counter must be many times faster than the bandwidth of the input signal.

The conversion time, t_c, is dependent on the value of the input signal and can be described as

$$tc = \frac{Vin}{Vref} .2^N . Tck$$

where Tck is the period of the clock. The sampling rate is inversely proportional to the conversion time and can be written as

$$fsample = \frac{Vref}{Vin.2^N} . fck$$

Dual-slope Architecture

A slightly more sophisticated design known as the dual-slope integrating ADC shown in Fig. 2.8 eliminates most of the problems encountered when using the single slope converter.

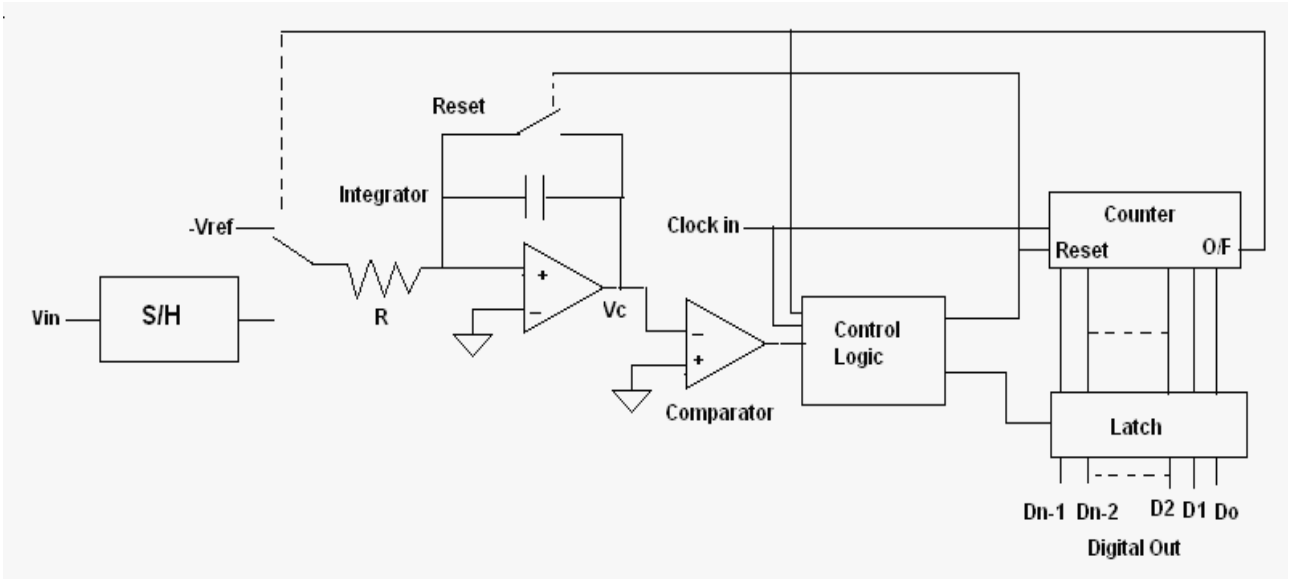


Fig. 2.8 Block diagram of dual-slope ADC

Here two integrations are performed, one on the input signal and one on V_{ref}. the input voltage in this case is assumed to be negative, so that the output of the inverting integrator results in a positive slope during the first integration.

Fig. 2.9 illustrates the behavior for the two separate pulses.

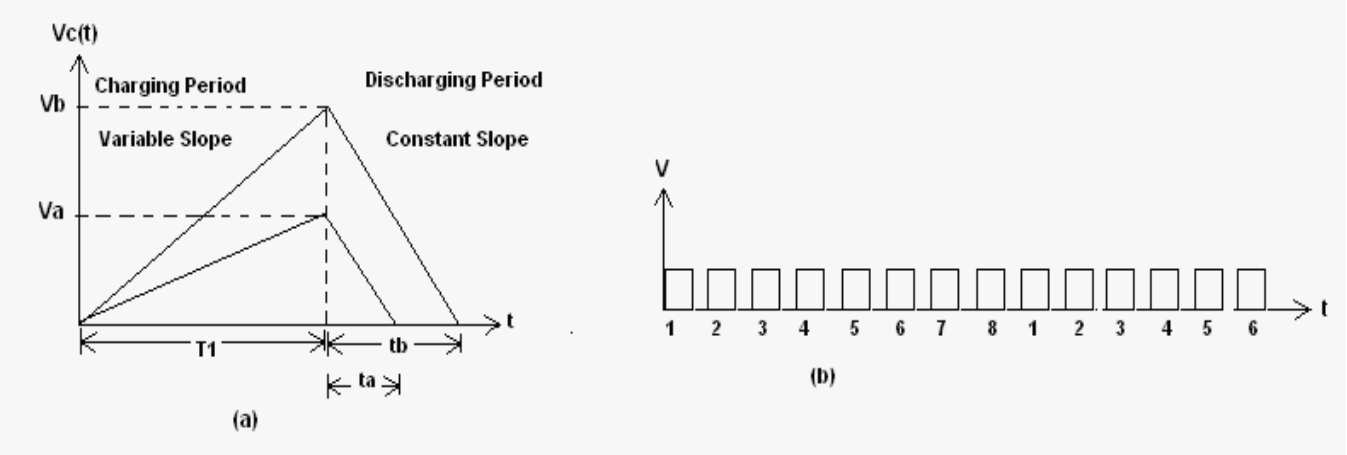


Fig. 2.9 Integrating periods and counter output for two separate samples of a 3-bit dual slope ADC.

The first integration is of fixed length, dictated by the counter, in which the sampled-and-held signal is integrated, resulting in the first slope. After the counter overflows and is reset, the reference voltage is connected to the input of the integrator. Since v_{in} was negative and the reference voltage is positive, the inverting integrator output will begin discharging back down to zero at a constant slope. A counter again measures the amount of time for the integrator to discharge, thus generating the digital output.

The first slopes varies according to the value of the input signal, while the second slope dependent only on V_{ref}, is constant. Similarly, the time required to generate the first slope is constant, since it is limited by the size of the counter. However the discharging period is variable and results in the digital representation of input voltage.

2.2.4 Successive Approximation ADC

The successive approximation converter basically performs a binary search through all possible quantization levels before converging on final digital answer. The block diagram is shown in figure 2.10. An N-bit register controls the timing of the conversion where N is the resolution of the ADC. V_{in} is sampled and compared to the output of the DAC. The comparator output controls the direction of the binary search and the output of the successive approximation register (SAR) is the actual digital conversion.

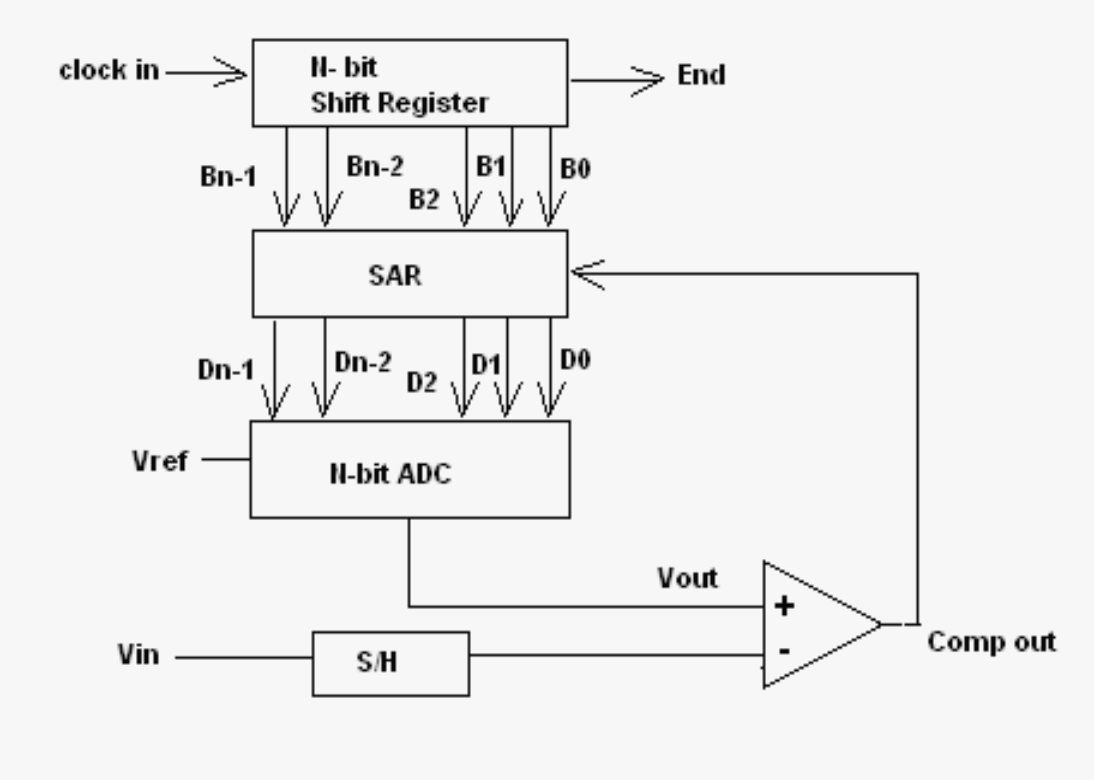


Fig. 2.10 Block diagram of successive approximation ADC

The successive approximation algorithm is as follows-

1. A 1 is applied to the input of the shift register. For each bit converted, the 1 is shifted to the right 1-bit position. B_{N-1} = 1 and B_{N2} through B_0=0.

2. The MSB of the SAR, D_{N-1}, is initially set to 1, while the remaining its, D_{N-2} through D_0, are set to 0.
3. Since the SAR output controls the DAC and the SAR output is 100…0, the DAC output will be set to Vref/2.
4. Next V_{in} is compared to Vref/2. If Vref/2 is greater than V_{in}, then the comparator output is a 1 and the comparator resets D_{N-1} to 0. If Vref/2 is less than V_{in}, then the comparator output is a 0 and the comparator resets D_{N-1} to 1. D_{N-1} is the actual MSB of the final digital output code.
5. The 1 applied to the shift register is then shifted by one position so that B_{N-2}=1 while the remaining all bits are 0.
6. D_{N-2} is set to 1, D_{N-3} through D_0 remain 0, while D_{N-1} remains the value from the MSB conversion. The output of the DAC will now either equal Vref/4 (if D_{N-1}=0) or 3Vref/4 (if D_{N-1}=1).
7. Next, V_{in} is compared to the output of the DAC. If the DAC output is greater than V_{in}, the comparator resets D_{N-2} to 0. If V_{in} is less than the DAC output, D_{N-2} remains a 1.
8. The process repeats until the output of DAC converges to the value of V_{in} within the resolution of the converter.

3.2.5 Algorithmic ADC

The algorithmic ADC, also called **cyclic** or **recirculating** converter was has been known and utilized since in various forms since 1960s. It was first realized by Hornak in a partially integrated form using a transformer to achieve a gain of two in 1975. Subsequently Mc. Charles achieved full integration of analog portion of the converter using a metal gate CMOS technology.

A block diagram of the converter is shown in Fig. 2.11.

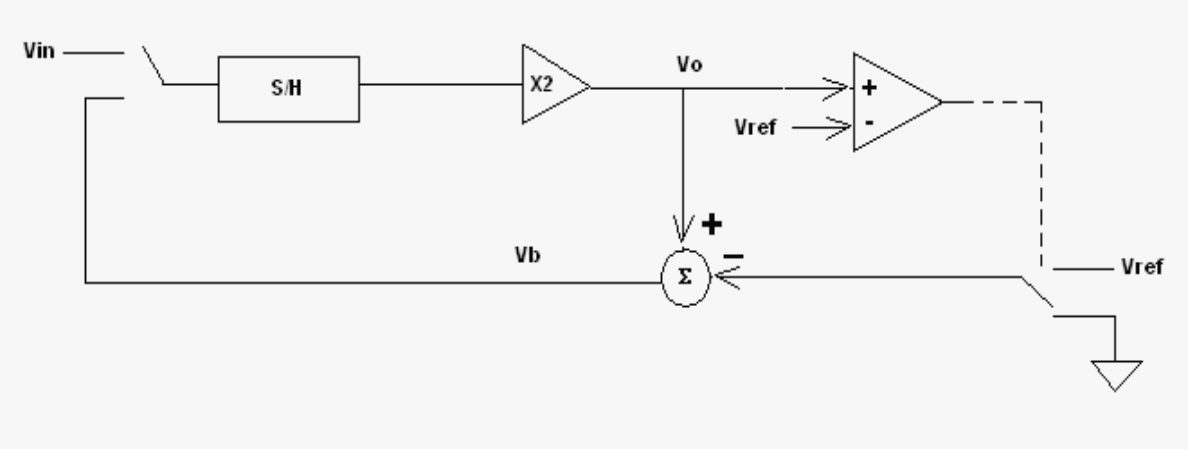


Fig. 2.11 Block diagram of the Algorithmic ADC

The algorithmic ADC consists of an analog signal loop which contains-

1. A sample-and-hold amplifier
2. A multiply-by-two amplifier
3. A comparator
4. A reference subtraction circuit.

The operation of the converter consists of first sampling the input signal onto the sample/hold amplifier. This is done by selecting the input signal instead of the loop signal using select switch. The input signal is then passed to the multiply-by-two amplifier where it is amplified. To extract the digital information from the input signal, the resultant signal, V_o is compared to the reference. If it is larger than the reference, the corresponding bit is set to 1 and the reference is then subtracted off from V_o. Otherwise, this bit is set to 0 and the signal V_o is kept unchanged. The resultant signal, denoted by V_b is then transferred, by means of switch. Back into the analog loop for further processing. This process continues until the desired numbers of bits have been obtained, whereupon a new sampled value of the input signal will be

processed. Thus, the digital data comes out from the converter in a serial manner, the MSB first.

The algorithmic ADC can be constructed with very little precision hardware. Its implementation in a monolithic technology can therefore be relatively area-sparing. It also possesses inherent S/H capability because the S/H amplifier is an integral part of the converter. It also possesses floating-point operation capability i.e. the input signal can be amplified 2^n times before the A/D conversion commences. These properties are very desirable for the design of single-chip complete data acquisition system.

Chapter 3 : CURRENT MIRRORS

Current mirrors are basic building blocks of almost all analog and mixed mode circuit structures. Hence, the characteristics of these current mirrors decide their performance. Depending upon the characteristics of the input output ports, several implementations for the current mirrors are available. The selection of a suitable current mirror for a particular application becomes important, which needs better understanding of all types of current mirrors, so that an appropriate current mirror can be selected.

Current mirrors are used either as **active load** or as **biasing networks**. The use of current mirrors in biasing structures results in better insensitivity to the variations in power supply and temperature. They are more economical in terms of die area if used as active loads.

3.1 BASIC CURRENT MIRROR

As the name suggests, a current mirror is expected to perform the similar functions with the electrical current as the plane optical mirror does for the optical signals. Hence a current mirror is a three terminal device whose output current at any instant of time is independent of voltage applied across its terminals and depends solely on the input current. The output current is the scaled version of the input current. Thus, in other words, **a current mirror reverses the direction of current injected into the low impedance input port and allows its true or scaled version to flow into a high impedance output port**. However the direction of the output current can also be reversed.

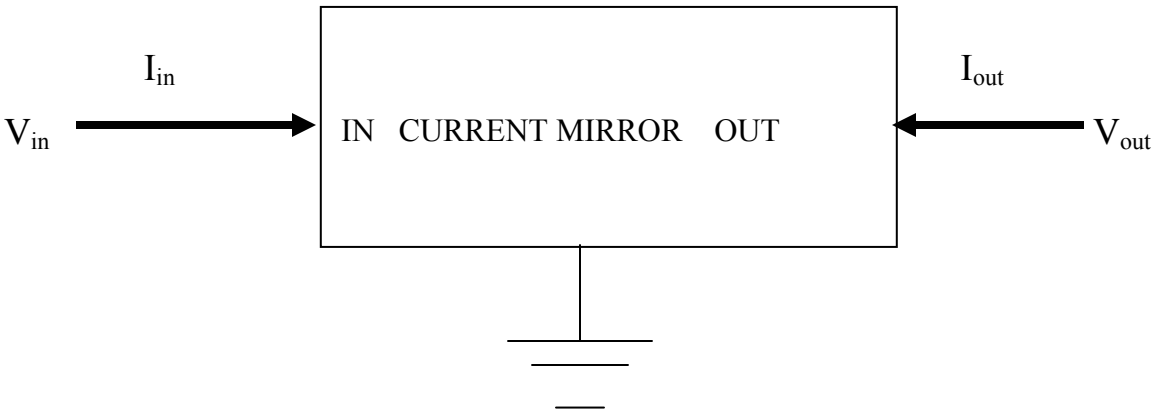


Fig 3.1. Block representation of a Current Mirror

For any high performance system, a current mirror must possess the following characteristics: -

- Current transfer ratio, which is precisely set by the (W/L) ratios, independent of temperature.
- Very high output impedance (high R_{out} and low C_{out}). As a result, the output current is independent of output voltages.
- Low input resistance (R_{in}).
- Low input and output compliance voltages.

Almost all analog circuit structures whether they operate as current mode devices or voltage mode devices, use current mirror in their design. To name a few such devices, following devices are based on the use of the current mirrors.

1. Operational amplifiers.
2. Operational trans-conductance amplifiers.
3. Operational trans-resistance amplifiers.
4. Current feedback amplifiers.
5. Current conveyors.
6. Operational floating conveyors.
7. Digital to analog converters.

8. Analog to digital converters.

3.2 CLASSIFICATION OF CURRENT MIRRORS

All practical current mirrors are plagued with non-idealities and all possible current mirror designs are for getting near ideal properties. The main sources of non-idealities in the current mirror characteristics include-

1. Channel length modulation.
2. Threshold voltage offset between input and output transistors.
3. Imperfect Geometrical matching.

Other sources of non-idealities are the environmental born. These sources such as temperature effects can be minimized but cannot be completely eliminated. All the techniques adopted for the design of current mirrors are directed towards getting near ideal current mirror structures. In this process, many circuit configurations for the current mirrors were proposed. Suitability of a particular current mirror depends on the type of applications. In those applications where the slow processing is required, use of high performing mirror is a waste. Though there is no formal classification of current mirrors, they can be classified depending upon their properties. Some of the current mirrors are named after their inventors such as Widlar current mirror, Wilson current mirror etc. In general, a current mirror can fall in any of the following categories-

1. Simple current mirror
2. Source degenerate current mirror
3. High output impedance current mirror
4. Wide swing current mirror
5. Enhanced output impedance current mirror
6. Low voltage current mirror

Though all these practical current mirror structures do not possess ideal current mirror characteristics. Even then a current mirror may be found suitable for a certain application and one has to select an appropriate current mirror.

3.3 CURRENT MIRROR STRUCTURES

3.3.1 Simple Current Mirror

Figure 3.2 shows the basic structure for a current mirror. In no-saturation region the MOSFET is not a good current source. Hence, it is assumed that both the transistors are in saturation region.

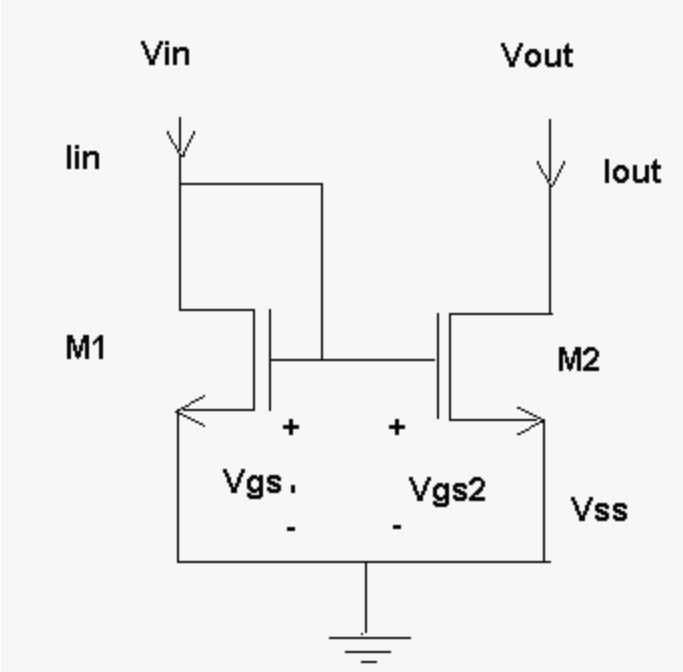


Fig 3.2 Simple current mirror structure

The voltage across the output transistor M2 must be larger than V_{eff} (=V_{GS} - V_T). If the finite output impedance of the transistors are ignored, and it is assumed that both transistors have same size, then M1 and M2 will have

same current since they both have same gate source voltage. In the most general case the current transfer function which is defined as the ratio of mirrored current (I_{out}) to the input current (I_{in}) is given by-

$$\frac{Iout}{Iin} = \left[\frac{L_1 W_2}{L_2 W_1}\right]\left[\frac{V_{GS} - V_{T2}}{V_{GS} - V_{T1}}\right]^2 \left[\frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}\right]\left[\frac{K_2}{K_1}\right] \quad (1)$$

Normally, the components of current mirror are processed on the same integrated circuit and all the physical parameters (V_T, K', etc) are identical for both M1 and M2. As a result, the previous equation simplifies to-

$$\frac{Iout}{Iin} = \left[\frac{L_1 W_2}{L_2 W_1}\right]\left[\frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}\right] \quad (2)$$

If $V_{DS2} = V_{DS1}$, then the above equation further reduces to

$$\frac{Iout}{Iin} = \left[\frac{L_1 W_2}{L_2 W_1}\right] \quad (3)$$

Thus the current transfer ratio is under the control of a circuit designer. However the ideal conditions do not exist and there are three sources of non-idealities in a current mirror. There is finite output impedance and the input impedance is also not zero. These parameters are given as

$$V_{in}(\min) = V_{DS}(\text{sat}) + V_T \quad (4)$$

$$V_{out}(\min) = V_{DS}(\text{sat}) \quad (5)$$

$$R_{in} = \frac{1}{g_{m1}} \quad (6)$$

$$R_{out} = \frac{1}{g_{O2}} = \frac{1}{\lambda I_{DQ2}} \quad (7)$$

There is a tradeoff between output impedance (R_{out}) and output capacitance (C_{out}). Bigger size transistors achieve higher $R_{out,\ which}$ is always desired for a current mirror. But there will be higher C_{out} associated bigger size

transistors, which obviously degenerates the frequency response of a current mirror.

The advantages offered by a simple current mirror include its simple architecture and high output voltage swing capabilities. However, these mirrors are generally plagued with low output impedance characteristics. This low output impedance may not be sufficient for many applications. Thus there is a need to investigate some other circuit structures for the current mirror applications.

3.3.2 Source degenerate Current Mirror

First proposed source degenerate current mirror was the Widlar current mirror. The source degeneration was used for increasing the output impedance of the simple mirror. The modified MOSFET version of the mirror is shown in Fig 3.3. For this circuit the output impedance is given by-

$$V_{in}(\min) = V_{DS}(\text{sat}) + V_T + I_{in} R_s \quad (8)$$

$$V_{out}(\min) = V_{DS}(\text{sat}) + I_{out} R_s \quad (9)$$

$$R_{in} \approx \frac{1}{g_{m1}} + R_S \quad (10)$$

$$R_{out} \approx \frac{R_s g_{m2}}{g_{O2}} \quad (11)$$

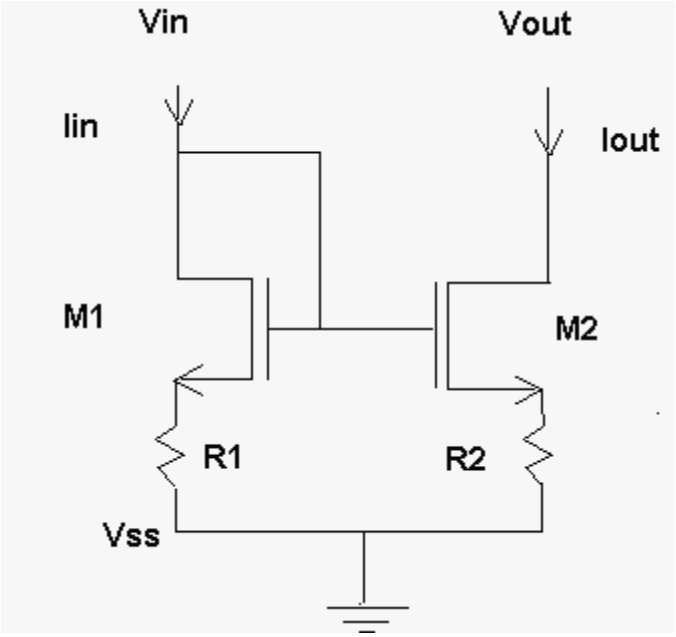


Fig. 3.3 Source degenerated current mirror

3.3.3 High output impedance Current Mirror

Various current mirrors like Cascode current mirror, Wilson current mirror, improved Wilson current mirror etc fall in this category.

Cascode Current Mirror

Using longer transistor is a good idea to achieve high output impedance but such a structure consumes more Silicon area, and does not have good transient response. Cascode structure is an alternative to obtain high output impedance and good transient response. A cascode current mirror structure is shown in Fig. 3.4

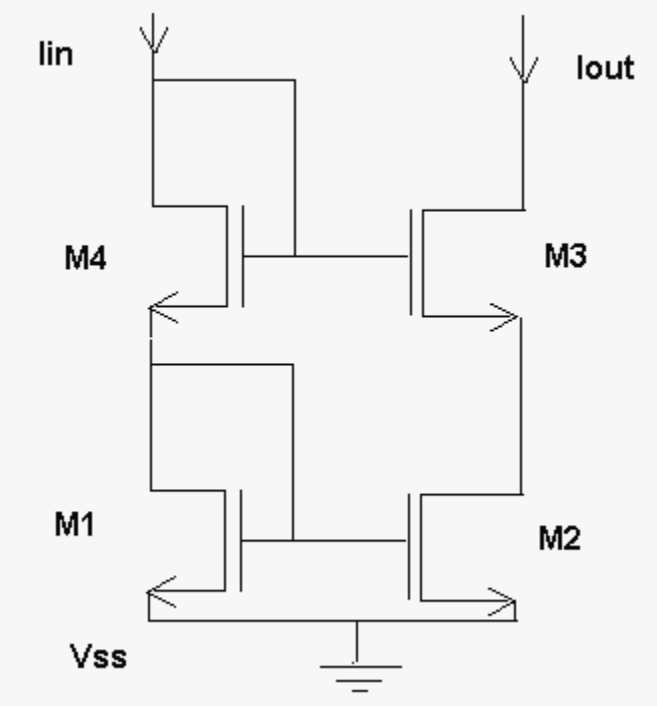


Fig. 3.4 A Cascode current mirror structure

If we look into the transistor M2, the output impedance is simply $1/g_{o2}$. If we replace the transistor by an equivalent resistance of value equal to $1/g_{o2}$, then the circuit resembles to a source degenerated current mirror. Thus, the structure can be expressed as-

$$R_{in} \approx \frac{1}{g_{m1}} + \frac{1}{g_{m3}} \tag{12}$$

$$R_{out} \approx \frac{g_{m2}}{g_{O2} g_{o4}} \tag{13}$$

The other parameter of interest in the design of a current mirror is the output and input compliance voltages, which should be as low as possible for a current mirror. For the cascode current mirror the output compliance voltage is given by-

$V_{in}(min) = 2V_{DS}(sat) + 2V_T$ (14)

$V_{out}(min) = 2V_{DS}(sat) + V_T$ (15)

The advantages offered by such a structure is high output impedance, and relatively good transient response. However, such cascode structure possesses a low output voltage swing. There are several other improved versions of cascode current mirror, which require low output compliance voltage and have high output impedance.

Wilson Current Mirror

The output impedance of a current mirror can also be increased through negative feedback. The Wilson current mirror, shown in Fig. 3.5 implements this concept. The feedback is through M2, which activates M1 to raise the output impedance.

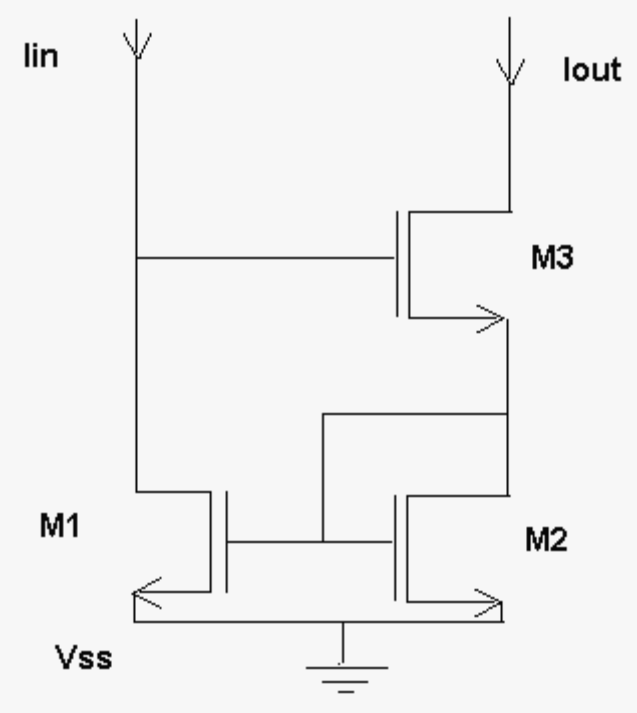


Fig. 3.5 A Wilson Current Mirror

This circuit has the following parameters-

$$R_{in} \approx \frac{1}{g_{m1}} \tag{16}$$

$$R_{out} \approx \frac{g_{m2}}{g_{O}^{2}{}_{2}} \tag{17}$$

$$V_{in}(\min) = 2V_{DS}(\text{sat}) + 2V_T \tag{18}$$

$$V_{out}(\min) = 2V_{DS}(\text{sat}) + V_T \tag{19}$$

The merit of the circuit lies in its capability to provide high output impedance, due to the use of negative feedback mechanism. Since the cascode of two transistors have been used at the output port, the available output voltage swing reduces.

Improved Wilson Current Mirror

The Wilson mirror operates with larger dc value of V_{DS} on M3 than on M2. For large threshold voltages this leads to drain current mismatch due to finite output resistance of the transistors. This can be overcome by adding M4. This transistor equalizes V_{DS} on M2 and M3. The resultant circuit is shown in Fig. 3.6

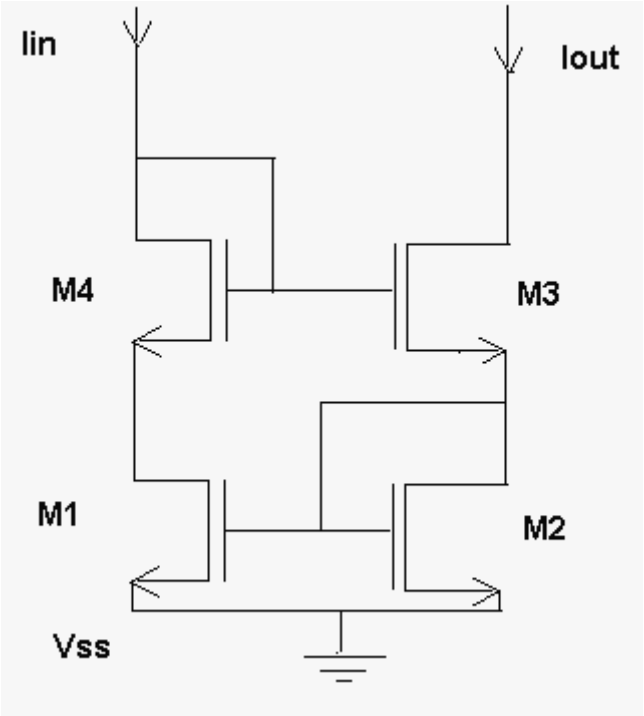


Fig. 3.6 Modified Wilson Mirror

The various performance parameters are given as-

$$R_{in} \approx \frac{1}{2g_{m1}} \tag{20}$$

$$R_{out} \approx \frac{g_{m2}g_{m3}}{g_{m2}g_{o1}g_{o3}} \tag{21}$$

$$V_{in}(\min) = 2V_{DS}(\text{sat}) + 2V_T \tag{22}$$

$$V_{out}(\min) = 2V_{DS}(\text{sat}) + V_T \tag{23}$$

The improved Wilson mirror offers better match between I_{in} and I_{out} and high output impedance. The circuit has high output impedance butt the available output voltage swing is low.

3.3.4 Wide Swing Current Mirror

As newer technologies with shorter channel are emerging, reasonably high output impedance cannot be obtained through the short channel MOSFETs. Unfortunately the use of conventional cascode lengths are used, the output impedance of the transistor degrades due to channel length modification effects. As a result, conventional cascode current mirrors are used to have mirrors limit the output voltage swing, which may be tolerated in certain applications. Fortunately, circuits exist which don't limit signal swing as much as the circuits discussed so far. One of such circuit is shown in Fig. 3.7. The basic idea of current mirror is to bias the drain-source voltages of the transistors m2 and M3 to be close to the minimum possible value without letting them go into the triode regions.

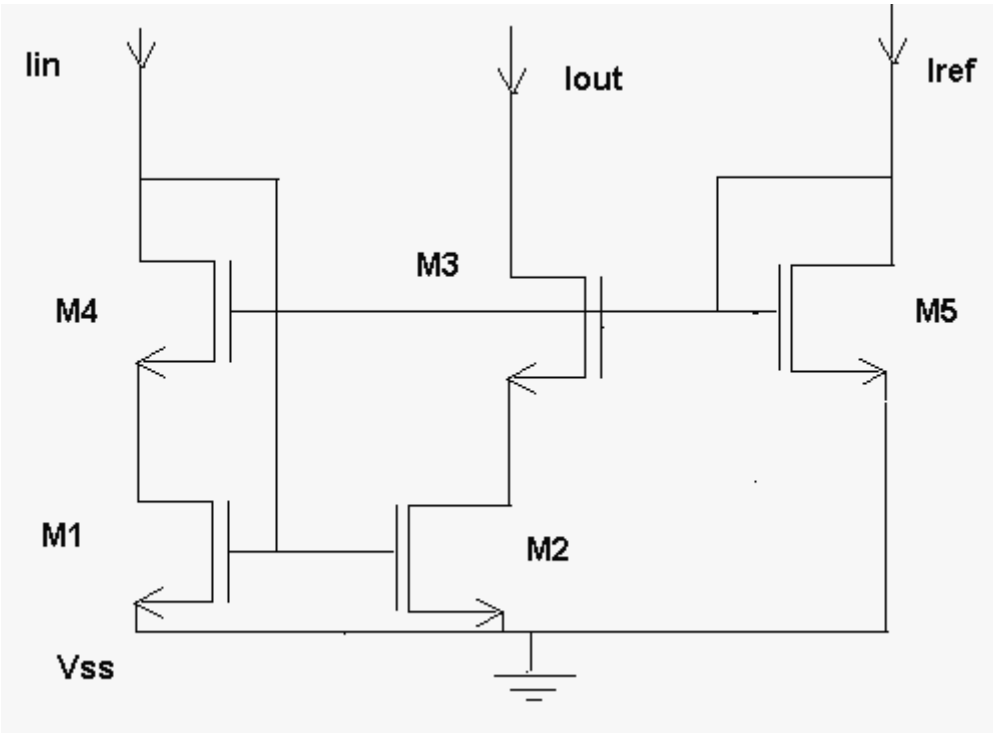


Fig. 3.7 Wide Swing Current Mirror structure

Various parameters of this circuit are given by-

$$R_{in} \approx \frac{1}{g_{m1}} \tag{24}$$

$$R_{out} \approx \frac{g_{m2} g_{m3}}{g_{o2} g_{o4}} \tag{25}$$

$$V_{in}(\min) = 2V_{DS}(\text{sat}) + 2V_T \tag{26}$$

$$V_{out}(\min) = 2V_{DS}(\text{sat}) + V_T \tag{27}$$

The circuit has the advantage of high output and input voltage than a conventional cascode current mirror. This current mirror also provides high output impedance. However, this circuit requires additional bias circuit and hence consumes more power.

3.3.4 Enhanced Output Impedance Current Mirror

This is another method to use the negative feedback to increase the output impedance of a current mirror. One of the circuit structures is shown in Fig.3.8.

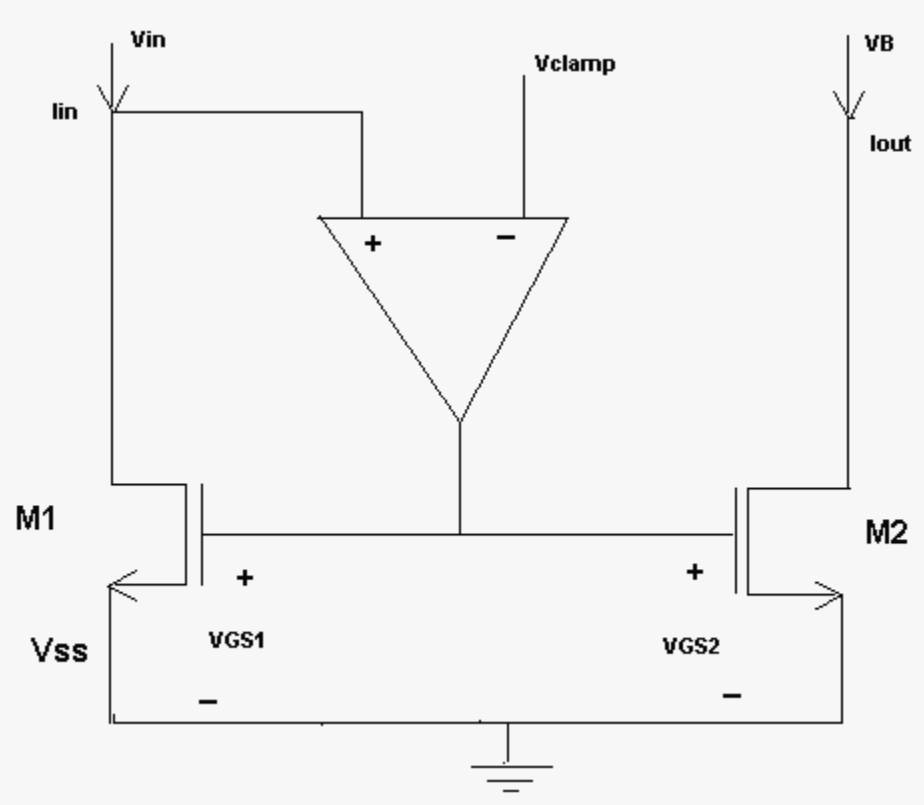


Fig.3.8Enhanced Output Impedance Current Mirror

The various performance parameters of the circuit are given by-

$$R_{in} \approx \frac{1}{g_{m1}} \tag{28}$$

$$R_{out} \approx \frac{g_{m3}(1+A)}{g_{o2}g_{o3}} \tag{29}$$

$$V_{in}(\min) = V_{DS}(\text{sat}) + V_T \tag{30}$$

$$V_{out}(\min) = 2V_{DS}(\text{sat}) \tag{31}$$

The input and output compliance voltages of this current mirror are similar to that of wide swing current mirror. It may be seen that the gain of the amplifier is proportional to the gain of the amplifier and hence it can be increased easily. The requirement of higher power supply voltage and larger power consumption are the main disadvantages of this circuit. Further the

poles and zeroes of the feedback amplifier could cause the stability problems.

3.3.5 Low Voltage Current Mirrors

At the low voltage, the design of analog cells is different from the design that operates at higher voltage levels. All the current mirrors so far discussed have high signal swings at output node but the voltage swing at input node is restricted. This restriction is imposed due to need of having minimum voltage of at least one V_T at the input node. Thus these current mirrors are unsuitable for embedding them in low voltage circuit structures. The aim of high performance low-voltage current mirrors is to reduce the input impedance and increase the output impedance with low input and output compliance voltages. Not all low voltage design techniques are suited for very high frequency LVCMs.

3.4 CURRENT MIRROR SYMBOL

There are a number of different current mirror circuits. They have various advantages and disadvantages and can be used in particular application. Thus for architectural point of view it is often desirable to describe the circuit without showing which particular current mirror is used. In such cases we have to use the symbol for a current mirror. These symbols are shown in Fig. 3.9 for both NMOS and PMOS type of current mirrors. The arrow is on the input side of the current mirror, which is low input impedance side. The arrow also designates the direction of current flow on the input side. The ratio 1:K represents the current gain of a current mirror.

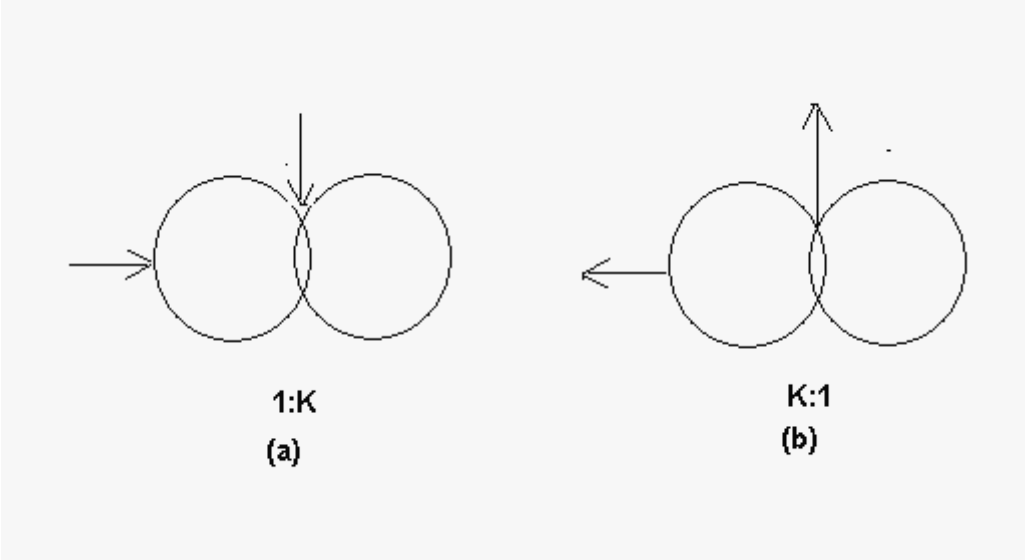


Fig. 3.9 Current mirror symbols (a) NMOS type Current Mirror (b) PMOS type Current Mirror

3.6 EQUIVALENT CIRCUIT OF THE CURRENT MIRROR

We generally do not care for the internal structure of the current mirror as long as we know its complete characteristics. Any current mirror realization, which can give desirable characteristics to the analog circuit structures, can be assumed. The only criterions of selection of a suitable current mirror are the characteristics can meet the specifications of a particular application and the simplicity of its architecture. Thus a current mirror can be viewed as 2-port network and can be modeled using hybrid (*h*) parameters similar to the modeling of a transistor. The *h* parameters for the structure can be defined as-

$$\begin{bmatrix} V_{in} \\ I_{out} \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_{in} \\ V_{out} \end{bmatrix} \tag{32}$$

Once these parameters can be extracted for the current mirror, they can be used to draw its equivalent circuit as shown in Fig. 3.10. The input circuit of the equivalent circuit contains a dependent voltage source while the output circuit contains a dependent current source. Thus the presence of these dependent sources complicates the analysis of the current mirror based circuits and the evaluation of such circuits becomes quiet difficult. Thus it is desirable to use some simple equivalent circuit of the current mirror. Such a circuit can facilitate hand calculations with reasonable accuracy. One such simple circuit that can serve as an equivalent circuit for the current mirror is shown in Fig. 3.11

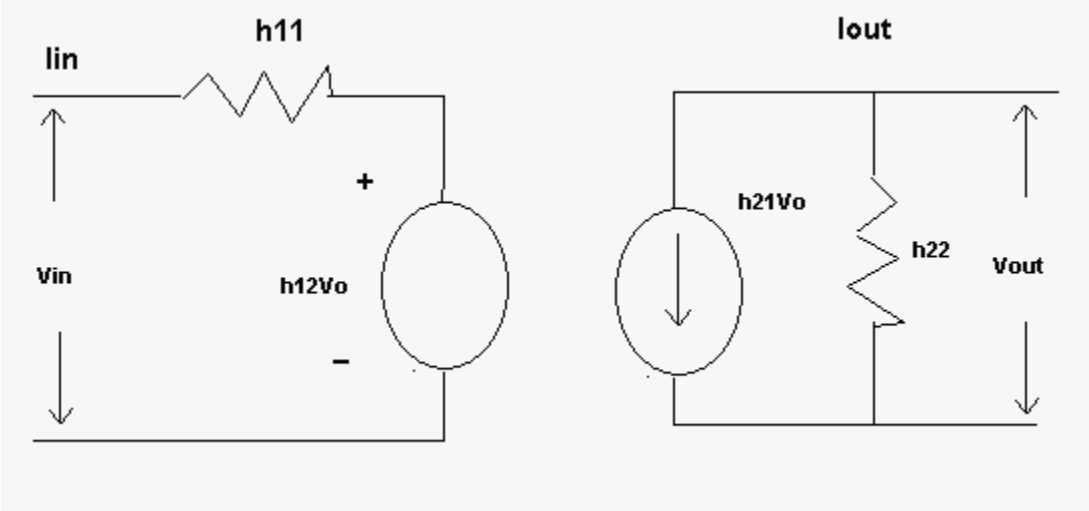


Fig. 3.10 Equivalent circuit of current mirror based on *h*-parameters.

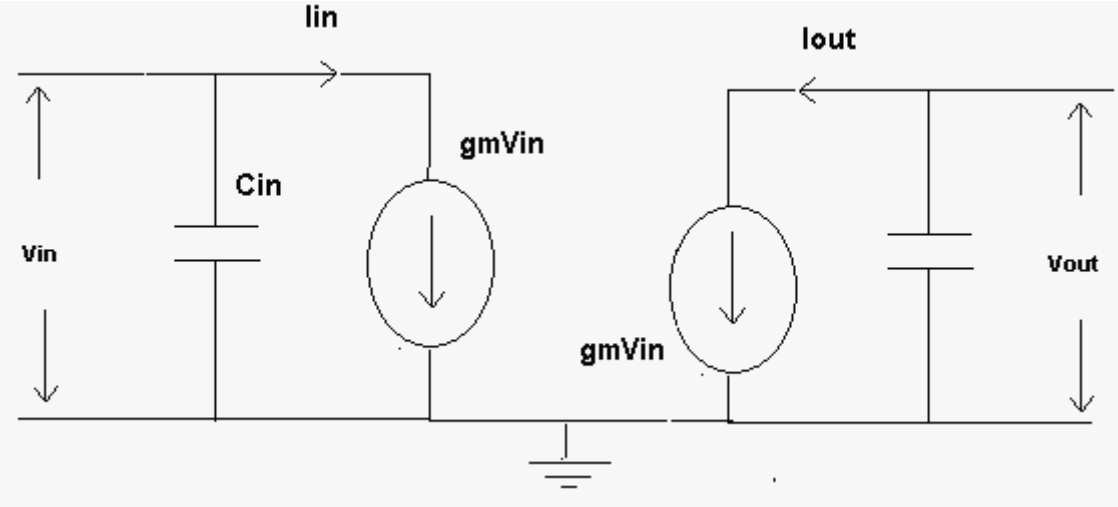


Fig. 3.11 Simplified equivalent circuit of a current mirror

The input impedance of this circuit is assumed to be $1/g_m$ while the output impedance is assumed to be g_o.

Table 3 gives a comparison of characteristic parameters of various current mirrors. An appropriate current mirror can be selected for a particular application.

Table 3: Table of Comparison Of various Current Mirrors: -

CM Structure	Input compliance voltage	Output compliance voltage	Input impedance	Output impedance
Simple CM	$V_{DS}(sat) + V_T$	$V_{DS}(sat)$	$\frac{1}{g_{m1}}$	$\frac{1}{\lambda I_{DQ2}}$
Source Degenerate CM	$V_{DS}(sat) + V_T + I_{in} R_s$	$V_{DS}(sat) + I_{out} R_s$	$\frac{1}{g_{m1}} + R_S$	$\frac{R_s g_{m2}}{g_{O2}}$
Cascode CM	$2V_{DS}(sat) + 2V_T$	$2V_{DS}(sat) + V_T$	$\frac{1}{g_{m1}} + \frac{1}{g_{m3}}$	$\frac{g_{m2}}{g_{O2} g_{o4}}$
Wilson CM	$2V_{DS}(sat) + 2V_T$	$2V_{DS}(sat) + 2V_T$	$\frac{1}{g_{m1}}$	$\frac{g_{m2}}{g_{O}^{2}{}_{2}}$
Improved Wilson CM	$2V_{DS}(sat) + 2V_T$	$2V_{DS}(sat) + V_T$	$\frac{1}{2g_{m1}}$	$\frac{g_{m2} g_{m3}}{g_{m2} g_{o1} g_{o3}}$
Wide swing CM	$V_{DS}(sat) + V_T$	$2V_{DS2}(sat) + 2V_{DS4}(sat)$	$\frac{1}{g_{m1}}$	$\frac{g_{m2} g_{m3}}{g_{o2} g_{o4}}$
Enhanced output impedance CM	$V_{DS}(sat) + V_T$	$2V_{DS}(sat)$	$\frac{1}{g_{m1}}$	$\frac{g_{m3}(1+A)}{g_{o2} g_{o3}}$

Chapter 4- Current Comparators

Widespread interest in "affordable-anywhere-anytime" wireless communication and computation has created a critical need for low-power low-voltage analog and digital integrated circuits. Not only do we want our systems to run faster, but we also want them to run on little or no power. That means increasing the speed and performance of all the components in a system while staying within a restrictive power budget. The demand for higher bandwidth, smaller supply voltage and lower power consumption is also driven by the increasing complexity of electronic equipment. To be able to integrate more functions and more complex functions on a single integrated circuit, the minimum feature size continues to reduce, forcing smaller supply voltages. However the threshold voltage does not scale down proportional to the supply voltage. This introduces many new challenges in designing low-power circuits that meet speed, accuracy, and noise requirements.

Comparators are the second most widely used current mode components, after current mirrors. They have always been, and are still, an important building block in electronic systems including oscillators, data converters and other front-end signal processing applications. A critical design aspect for comparators is good trade-off between sensitivity, speed, and power consumption. Speed, in fact, can usually be increased at the expense of higher power consumption, while sensitivity requires high gain and hence low bias current, which leads to a slower time response.

4.1 Voltage mode current comparator Vs Current mode comparator

A voltage-mode comparator is a circuit that compares the instantaneous value of an input signal with a reference voltage and produces a logic output level depending on whether the input is larger or smaller than the reference level. However, for CMOS voltage-comparators, transistor mismatch is unavoidable causing threshold shifting. Moreover, these circuits tend to be power-hungry, partly due to the difficulty in reducing the supply rails, and also the need for the use of a significant number of physical resistors.

In contrast, current-mode comparators are more economical in terms of power consumption than their voltage-mode counterparts. In its simplest form, a current comparator is a device which discriminates between two incident currents instead of two voltages.

4.2 Basic CMOS current comparator

Fig. 4.1 shows the basic CMOS current comparator. Transistors M1, M2 make up the n-type current mirror and M3 and M4 the p-type current mirror. The input current I_{in} and the output current I_{ref} are replicated by the current mirrors at the drains of M2 and M4 are connected together to give the output V_{out}. The output voltage changes from high to low depending on the values of input current and output current.

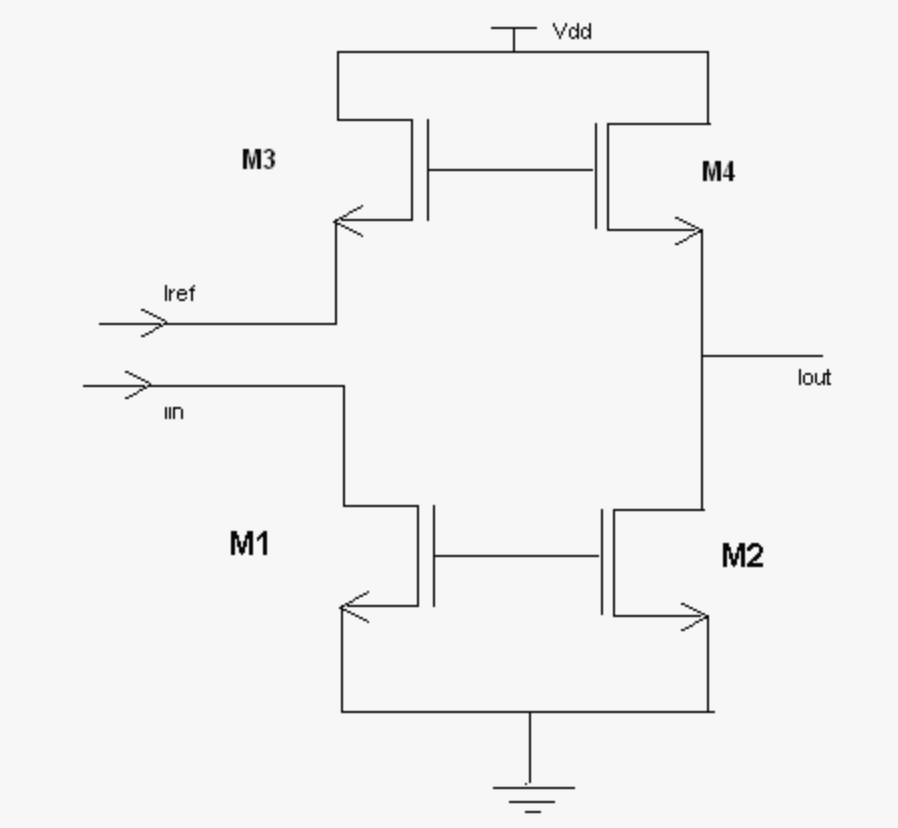


Fig 4.1 Basic CMOS current Comparator

4.3 Current comparator with inverter output stages

In order to obtain better circuit performance, basic current mirrors were replaced by cascode current mirrors. Moreover, to improve the noise margin and to obtain high sensitivity the gain of the current comparator should be high. Three CMOS inverter stages are added to the output stage to achieve full output voltage swing between 0 and 5. Fig. 4.2 shows the current mirror with cascode current mirrors as input stage and three inverters making the output stage.

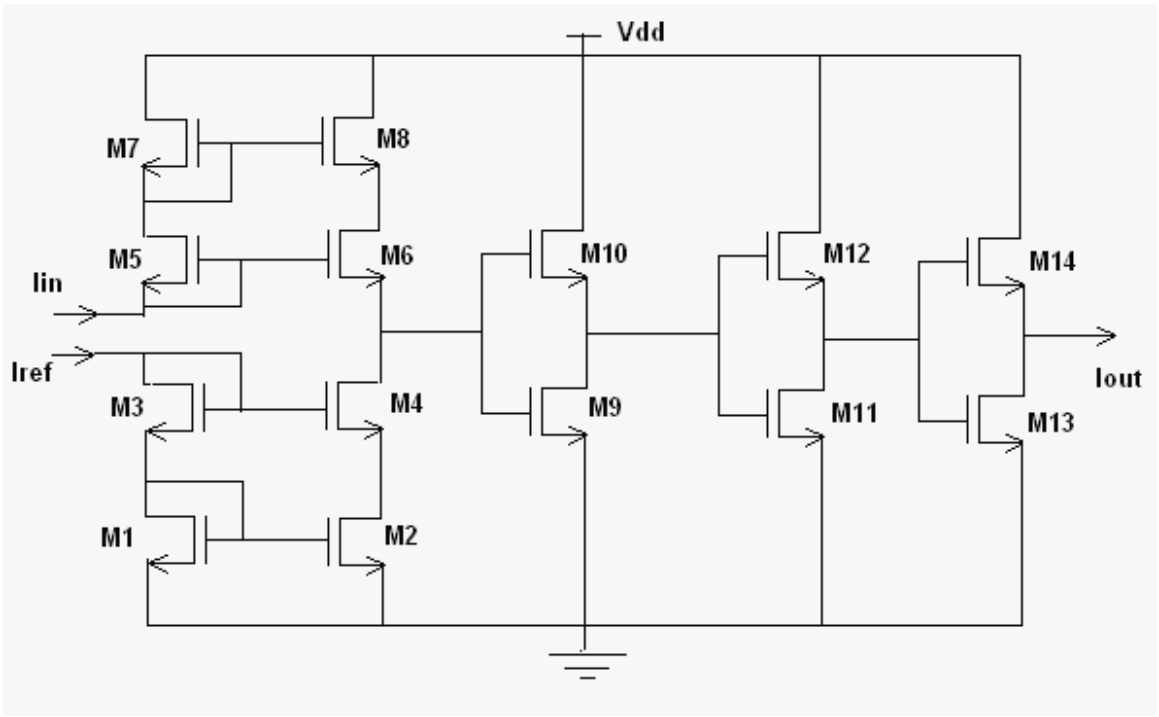


Fig. 4.2 Current comparator with inverter output stages

Chapter 5- Simulations

(I) The current-mode ADC

For the current mode ADC, the algorithmic style of analog to digital conversion was selected because presently this style of conversion occupies the smallest amount of silicon area. The algorithmic ADC conversion technique takes the advantage of relatively simple hardware to produce ADC's. The technique can be used to produce either a gray-code or a binary-code output as is done in this research work. A conceptual implementation of current-mode ADC is shown in Fig. 5.1.

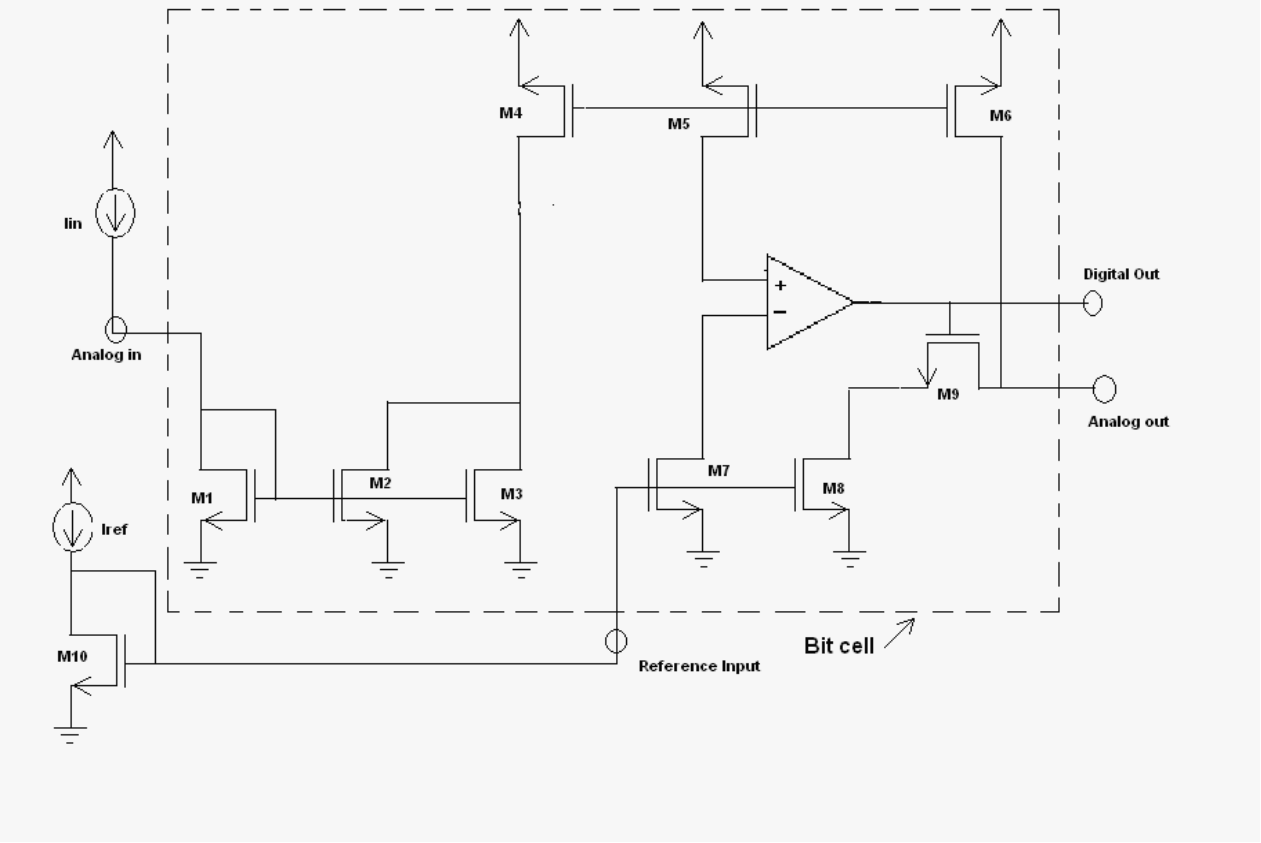


Fig. 5.1 A bit cell that implements a 1-b algorithmic conversion

The circuit performs a 1-b algorithmic analog-to-digital conversion in the following manner. The input current I_{in} is first multiplied by 2 using the current mirror composed of M1, M2 and M3. Following the multiplication, the signal $2I_{in}$ is mirrored from M4 through M5 to the comparator and through M6 to the output. The comparator is used to compare $2I_{in}$ (from M5) with $I_{ref,}$ the reference current (from M7). If $2I_{in}$ is less than I_{ref}, the digital output goes low and M9 remains off resulting in an out put current of $2I_{in}$ (from M6). On the other hand if $2I_{in}$ exceeds I_{ref}, the digital output will be high causing M9 to be on. With M9 on, I_{ref} (from M8) will be subtracted from 2Iin (from M6) resulting in an output current of $2I_{in}$- I_{ref}. This completes the 1-b algorithmic conversion.

To complete the N-bit conversion, N bit cells are cascaded with the analog output of one call connected to the analog input of the following cell as illustrated in Fig. 5.2. Transistor M10 is shared by all bit cells. The resulting sequence of bit cell does not require control signals. Therefore this configuration will result in a very compact circuit that can be easily modified for different solutions.

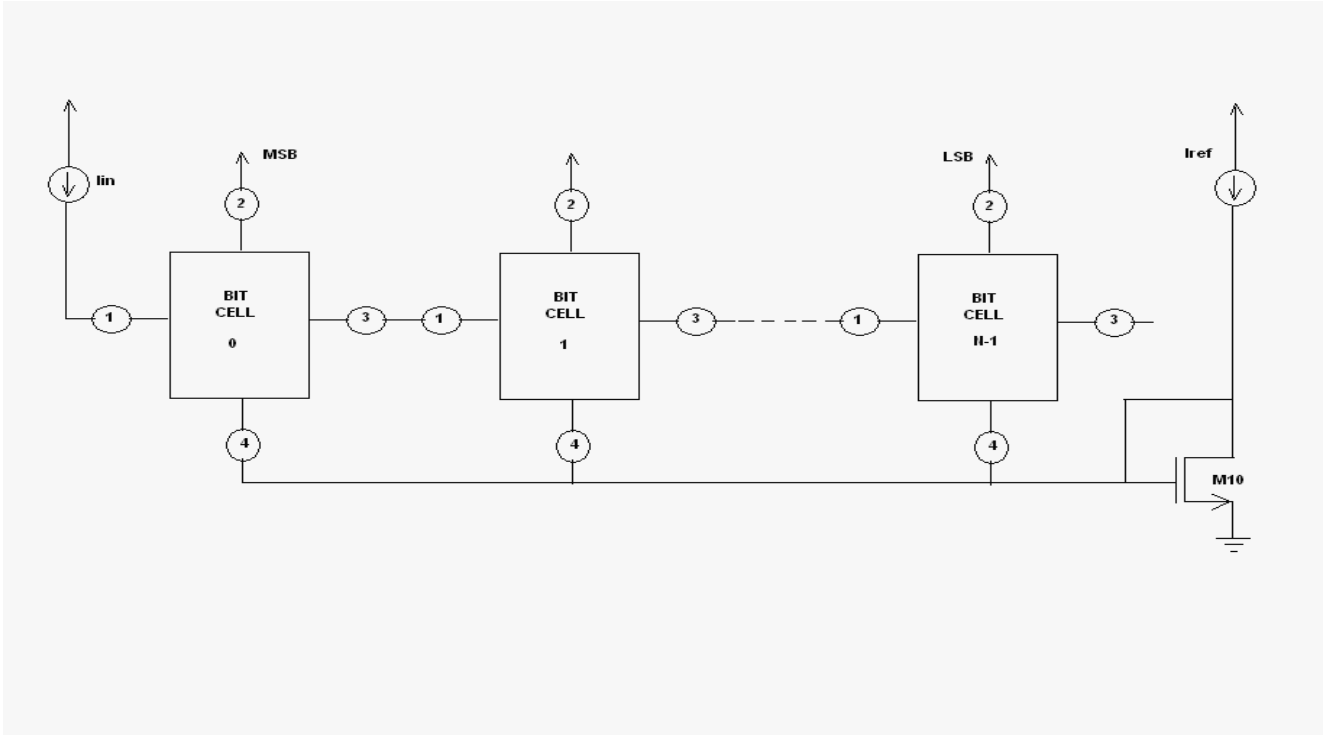


Fig. 5.2 Cascade of bit cell for an N-bit converter.

The converter speed is determined by the rate at which the signal propagates through the cascade of bit cells. Within each bit cell, the rate of signal propagation is determined by the settling time of the current mirrors, which can be improved by shorter channel length devices.

The current-mode algorithmic ADC with its relatively few components, lack of control circuitry, and easily varied resolution, will be small, versatile, and fast. Consequently, this circuit will be ideal for use in the VLSI environment.

(II) Design of Current-Mode ADCs

The algorithmic current-mode ADC is composed of current comparators and current mirrors. Due to the need for N comparators, 2N current mirrors for an N-bit ADC, these components should be made as small as possible without sacrificing the accuracy of the overall converter.

An appropriate current comparator can be implemented using the inverter cascade as shown in Fig. 5.3.

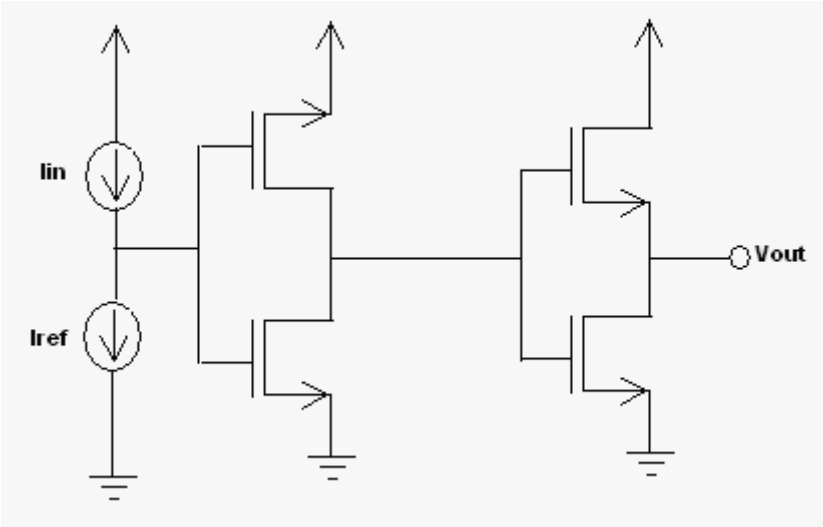


Fig. 5.3 Basic Current Comparator

Although a comparator of this type will display a low PSSR when used as a voltage comparator, this problem not significant when the circuit is used as a comparator. Further, this problem can be solved by using other more versatile current comparators as discussed in chapter 4. The first inverter in the basic current comparator operates as an integrating current-to-voltage converter and hence effectively filters out the power supply noise. At the same time, the integrating nature of the comparator ensures that there is no inherent dc offset in the comparator. Consequently, the inverter cascade

provides a simple, small, and effective current-to-voltage converter/comparator.

Current mirrors suitable for use in the algorithmic current-mode ADC must display excellent current matching. To achieve the best possible current matching, the devices must display both a high output resistance and good device matching characteristics. To improve the device output resistance, long channel length devices must be used. To improve the device matching, both the channel length and the channel width must be significantly larger than the minimum feature size permitted by the technology. Consequently, to achieve good accuracy in ADC, the use of larger devices in the current mirrors is essential.

Although increasing the device size reduces the device mismatches, the mismatches cannot be eliminated completely. Hence, even if a sufficiently high output resistance can be obtained, the device mismatches will limit the converter accuracy. These mismatches lead to the current error defined as-

$$\frac{\Delta I}{\Delta I_{IN}} = \frac{I_{out} - I_{IN}}{I_{IN}}$$

where I_{IN} is the mirror input current, I_{out} is the mirror output current, ΔI is the difference between the input and output current.

Although the device mismatches will theoretically limit the converter resolution to the 8-b range, in practice, it is found that the primary source of error in the circuit of Fig. 5.1 is the subtraction operation at the bit cell output. The most significant error for the converter will occur at 10….00 to 10….01 transition, which corresponds to an input slightly larger than half the full scale input. In that case the output of the first section will be very small (i.e. $I_{out} = 2I_{IN} - I_{ref}$), causing the voltage at the output to be pulled down to the threshold voltage of the n-channel device present in the input stage of

the following bit cell. The low output voltage causes the reference mirroring device M8 in Fig. 5.1 to come out of saturation, resulting in a significant current error. This error is then amplified in successive stages of the converter leading to conversion errors and possibly missed codes.

To solve the subtraction problem, the bit cell input voltage, even for extremely low currents, must be kept as high as possible while still maintaining the highest possible output resistance for each current mirror. Both objectives can be met using **Cascoded current mirrors** as shown in Fig. 5.4

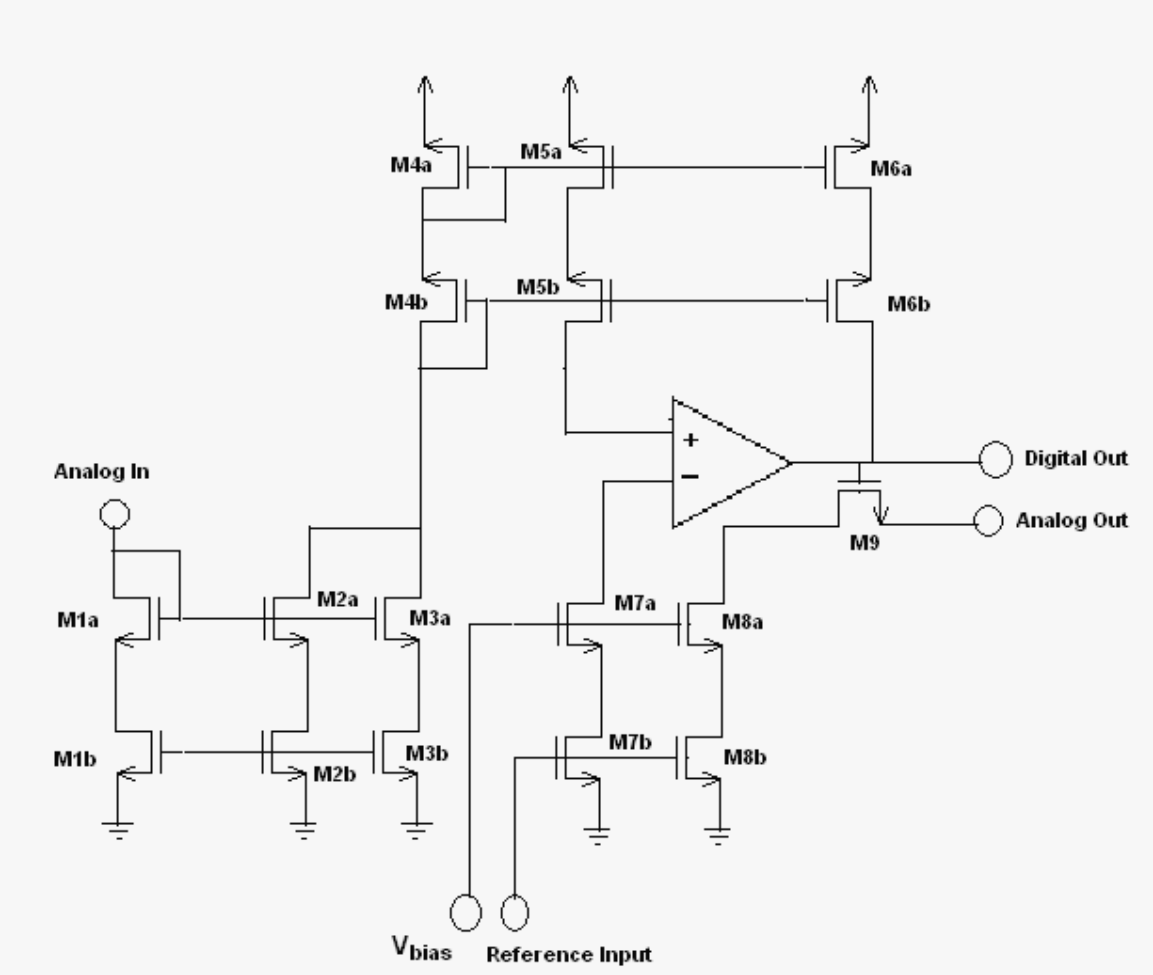


Fig. 5.4 Schematic of the bit cell using Cascoded mirrors

By selecting an appropriate bias point (V_{bias}) for the reference current mirror, one can ensure that both transistors M8a and M8b remain in saturation even when the analog output goes as low as $2V_T$, thereby ensuring that the reference mirror's high output resistance is maintained at all times. Another advantage of the cascoded mirror is their significantly increased output resistance which arises from the buffering action provided by the devices in Fig. 5.4 which isolate b devices from differences between the input and output voltages.

Unfortunately, the use of cascoded current mirrors significantly reduce the dynamic range and hence the resolution of the ADC Although current errors due to the device finite output resistance are reduced by using the cascoded current mirrors, the mirrors still display a current error due to device mismatches. Like the basic current mirrors, the cascoded current mirrors will display a relative current error equal to the magnitude of the β mismatches. These mismatches limit the cascoded current mirror ADC resolution to 8 b. For V_T mismatches, the cascoded current mirrors display a significantly large error.

To achieve greater resolutions, a current mirror that does not suffer from V_T mismatches or the device finite output resistance can be used. The effects of V_T mismatches can be reduced by operating the mirroring transistors with the highest possible gate voltage. Simultaneously, the drain-to-source voltage of the mirroring devices must be buffered from the differences between the mirror input and output voltages.

One approach to buffering the mirror drain-to-source voltage without restricting the device gate voltage is to replace the basic current mirror shown in Fig. 5.5(a) with the active current mirror shown in Fig. 5.5(b).

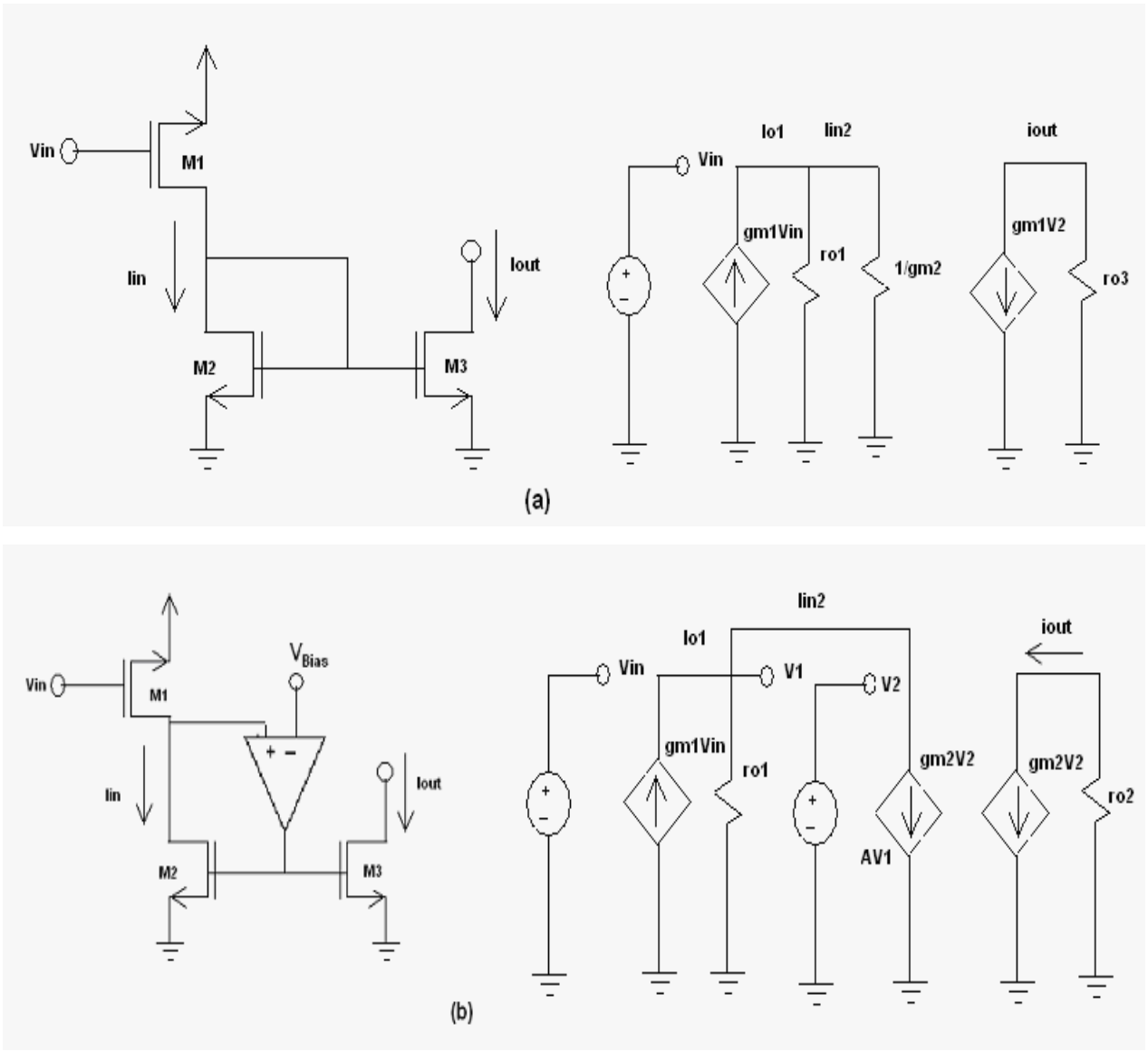


Fig. 5.5 Current mirror structures and their small-signal models. (a) The basic current mirror and its small-signal model. (b) The active current mirror and its small-signal model.

The active current mirror is a simplified current conveyor and its primary advantage is that its input voltage can be fixed independent of the mirroring device gate voltage. By keeping the mirror output and input terminals at the

same potential, the detrimental effects of the device finite output resistance will be eliminated.

The active current mirror reduces current mismatches due to the device finite output resistance, not by increasing the output resistance itself, but by reducing the mirror input resistance. Consider the circuit of fig. 5.5(a). The output current source of M1 drives the parallel combination of r_o, the device output resistance, and the mirror's effective input resistance, 1/gm, causing current division to occur. Thus, the current mirror input current, I_{in2}, can be represented as-

$$\frac{i_{in2}}{i_{o1}} = \frac{r_o}{r_o + 1/gm}$$

where i_{o1}, is the output current of the input current source M1. Therefore to obtain a current transfer ratio closer to unity, either r_o must be increased or 1/gm must be decreased. When the current mirror in Fig. 5.5(a) is replaced by the active current mirror in Fig. 5.5(b) the small signal model of the current mirror changes, resulting in the following current transfer function-

$$\frac{i_{in2}}{i_{o1}} = \frac{r_o}{r_o + 1/Agm}$$

where A is the amplifier gain. The current mirror effective input resistance is reduced by a factor equal to the amplifier gain. Therefore the active current mirror reduces current mismatches by reducing the current mirror input resistance.

The amplifier used in the active current mirror is shown in Fig. 5.6. The circuit consists of a differential pair to provide the necessary gain and compensation network to ensure circuit stability.

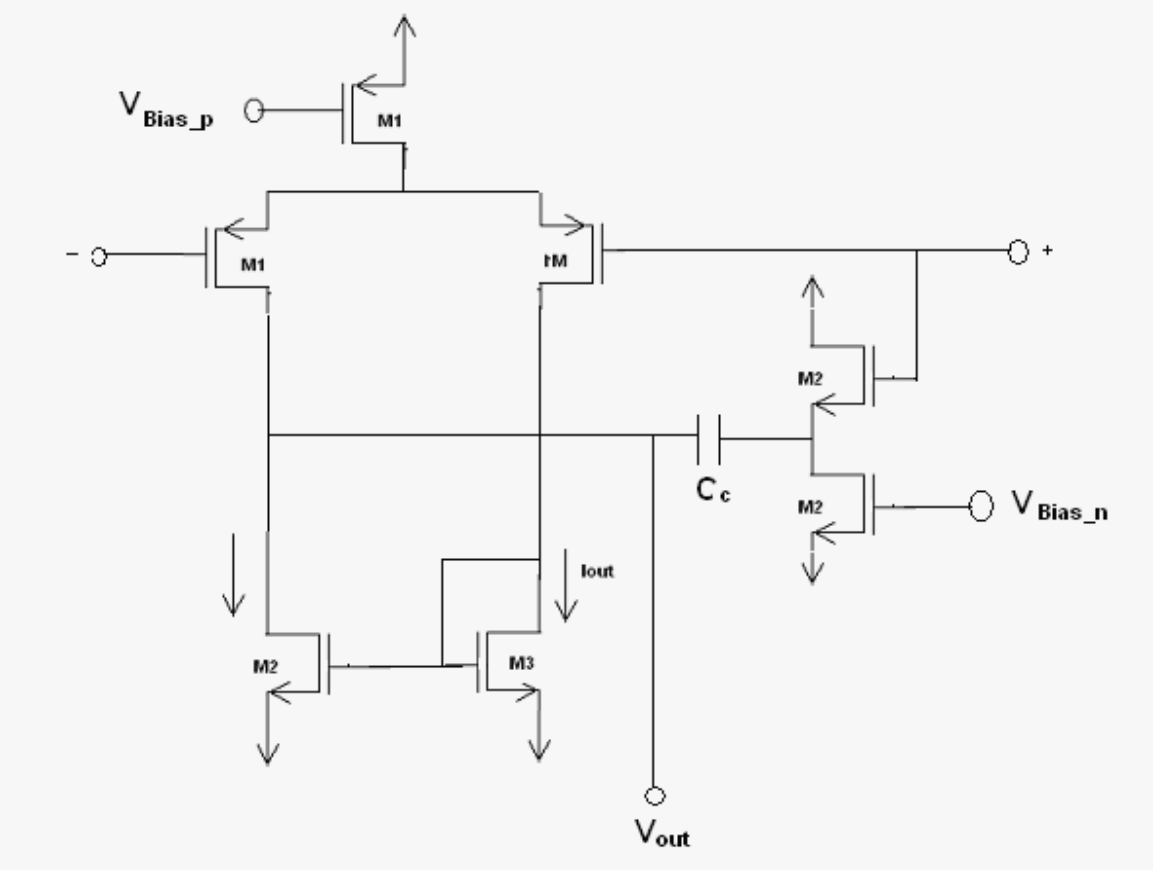


Fig. 5.6 Schematic of the amplifier used for active current mirror

A bit cell designed using the active current mirror is illustrated in Fig. 5.7.For proper operation, both active mirrors should be biased at the same potential and this potential should be equal to the comparator threshold voltage. Such a biasing arrangement ensures that the input and output devices for each current mirror will have the same drain-to-source potential. Ideally, for matched n- and p- channel devices, the bias point should be midway between the two supplies ($\pm V_{DD}/2$) allowing gate voltages as high as $V_{DD}/2 = |V_T|$ to be used. Hence the active current mirror's maximum gate voltage $V_{DD}/2 = |V_T|$, will be higher than was allowed for the basic current mirror, which was $V_{DD}/2 + |V_T|/2$, by $|V_T|/2$. Therefore, the effect of the

devices' finite r_o is minimized without restricting the mirror's dynamic range.

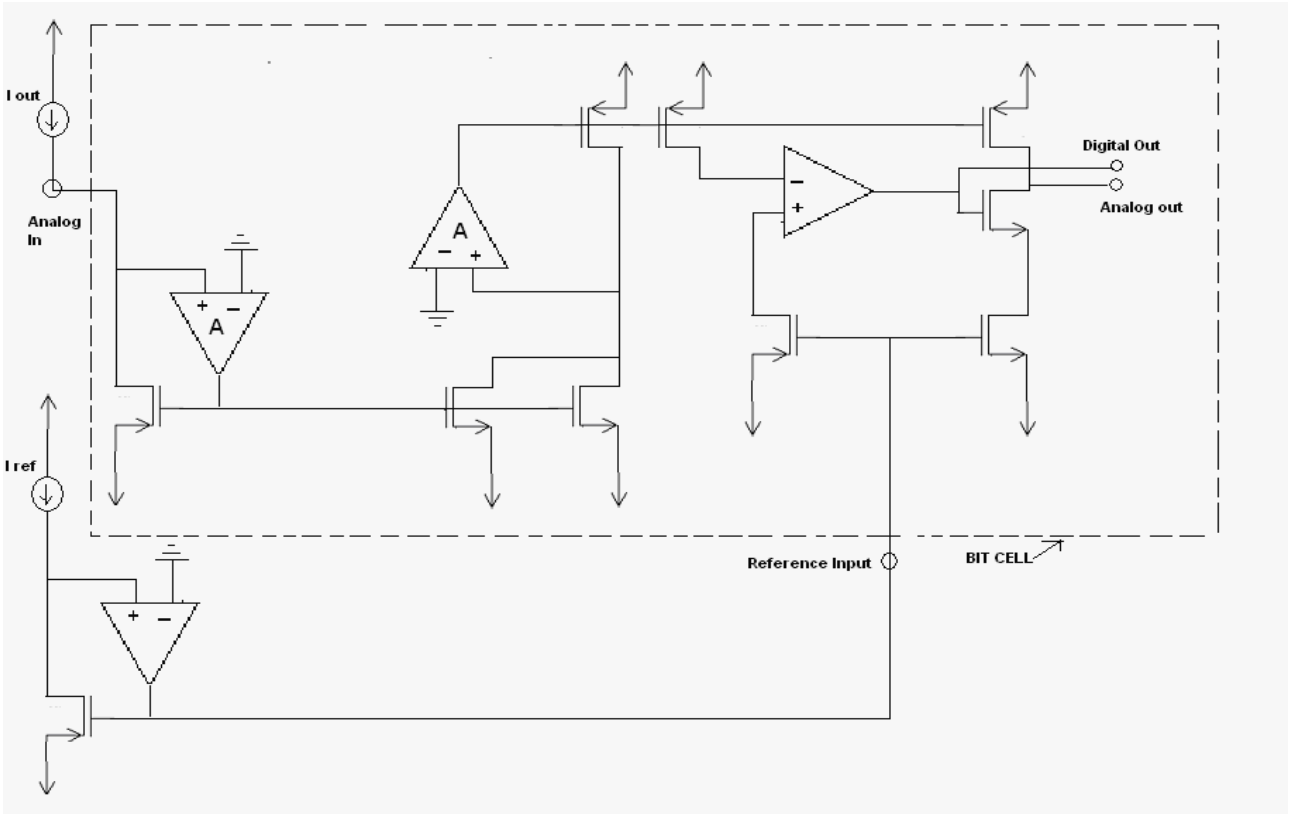


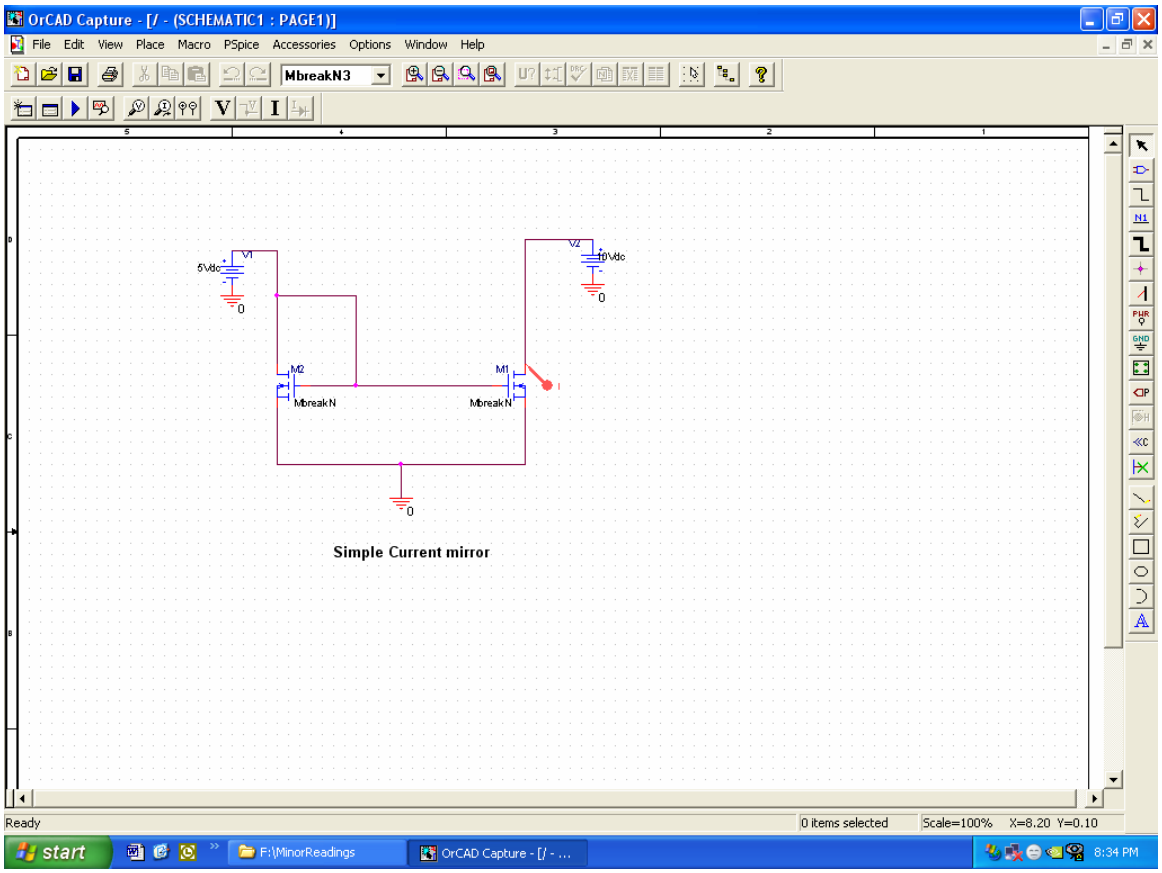
Fig. 5.7 Bit Cell for a current-mode ADC using active current mirrors.

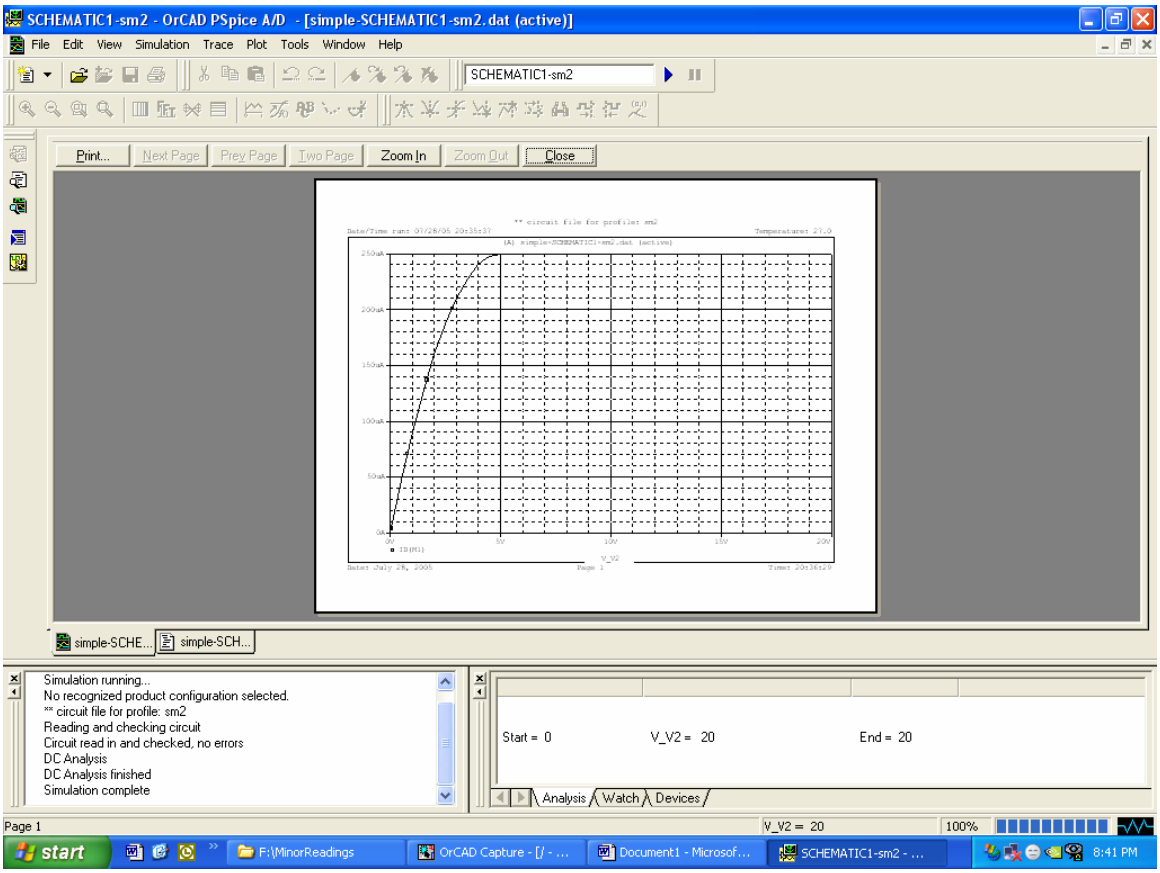
Along with improved performance, the active current mirrors simplify the ADC operation. Previously, the voltage at the circuit input was dependent on the current level and, as a result, a very high resistance current source was required to drive the input if accurate conversions were desired. By using active current mirrors, both the signal input and the reference input terminals have almost zero input resistance, and relatively low resistance current sources can be used to drive the ADC without reducing the converter accuracy.

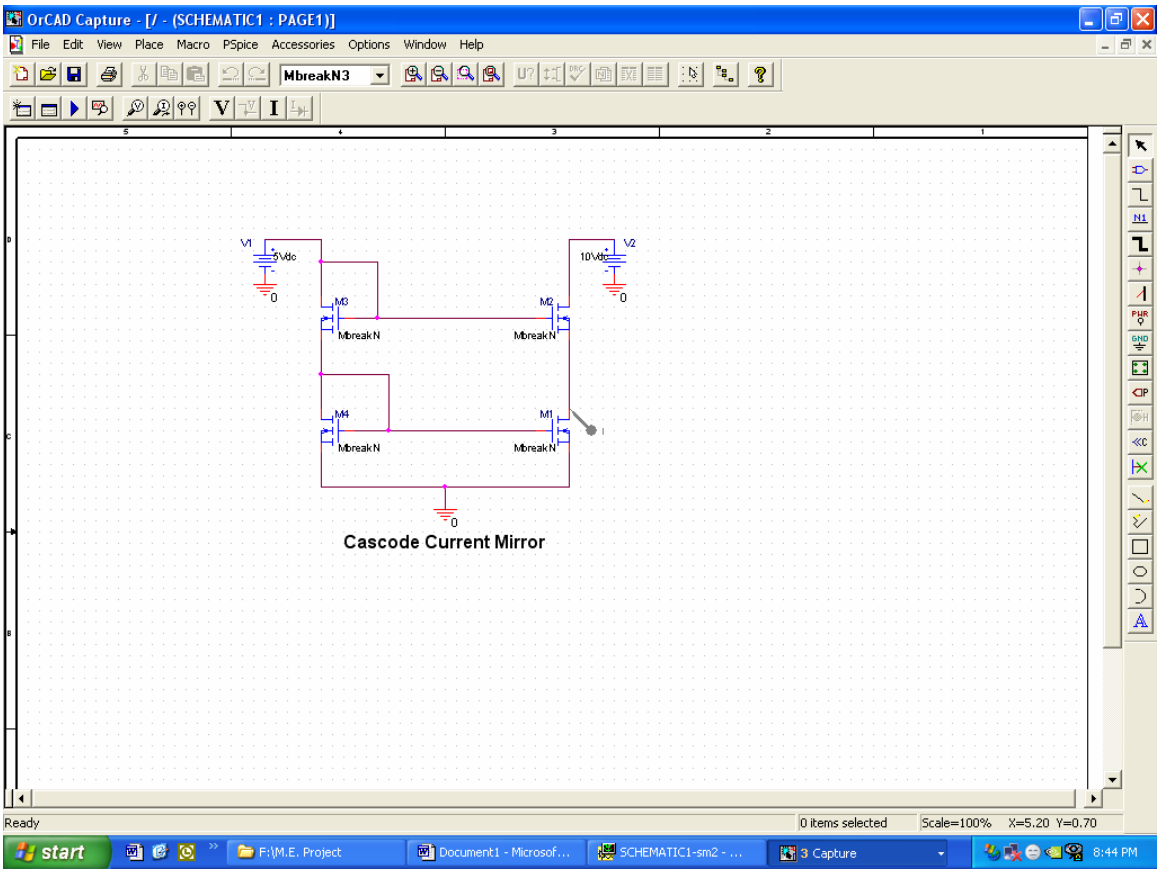
Chapter 6: Simulation Results

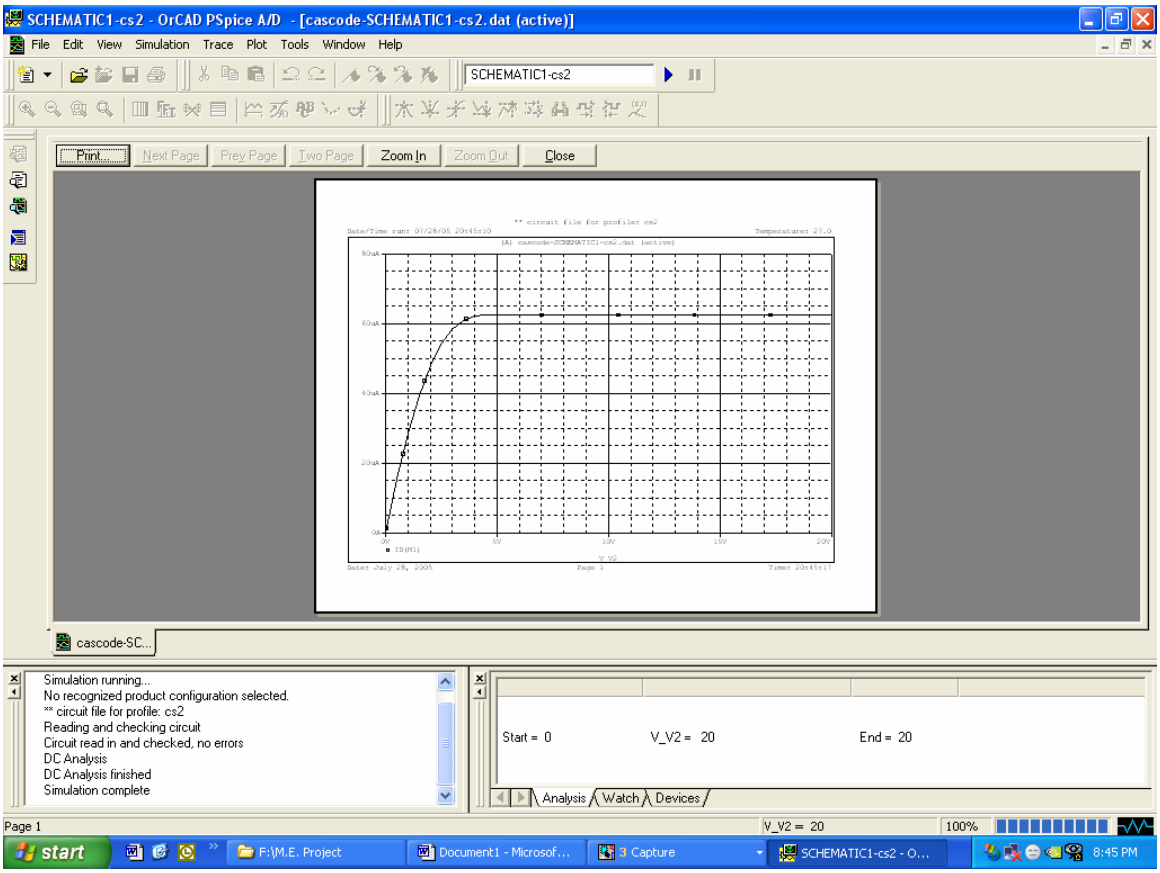
Four different 1-b ADC circuits have been designed. The first circuit uses the basic current mirror and the basic current comparator. The second circuit uses a cascoded current mirror and the basic current comparator to implement a bit cell. The circuit uses the cascoded current mirror along with the current comparator with inverter output. The fourth circuit uses an active current mirror with a basic current comparator at the output.

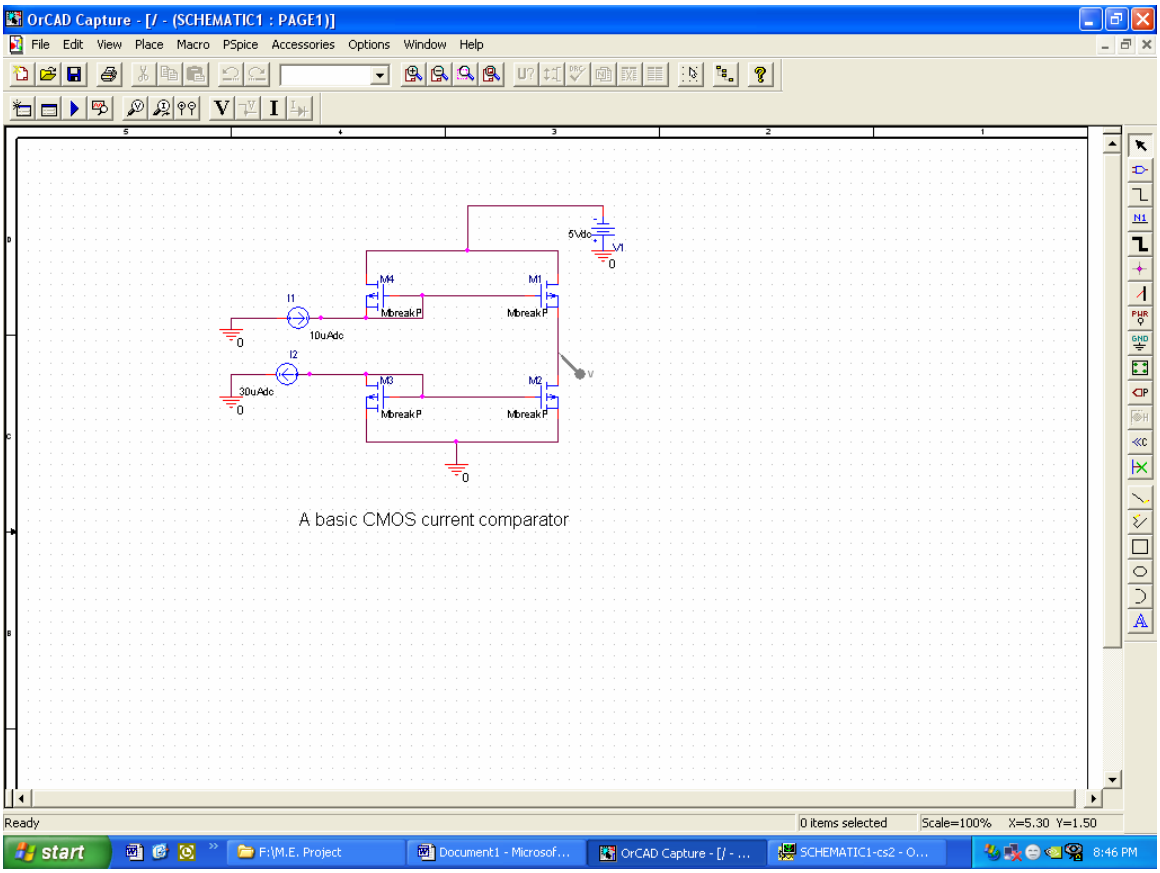
Before testing the ADC, the performance of the current mirrors itself was assessed.

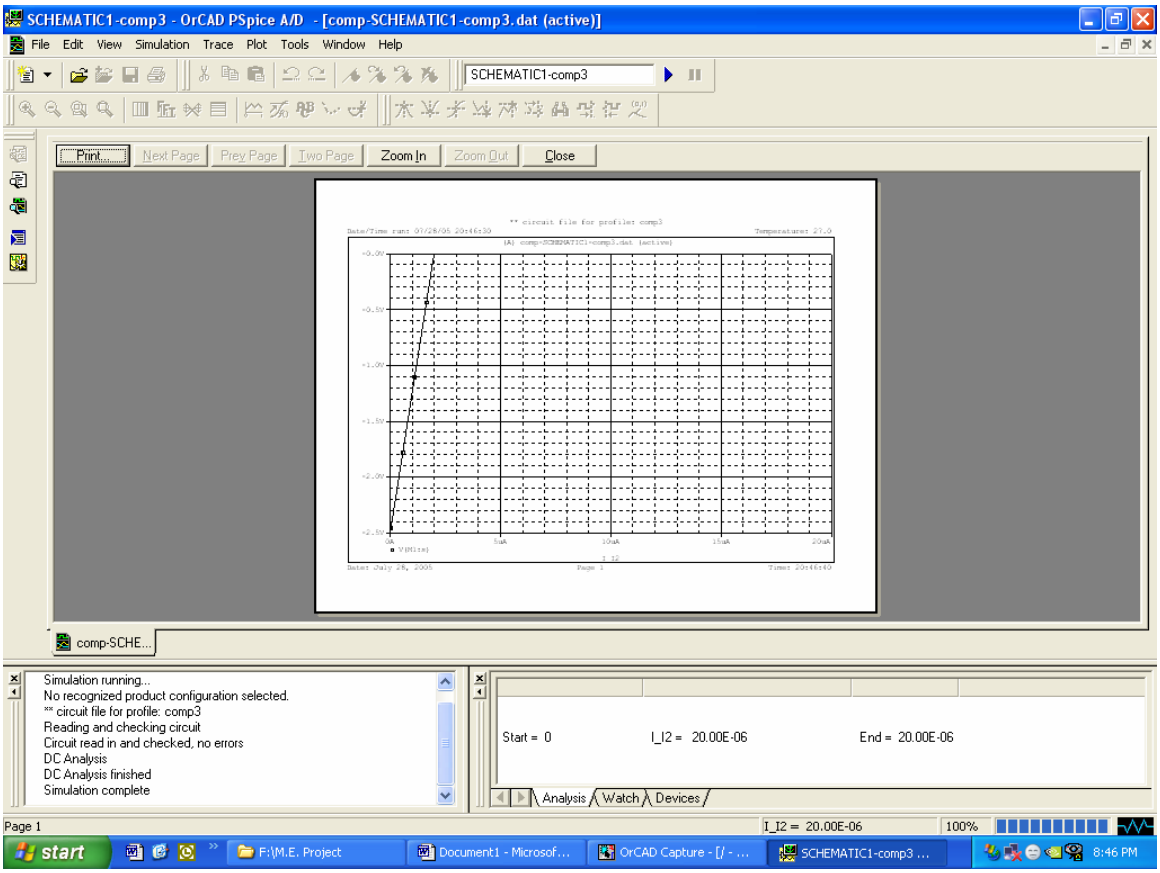

OrCAD Capture - [/ - (SCHEMATIC1 : PAGE1)]
File Edit View Place Macro PSpice Accessories Options Window Help
MbreakN3
V1
5Vdc
0
V2
10Vdc
0
M2
MbreakN
M1
MbreakN
0
Simple Current mirror
Ready
0 items selected
Scale=100%
X=8.20 Y=0.10
start
F:\MinorReadings
OrCAD Capture - [/ - ...
8:34 PM

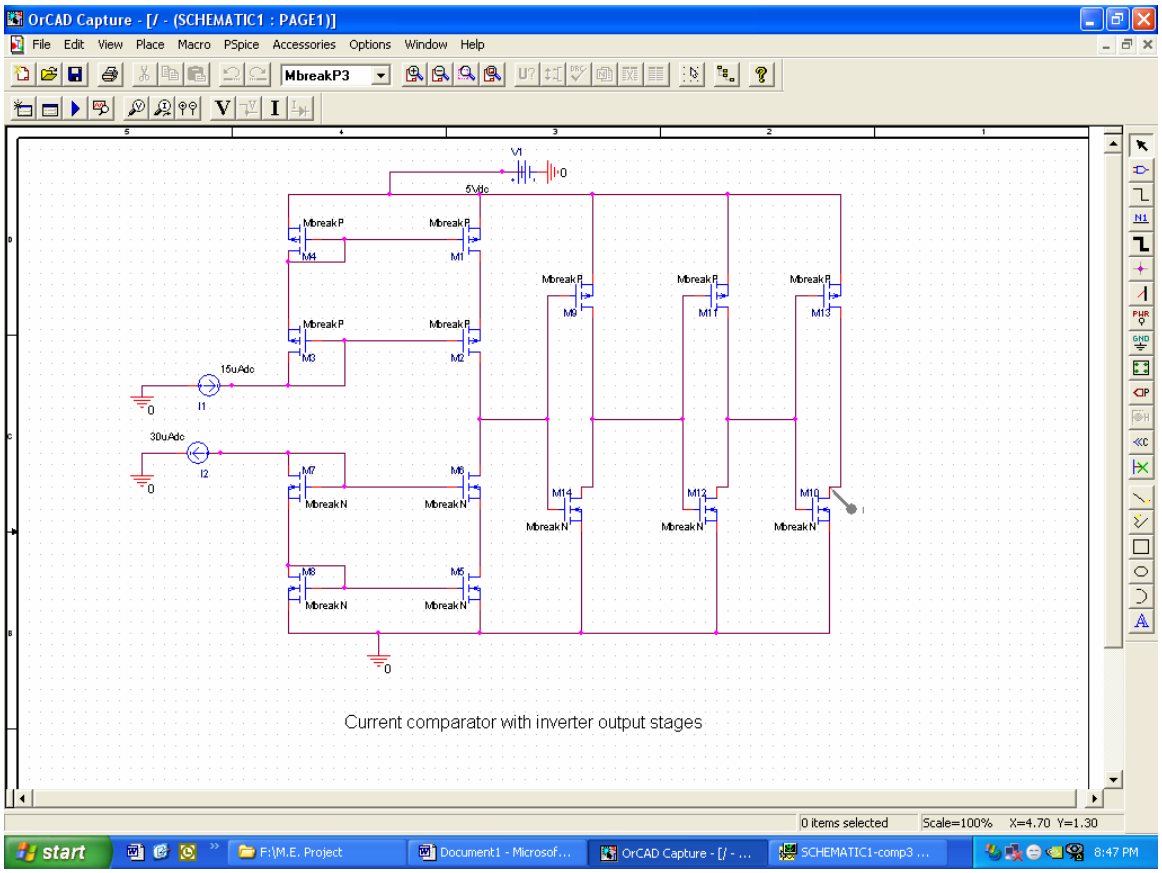

SCHEMATIC1-sm2 - OrCAD PSpice A/D - [simple-SCHEMATIC1-sm2.dat (active)]
File Edit View Simulation Trace Plot Tools Window Help
SCHEMATIC1-sm2
Print... Next Page Prev Page Two Page Zoom In Zoom Out Close
** circuit file for profiler sm2
simple-SCHE... simple-SCH...
Simulation running...
No recognized product configuration selected.
** circuit file for profile: sm2
Reading and checking circuit
Circuit read in and checked, no errors
DC Analysis
DC Analysis finished
Simulation complete
Start = 0
V_V2 = 20
End = 20
Analysis Watch Devices
Page 1
V_V2 = 20
100%
start
F:\MinorReadings
OrCAD Capture - [/ - ...
Document1 - Microsof...
SCHEMATIC1-sm2 - ...
8:41 PM

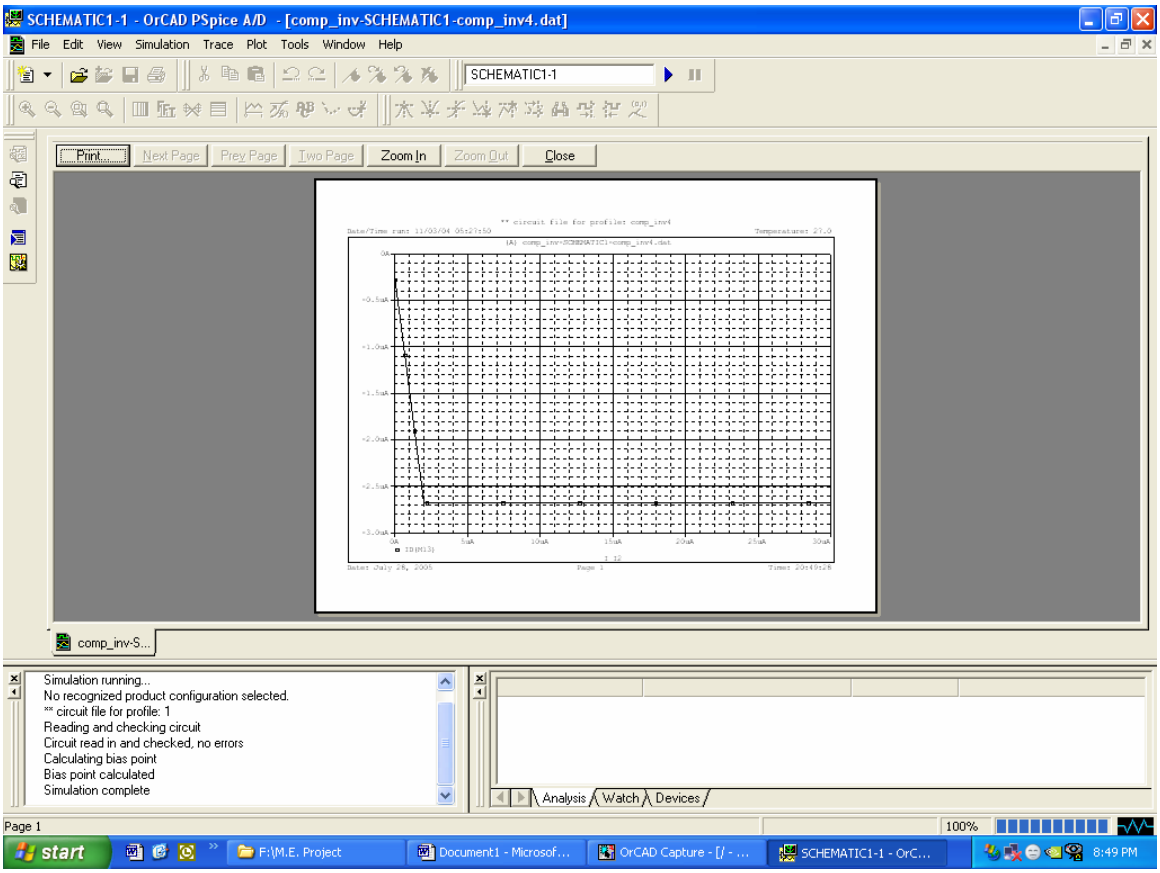

OrCAD Capture - [/ - (SCHEMATIC1 : PAGE1)]
File Edit View Place Macro PSpice Accessories Options Window Help
MbreakN3
V1
5Vdc
0
V2
10Vdc
0
M3
MbreakN
M2
MbreakN
M4
MbreakN
M1
MbreakN
0
Cascode Current Mirror
Ready
0 items selected
Scale=100%
X=5.20 Y=0.70
start
F:\M.E. Project
Document1 - Microsof...
SCHEMATIC1-sm2 - ...
3 Capture
8:44 PM

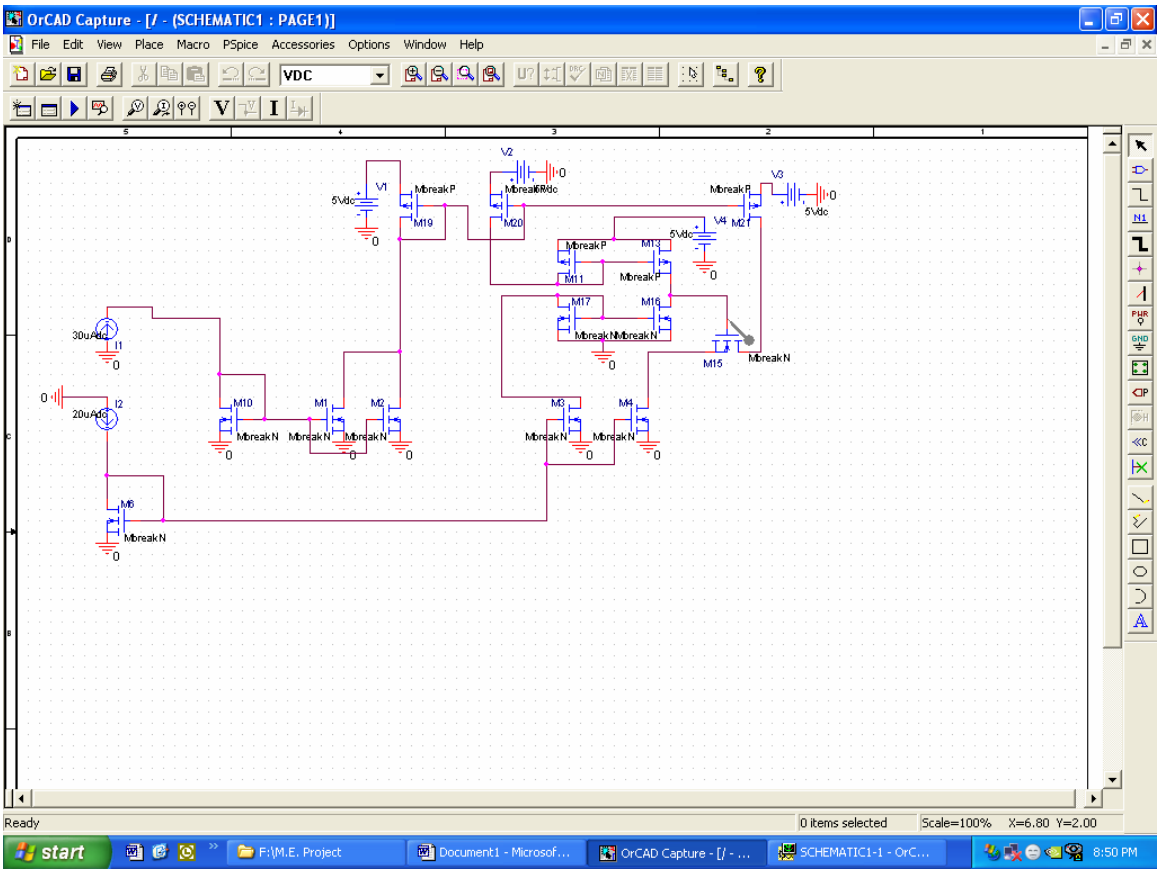

SCHEMATIC1-cs2 - OrCAD PSpice A/D - [cascode-SCHEMATIC1-cs2.dat (active)]
File Edit View Simulation Trace Plot Tools Window Help
SCHEMATIC1-cs2
Print... Next Page Prev Page Two Page Zoom In Zoom Out Close
cascode-SC...
Simulation running...
No recognized product configuration selected.
** circuit file for profile: cs2
Reading and checking circuit
Circuit read in and checked, no errors
DC Analysis
DC Analysis finished
Simulation complete
Start = 0
V_V2 = 20
End = 20
Analysis Watch Devices
Page 1
V_V2 = 20
100%
start
F:\M.E. Project
Document1 - Microsof...
3 Capture
SCHEMATIC1-cs2 - O...
8:45 PM

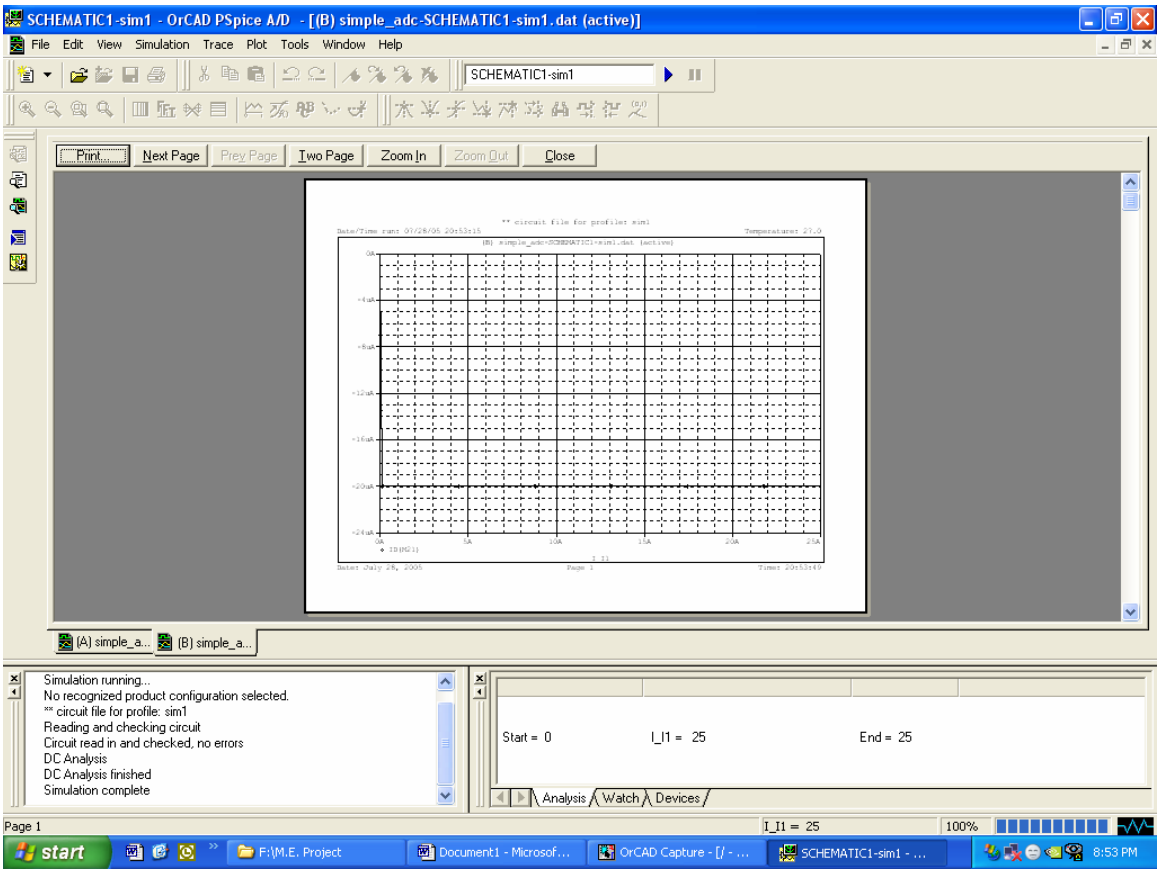

OrCAD Capture - [/ - (SCHEMATIC1 : PAGE1)]
File Edit View Place Macro PSpice Accessories Options Window Help
5Vdc
V1
0
M4
M1
I1
MbreakP
MbreakP
10uAdc
0
I2
M3
M2
30uAdc
MbreakP
MbreakP
0
0
A basic CMOS current comparator
Ready
0 items selected
Scale=100%
X=5.30 Y=1.50
start
F:\M.E. Project
Document1 - Microsof...
OrCAD Capture - [/ - ...
SCHEMATIC1-cs2 - O...
8:46 PM

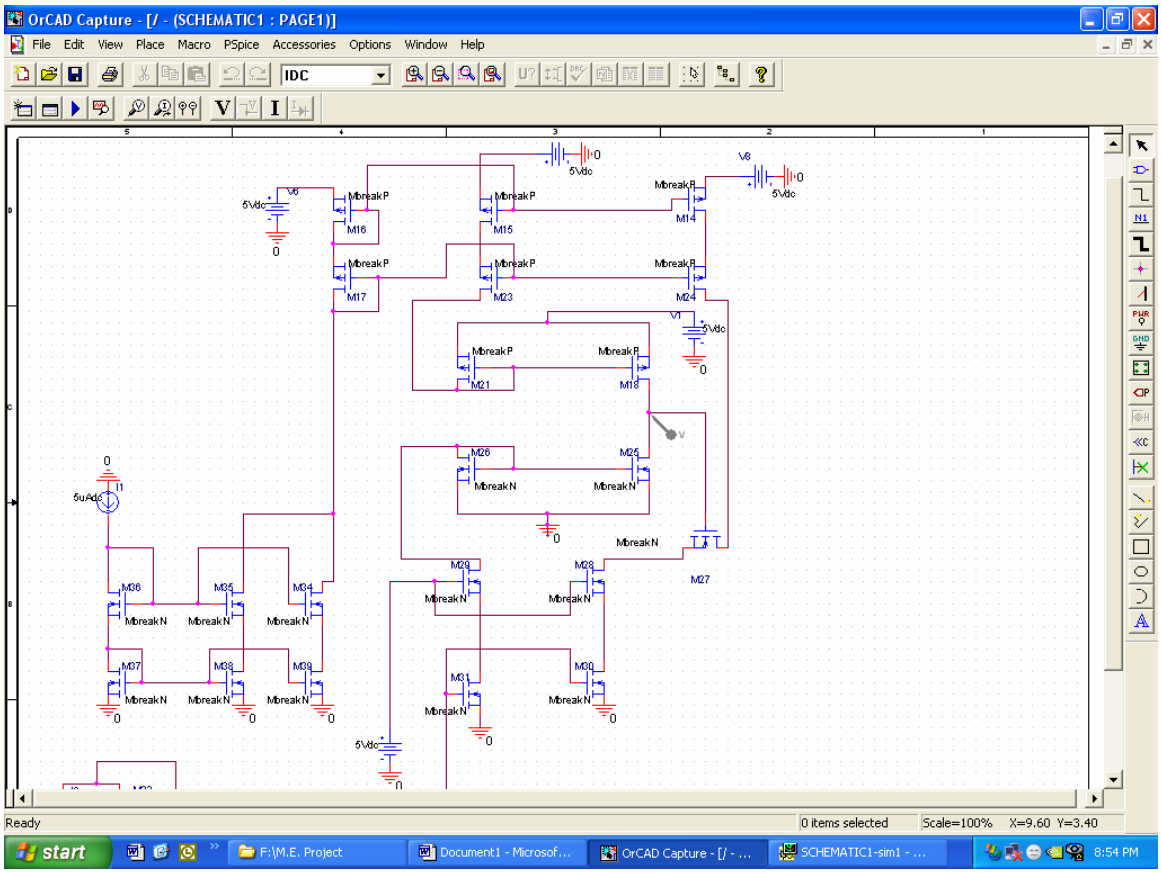

SCHEMATIC1-comp3 - OrCAD PSpice A/D - [comp-SCHEMATIC1-comp3.dat (active)]
File Edit View Simulation Trace Plot Tools Window Help
SCHEMATIC1-comp3
Print
Next Page
Prev Page
Two Page
Zoom In
Zoom Out
Close
comp-SCHE...
Simulation running...
No recognized product configuration selected.
** circuit file for profile: comp3
Reading and checking circuit
Circuit read in and checked, no errors
DC Analysis
DC Analysis finished
Simulation complete
Start = 0
I_I2 = 20.00E-06
End = 20.00E-06
Analysis
Watch
Devices
Page 1
I_I2 = 20.00E-06
100%
start
F:\M.E. Project
Document1 - Microsof...
OrCAD Capture - [/ - ...
SCHEMATIC1-comp3 ...
8:46 PM

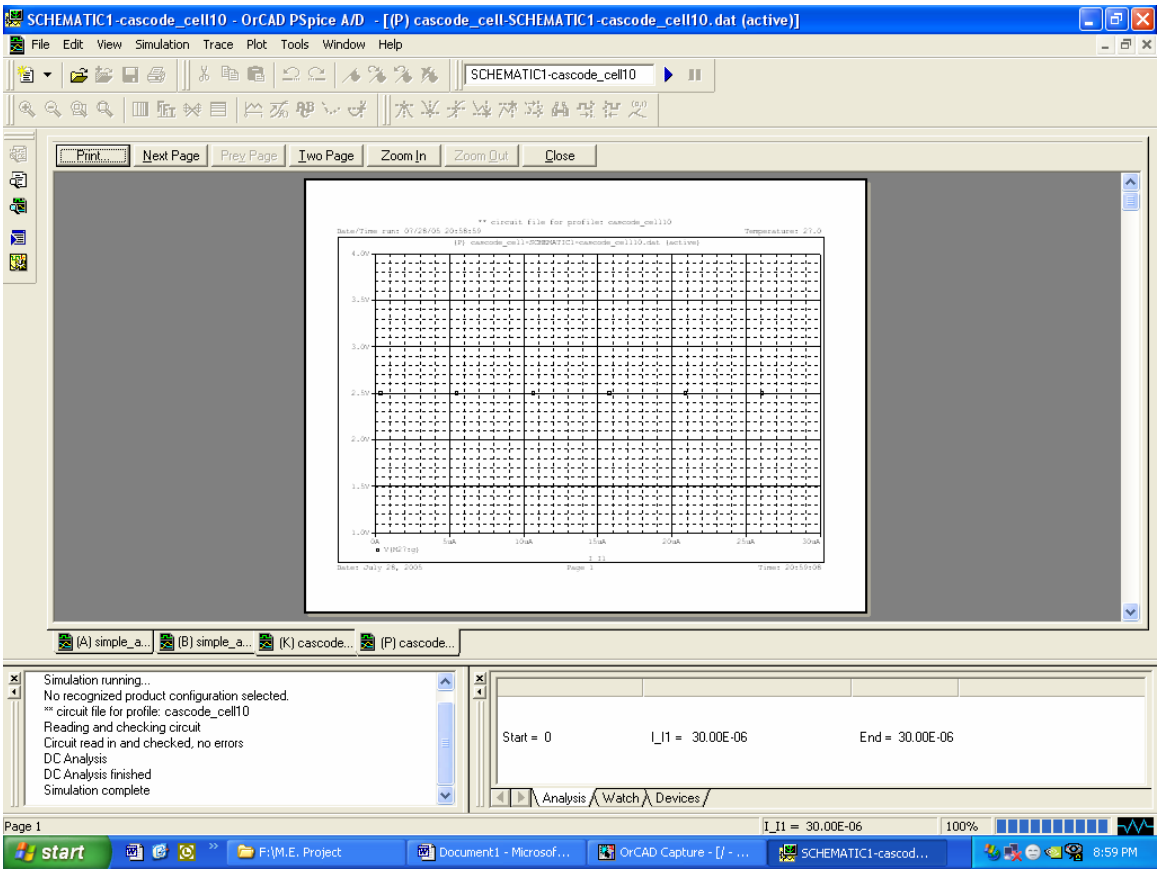

OrCAD Capture - [/ - (SCHEMATIC1 : PAGE1)]
File Edit View Place Macro PSpice Accessories Options Window Help
MbreakP3
V1
0
5Vdc
MbreakP
M4
M1
M3
M2
M9
M11
M13
15uAdc
I1
30uAdc
I2
M7
M6
M8
M5
MbreakN
M14
M12
M10
Current comparator with inverter output stages
0 items selected
Scale=100%
X=4.70 Y=1.30
start
F:\M.E. Project
Document1 - Microsof...
OrCAD Capture - [/ - ...
SCHEMATIC1-comp3 ...
8:47 PM

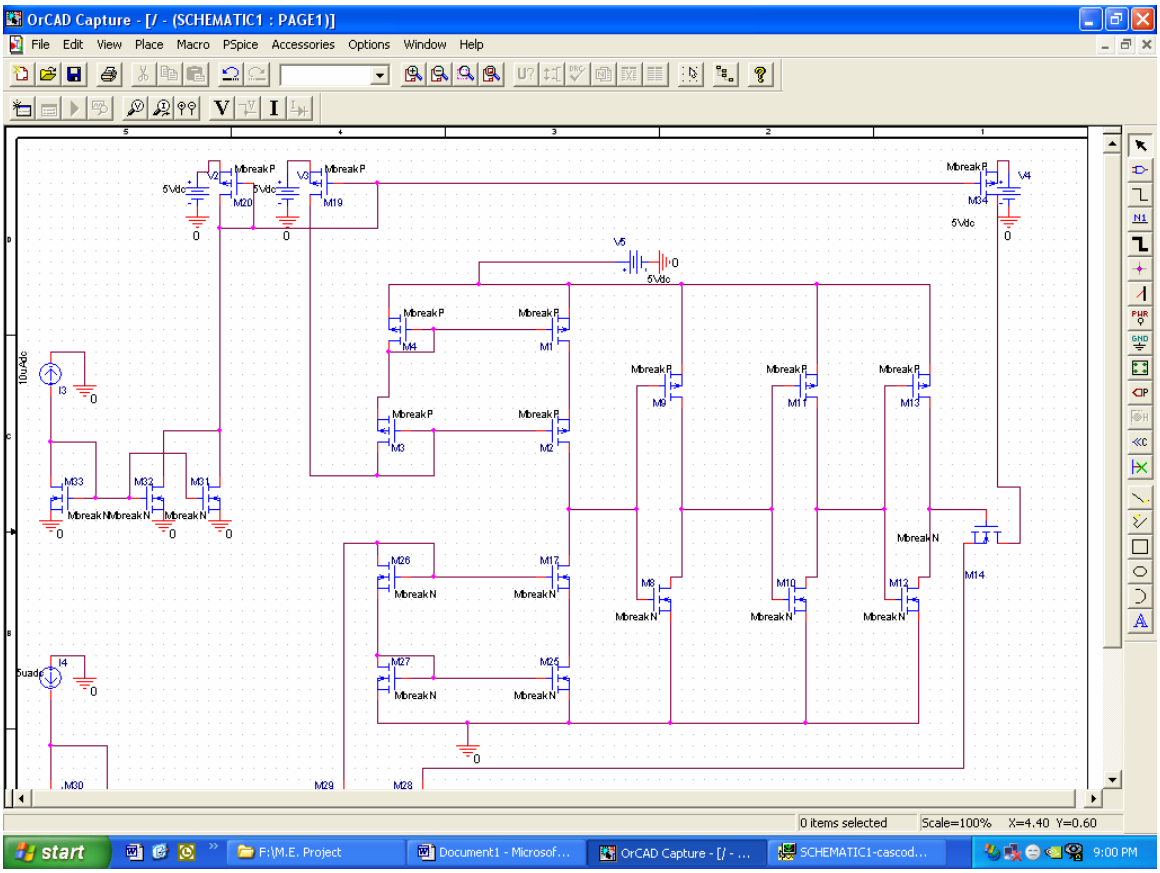

SCHEMATIC1-1 - OrCAD PSpice A/D - [comp_inv-SCHEMATIC1-comp_inv4.dat]
File Edit View Simulation Trace Plot Tools Window Help
SCHEMATIC1-1
Print
Next Page
Prev Page
Two Page
Zoom In
Zoom Out
Close
comp_inv-S...
Simulation running...
No recognized product configuration selected.
** circuit file for profile: 1
Reading and checking circuit
Circuit read in and checked, no errors
Calculating bias point
Bias point calculated
Simulation complete
Analysis
Watch
Devices
Page 1
100%
start
F:\M.E. Project
Document1 - Microsof...
OrCAD Capture - [/ - ...
SCHEMATIC1-1 - OrC...
8:49 PM

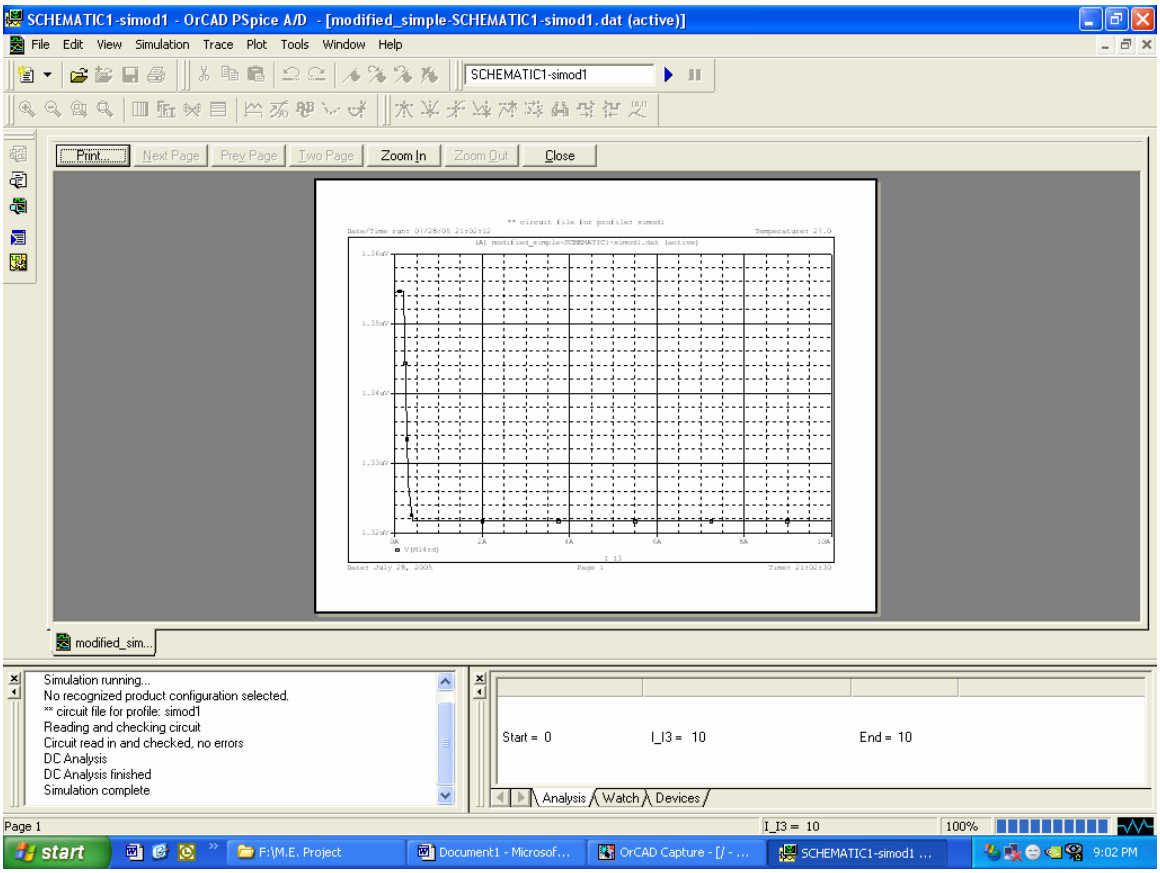

OrCAD Capture - [/ - (SCHEMATIC1 : PAGE1)]
File Edit View Place Macro PSpice Accessories Options Window Help
VDC
V1
V2
V3
V4
5Vdc
I1
I2
30uAdc
20uAdc
M1
M2
M3
M4
M6
M10
M11
M13
M15
M16
M17
M19
M20
M21
MbreakP
MbreakN
Ready
0 items selected
Scale=100%
X=6.80 Y=2.00
start
F:\M.E. Project
Document1 - Microsof...
OrCAD Capture - [/ - ...
SCHEMATIC1-1 - OrC...
8:50 PM

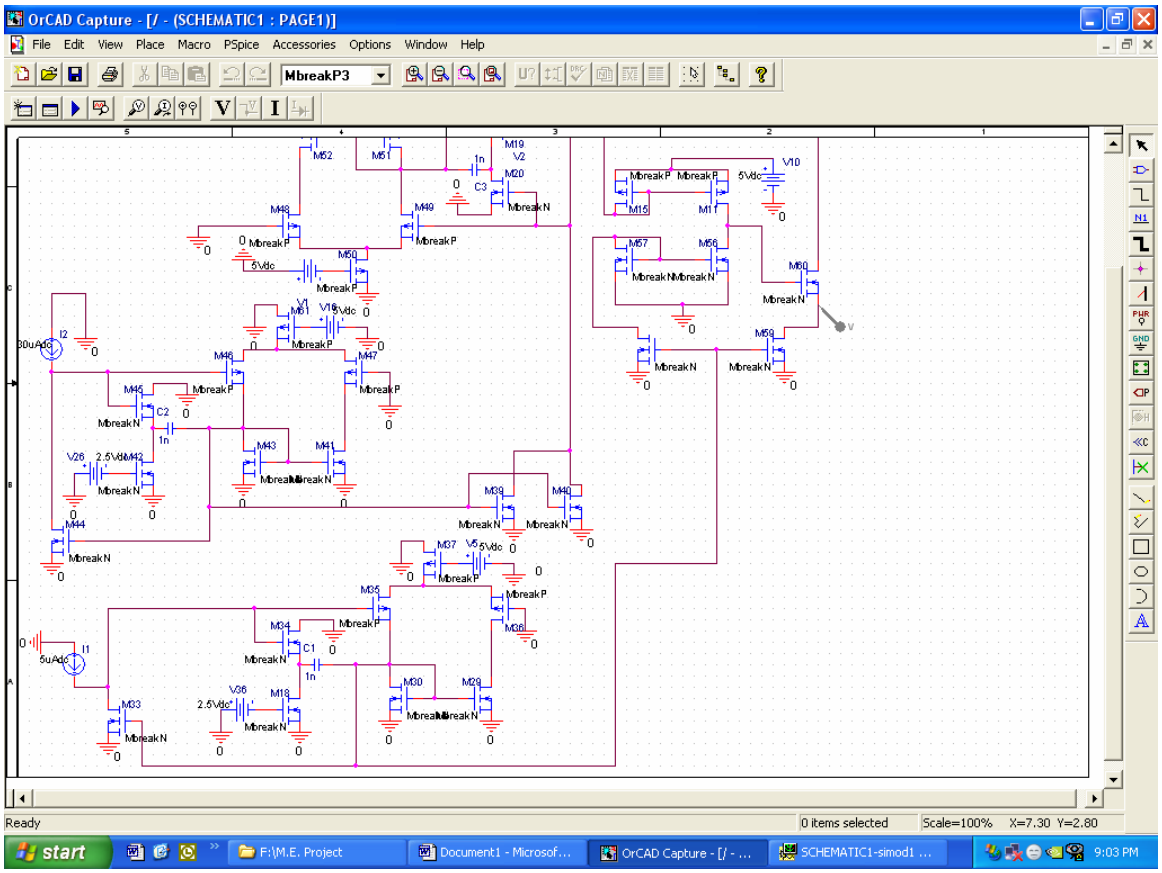

SCHEMATIC1-sim1 - OrCAD PSpice A/D - [(B) simple_adc-SCHEMATIC1-sim1.dat (active)]
File Edit View Simulation Trace Plot Tools Window Help
SCHEMATIC1-sim1
Print
Next Page
Prev Page
Two Page
Zoom In
Zoom Out
Close
(A) simple_a...
(B) simple_a...
Simulation running...
No recognized product configuration selected.
** circuit file for profile: sim1
Reading and checking circuit
Circuit read in and checked, no errors
DC Analysis
DC Analysis finished
Simulation complete
Start = 0
I_I1 = 25
End = 25
Analysis
Watch
Devices
Page 1
I_I1 = 25
100%
start
F:\M.E. Project
Document1 - Microsof...
OrCAD Capture - [/ - ...
SCHEMATIC1-sim1 - ...
8:53 PM

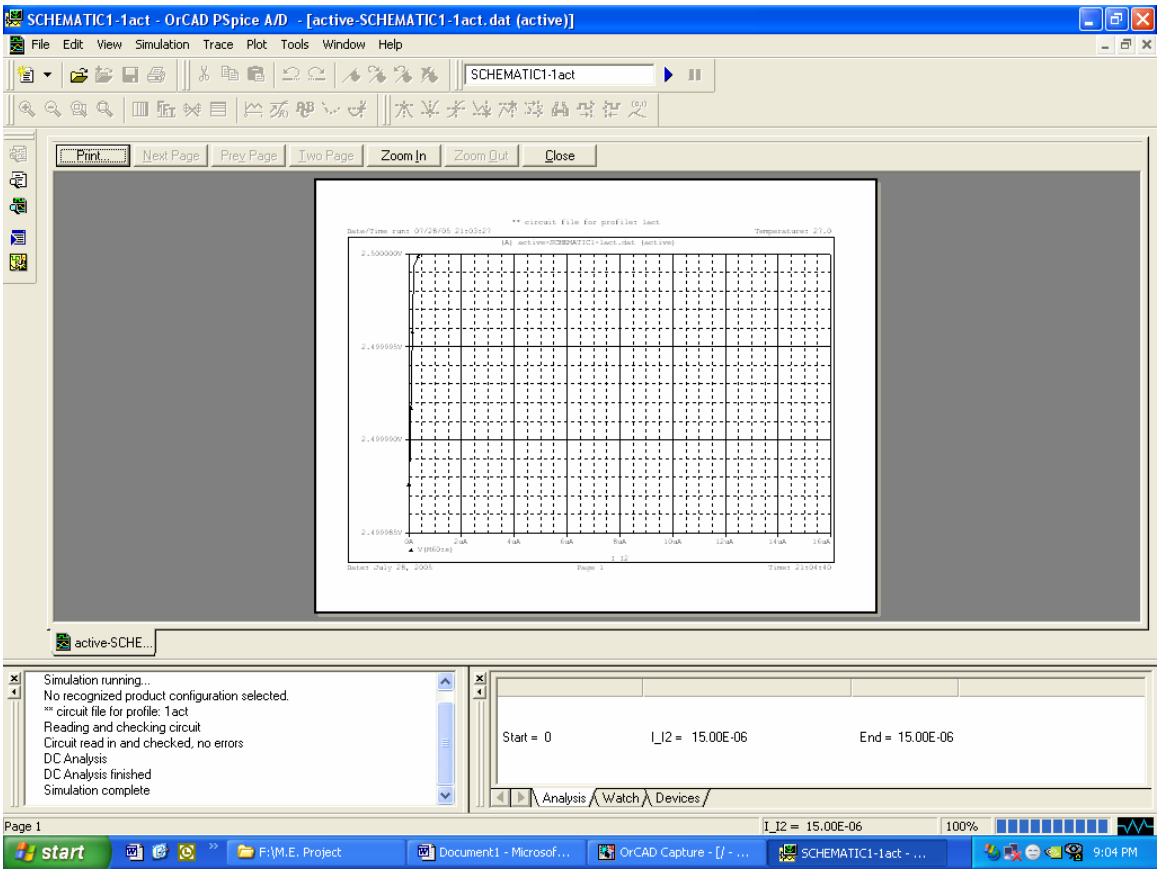

OrCAD Capture - [/ - (SCHEMATIC1 : PAGE1)]
File Edit View Place Macro PSpice Accessories Options Window Help
IDC
5Vdc
MbreakP
MbreakN
M16
M15
M14
M17
M23
M24
M21
M18
M26
M25
M27
M29
M28
M36
M35
M34
M37
M38
M39
M31
M30
5uAdc
I1
V6
V8
V1
Ready
0 items selected
Scale=100%
X=9.60 Y=3.40
start
F:\M.E. Project
Document1 - Microsof...
OrCAD Capture - [/ - ...
SCHEMATIC1-sim1 - ...
8:54 PM


SCHEMATIC1-cascode_cell10 - OrCAD PSpice A/D - [(P) cascode_cell-SCHEMATIC1-cascode_cell10.dat (active)]
File Edit View Simulation Trace Plot Tools Window Help
SCHEMATIC1-cascode_cell10
Print
Next Page
Prev Page
Two Page
Zoom In
Zoom Out
Close
(A) simple_a...
(B) simple_a...
(K) cascode...
(P) cascode...
Simulation running...
No recognized product configuration selected.
** circuit file for profile: cascode_cell10
Reading and checking circuit
Circuit read in and checked, no errors
DC Analysis
DC Analysis finished
Simulation complete
Start = 0
I_I1 = 30.00E-06
End = 30.00E-06
Analysis
Watch
Devices
Page 1
I_I1 = 30.00E-06
100%
start
F:\M.E. Project
Document1 - Microsof...
OrCAD Capture - [/ - ...
SCHEMATIC1-cascod...
8:59 PM


OrCAD Capture - [/ - (SCHEMATIC1 : PAGE1)]
File Edit View Place Macro PSpice Accessories Options Window Help
MbreakP
MbreakN
5Vdc
10uAdc
5uadc
M1
M2
M3
M4
M9
M11
M13
M14
M17
M19
M20
M25
M26
M27
M28
M29
M30
M31
M32
M33
M34
I3
I4
V2
V3
V4
V5
0 items selected
Scale=100%
X=4.40 Y=0.60
start
F:\M.E. Project
Document1 - Microsof...
OrCAD Capture - [/ - ...
SCHEMATIC1-cascod...
9:00 PM


SCHEMATIC1-simod1 - OrCAD PSpice A/D - [modified_simple-SCHEMATIC1-simod1.dat (active)]
File Edit View Simulation Trace Plot Tools Window Help
SCHEMATIC1-simod1
Print... Next Page Prev Page Two Page Zoom In Zoom Out Close
modified_sim...
Simulation running...
No recognized product configuration selected.
** circuit file for profile: simod1
Reading and checking circuit
Circuit read in and checked, no errors
DC Analysis
DC Analysis finished
Simulation complete
Start = 0
I_I3 = 10
End = 10
Analysis Watch Devices
Page 1
I_I3 = 10
100%
start
F:\M.E. Project
Document1 - Microsof...
OrCAD Capture - [/ - ...
SCHEMATIC1-simod1 ...
9:02 PM


OrCAD Capture - [/ - (SCHEMATIC1 : PAGE1)]
File Edit View Place Macro PSpice Accessories Options Window Help
MbreakP3
Ready
0 items selected
Scale=100% X=7.30 Y=2.80
start
F:\M.E. Project
Document1 - Microsof...
OrCAD Capture - [/ - ...
SCHEMATIC1-simod1 ...
9:03 PM


SCHEMATIC1-1act - OrCAD PSpice A/D - [active-SCHEMATIC1-1act.dat (active)]
File Edit View Simulation Trace Plot Tools Window Help
SCHEMATIC1-1act
Print... Next Page Prev Page Two Page Zoom In Zoom Out Close
active-SCHE...
Simulation running...
No recognized product configuration selected.
** circuit file for profile: 1act
Reading and checking circuit
Circuit read in and checked, no errors
DC Analysis
DC Analysis finished
Simulation complete
Start = 0
I_I2 = 15.00E-06
End = 15.00E-06
Analysis Watch Devices
Page 1
I_I2 = 15.00E-06
100%
start
F:\M.E. Project
Document1 - Microsof...
OrCAD Capture - [/ - ...
SCHEMATIC1-1act - ...
9:04 PM

Chapter 7: Conclusion

The performance of current-mode algorithmic ADCs has been shown to be dependent on the type of current-mirror used in the design. When a basic current mirror is used, relatively small circuits can be made. Unfortunately, inaccuracies in the subtraction operation limit converters of this type to low resolutions. Cascode mirror will eliminate the subtraction problem and their higher output resistance allows shorter channel length devices to be used, thereby providing higher operating speeds as well. Unfortunately, the cascode mirror's limited dynamic range will not allow one to take full advantage of the device matching accuracy. The active current mirrors have a dynamic range comparable to that of the basic current mirror and yet do not suffer from the effects of the device's finite r_o. Hence, the active current mirror can be used to achieve resolutions comparable to that of the device mismatches. The active current mirror's only significant drawback is its higher power consumption. Consequently, the basic current mirror and the cascode mirror configurations are better suited for low-power, low resolution converters, while the active current mirror configurations are better suited for higher resolution, higher speed converters.

Chapter 8: References

1. J. Sarao, H.H.L. Kwok, "Current Mode Building Blocks and their application in ADCs,"PACRIM. 2001 IEEE Pacific Rim Conference on Communications, Computers and signal Processing, Volume: 1, 26-28 Aug. 2001 Pages: 283 - 286 vol.1.
2. D. G. Nairn, A.T. Salma, "Current-Mode Alogorithmic Analog-to-Digital Converters," *IEEE J. Solid-State Circuits*, vol.25, pp.997-1004, August 1990.
3. Veepsa Bhatia, Neeta Pandey, H.M. Rai, "Improving Signal Processing with ADC's based on Current mode Algorithm", National Conference Sant Longowal Institute of Engineering and Technology, Nov. 2003.
4. Veepsa Bhatia, Neeta Pandey, "Improving Signal Processing in ADC's :A current mode approach", National Conference on VLSI Design and Technology, Bharati Vidyapeeth's College of Engg., pp 50-54, April 2004.
5. P.W.Li, M. J. Chin, P.R. Gray "A Ratio-independent Algorithmic Analog-to-Digital Conversion Technique," *IEEE J. Solid-State Circuits*, vol.19, pp.828-836, December 1984.
6. N. Oki, J.D. Soldera, "An Algorithmic of Analog-to-Digital Converter using Current-mode and Digital CMOS process," *1998 Midwest Symposium on Systems and circuits*, August 09-12, 1998, South Bend, Indiana.
7. G. Palmisano and G. Palumbo, "Offset-compensated low-power current comparator," *Electronics Letters*, vol.30, No. 20, Sep. 1994.

8. C. Wang, M. Ahmad and M. Swamy, "Low-power current comparator cell for weak current operation," *Proceedings of IEEE International Symposium on Circuits and Systems*, vol.1, pp.544-547, 2001.

9. A. Demosthenous and J. Taylor, "2.8 V asynchronous high-speed current comparator for sequence detection applications," *Electronics Letters*, vol. 34, no. 18, pp.1714-1715, Sep. 1998.

10. A. Boni, C. Morandi and S. Padoan, "2.5-V BiCMOS comparator with current-mode interpolation," *IEEE J. Solid-State Circuits*, vol.34, pp.892-897, June 1999.

11. A. Bony and C. Morandi," High-speed, low-power BiCMOS comparator using a PMOS variable load," *IEEE J. Solid-State Circuits*, vol.33, pp.143-146, Jan. 1998.

12. F. Kaess, B. Hochet, R. Kanan and M. Declercq, "High-speed GaAs Comparators for Low-power 8-bit ADCs," *IEEE J. Solid-State Circuits*, pp. 13-16, 1998.

13. M. Hafizi and J. F. Jensen, "Ultra-fast, Low-power Integrated Circuits in a scaled Submicron HBT IC technology," *IEEE Radio Frequency Integrated Circuit Symposium*, pp. 87-90, 1997.

14. M. Byung-moo and K. Soo-won, "High performance CMOS current comparator using resistive feedback network," *Electronics Letters*, vol. 34, No. 22, Oct. 1998.

15. J Sarao and H H L Kwok, "Current mode building blocks and their application in ADCs".

16. *CMOS Circuit Design, Layout and Simulation*, Baker, Li and Boyce, Prentice Hall of India publication.