

CHAPTER 1

INTRODUCTION

1.1 Introduction:

Information is the data or details related to an object or event. Signal carries the information about magnitude or time relating to an object or event i.e. physical quantity.

Output of a transducer is usually a voltage or some form of electrical signal. The two most important properties of voltage are its magnitude and frequency, though polarity may be considered in some cases. Many transducers develop low voltage of order of mV and some even of micro volts. A fundamental problem is to prevent this signal being contaminated by unwanted signals like noise due to an extraneous source which may interfere with original signal. Another problem is that a weak signal may be distorted by processing equipment. The signal after being sensed cannot be directly transmitted to the next stage without removing interfering sources, as otherwise highly distorted results may be obtained which are far from true. Many a times it becomes necessary to perform several operations before it is transmitted further. These processes may be linear like amplification, attenuation, integration, differentiation, addition, subtraction and filtering. Some nonlinear process like modulation, detection, sampling, chopping, clipping etc. are also performed on the signal to bring it to the desired form to be accepted at the next stage of a system. This process of conversion is called signal conditioning. The term signal processing includes many other functions in addition to variable conversion and variable manipulation. In fact the element that follows the primary sensing element in any instrument is called signal conditioning element. Signal processing/conditioning can be done in both analog as well as digital domain. In digital domain the signal processing is done with the help of microprocessors, digital signal processors or general purpose computers along with A/D and D/A converters whereas in analog domain the signal processing tasks are performed with the help of amplifiers resistors and capacitors. The amplifiers used may be a voltage amplifier, or a current amplifier, a transresistance amplifier or a transconductance amplifier. Some new amplifier configurations, which are derived from a combination of various basic amplifier topologies, have also been used in analog signal processing. Some of the signal processing schemes use single ended inputs and the output of these schemes is always ground referred whereas others use differential inputs and may give single ended/fully differential output.

1.2 An overview of the prominent developments in the area of analog circuits and signal processing:

In the following, we present a brief overview of only some of the important developments in the area of analog circuit design and signal processing. This overview is based on the material presented in [1]

The universal op-amp- Undoubtedly, the integrated circuit operational amplifier popularly known as op-amp has been the most important active building block of analog circuit design since long because of its very well understood architecture and versatility. In the area of analog circuits, almost everything can be done using op-amps. One can realize using op-amps, all linear circuits such as the four controlled sources (VCVS, VCCS, C CVS and CCCS), integrators, differentiators, summing and differencing amplifiers, variable-gain differential/ instrumentation amplifiers, filters, oscillators etc. Op-amps can also be used to realize a variety of non-linear functional circuits such as comparators, Schmitt trigger, sample and hold amplifiers, precision rectifiers, multi vibrators, log-antilog circuits and a variety of relaxation oscillators. Since op-amp based circuits invariably employed RC elements, such circuits posed difficulty in their realization in monolithic integrated form since resistors and hence, RC time constants, could not be implemented very precisely. Particularly, search for fully integrable filters did not find RC op amp filter circuits to be favourable candidates for this purpose. The circuit symbol and the port relation of the op-amp are shown in fig1.1

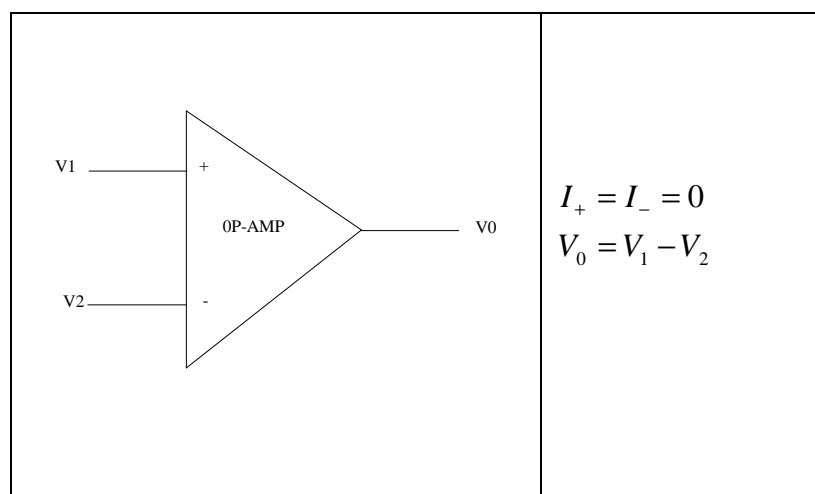


Fig. 1.1 (a) Symbol of OP-AMP, (b) Port relation

The operational Trans conductance Amplifier (OTA):-The OTA-C circuits employ only transconductors and capacitors to build various functional circuits and thus, do not require any resistors. Furthermore, since the internal circuits of OTAs also can be designed without using any resistors, the resulting circuits are completely resistor-less. Since the trans conductance of an OTA is electronically controllable through an external DC bias voltage/current, the resulting OTA-C circuits are suitable for realizing electronically controllable functions and were amenable to integration in both bipolar and CMOS technologies.

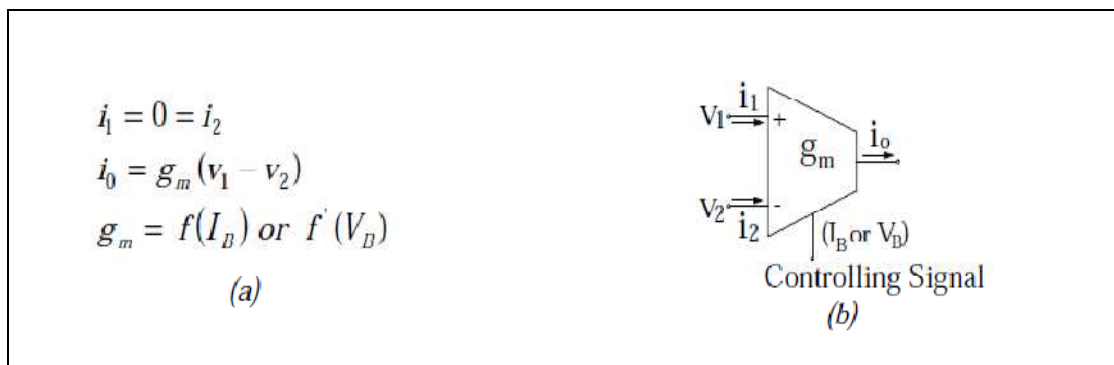
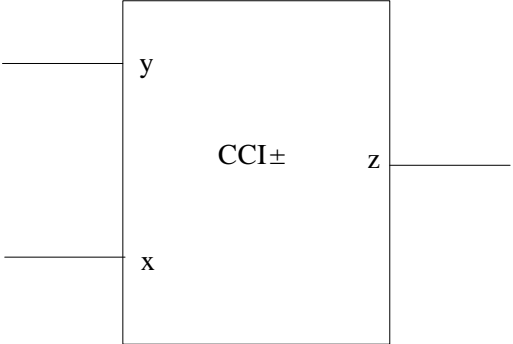
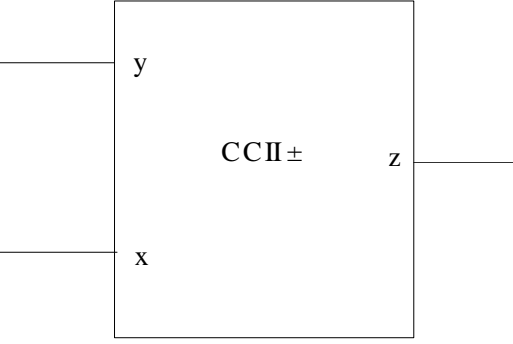


Fig. 1.2 (a) characterizing equation of OTA and, (b) notation of OTA

Current Conveyors- Current Conveyors (CC) introduced by Sedra and Smith during 1968-1970 [2] is the basic building block of a number of contemporary applications both in the current and the mixed modes. The principle of the current conveyor of the first generation was published in 1968 by K. C. Smith and A. S. Sedra in 1968. Two years later, today's widely used second-generation CCII was described in, and in 1995 [3] the third-generation CCIII [4] was introduced by Fabre and his co-workers. However, initially, during that time, the current conveyor did not find many applications because its advantages compared to the classical operational amplifier (Op Amp) were not widely appreciated and any IC implementation of Current Conveyors was not available commercially. An IC CC, namely PA630, was introduced by Wadsworth in 1989[5] (mass produced by Phototronics Ltd. of Canada) and about the same time, the now well known AD844 (operational transimpedance amplifier or more popularly known as a current feedback op-amp) was recognized to be internally a CCII+ followed by a voltage follower [6]. An excellent review of the state-of-the-

art of current-mode circuits prior to 1990 was provided by Wilson [7]. Today, the current conveyor is considered a universal analogue building block with wide spread applications in the current, voltage, and mixed mode signal processing. Its features find most applications in the current mode, when its so-called voltage input y is grounded and the current, flowing into the low-impedance input x , is copied by a simple current mirror into the z output.

Since 1995 in particular, many successive modifications and generalizations of the basic principle of CCII have appeared in literature.

	$I_Y = I_X$ $V_X = V_Y$ $I_Z = \pm I_X$
	$I_Y = 0$ $V_X = V_Y$ $I_Z = \pm I_X$

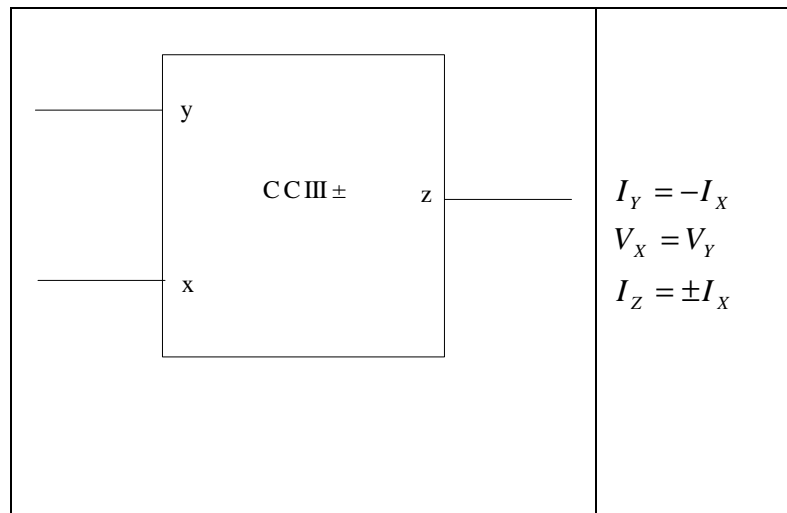


Fig. 1.3 Basic block and port relation of current conveyor

Current feedback amplifier- Current feedback amplifier popularly known as CFOA has been developed as a high speed operational amplifier which does not suffer from the slew rate limitations of the internally compensated voltage amplifier. Also the constant gain bandwidth product limitation of the voltage amplifier does not affect the CFOA as the bandwidth can be varied independent of the gain. Functionally the CFOA can be thought of as a cascade of a CCII+ and a voltage follower. This building block is gaining fast popularity in the signal processing community.

Operational transresistance amplifier, Current differencing buffered amplifier etc.- Operational transresistance amplifier (OTRA), Current differencing buffered amplifier (CDBA), CCCDBA, DC-CDBA, CDTA, CCCDTA, DC-CDTA, CTTA, CD-CTTA, CCTA, CCCCTA, DC-CCTA, OFA are some of the other recently proposed active building blocks that have been used in analog signal processing.

1.3 Single-ended versus fully balanced processing:

There is a real danger noise from extraneous sources tend to be injected into the analogue signal processing circuitry, where they may cause a serious deterioration of the signal noise ratio. The “noise” may be coupled into the filter either directly or via the substrate, the power supply, or the ground lines. To reduce these problem, designers of analogue ICs usually build their circuitry as differential rather than single-ended structure. A further improvement is obtained if the circuitry is not simply differential but fully balanced, with completely

symmetrical layout so that all parasitic injection couple equally into the inverting and the non-inverting signal paths common mode signals. The differential nature of the circuits along with good power supply and common mode rejection then assures that extraneous “noise” voltage contaminate the main signal only minimally. Of course, this design approach does not come without cost, because, as it require duplication of much of the circuitry. In spite of the practical advantages of balanced designs, we believe that the derivations of a single ended filter and its operation are easier to understand than those of a balanced differential design. Moreover, once a single-ended design has been founded, it is quite easy to convert it into fully balanced configuration if required.

A general rule to follow when converting a given single ended circuit into a balanced one is the following [8]:

Draw the single ended circuit and identify the ground node(s). Mirror the whole circuit at ground, duplicating all the elements and divide the gain of all active devices by 2. Change the sign of gain of all mirrored active elements and merge any so resulting pair with inverting-non inverting gains into one balanced differential output device. Because signals of both polarities are now available, realize any devices whose sole effect in the original circuit is a sign inversion by a simple crossing of wires.

Before illustrating the application of this simple rule with a few examples which are useful as building blocks for active filters, Let us emphasize an important point to remember: in many op amp circuits, additional op amps are used for active compensation or to achieve a phase change; the high Q integrator and the non inverting phase-lead integrator are good examples.

Fully Differential Op Amp Integrators-Inverting integrator is redrawn together with their mirror images as specified in our conversion rule. Fig 1.4 contains the final converted circuits with final differential inputs and outputs. The function of the corresponding two op amps is implemented by crossed wires. A non inverting integration can be obtained simply from the balanced miller integrator by crossing its output wires, because output voltages of both polarities are now available. We can see that the no. Of elements has been doubled i.e. it requires more elements, so the cost & complexity of circuit increases. This is the main drawback of fully balanced processing.

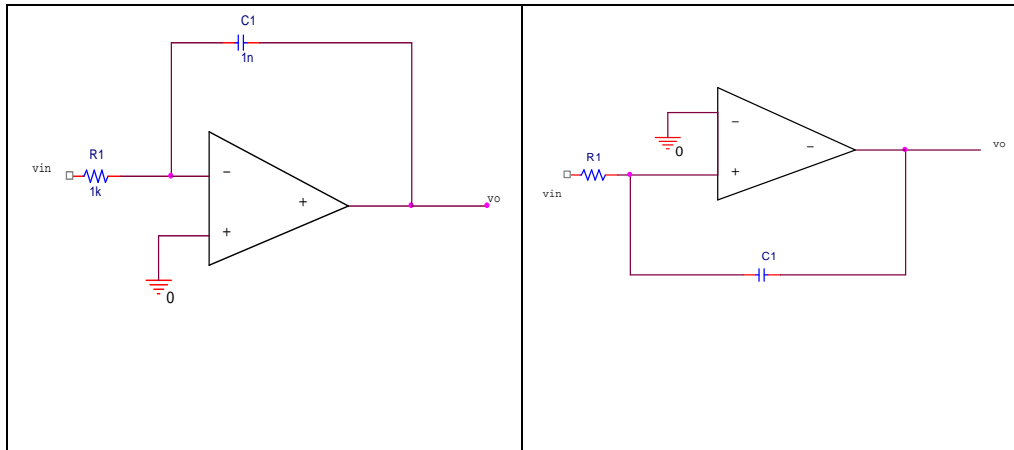


Fig. 1.4(a) Inverting op amp integrator and mirror image

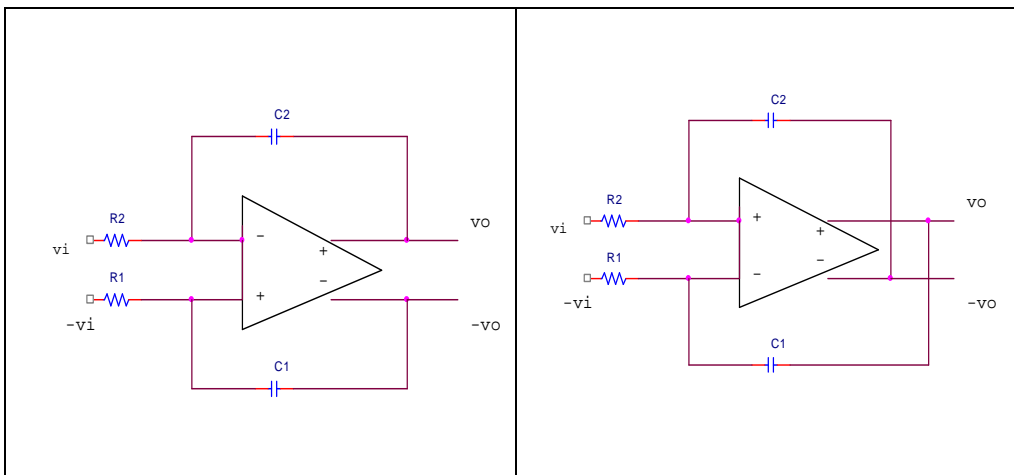


Fig. 1.4(b) fully balanced version of integrators

Advantages of fully differential signal processing-Fully-differential signal processing is becoming a more and more used technique due to higher dynamic range and power supply rejection compared to single-ended (SE) counterparts. These parameters are especially relevant in low power circuits. The other inherent advantages of fully-differential circuits include immunity from common-mode noise signals and lower harmonic distortion.

In the first chapter general introductions signal processing like development in the area of analog circuits and signal processing, single ended versus fully balanced signal processing, advantages of differential signal processing has been presented . In the second chapter general introduction and description of various fully differential active elements and their applications have been presented. In the third chapter few realizations of various types of

signal processing circuits such as current-mode amplifiers, integrators, differentiators and biquad filters in CMOS technology using the following types of active building blocks have been presented. (i) Fully differential second generation Current Conveyor. (ii) Differential voltage current conveyor. (iii) current differencing buffered amplifier. In the fourth chapter a newly introduced building block namely Current Differencing Current Conveyor which has been introduced very recently has been implemented using DVCC and used to realize various fully-differential signal processing circuits such as fully-differential current-mode amplifier, fully-differential biquad filter, fully-differential biquad filter with tunable gain. This fully differential filter requires minimum passive components (all of which are grounded).

1.4 REFERENCES:

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CHAPTER 2

FULLY DIFFERENTIAL ACTIVE BUILDING BLOCKS AND THEIR APPLICATIONS

2.1 Introduction:

This chapter presents the result of some studies of fully differential building blocks for instrumentation application which include universal current mode filter, current mode amplifier, current mode lossy and lossless integrator, current mode differentiator etc. The building blocks considered are DVCC, ICCII, DCCII, MDCC, DDCC, FDCCII, MCCIII, CCCII, CGCII, DDA, DDOFA, & CDBA etc.

The main thrust of the work presented here has been on the review of the prominent work in the area of fully differential active building block. The recently developed Fully Differential signal processing with their so many advantages has been used to develop many processing elements used in instrumentation and control.

2.2 Fully differential signal processing:

Fully-differential signal processing is becoming a more and more used technique due to higher dynamic range and power supply rejection compared to single-ended (SE) counterparts. These parameters are especially relevant in low power circuits. The other inherent advantages of fully-differential circuits include immunity from common-mode noise signals and lower harmonic distortion.

A number of fully-differential active building blocks (FDABB) and fully-differential circuit have appeared during the last two decades. It is, therefore, worthwhile to review these works.

2.2.1 Differential voltage Current Conveyor:

It has widely gone unnoticed in the literature, that the Differential voltage Current Conveyor (DVCC) was first proposed by Pal in as early as 1989[8]. Although it was then realized by op-amps, Elwan and Soliman have presented a CMOS implementation of the building block in 1997. its symbolic diagram and its CMOS implementation proposed by them. The DVCC is characterized by the following equations:

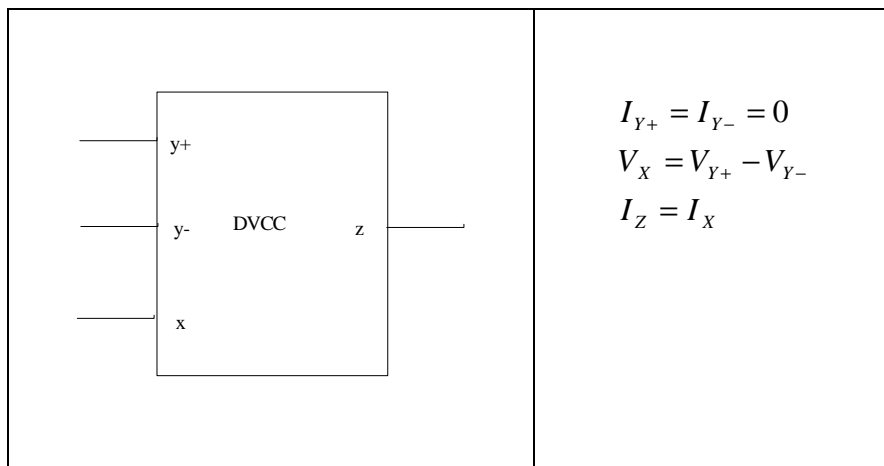


Fig. 2.1 DVCC notation and port relation

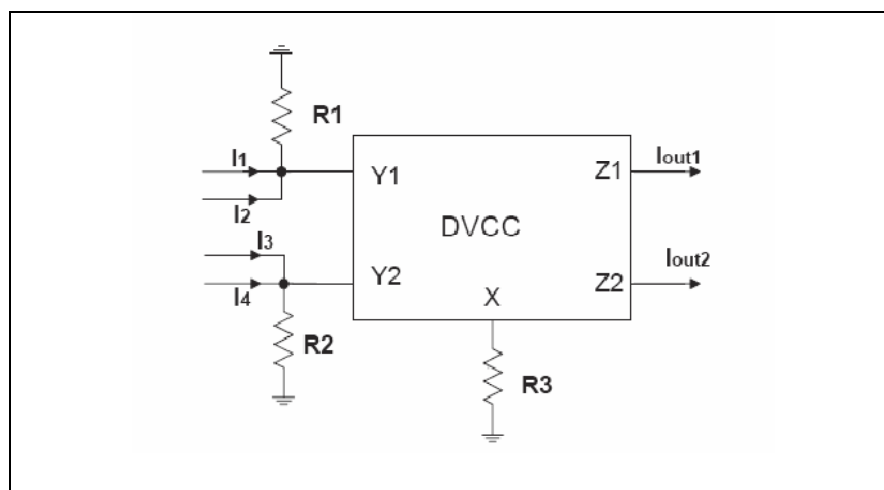


Fig. 2.2 Summer substructure using DVCC

In this the original “voltage” input y is split into a pair of inputs Y_1 and Y_2 . The voltage of the x terminal is then given by the voltage difference of the voltage inputs. This offers more freedom during the design of voltage- and mixed-mode applications.

DVCC with the complementary pair of z_1 and z_2 terminals is known as DVCCC (Differential Voltage Complementary CC) [8]. As a special case of DVCCII for y_1 grounded, the ICCII (Inverting CCII) is described in [9]. On the contrary, DDCC (Differential Difference CCII) is an extension of DVCCII [10], Voltage at the x terminal is given by a combination of voltages at three terminals $y_1, y_2,$ and y_3 . Splitting the z terminal of DDCC into a pair of z terminals with currents $I_z = I_x$ yields DDCCC (Differential Difference Complementary CC) [11]. Another generalization of the classical CCII is DCC (Differential Current Conveyor), in which the x input is replaced by the pair of x_1 and x_2 . The current through the z terminal is given by the difference of currents through the x_1 and x_2 terminals. MDCC (Modified Differential Current Conveyor) [12] is a simplification of DCC on the assumption that signal (voltage) at the y terminal is zero.

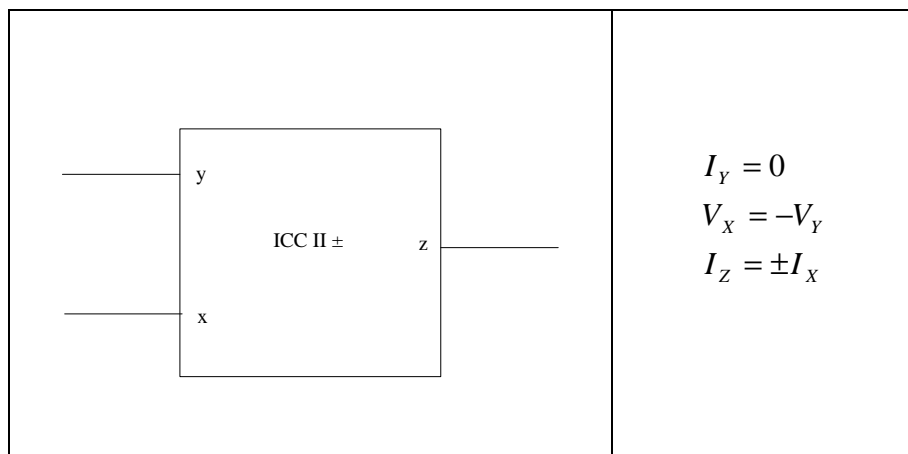


Fig. 2.3 ICCII notation and port relation

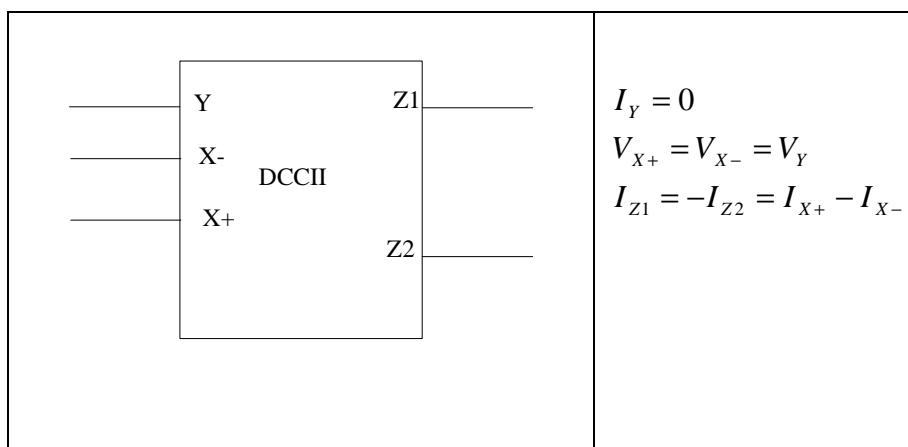


Fig. 2.4 DCCII notation and port relation

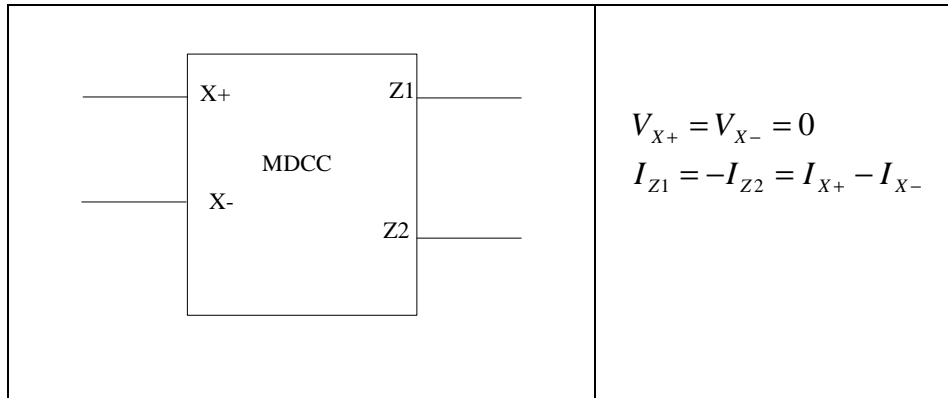


Fig. 2.5 MDCC notation and port relation

2.2.2 Differential difference current conveyor:

The next important contribution in the development of fully-differential active building block was the introduction of Differential Difference Current Conveyor (DDCC) in 1996 by Chin, Liu, Tsao and Chen [10]. They presented a CMOS version of DDCC. This device combined the advantages of the conventional Current Conveyor and the DDA element. The device was used to realise a differential-squarer circuit, differential-integrator circuit (all in voltage-mode) and a current-mode biquad filter. There was no attempt to use the block to realise fully-differential circuits (circuits in which the output is also available in differential form).

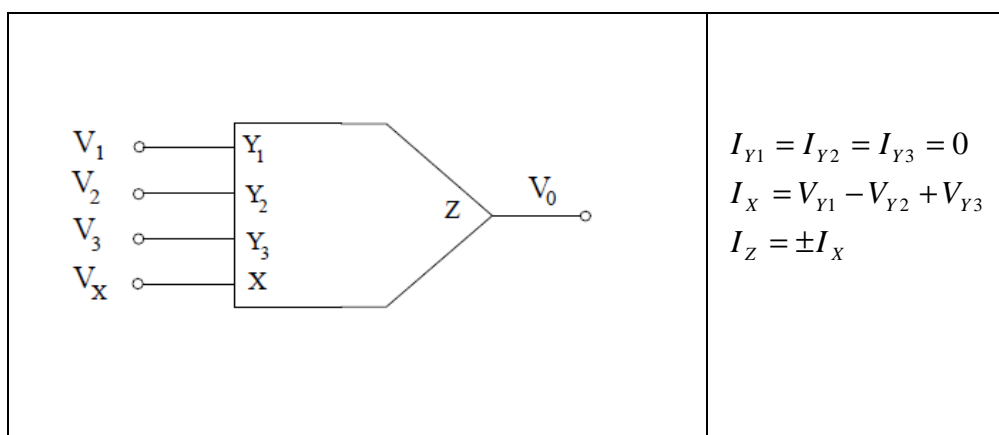


Fig. 2.6 DDCC symbol and port relation

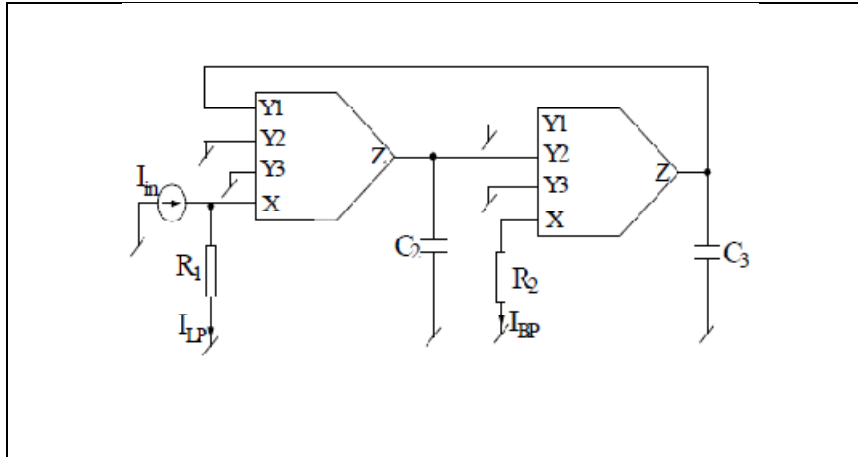


Fig. 2.7 CM biquad filter using DDCC

In the same year, 1996, Walker and Green proposed the use of fully-differential transconductor to design fully-differential voltage-mode filters. In their work, they had used fully-differential transconductor blocks in which no extra common-mode feedback circuitry was required.

Szczepanski, Jakusz and Schaumann in 1997 presented a fully-balanced CMOS OTA structure for VHF applications. The proposed CMOS OTA was shown to be highly linear and was used to design fully-differential voltage-mode and current-mode ladder filters.

2.2.3 Fully differential second generation Current Conveyor:

The fully differential second generation Current Conveyor (FDCCII) was introduced by El-Adawy, Soliman and Elwan. FDCCII (Fully Differential CCII) [13] is an important generalization of the conventional CCII. The x , y , and z terminals occur here in pairs. The basic circuit equations of the CCII are now valid for differences of voltages or currents which correspond to these pairs. FDCCII is thus designed for applications with fully differential architecture for fast signal processing. This type of conveyor is called FBCCII (Fully Balanced CCII) [14].

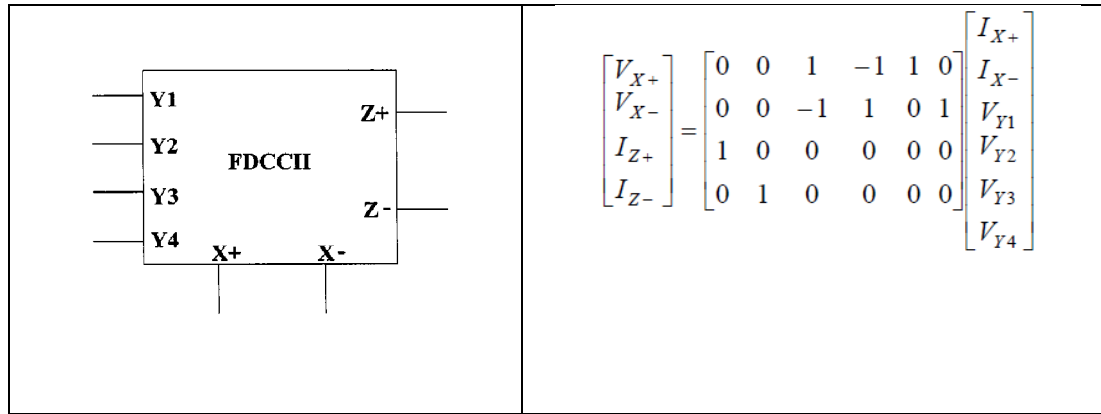


Fig. 2.8 FDCCH notation and port relation

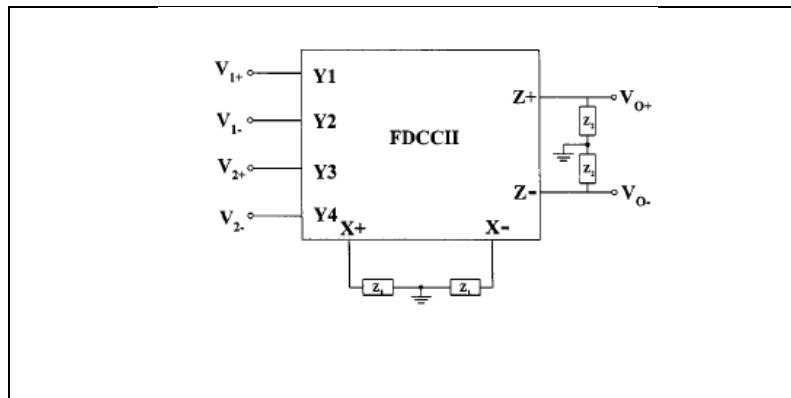


Fig. 2.9 Fully differential amplifier using FDCCH

The so-called modified CCII (MCCII) provides such an operation that the current through the z terminal does not depend on the direction of current I_x , i.e. $I_z = \text{abs}(I_x)$. This feature can be used with advantage to implement economically full-wave rectifiers. Joining two current conveyors CCII- yields the so-called Operational Floating Conveyor (OFC) [16]. OFC is a universal differential-input differential-output building block, enabling current, voltage, and mixed-mode applications. An extreme embodiment of universality is the so-called UCC (Universal Current Conveyor) [17]. By means of this element, one can implement all the above types of current conveyor. However, such universality is at the cost of non-optimal parameters for a concrete application.

A modification of the third-generation current conveyor is MCCIII [18]. Modified CCIII is equipped with a couple of z_1 and z_2 terminals. Currents through these terminals are of opposite directions and the following equalities hold: $I_{z1} = -2I_x$, $I_{z2} = I_x$. Unequal values of the currents enable the design of interesting applications.

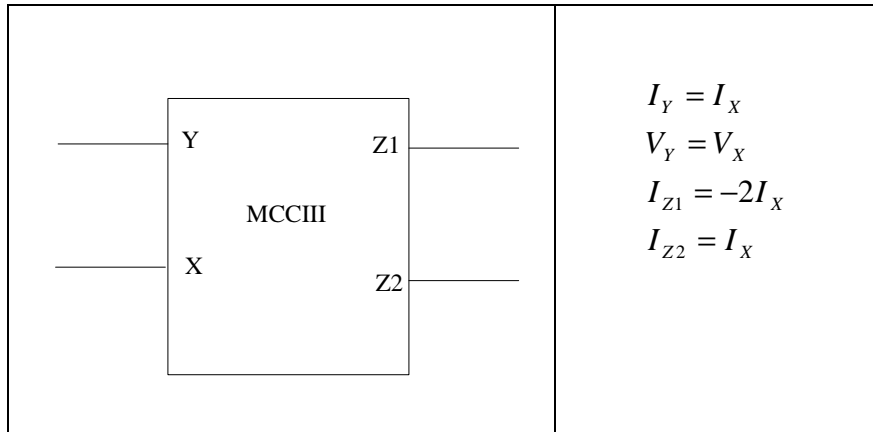


Fig. 2.10 MCCIII notation and port relation

The non-zero x -terminal impedance is an important parasitic parameter of the current conveyor, which negatively affects its behaviour, particularly in filtering applications. However, this phenomenon is paradoxically utilized in a new type of conveyor, namely CCCII (Current Controlled Conveyor) [19-21], where the resistance of x terminal is controlled electronically via the bias current. It can be shown that this active device can be used in filters whose parameters may be controlled electronically. Such a feature has been inherent in the so-called gmC filters, i.e. filters, compounded only of OTAs and capacitors.

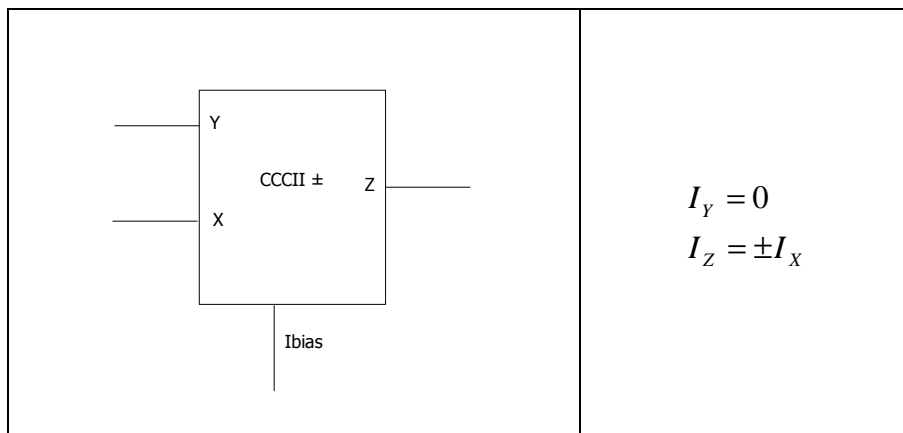


Fig. 2.11 CCCII notation and port relation

Another method for controlling electronically the parameters of applications employing current conveyors is based on conveyors with variable current gain I_z/I_x . such a conveyor is identified by the abbreviation CGCCII (Current Gain CCII). The current conveyor of such a type, concretely CCII, was formerly manufactured by Elantec under the code EL2717 [22]. The variable gain is implemented via transforming current I_z into voltage by means of resistors, and via back transformation of voltage into current by gains of electronically gm -controlled OTA. The most recent solution is characterized by digital control of the gain,

utilizing the so-called CDN (Current Division Network) and DCCF (Digitally Controlled Current Follower) [23].

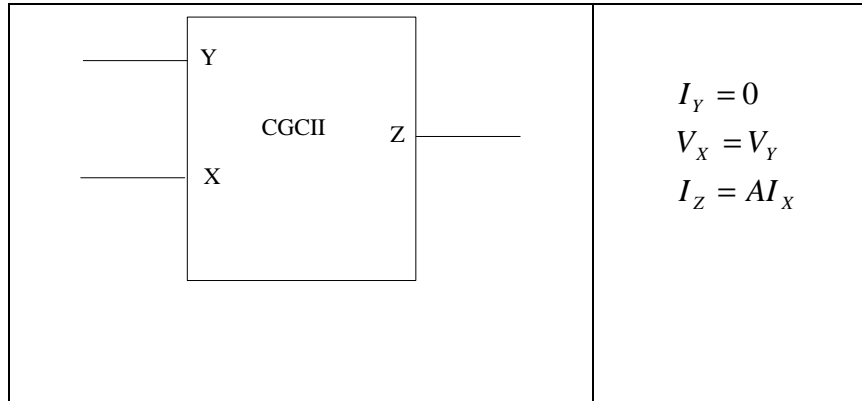
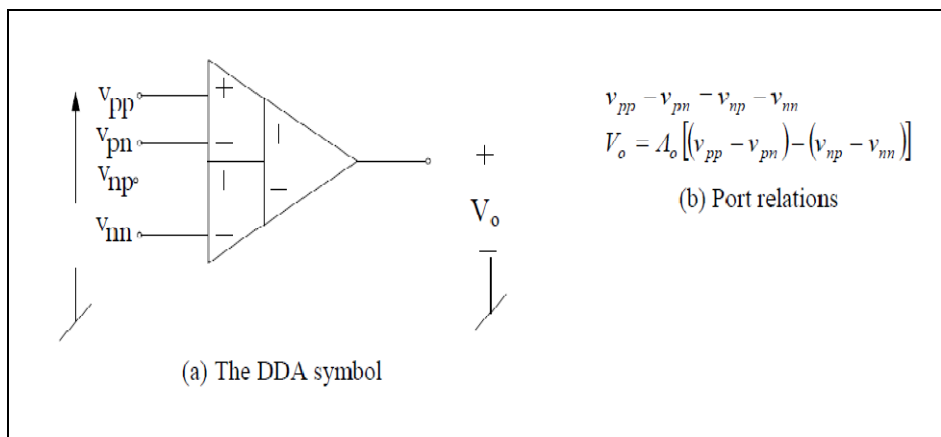


Fig. 2.12 CGCII notation and port relation

2.2.4 Differential difference amplifier:

In 1987, Sackinger and Guggenbuhl introduced a new active building block termed as the Differential Difference Amplifier (DDA) [24].



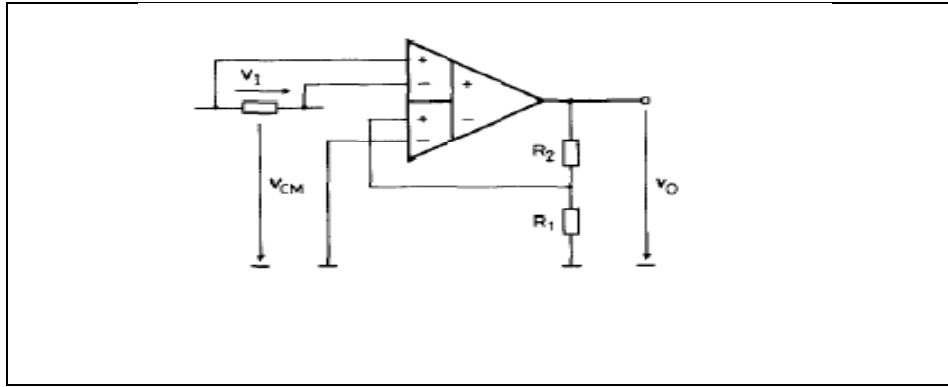


Fig. 2.13 A programmable instrumentation amplifier using DDA

This differential active building block was used to implement a number of voltage-mode circuits like instrumentation amplifiers, inverting buffers, comparators and a voltage-controlled current source. Though the DDA element was designed to take differential-inputs, the output available from the block was ground referred.

In contrast to the conventional Op-Amp, DDA has four high-impedance inputs pp , pn , np , and nn . Whereas the Op-Amp amplifies the difference voltage $V_p - V_n$ and provides the equality $V_p = V_n$ with the help of negative feedback, the DDA responds to the “generalized” difference voltage $(V_{pp} - V_{pn}) - (V_{np} - V_{nn})$, and maintains the equality $V_{pp} - V_{pn} = V_{np} - V_{nn}$ via the feedback. Among other things, this principle enables an implementation of applications with high signal dynamics with a minimum number of additional elements and without the necessity of satisfying the limiting matching conditions between the parameters of such elements [25].

2.2.5 Differential Difference Operational Floating Amplifier (DDOFA):

In 1998, Mahmoud and Soliman introduced a new fully-differential active building block which they named as ‘Differential Difference Operational Floating Amplifier (DDOFA)’ [26]. This block was a truly differential block in the sense that the input voltages were taken in differential form and the output current was also available in differential form. This fully-differential active building block was shown to be useful in a number of voltage-mode applications like lossless and lossy integrator, grounded and floating resistors, current-integrators, mixed mode and voltage mode biquad filters, differential-integrators, multipliers and divider cells.

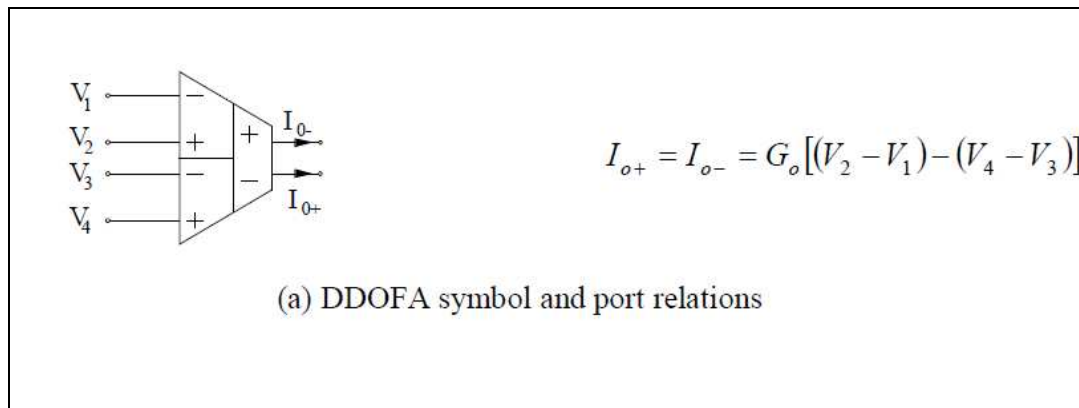


Fig. 2.14

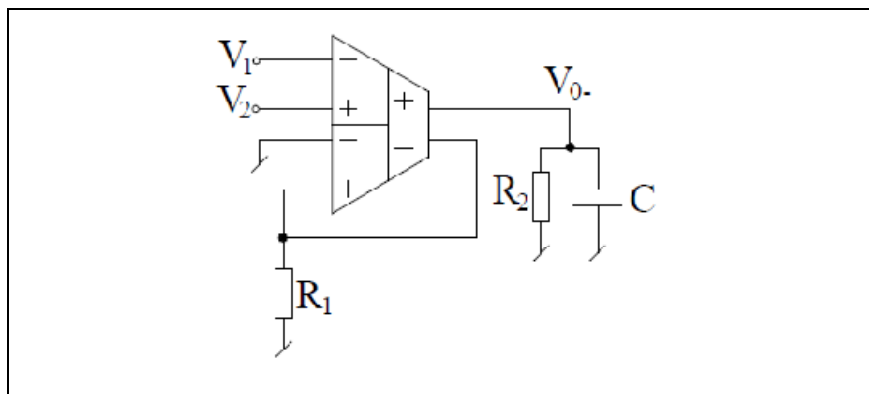


Fig. 2.15 Lossless integrator using DDOFA

2.2.6 Differential Difference Complementary Current Feedback Operational Amplifier:

Differential Difference Complementary Current Feedback Operational Amplifier (DDCCFA) was formally proposed by Gupta and Senani in 2005[27]. It was shown that a single DDCCFA is sufficient to generate SRCO circuits possessing the following properties simultaneously: (a) use of a single ABB (b) employment of two GCs along with a minimum number (only three) of resistors (c) non-interacting controls of condition of oscillation and frequency of oscillation (d) a simple condition of oscillation (i.e. not more than one condition) and (e) availability of current-mode and voltage mode outputs both.

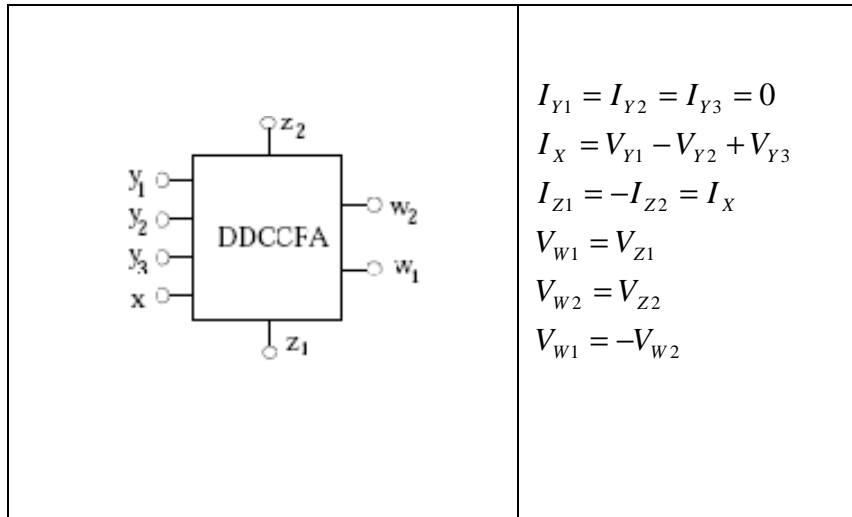


Fig. 2.16 DDCCFA notation and port relation

Employing DDCCFAs, all previously known building blocks can be derived as special cases and hence, a DDCCFA can be considered to be the most universal building block known till date.

2.2.7 Current differencing buffered amplifier:

The Current Differencing Buffered Amplifier (CDBA) [28] was introduced by Acar and Ozuguz. The characterizing equations and symbolic notation of the CDBA is given in Fig2.17.

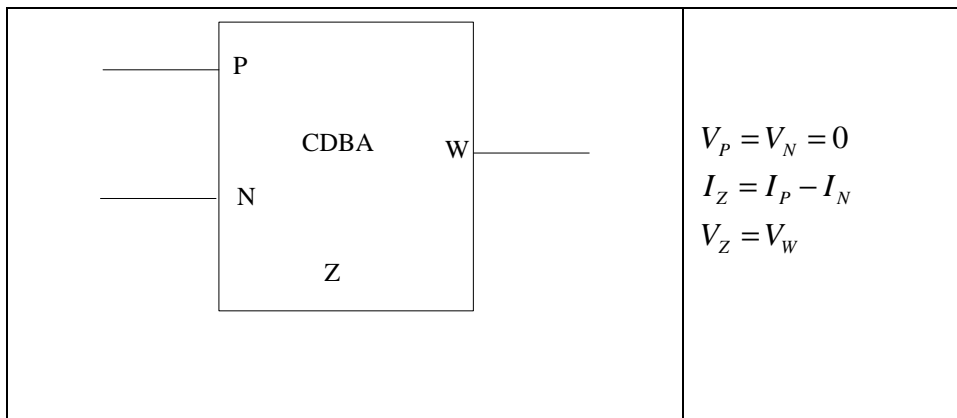


Fig. 2.17 CDBA notation and port relation

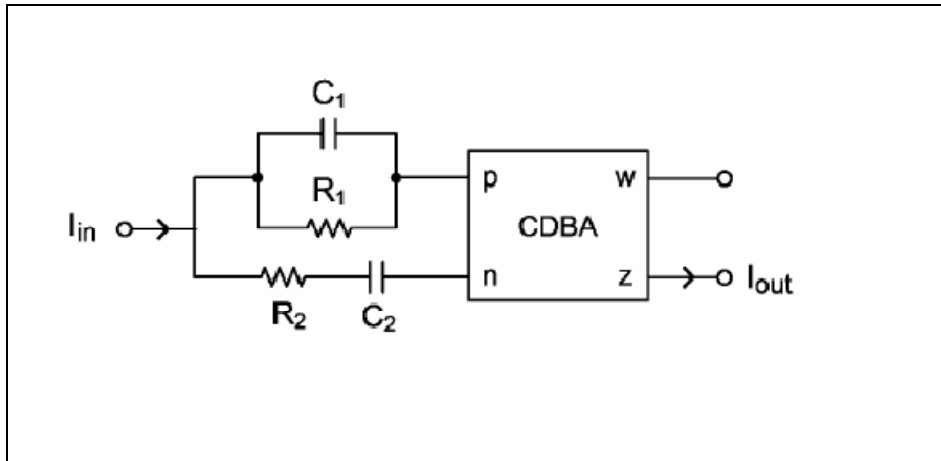


Fig. 2.18 Current mode second order notch filter using CDBA

In 1992 and 1999, two papers were published which introduced new circuit elements OTRA (Operational Trans resistance Amplifier) and CDBA (Current Differencing Buffered Amplifier) [28]. The latter is also known as DCVC (Differential Current Voltage Conveyor) [29]. CDBA, a generalization of OTRA, is a universal element for filter design, primarily for voltage-mode operation. Numerous papers were published about CDBA applications [30-36]. Some of the applications profit from the basic CDBA feature, i.e. the non-problematic implementation of both non inverting and inverting integrator as a building block of filters of arbitrary order.

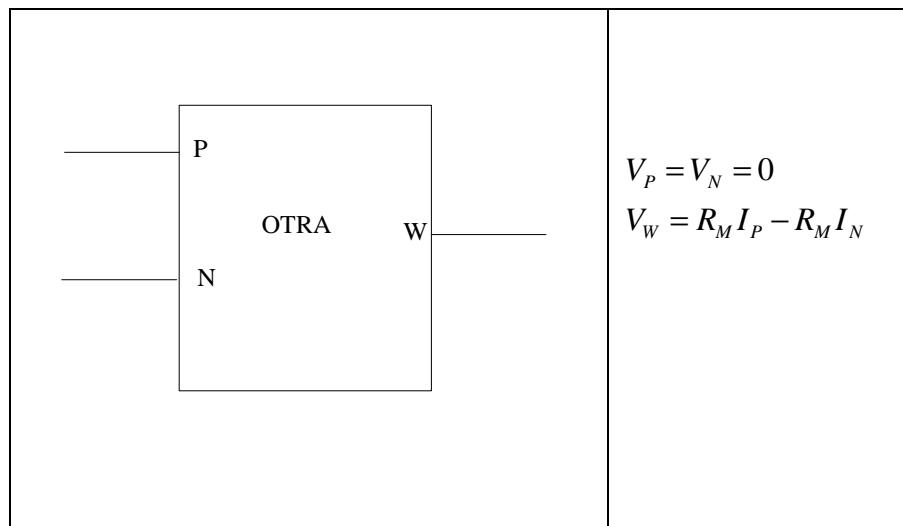


Fig. 2.19 OTRA notation and port relation

CDBA contains the so-called CDU (Current Differencing Unit) and the voltage unity-gain buffer. Basically, CDU is a current conveyor of the MDCC type: It has two low-impedance terminals, p and n . The difference of currents I_p and I_n flows out of the z terminal and the

corresponding voltage drop on the external impedance is copied by the buffer to the w output. That is why the additional impedances are necessary for implementing the feedbacks from the voltage output to the current inputs. It is inconvenient from the point of view of simplicity and low power consumption. Another drawback is the impossibility of direct electronic control of circuit parameters such as that for the OTA-based applications. This problem is solved via two different approaches. The nonzero parasitic resistances of p and n terminals of the CDU are controlled electronically via bias currents. The p and n terminals thus act as voltage input terminals. These voltages are then transformed into currents, whose values are electronically controlled. In fact, this approach represents a transition to a “pure” voltage mode. Another solution is described in the form of a new circuit element called DC-CDBA (Digitally Controlled CDBA) [38]. The output current of the current differencing unit is modified in the CDN (Current Division Network), whose current output is connected to the z terminal of the voltage buffer input. The CDN block works as a current attenuator with digitally controlled attenuation. Such a concept of controlling the parameters seems to be optimal, because in contrast to the analogue control a greater accuracy of the parameter range of more active elements in the application can be guaranteed.

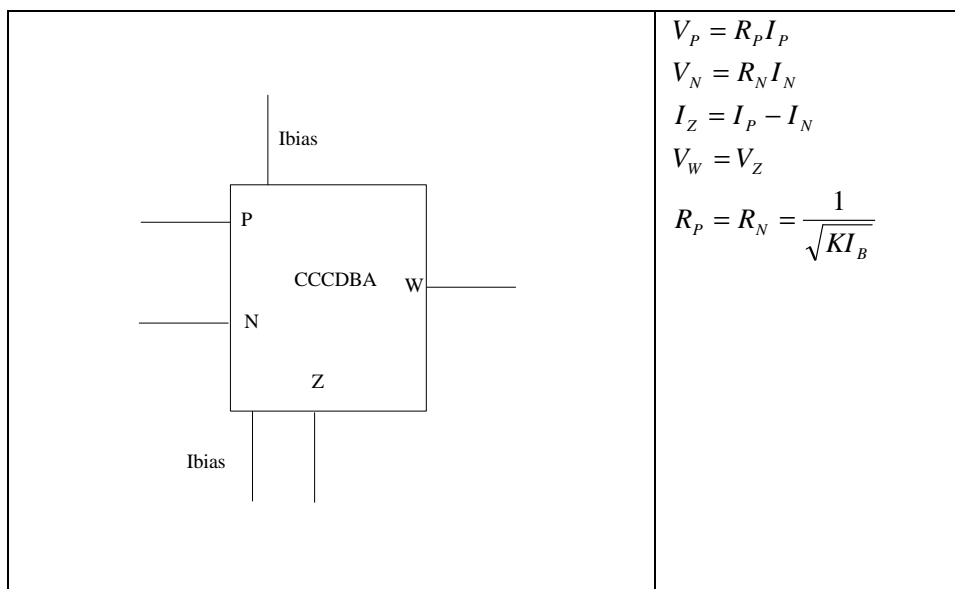


Fig. 2.20 CCCDBA notation and port relation

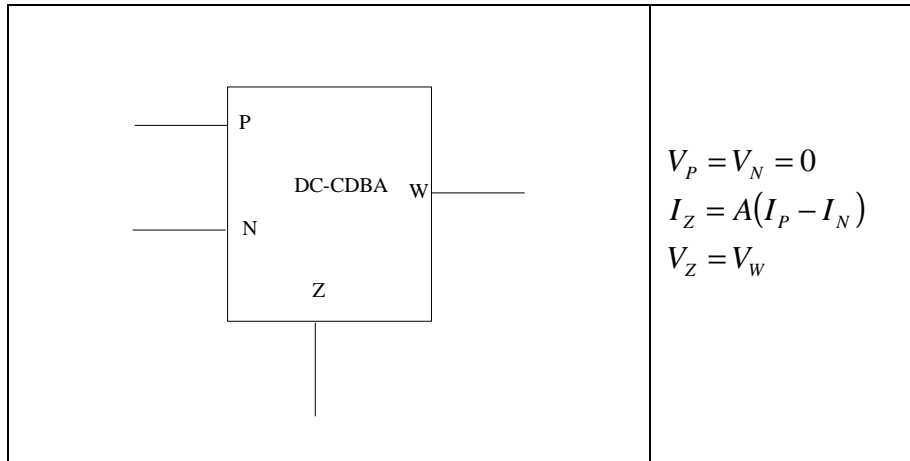


Fig. 2.21 DC-CDBA notation and port relation

The input part of the CDTA [39] is formed – much like for the CDBA – by the current differencing unit (CDU). It is followed by the multiple-output OTA. The difference of currents I_p and I_n flows out of the z terminal, causing a voltage drop on the external impedance. This voltage is then transformed via the internal OTA back into the current I_x . From the point of view of currents I_p , I_n , and I_x , the circuit operates as a current-mode amplifier. Its gain is given by the product of external impedance and internal transconductance. When the z -terminal voltage is maintained within relatively low levels, then the circuit operation approaches the ideal current mode. In principle, CDTA applications do not require the use of external resistors, which are substituted by internal transconductors. Analogously to the well-known “ gmC ” applications, the “CDTA-C” circuits are formed by CDTA elements and grounded capacitors. Such structures are well-suited for on-chip implementation. In the last decade, lots of papers about the CDTA and its applications have been published in international journals and at conferences [40-42]. Within the frame of EURO PRACTICE, the very first CDTA chip in CMOS technology has been fabricated.

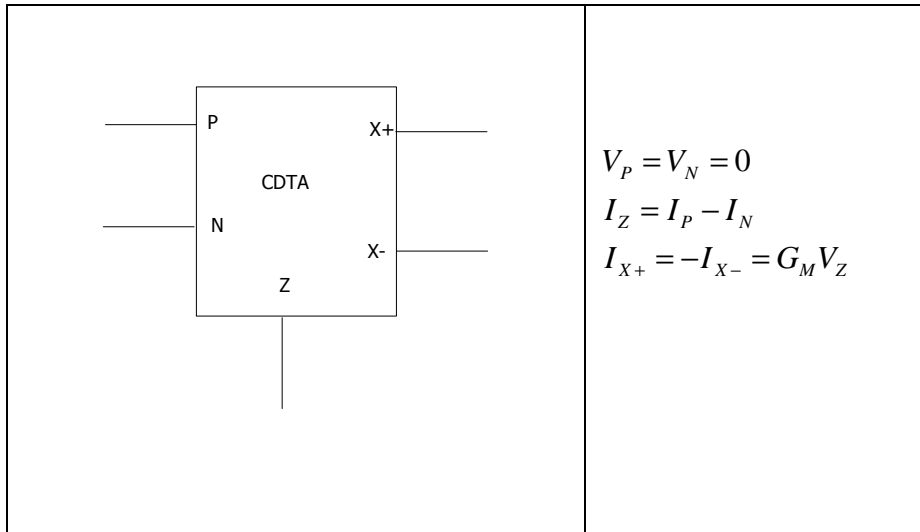


Fig. 2.22 CDTA notation and port relation

The CDTA modification [43-45] is called CCCDTA (Current Controlled CDTA). It is an analogy to CCCDBA, where the electronic control is based on the dependence of parasitic input resistances of the CDU on the bias current. The above mentioned drawback consists in moving the circuit operation to the voltage mode.

Note that the CDU, which is an important component of the above elements, is a special case of DCCII with the y terminal grounded, i.e. MDCC with z_2 terminal omitted.

GMCI (Generalized Current Mirror and Inverter) [46] is an element which is in a certain sense a dual element to the CDU. GMCI has x , z_1 , and z_2 terminals and its equations are as follows: $I_{z1} = aI_x$, $I_{z2} = bI_x$. Usually $a=1$, $b=-1$. Then GMCI is reduced to current mirror and current inverter, jointly excited from the low-impedance x terminal. This element has been published formerly under the name DOCF (Double Output Current Follower).

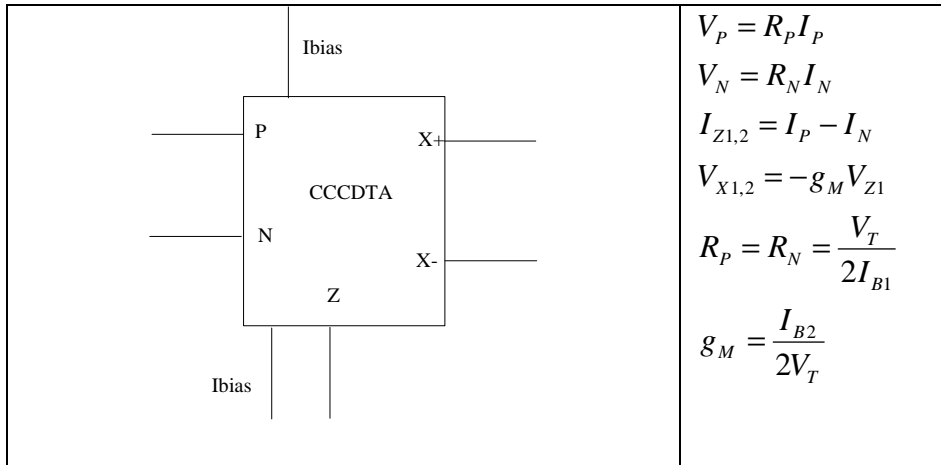


Fig. 2.23 CCCDTA notation and port relation

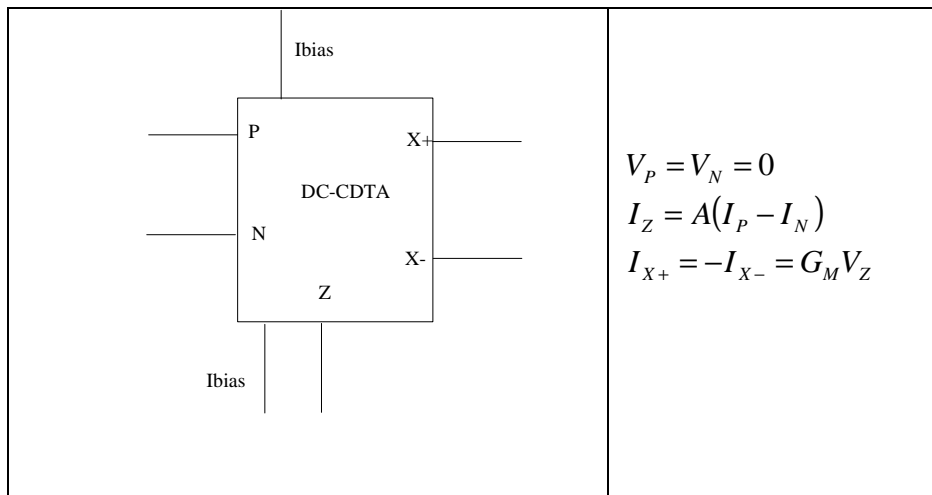


Fig. 2.24 DC- CDTA notation and port relation

A novel circuit element, CTTA (Current-Through Trans conductance Amplifier), is described [48]. In contrast to the CDTA, its input block is the so-called CTU (Current through Unit). The pair of input terminals serves as a voltage short circuit. The terminal current is copied to the output terminal. The CTU is designed as an ideal current sensor because it converts a current flowing through an arbitrary branch to its copy, which flows to an independent load for subsequent processing.

The CTU can be theoretically synthesized from the FTFN after connecting its input and output gates in parallel. However, among other things, the parasitic gate impedances as well as impedances of the individual terminals can cause a serious realization problem, because a part of the current sensed can leak through them out of the CTU.

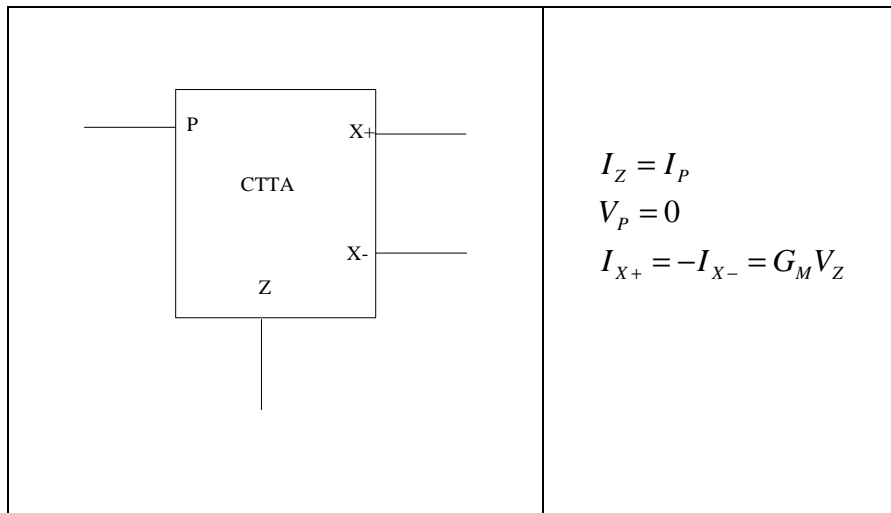


Fig. 2.25 CTTA notation and port relation

In respect of the difficulty of practical implementation of the CTTA, a simplified version called CCTA (Current Conveyor Trans conductance Amplifier) has been described in [49]. Instead of the CTU, the well-known CCIII (Current Conveyor of the third generation) is used here, enabling also the current sensing.

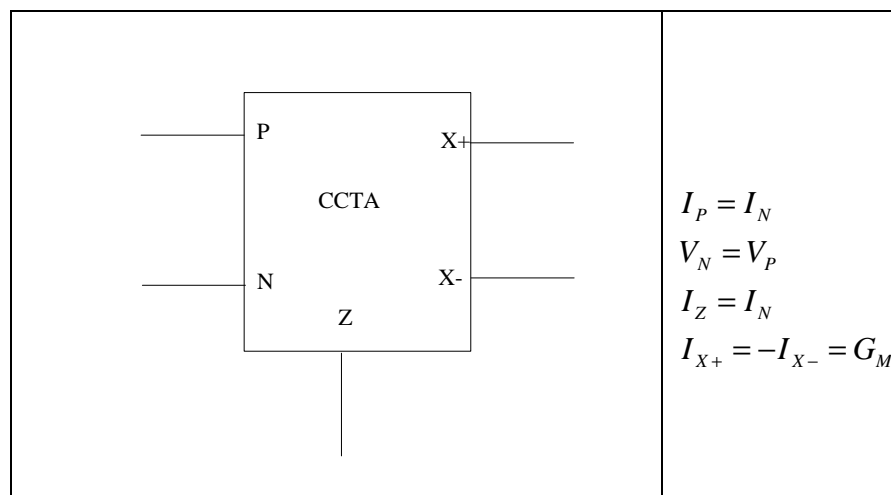


Fig. 2.26 CCTA notation and port relation

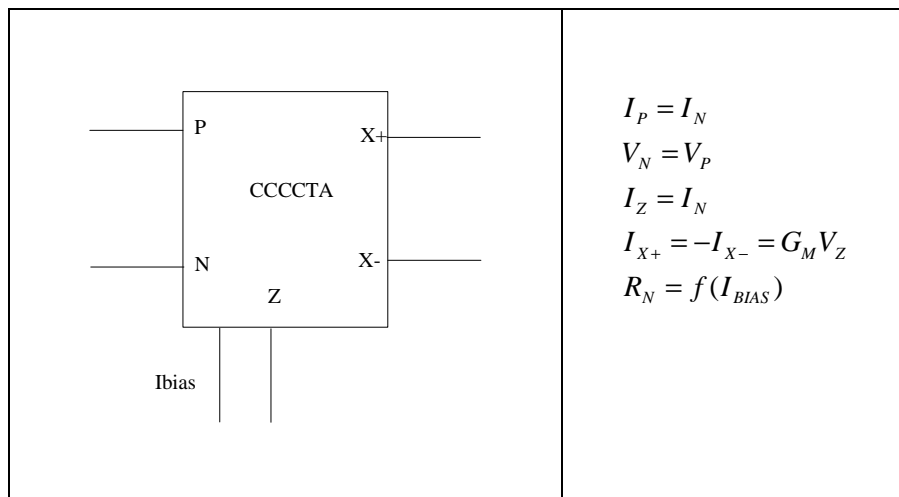


Fig. 2.27 CCCCTA notation and port relation

A generalization to the so-called CCCCTA (Current Controlled CCTA) [50] is given, where the above principle of electronic tuning of the parasitic resistance of the x terminal is utilized.

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CHAPTER – 3

CMOS/BIPOLAR IMPLEMENTATION OF SELECTED FULLY DIFFERENTIAL ACTIVE BUILDING BLOCKS AND THEIR APPLICATIONS

3.1 Introduction:

In the previous chapter a detailed review of some of the important works on fully differential active elements has been presented. In the present chapter CMOS implementation of few applications of some these building blocks has been presented.

The following building blocks and associated applications have been presented:

1. Fully differential current conveyor (FDCCII)
2. Differential voltage current conveyor (DVCC).
3. Current differencing buffered amplifier (CDBA).

As the signal after being sensed cannot be directly transmitted to the next stage without removing interfering sources, as otherwise highly distorted results may be obtained which are far from true. Many a times it becomes necessary to perform several operations before it is transmitted further. These processes may be linear like amplification, attenuation, integration, differentiation, addition and subtraction. Using these blocks the implementation of various applications like fully differential current mode amplifier, voltage mode amplifier, integrator, differentiator, fully balanced universal filter, notch filter etc. have been presented and simulated on Pspice.

3.2 Second generation fully differential current conveyor (FDCCII):

The proposed block is an extension of the second-generation current conveyor (CCII) introduced by Sedra and Smith [1] in 1970. The CCII is a versatile building block and is described by the following matrix equation:

$$\begin{bmatrix} V_X \\ I_Z \\ I_Y \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_Z \\ V_Y \end{bmatrix}.$$

The FDCCII is an eight-terminal analogue building block [2] shown symbolically in Fig. 3.1 with a describing matrix equation of the form:

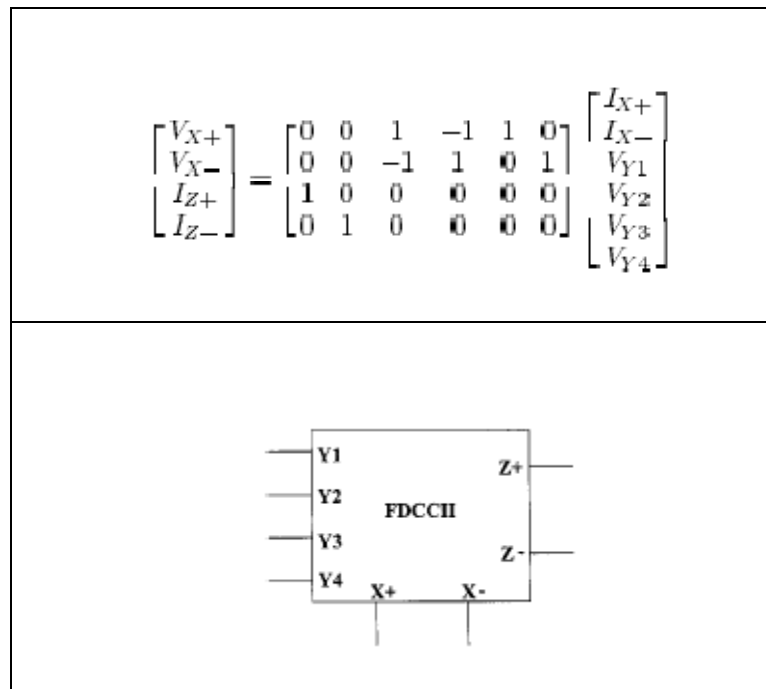


Fig. 3.1 FDCCII block and port relations

A CMOS realization of the FDCCII is shown in Fig. 3.2 All transistors are assumed to be operating in the saturation region. The input voltage is applied to the gates of the differential pair transistors M1 and M2.

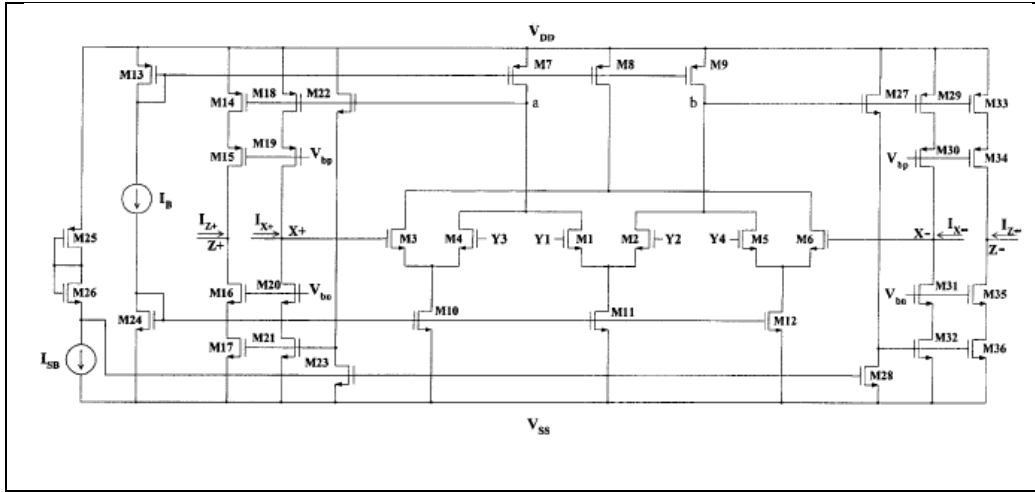


Fig. 3.2 CMOS Realization of FDCCII

It is clear that

$$V_{X+} = V_{Y3} + (V_{Y1} - V_{Y2})$$

$$V_{X-} = V_{Y4} - (V_{Y1} - V_{Y2})$$

Furthermore

$$I_{Z+} = I_{X+}$$

Similarly

$$I_{Z-} = I_{X-}$$

It is worth mentioning that the proposed FDCCII can be divided into two separate CCII's by connecting and terminals Y1 & Y2 to ground by using Y3, X+ & Z+ as the terminals of the first CCII and Y4, X- & Z- as the terminals of the second CCII. The proposed FDCCII has been simulated with PSPICE using the AMI 1.2 m CMOS technology provided by MOSIS. The aspect ratios of the transistors are given in Table I. The supply voltages used are 1.5 V, while the tail current I_B is 50 uA and the standby current I_{SB} is 20uA.

Transistor aspect ratio

Transistor	W(μm)/l(μm)
M1, M2, M3, M4, M5, M6	60 /4.8
M7, M8, M9, M13	480/4.8
M10, M11, M12, M24	120/4.8
M14, M15, M18, M19, M25, M29, M30, M33, M34	240/2.4
M16, M17, M20, M21, M26, M31, M32, M35, M36	60/2.4
M22, M23, M27, M28	4.8/4.8

3.2.1 Simulation results:

3.2.1.1 Current mode amplifier using two separate CCII's of FDCCII:

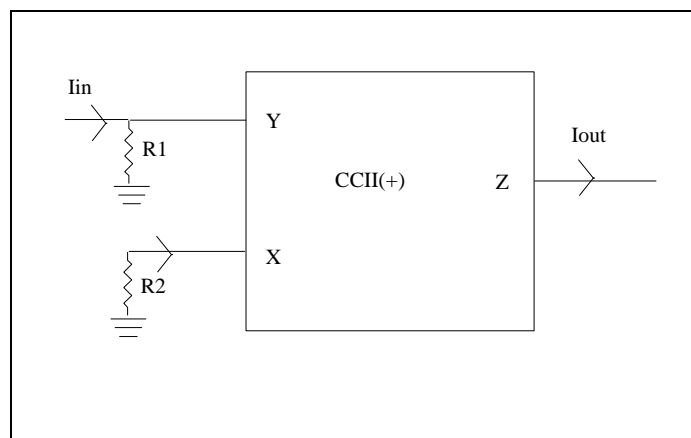


Fig. 3.3 CM Amplifier using CCII

Current mode amplifier using CCII shown in fig.3.3 the current-mode amplifier can be found as:

$$\frac{I_{OUT}}{I_{IN}} = \frac{R_1}{R_2}$$

The gain of the amplifier can be adjusted by changing R_1 and/or R_2 .

The value of the component used are $R_1 = 10K$, $20K$ and $30K$, and $R_2 = 10K$ to give a value of gain equal to 1, 2 and 3

And approximately bandwidth of the circuit is $6MHz$

The simulated output result are shown in fig.3.4

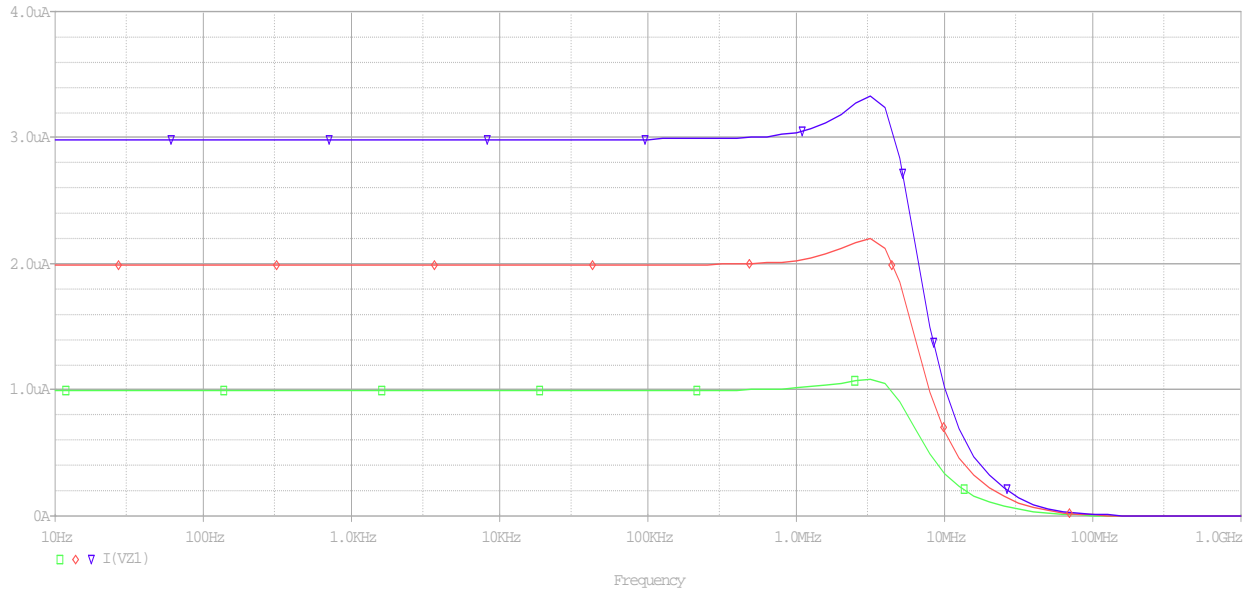


Fig. 3.4 Frequency response of current amplifier

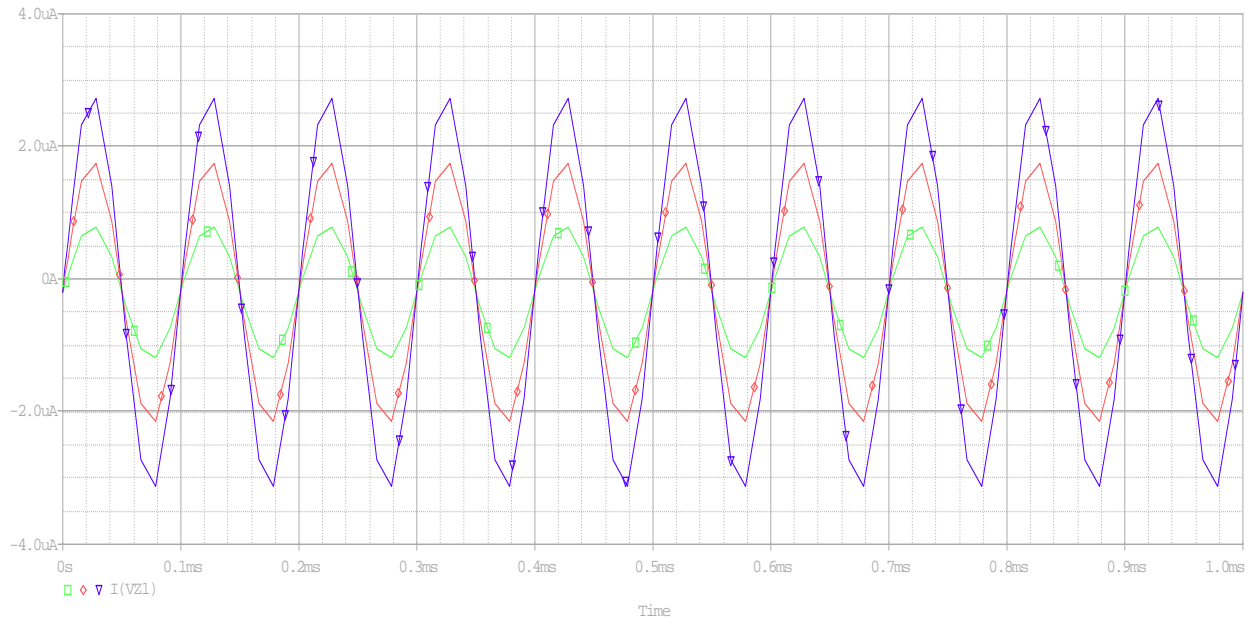


Fig. 3.5 Transient response of current amplifier

3.2.1.2 Fully differential amplifier:

Certain applications require the use of fully differential signal processing to extend the dynamic range of the signal, cancel even harmonics, and suppress undesirable CM signals. A fully differential amplifier that is used as a basic cell to realize fully differential filters is shown in Fig. 3.5. It can be shown that the differential mode (DM) output voltage is given by:

$$V_{Od} = \frac{Z_2}{Z_1}(2V_{1d} + V_{2d})$$

Where

$$V_{id} = \frac{1}{2}(V_{i+} - V_{i-})$$

$$V_{od} = \frac{1}{2}(V_{o+} - V_{o-})$$

However, to suppress the CM input signals, external inputs should be applied to the Y1 and Y2 terminals where the CM gain is zero. In short, to implement a fully differential filter, Y1 and Y2 terminals are used for the external inputs while Y3 and Y4 terminals are used for the feedback signals.

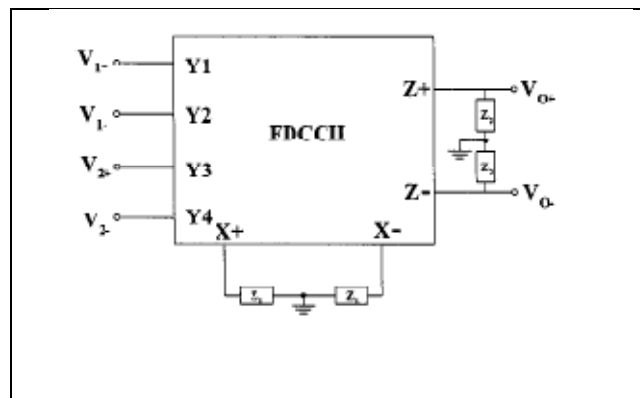


Fig. 3.6 Fully differential amplifier

The value of the component used are $Z_2 = 10K, 20K$ and $30K$, and $Z_1 = 10K$ to give a value of gain equal to 1, 2 and 3

And approximately bandwidth of the circuit is 6MHZ. The simulated output result are shown in fig.3.7

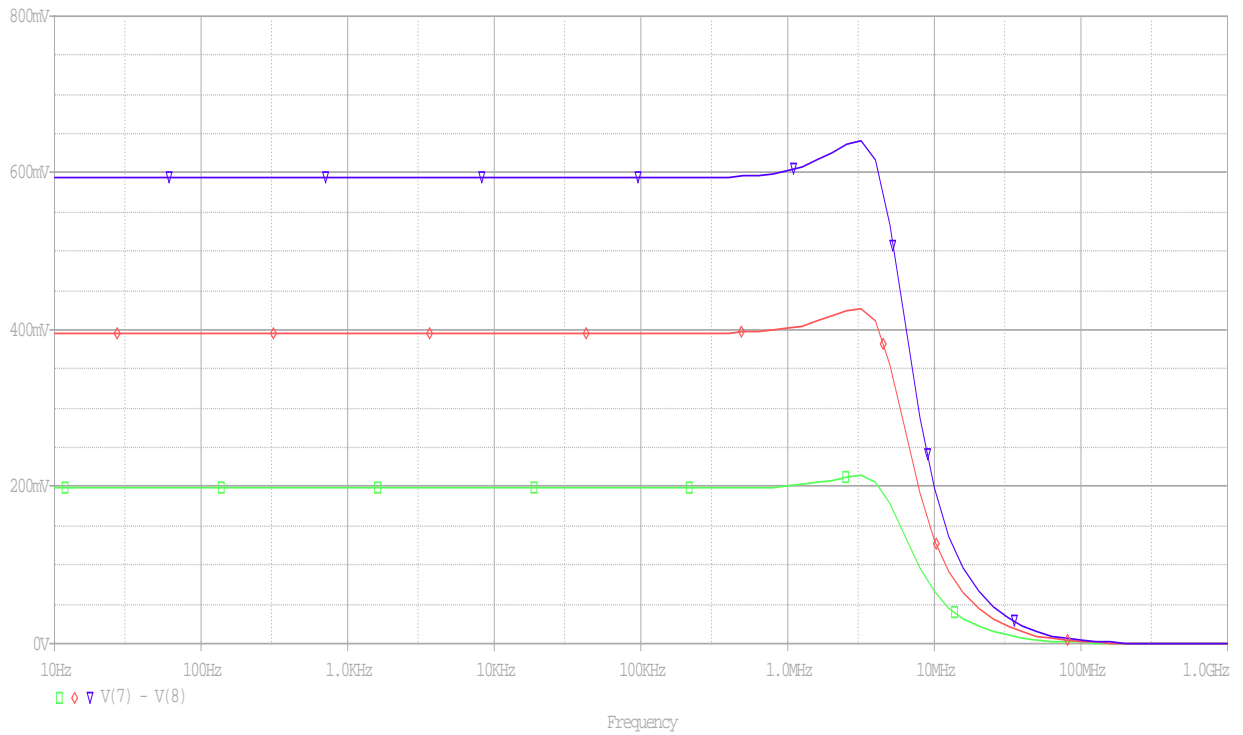


Fig. 3.7 Frequency response of voltage amplifier

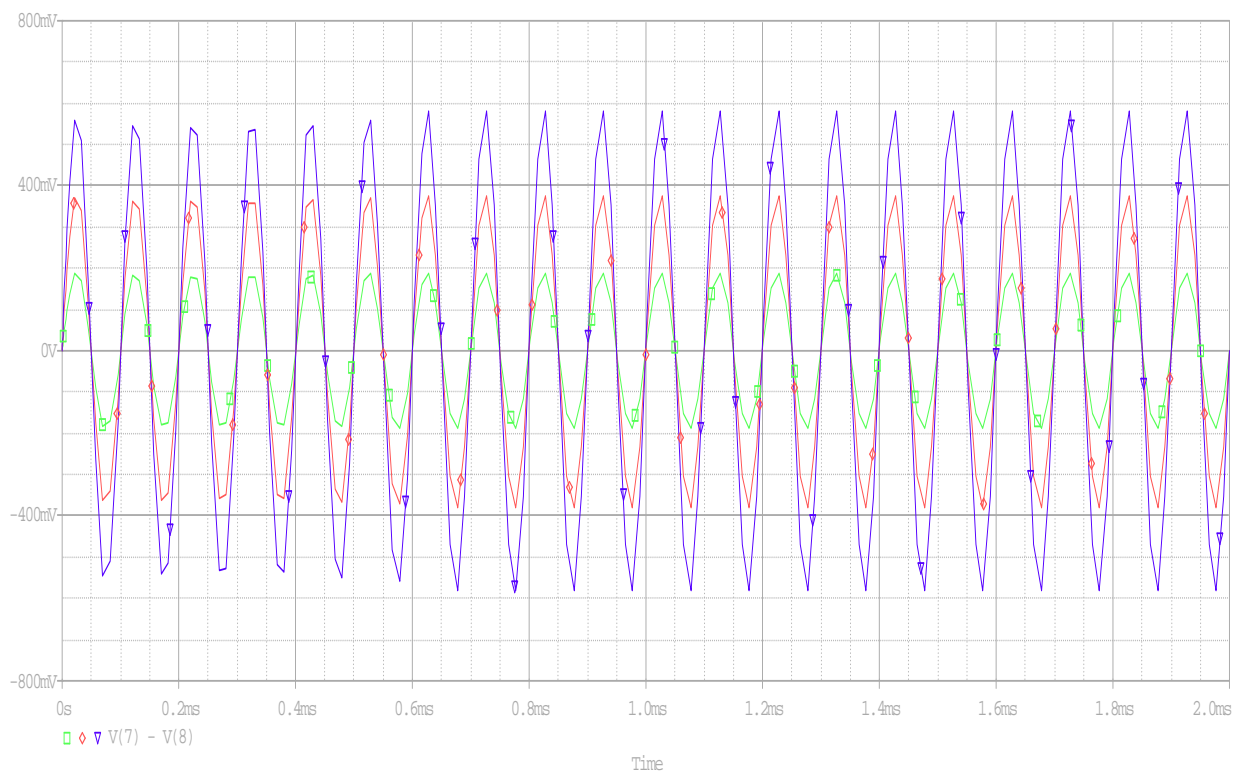


Fig. 3.8 Transient response of voltage amplifier

3.3 Differential voltage current conveyor:

The DVCC was first proposed by PAL as a modified current conveyor [9] and then developed and realized in CMOS technology by Elwan and Soliman [10].

The DVCC has the advantages of both of the second generation current conveyor (such as large signal bandwidth, great linearity, wide dynamic range) and the differential difference amplifier (DDA) (such as high input impedance and arithmetic operation capability). This element is a versatile building block for applications demanding floating input. The electrical symbol and related equations are given in Fig.3.9.

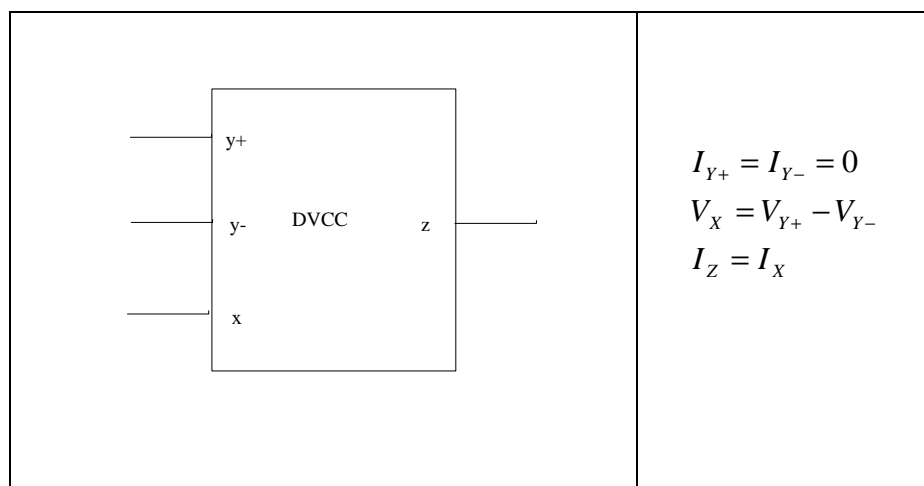


Fig. 3.9 Basic block of DVCC and related equation

3.3.1 The CMOS implementation of DVCC:

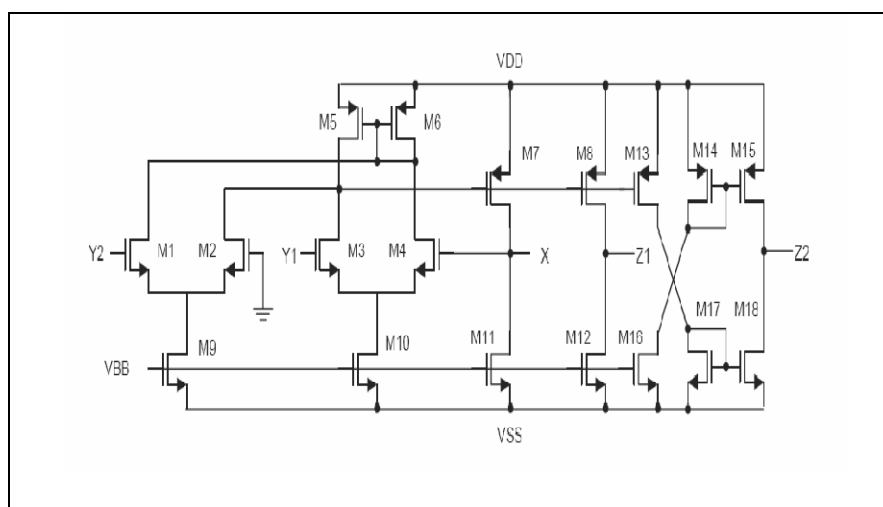


Fig. 3.10 The CMOS implementation of DVCC

The aspect ratios of the CMOS transistors of the DVCC are given in table below. MIETEC 0.5 μ m CMOS process model used for simulation. $V_{dd}=-V_{ss}=2.5V$

Transistor	W(μ m)/l(μ m)
M1, M2, M3, M4	0.8/0.5
M5, M6	4/0.5
M9, M10	14.4/0.5
M7, M8, M13, M14, M15	10/0.5
M11, M12, M16, M17, M18	45/0.5

3.3.2 Simulation results:

3.3.2.1 Current mode amplifier using DVCC:

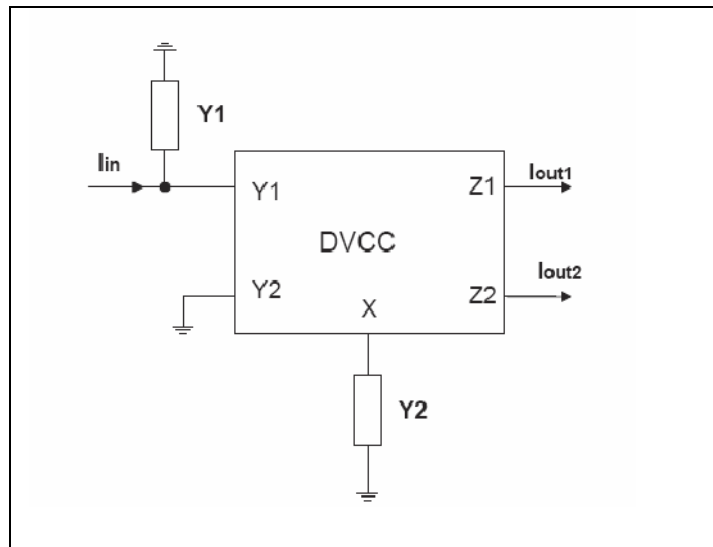


Fig. 3.11 DVCC based basic current processing block

If in fig.3.9 the admittances are $Y_1=1/R_1$ and $Y_2= 1/R_2$, the current-mode amplifier can be found as:

$$\frac{I_{OUT1}}{I_{IN}} = -\frac{I_{OUT2}}{I_{IN}} = \frac{R_1}{R_2}$$

The gain of the amplifier can be adjusted by changing R_1 and/or R_2 .

The following values of components were selected to realize a current-mode amplifier using DVCC are $R_1 = 10K, 20K$ and $30K$, and $R_2 = 10K$

And approximately bandwidth of the circuit is 180MEGHZ

The simulated output result are shown in fig.3.12

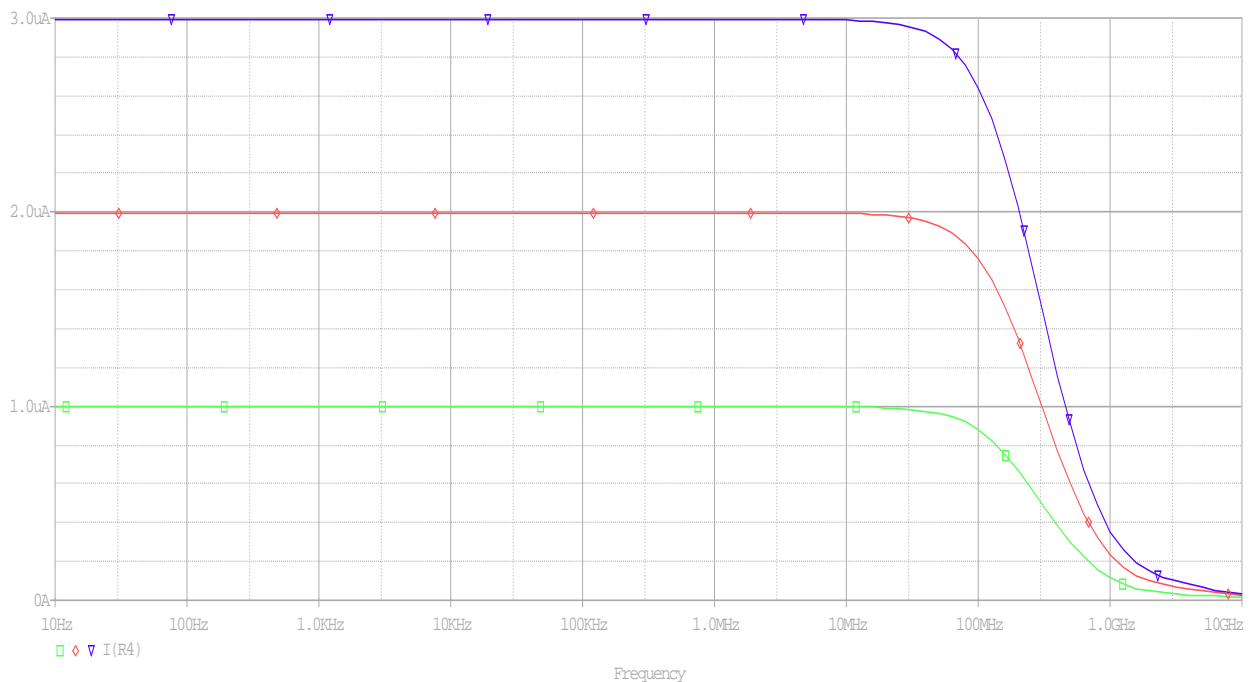


Fig. 3.12 Frequency response of current amplifier

3.3.2.2 Current mode integrator using DVCC:

If in fig.3.11 the admittances are $Y_1 = sC_1$ and $Y_2 = 1/R_2$. The current-mode integrator can be achieved as

$$\frac{I_{OUT1}}{I_{IN}} = \frac{-I_{OUT2}}{I_{IN}} = \frac{1}{sC_1R_2}$$

3.3.2.3 Differentiator using DVCC:

If the admittances are $Y_1=1/R_1$ and $Y_2=sC_2$ the current-mode differentiator can be obtained as

$$\frac{I_{OUT1}}{I_{IN}} = \frac{-I_{OUT2}}{I_{IN}} = sC_2R_1$$

The following values of components were selected to realize a current-mode integrator using CCII are $R_1=1K$ and $C_2=.1\mu F$.



Fig. 3.13 Output of differentiator

3.3.2.4 Summer/Substructure:

Differentiated input currents converted to voltages can be applied to the Y - terminals of the DVCC, which results in a current-mode summer/substructure circuit as shown in Fig.3.14 the output currents can be found as:

$$I_{OUT1} = -I_{OUT2} = \frac{R_1}{R_3}(I_1 + I_2) - \frac{R_2}{R_3}(I_3 + I_4).$$

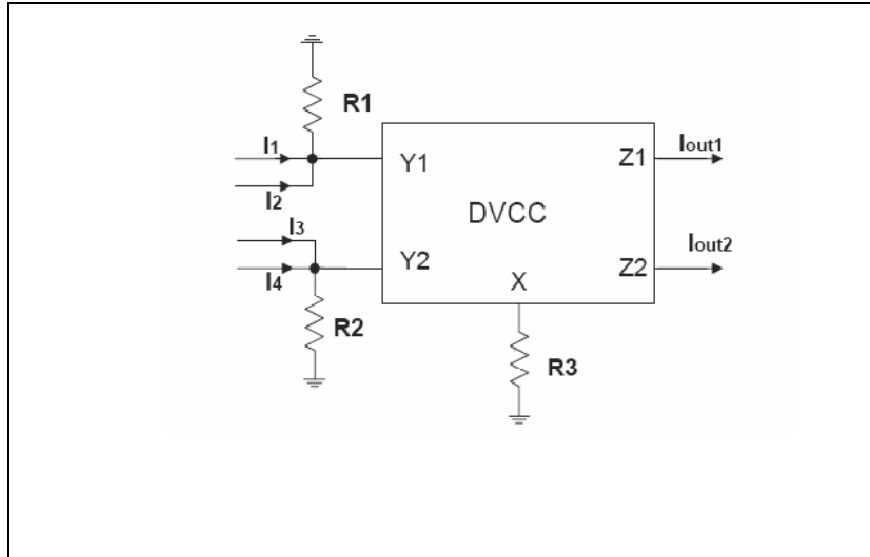


Fig. 3.14 DVCC based CM summer/substructure circuit

The following values of components were selected to realize a current-mode summer/substructure circuit which are $R_1=R_2=R_3=10K$. The simulated result are shown in fig.3.13

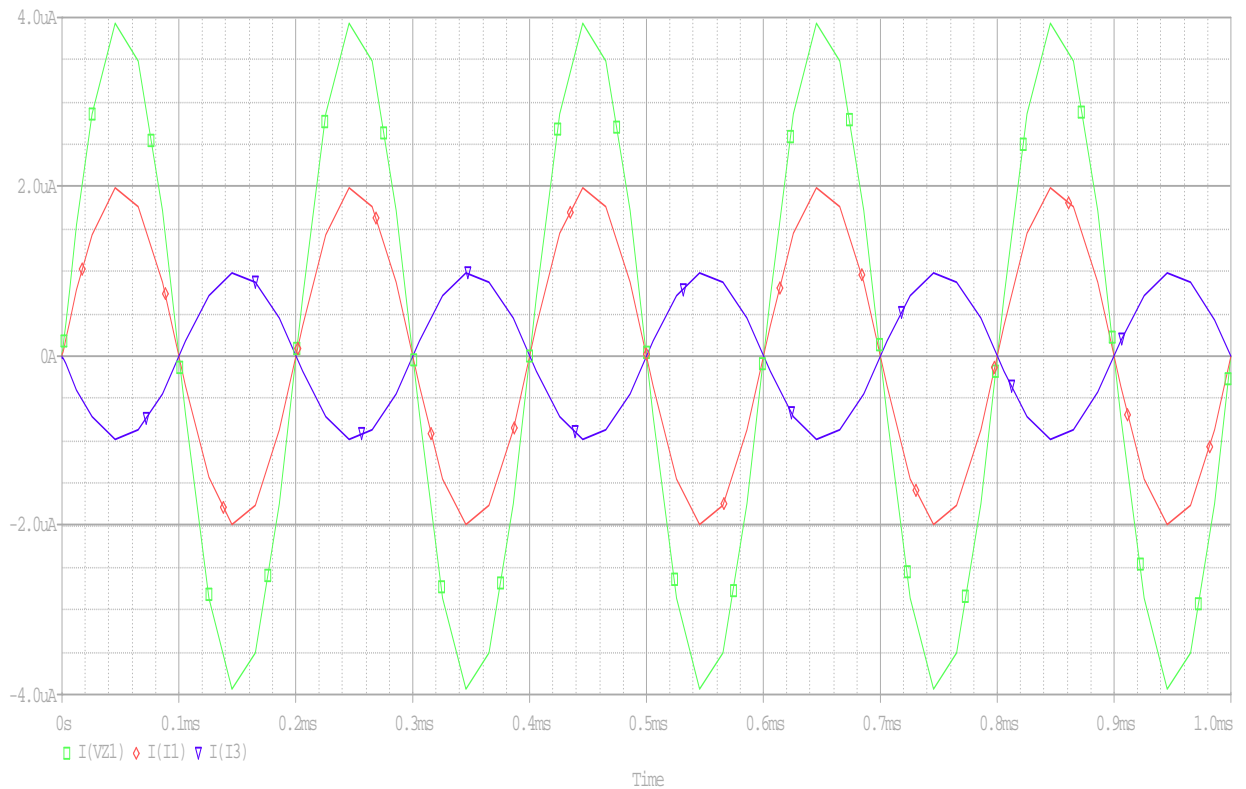


Fig. 3.15 Input and Output waveform of summer/substructure

3.3.2.5 Universal filter:

Using the terminal relation between the Y - and X -terminal and after the current to voltage ($I \rightarrow V$) conversions, the CM universal filter can be implemented from as shown in Fig. 3.16. It can be observed that the first stage is the summer and the second and third stages are the integrators circuit stages. The node analysis of the circuit of Fig. 3.16 yields the following current transfer functions:

$$\frac{I_{HP}}{I_{IN}} = \frac{\frac{R_1}{R_2} s^2}{s^2 + \frac{1}{C_1 R_2} s + \frac{R_1}{R_2 R_3 R_4 C_1 C_2}}$$

$$\frac{I_{BP}}{I_{IN}} = -\frac{\frac{R_1}{R_2 R_3 C_1} s}{s^2 + \frac{1}{C_1 R_2} s + \frac{R_1}{R_2 R_3 R_4 C_1 C_2}}$$

$$\frac{I_{LP}}{I_{IN}} = -\frac{\frac{R_1}{R_2 R_3 R_4 C_1 C_2} s}{s^2 + \frac{1}{C_1 R_2} s + \frac{R_1}{R_2 R_3 R_4 C_1 C_2}}$$

The natural angular frequency ω_0 and the quality factor Q of the filter can be expressed as

$$\omega_0 = \sqrt{\frac{R_1}{R_2 R_3 R_4 C_1 C_2}} \quad Q = \sqrt{\frac{R_1 R_2 C_1}{R_3 R_4 C_2}}$$

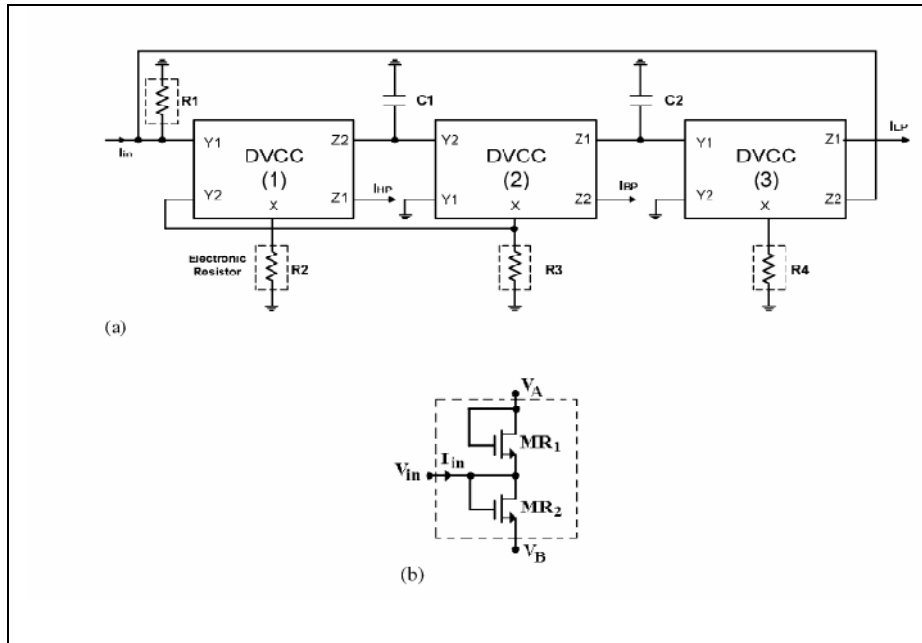


Fig. 3.16 (a) the proposed CM universal filter based on DVCC

(b) Electronic resistor

The following values of components were selected to realize a current-mode universal filter based on DVCC with a cut-off frequency of $f_0=15.719$ KHZ are $R_1=R_2=R_3=R_4=10K$ and $C_1=C_2=.001\mu F$. The simulated output result are shown in fig.3.17

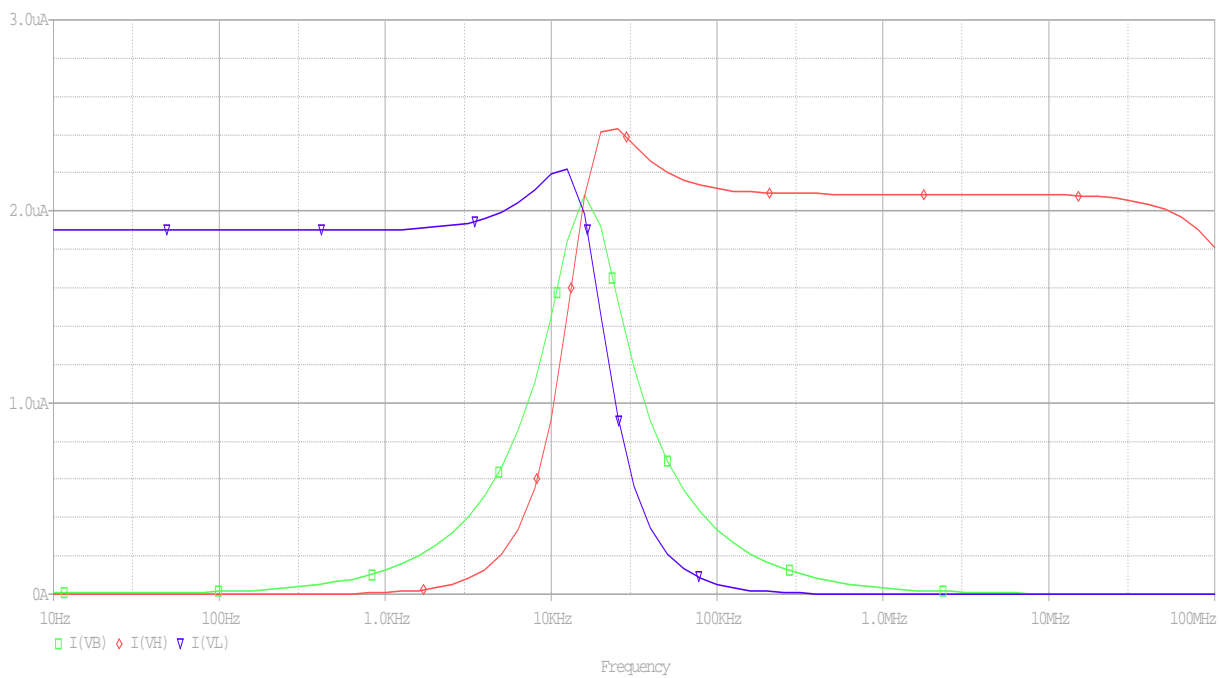


Fig. 3.17 Frequency response of current-mode universal filter using DVCC

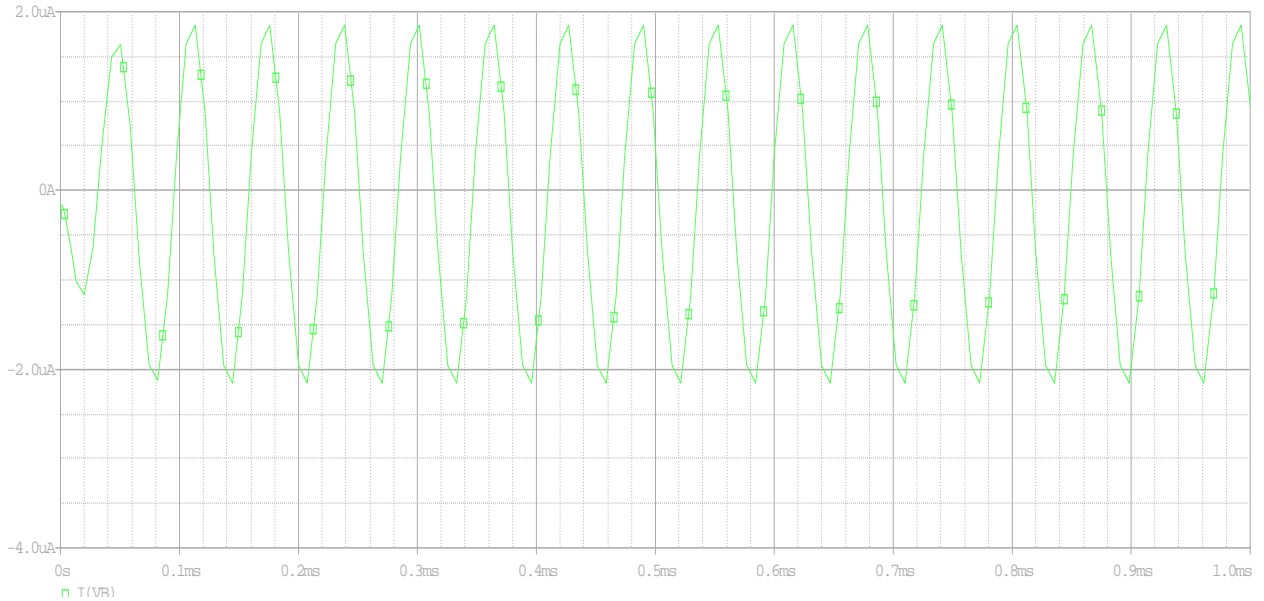


Fig. 3.18 Transient response of current-mode universal filter using DVCC

3.4 Current differencing buffered amplifier (CDBA):

The current differencing buffered amplifier (CDBA) is a recently reported active component [12-19], especially suitable for class of analogue signal processing application. The fact that the device can operate in both voltage and current modes provides flexibility and enables a variety of circuit designs. The basic building block and related equations are given in Fig.3.19.

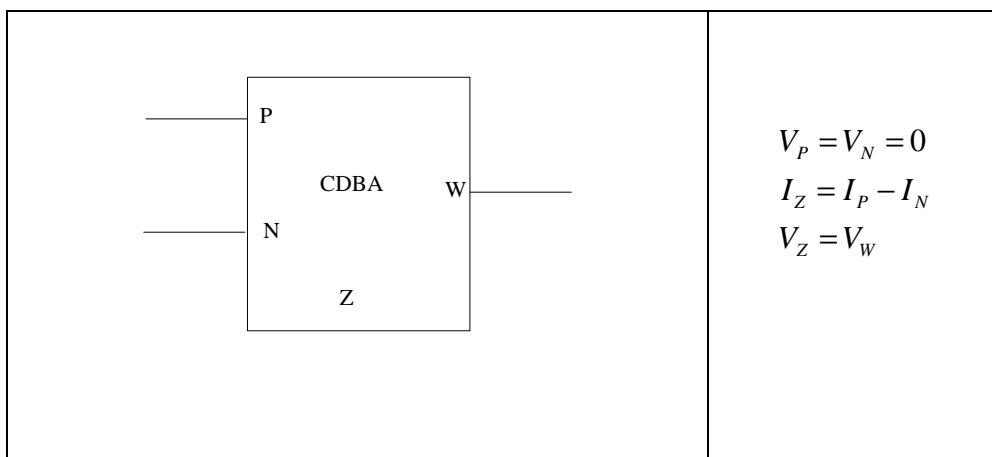


Fig. 3.19 Basic block of CDBA and related equation

3.4.1 The CMOS implementation of CDBA:

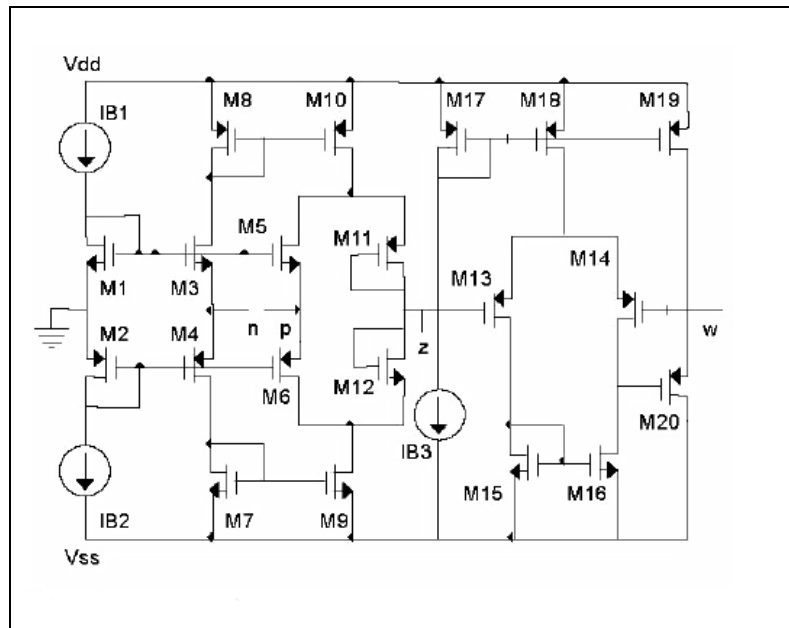


Fig. 3.20

Section current are $I_{B1}=I_{B2}=20\mu\text{A}$, while $I_{B3}=25\mu\text{A}$. $0.5\mu\text{m}$ CMOS process model used for simulation. Bias current of Current Differencing input. The aspect ratios of the CMOS transistors of the CDBA are given in table below. MIETEC $V_{dd}=-V_{SS}=2.5\text{V}$

Transistor aspect ratio

Transistor	$W(\mu\text{m})/l(\mu\text{m})$
M1-M10	150/1
M11, M12	4/2
M13, M14, M17, M18	5/1
M15, M16	100/1
M19	20/1
M20	200/1

3.4.2 Simulation results:

3.4.2.1 Voltage mode amplifier using CDBA:

If in fig.3.18 a voltage mode amplifier using CDBA is shown. The impedances are R_1 & R_2 and the voltage-mode amplifier can be found as:

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2}{R_1}$$

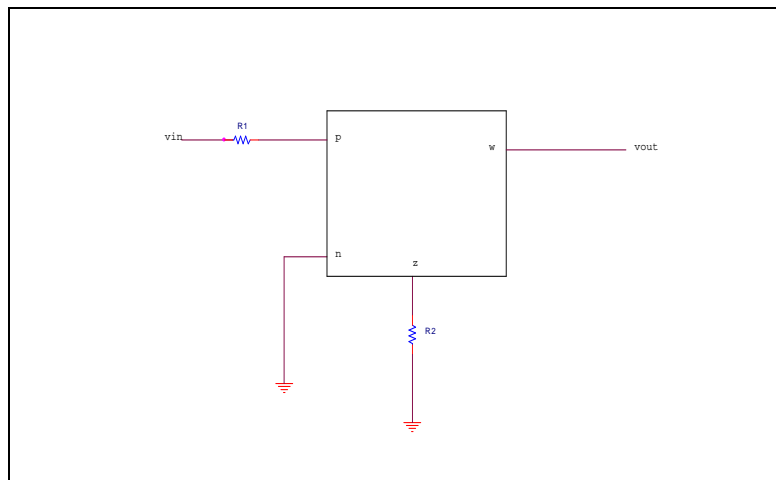


Fig. 3.21 Voltage Mode Amplifier using CDBA

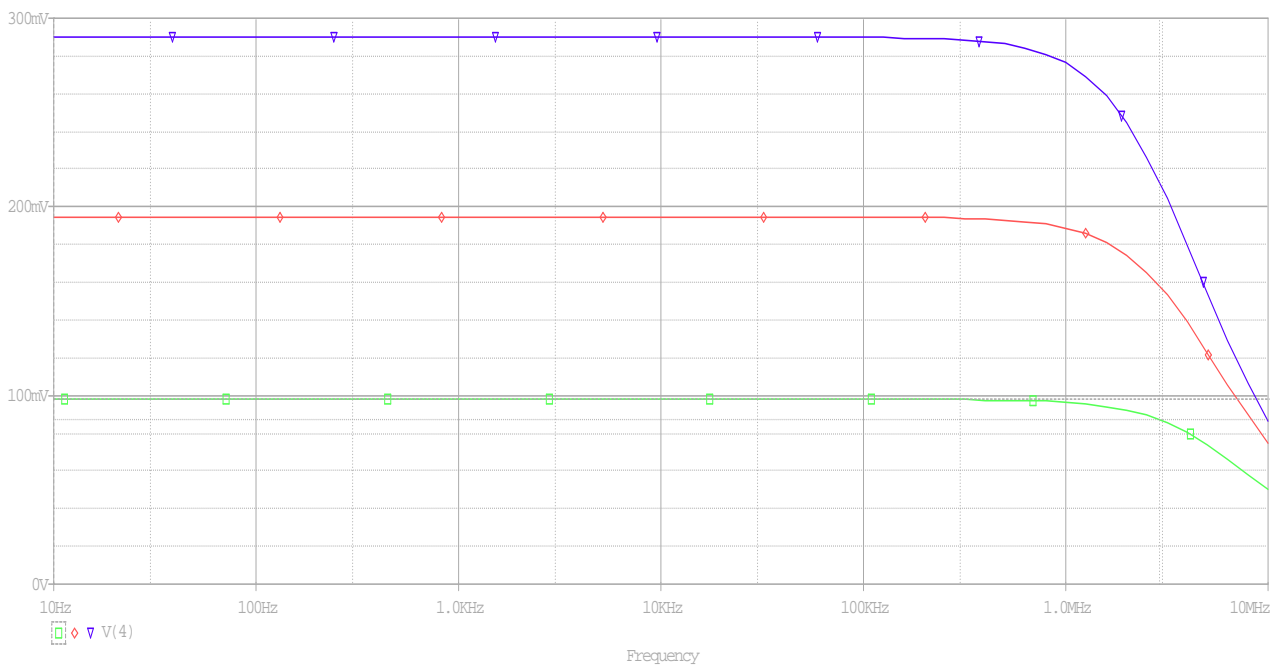


Fig. 3.22 Frequency response of Voltage Mode Amplifier

The gain of the amplifier can be adjusted by changing R_1 and/or R_2 . The following values of components were selected to realize a current-mode amplifier using DVCC are $R_2 = 100K$, $200K$ and $300K$, and $R_1 = 100K$, and approximately bandwidth of the circuit is $3MEGHZ$.

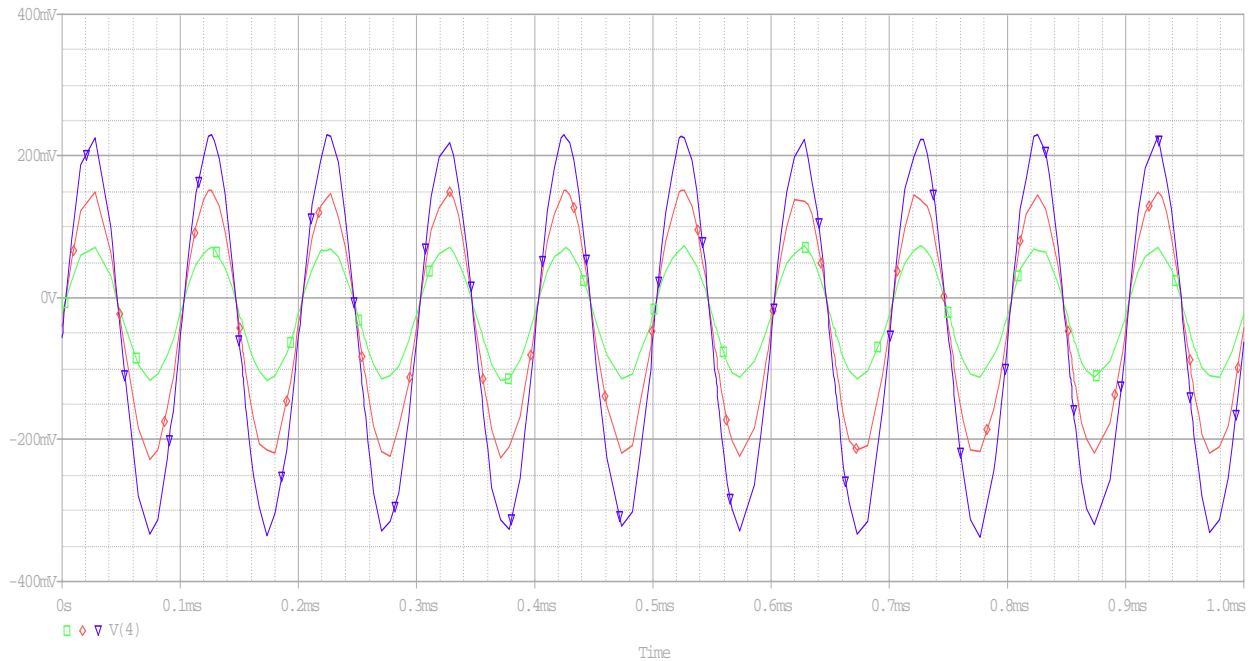


Fig. 3.23 Transient response of Voltage Mode Amplifier

3.4.2.2 Notch filter using CDBA:

A current-mode second-order notch filter circuit [19] is given in fig.3.21. The current transfer function of the circuit is given as follows:

$$\frac{I_{OUT}}{I_{IN}} = \frac{s^2 + s \left(\frac{1}{C_1 R_1} + \frac{1}{C_2 R_2} - \frac{1}{C_1 R_2} \right) + \frac{1}{C_1 C_2 R_1 R_2}}{s^2 + s \left(\frac{1}{C_1 R_1} + \frac{1}{C_2 R_2} + \frac{1}{C_1 R_2} \right) + \frac{1}{C_1 C_2 R_1 R_2}}$$

Therefore matching condition for the realization of the second-order notch filter will be $C_1 R_1 + C_2 R_2 = C_2 R_1$. The natural frequency, ω_0 and quality factor, Q for the filter can be expressed as:

$$\omega_0 = \sqrt{\frac{1}{C_1 C_2 R_1 R_2}}$$

$$Q = \frac{\sqrt{C_1 C_2 R_1 R_2}}{C_1 R_1 + C_2 R_2 + C_2 R_1}$$

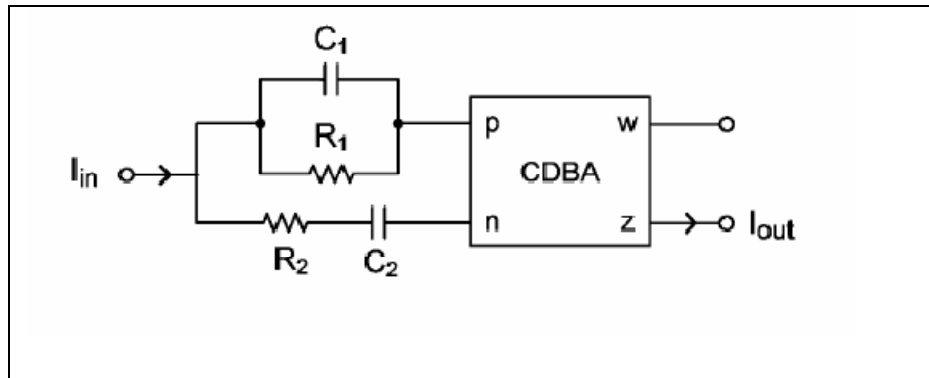


Fig. 3.24 Current Mode Second Order Notch Filter

The following values of components were selected to realize a current-mode second order notch filter using CDBA with a centre frequency $f_c = 127\text{KHZ}$ are $R_1=50\text{k}$, $R_2=25\text{K}$, $C_1=25\text{PF}$, And $C_2=50\text{PF}$.The simulated output result are shown in fig.3.25

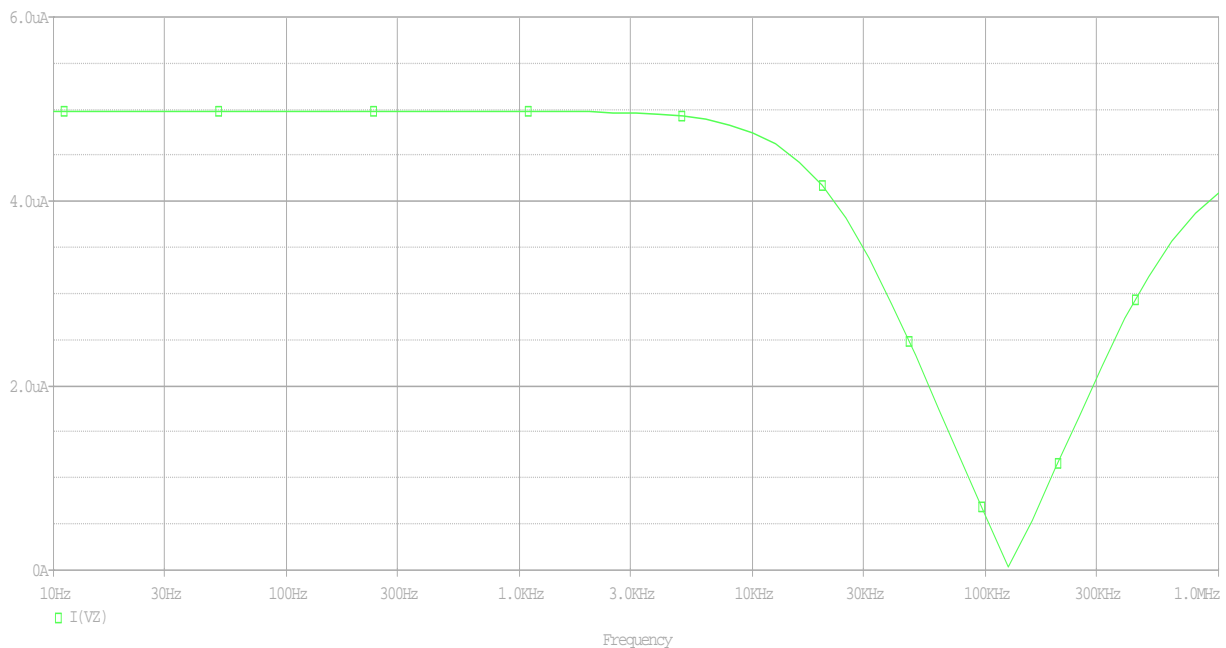


Fig. 3.25 Frequency response of notch filter using CDBA

3.5 CONCLUSION:

Various circuits for realizing analog signal processing functions used in instrumentation and control using various active elements (FDCCII, CDBA, & DVCC) have been analyzed and they are simulated in PSpice. Simulation results closely match with theoretical values.

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CHAPTER -4

CURRENT DIFFERENCING CURRENT CONVEYOR (CDCC) AND ITS APPLICATIONS

4.1 Introduction:

The CDCC (Current Differencing Current Conveyor) [7] has been proposed as a generalization of the CDeTA. The basic idea starts from the observation that OTA can be implemented by the 2nd-generation current conveyor and one resistor. The admittance of a two-pole connected between the x terminal of the CCII and the ground serves as the generalized transconductance. In this case, the operations of the CDCC and the CdeTA are similar. However, CDCC is more universal because of its “ i ” terminal, which can be used as an additional current input. Circuit diagram and related equation is given in fig.4.1

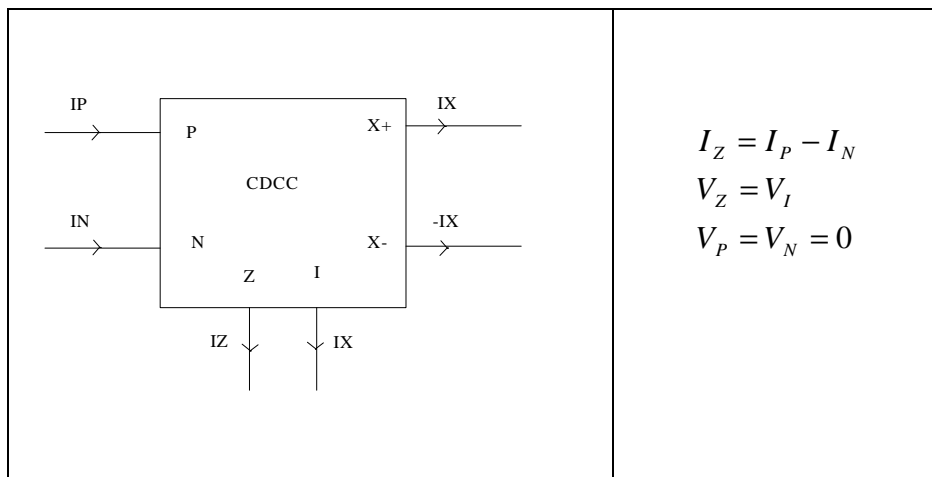


Fig. 4.1 Basic CDCC block and port relation

4.2 DVCC implementation of CDCC:

To implement CDCC we have taken three DVCC presented in chapter3. The proposed implementation is shown in Fig.4.2 where the two input currents are sensed using two DVCC. With all the Y terminals grounded the input impedance is very low. The two currents are subtracted at one of the input nodes and the corresponding current conveyor conveys the current difference to the Z terminal.

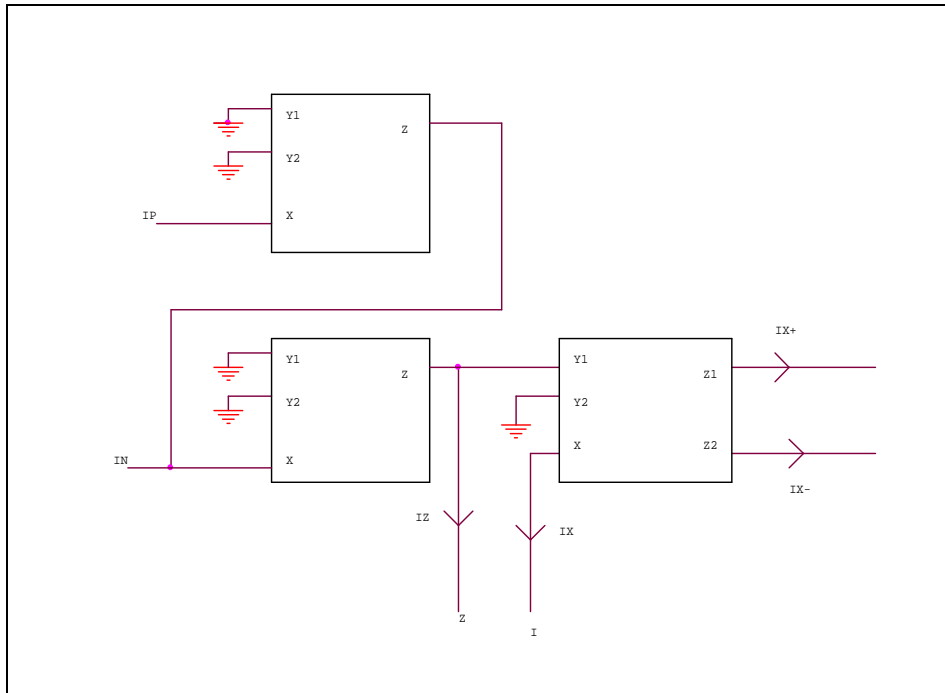


Fig. 4.2 DVCC implementation of CDCC

The CMOS implementation of DVCC

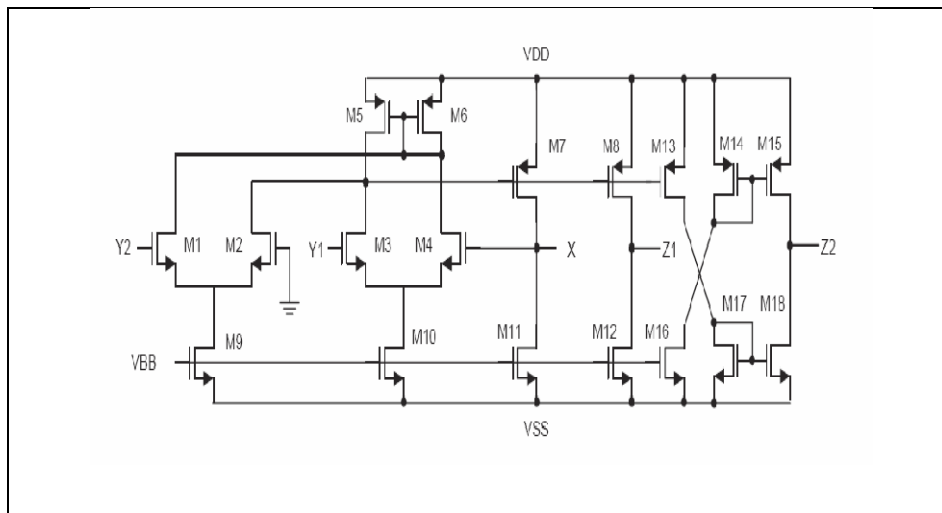


Fig. 4.3 The CMOS implementation of DVCC

4.3 Simulation results:

The CDCC has been implemented using DVCC described in chapter 3. The CDCC has been used to design the following signal processing blocks.

1. Fully differential current –mode amplifier
2. Fully differential current –mode universal filter
3. Fully differential current –mode universal filter with gain tunability

4.3.1 Current-mode fully differential amplifier using CDCC:

The proposed amplifier uses two grounded resistors and is shown below in Fig 4.4. The gain of the amplifier is given below as

$$\frac{I_{OUT}}{I_{IN}} = \frac{2R_1}{R_2}$$

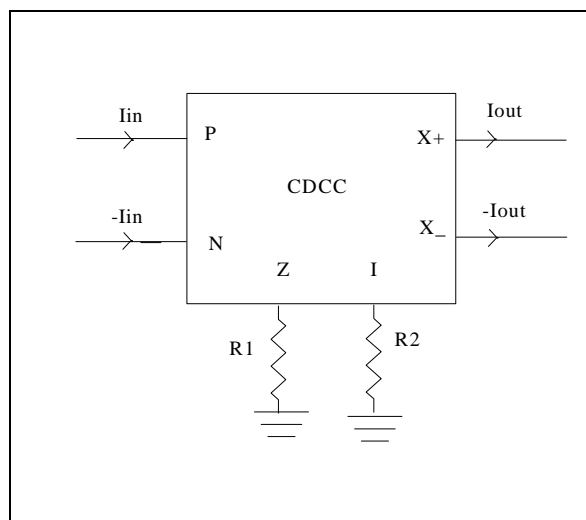


Fig. 4.4 Current mode fully differential amplifier using CDCC

The following values of components were selected to realize a gain of 1, 2 and 3 $R_1=1K$, 2K, 3K, and $R_2=1K$, with given input $I_{in} = 5\mu A$ (P-P). The frequency response measured in Pspice are given below in Fig. 4.5. The measured value of gain is (0.962, 1.92, 2.91,)

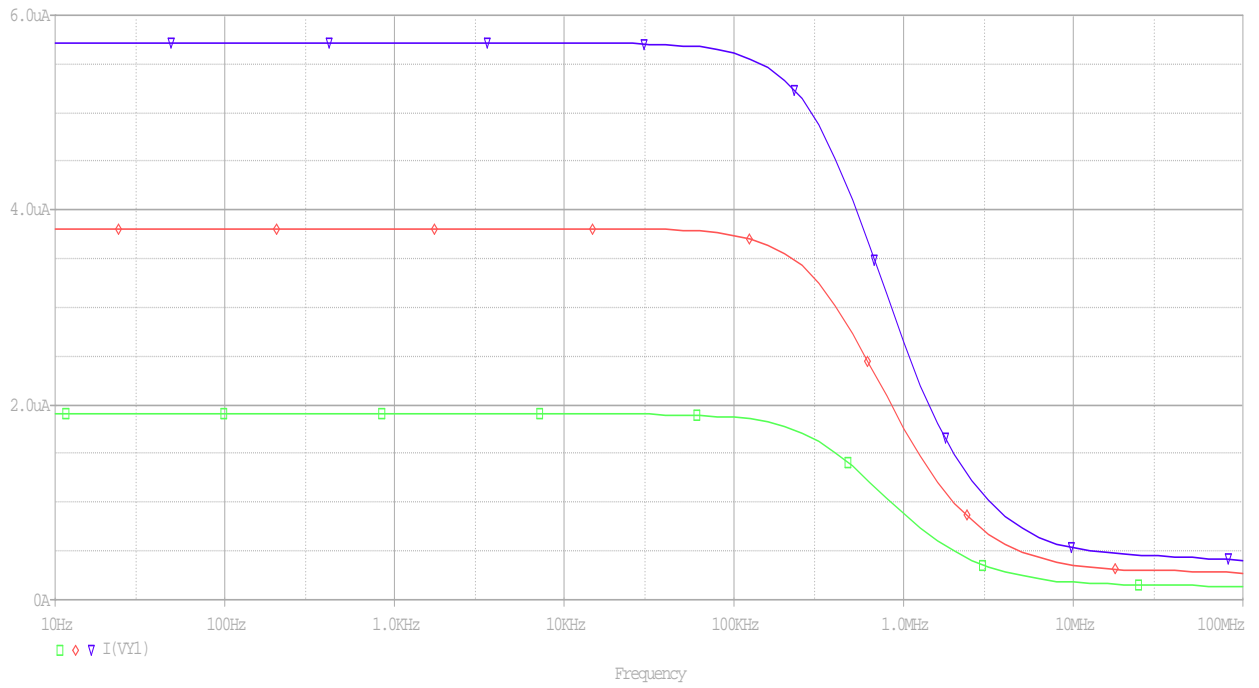


Fig. 4.5 Frequency response of amplifier

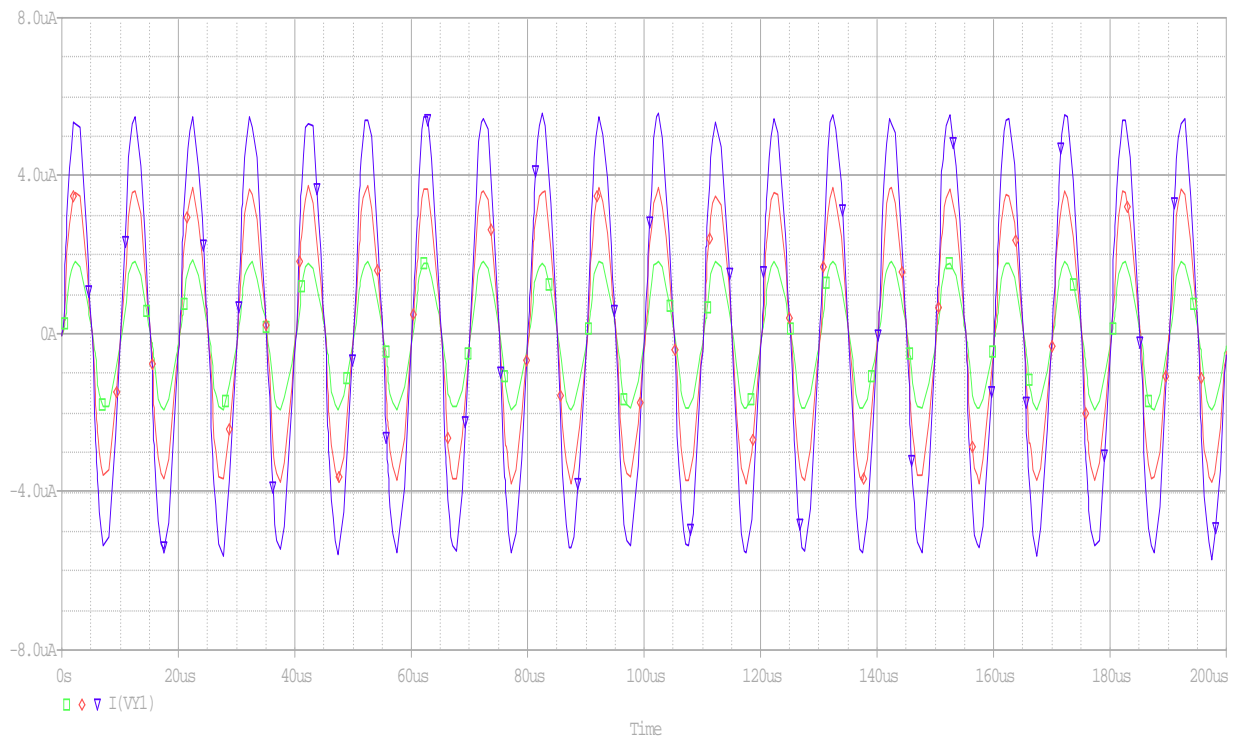


Fig. 4.6 Transient response of amplifier

4.3.2 Current-mode fully differential universal filter using CDCC:

Current-mode fully-differential universal filter using CDCC requires four CDCC blocks , first two having two outputs (two X-) and last two having six (Three X+ and Three X-) output current terminals. First two CDCC block attached in the circuit only for producing two IHP output, last two blocks are actual processing block

Last two CDCC blocks are lossy integrator connected in series. The circuit simultaneously provides the three basic filter functions, namely band pass (BP), high pass (HP) and low pass (LP) functions. The notch and all pass (AP) functions can be obtained by connecting appropriate output currents directly without using additional active elements. The output signals are obtained at high output impedance ports, which is important for easy cascading in CM operation.

Current-mode fully differential universal filter using CDCC is given in fig.4.7 various filter transfer functions are given below

$$\frac{I_{HP}}{I_{IN}} = \frac{s^2}{s^2 + \frac{2s}{R_1C_1} + \frac{4}{R_1C_1R_2C_2}}$$

$$\frac{I_{BP}}{I_{IN}} = \frac{\frac{2s}{R_1C_1}}{s^2 + \frac{2s}{R_1C_1} + \frac{4}{R_1C_1R_2C_2}}$$

$$\frac{I_{LP}}{I_{IN}} = \frac{\frac{4}{R_1R_2C_1C_2}}{s^2 + \frac{2s}{R_1C_1} + \frac{4}{R_1C_1R_2C_2}}$$

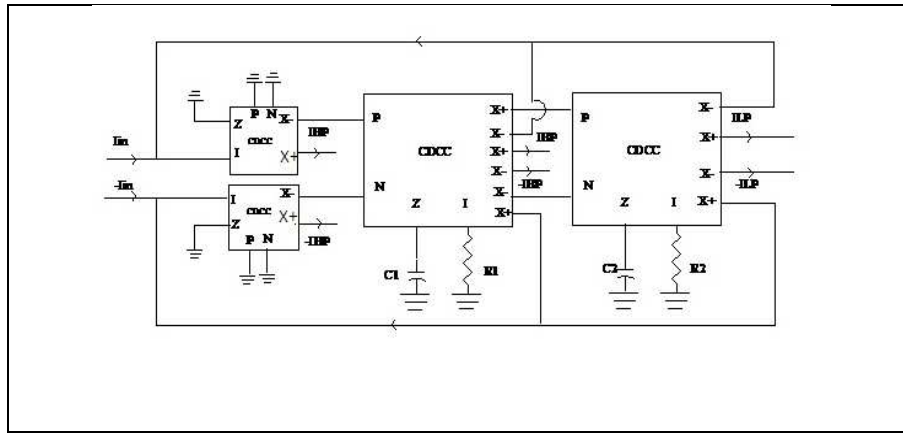


Fig. 4.7 Current mode fully differential universal filter

The natural frequency, ω_0 and quality factor, Q for the filter can be expressed as;

$$\omega_0 = \sqrt{\frac{4}{R_1 R_2 C_1 C_2}} \quad Q = \sqrt{\frac{R_1 C_1}{R_2 C_2}}$$

The following values of components were selected to realize a current-mode fully-differential universal filter with a cut-off frequency of $f_0 = 100\text{KHz}$ and The value of the component used are $R_1 = R_2 = 150\text{K}\Omega$, and $C_1 = C_2 = .00002\mu\text{F}$. The simulated result are shown in fig.4.8 (a) and (b)

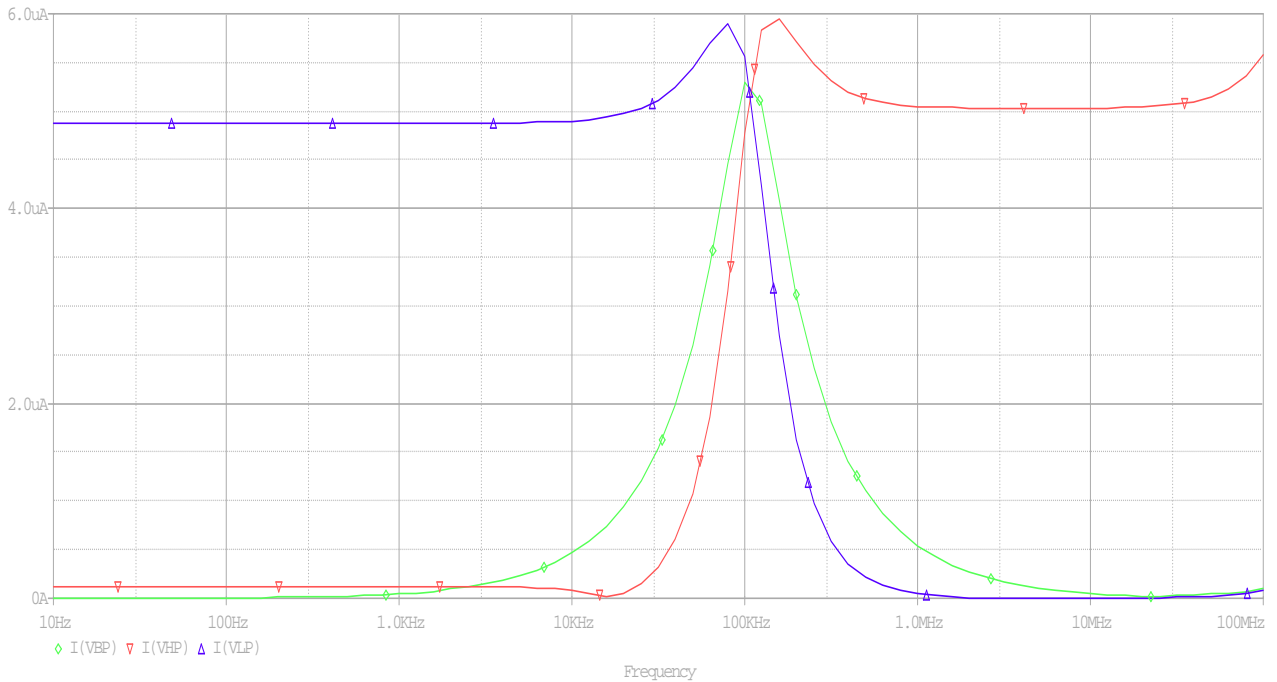


Fig. 4.8 (a) Frequency response of fully differential universal filter

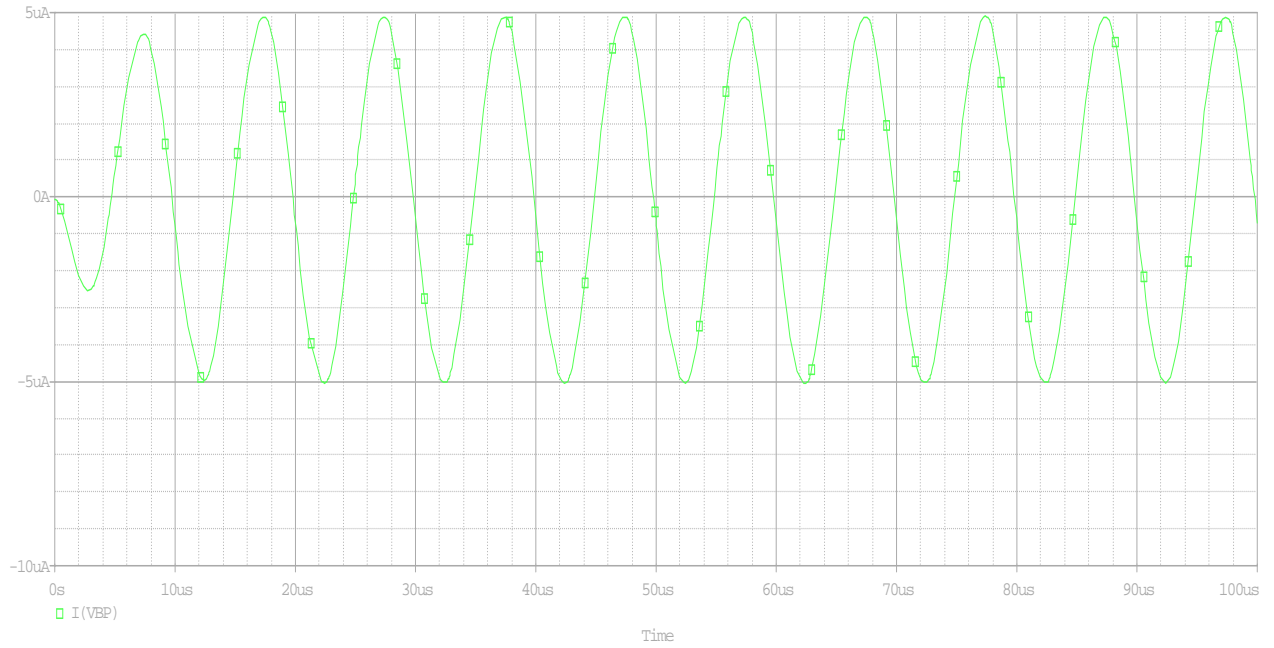


Fig. 4.8 (b) Transient response

4.3.3 Current-mode fully differential universal filter using CDCC with gain tuneability:

It requires two additional CDCC blocks so that we can amplify the input signal to get the desired value of gain. Current-mode fully differential universal filter with gain tuneability using CDCC is given in fig.4.9. Various filter transfer functions are given below:

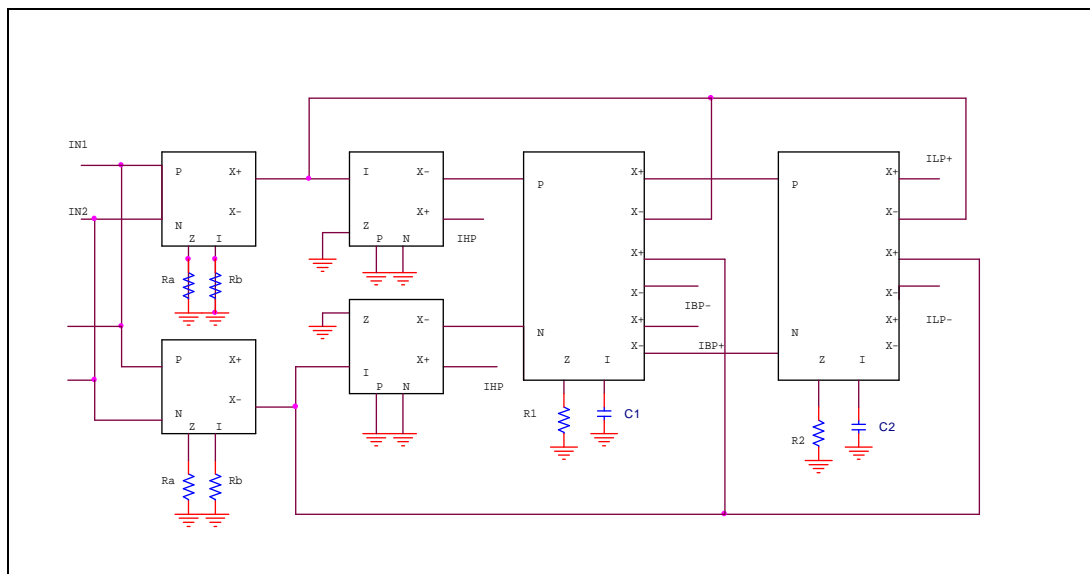


Fig. 4.9 Current mode fully differential universal filter with gain tuneability

$$\frac{I_{HP}}{I_{IN}} = \frac{\frac{R_a}{R_b} s^2}{s^2 + \frac{2s}{R_1 C_1} + \frac{4}{R_1 C_1 R_2 C_2}}$$

$$\frac{I_{BP}}{I_{IN}} = \frac{\frac{R_a}{R_b} \frac{2s}{R_1 C_1}}{s^2 + \frac{2s}{R_1 C_1} + \frac{4}{R_1 C_1 R_2 C_2}}$$

$$\frac{I_{LP}}{I_{IN}} = \frac{\frac{R_a}{R_b} \frac{4}{R_1 R_2 C_1 C_2}}{s^2 + \frac{2s}{R_1 C_1} + \frac{4}{R_1 C_1 R_2 C_2}}$$

The natural frequency, ω_0 and quality factor, Q for the filter can be expressed as;

$$\omega_0 = \sqrt{\frac{4}{R_1 R_2 C_1 C_2}}$$

$$Q = \sqrt{\frac{R_1 C_1}{R_2 C_2}}$$

The following values of components were selected to realize a current-mode fully-differential KHN biquad filter with a cut-off frequency of $f_0 = 100\text{KHZ}$ and The value of the component used are $R_1 = R_2 = 150\text{K}\Omega$, $C_1 = C_2 = 0.00002\mu\text{F}$ and $R_a = 20\text{k}$, $R_b = 10\text{k}$ to get the gain of value 2 The simulated result are shown in fig.4.10 (a) and (b)

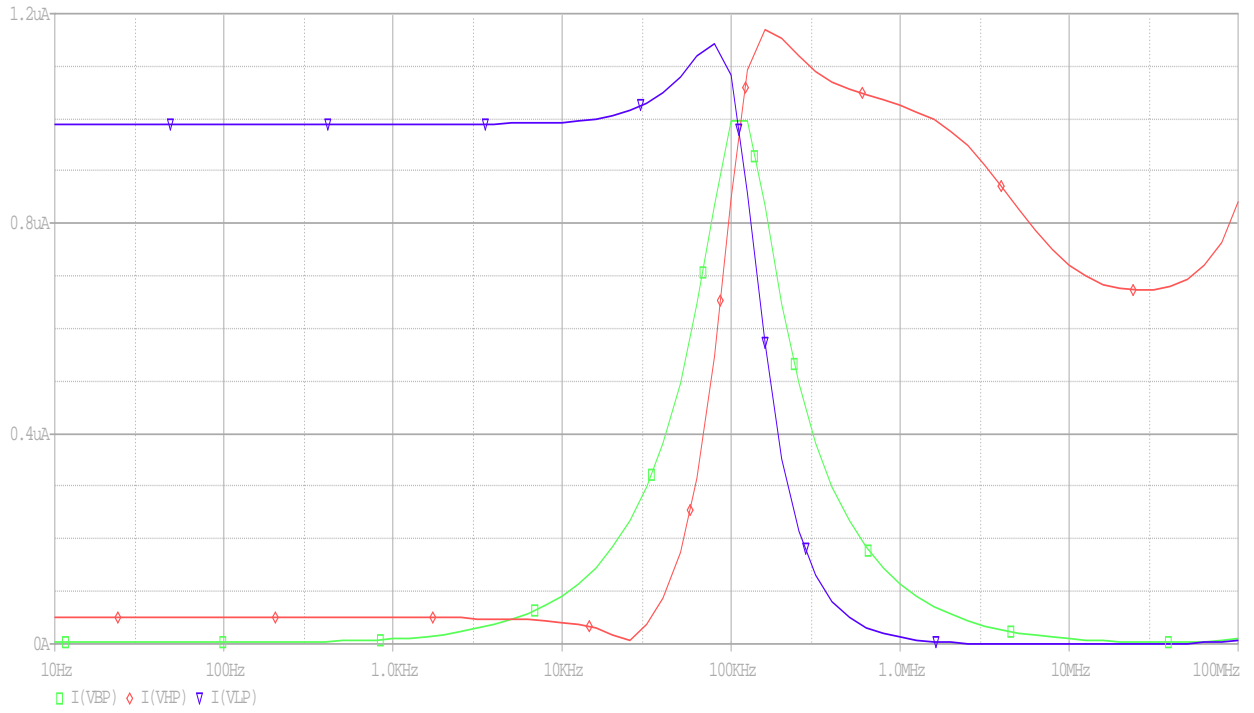


Fig. 4.10 (a) Frequency response of universal filter with tuneable gain

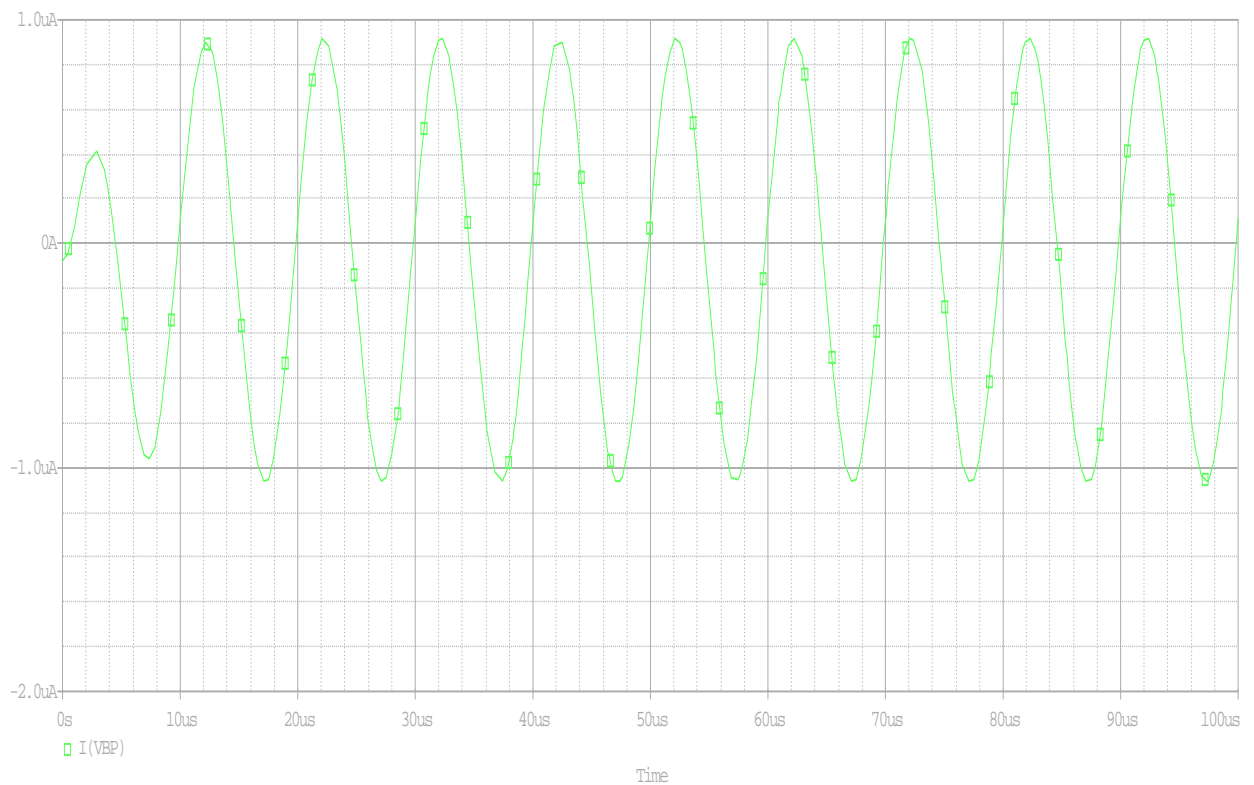


Fig. 4.10 (b) Transient response

4.4 CONCLUSION:

The newly proposed active element Current Differencing Current Conveyor (CDCC) is ideal for current mode fully differential functional circuits. In this work, A CMFD (current mode fully differential) Amplifier, CMFD universal filter circuit and a filter with gain tuneability has been presented. The Amplifier frequency response shows it has constant Bandwidth with variable gain. The filter employs four CDCCs, two capacitors and two resistors. All the passive elements are grounded, which is important in integrated circuit implementation. The filter provides the basic three filter functions (BP, HP and LP) simultaneously. The notch and all pass functions can be obtained by connecting appropriate output currents directly without using additional active elements. All the outputs are taken from high output impedances, which is important for cascade connections.

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CHAPTER -5

CONCLUSION

5.1 Introduction:

In the present dissertation some studies have been carried out on CMOS/Bipolar building blocks for instrumentation application.

In the first chapter general introduction of signal processing, evolution & advantage of current mode approach, difference between single ended and fully differential signal processing, and advantage of fully differential signal processing has been presented.

In the second chapter description of various types of fully-differential active building blocks such as differential difference amplifier, fully differential current conveyor, differential difference current conveyor etc. has been presented.

In the third chapter few sample realizations of various types of signal processing circuits such as current-mode amplifiers, integrators, differentiators and biquad filters in CMOS technology using the following types of active building blocks have been presented.

- (i) Second Generation Fully Differential Current Conveyor.
- (ii) Differential voltage Current Conveyor.
- (iii) Current Differencing Buffered Amplifier.

In the fourth chapter a newly introduced building block namely Current Differencing Current Conveyor and its DVCC implementation has been presented, that has been used to realize various fully-differential signal processing circuits such as fully differential current-mode amplifier, fully-differential current-mode integrator and fully-differential biquad filter, (with tuneable gain). This fully differential filter requires minimum passive components (all of which are grounded).

These signal processing circuits have been simulated on PSpice. Results closely match with theoretical values.

SCOPE FOR FURTHER WORK

In the present work the emphasis was on realization of fully-differential current-mode building blocks and associated applications. Lots of research activity is currently under way in the direction of development of fully-differential active building blocks. Several directions in which the present work can be extended have been given in reference 1 of chapter -1. Some of them are given below

- (i) Good CMOS implementations of Differential building blocks.
- (ii) Better methods of electronic controllability of relevant parameter of application circuits.
- (iii) Minimization of passive components required for a given signal processing applications.
- (iv) Minimization of active blocks required for a given signal processing application.