DSP Based Decomposed Multi User Digital Energy Metering System

A dissertation submitted towards the partial fulfillment of the requirement for the Award of the Degree of

Master of Engineering
in
Control & Instrumentation

Submitted by
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CERTIFICATE

This is to certify that the project entitled **"DSP Based Decomposed Multi User Digital Energy Metering System"**, which is being submitted by **Mr. Sandeep Sharma,** is a bonafide record of student's own work carried by him under my guidance and supervision in partial fulfillment of requirement for the award of the Degree of **Master of Engineering** in **Control & Instrumentation, Electrical Engineering Department, Delhi College of Engineering, University of Delhi.** The matter embodied in this project has not been submitted for the award of any other degree.

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Sandeep Sharma

Abstract

In the present scenario of power system a speculator growth of power quality related problems is noticed due to the rising use of all kind of power electronics devices. Widely used power electronic devices cause harmonics in voltage and current which complicates the energy transfer phenomena at harmonic frequencies. Control of power quality is one of the biggest challenges in all supply systems. Usually power quality monitoring is performed by the use of digital instruments based on Microprocessors and Digital Signal Processors. Real time harmonics and inter harmonics analysis and other real time calculations require the use of a DSP. The DSP internal RAM allows performing the temporal storage of sampled data and supporting the most time consuming computations. The present report discusses the drawbacks of traditional energy metering system, and provides a complete energy measurement setup using a Digital signal Processor. It aims to develop an energy meter that is cost effective (on account that it can monitor a number of users simultaneously), can be mounted on a distribution pole (or a place inaccessible to human interference), can measure active, reactive and harmonic power (using instantaneous reactive power theory) separately for each consumer.

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Chapter 1

Introduction

1.1 Introduction

Distribution electrical systems suffer from power quality problems such as current harmonics and reactive power burden. An accurate measurement of power amidst harmonics resulting from non-linear loads in power system has become more important because of increased significance of harmonics produced from non-linear loads. However voltage and current waveform distortion resulting from harmonic pollution has made the theory of power delivery a serious issue. The present accepted theory of instantaneous power assumes that, in a power supply system with non-linear loads, apparent power consists of active, reactive and distortion power (distortion volt-amp.). Distortion power is a measure of waveform distortion in power system. The distortion power occurs as a consequence of power due to currents and voltages of dissimilar frequencies [1-4]. The classical measurement of active and reactive power contains the term power factor. The power factor is not defined in satisfactory manner when waveform of current is distorted. The conventional energy meter (induction type) uses the classical definition of power and therefore gives erroneous results. Similar is the case with digital energy meters, which are prone to error due to presence of harmonics. Also these meters do not provide the complete metering solution as they measures only active power. Today correct measurement of reactive and distortion power is a major concern of power system industry.

Extraction of active and reactive currents has been reported in past for three phase power system for active filtering applications [7, 9]. The concept of p-q theory was extended for estimation of harmonic current component in single-phase system [8]. So far the utilization of theory has not been found for applications of energy estimation. An attempt has been done in this project to correctly estimate energy consumed by non linear loads [12]. Since these loads consume reactive as well as distortion power, the correct assessment of wastage of energy is a must.

1.2 Main Features

Decomposed

The most important feature of this energy meter is that it decomposes the active, reactive and harmonic content of the power which is of prime concern in the present scenario.

Pole Mounted

As this energy meter will be mounted on the distribution pole instead of the consumers' premises. This makes it tamper proof.

Multi-user

One energy meter will record the readings of a number of consumers connected to a particular pole providing an economic advantage.

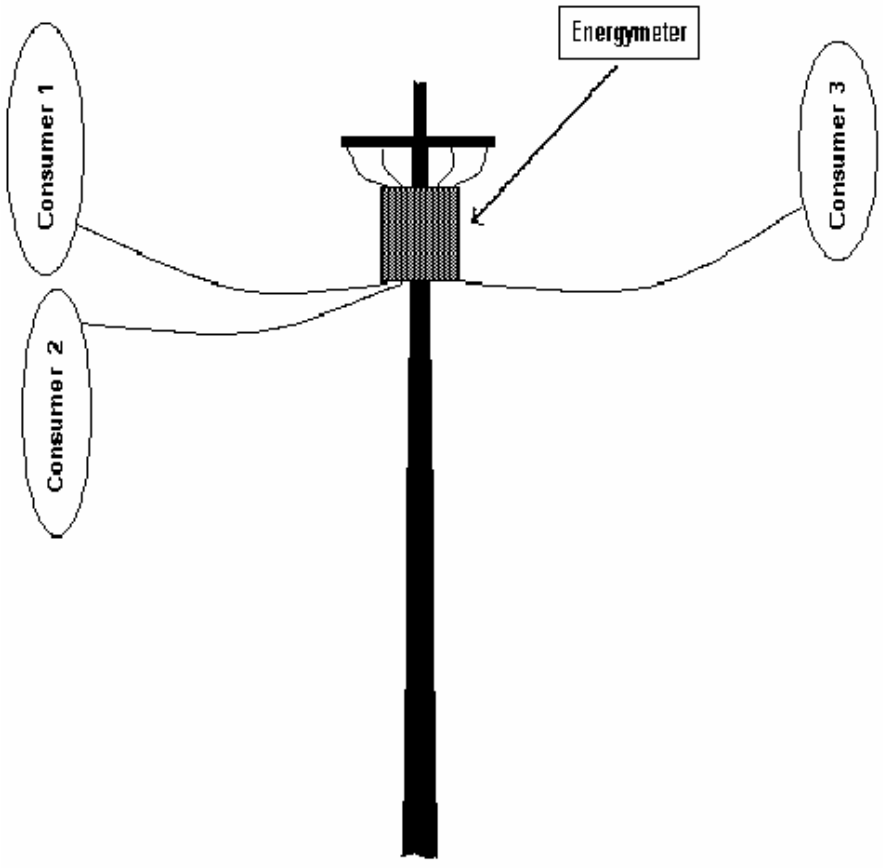


Figure 1.1 Pole Mounted Multi User Energy Meter

DSP Based

The use of DSP (TMS320VC5416) facilitates the real time processing and separation of real, reactive and harmonic power by using powerful algorithms.

Remotely Recording

The processed data is stored in the memory and is transmitted to the control room (central recording station) after few minutes for further processing (billing, load forecasting etc)

1.3 Principle of Operation

This energy meter works on the principle of instantaneous reactive power theory. The instantaneous values of voltages and currents are sampled for different consumers using voltage and current transducers (V9ltage sensors and Hall Effect Transducers). This data is sent to the ADC (Analog to Digital Converter) of Digital Signal Processor. DSP picks the data, processes it and stores the data for different consumers separately.

1.4 Advantages over conventional energy meters

Curbs power theft

Provides the complete record of the power sent from the substation and the power consumed by the various registered consumers and hence is helpful in detecting any unauthorized tapping of power in any locality.

Tamper proof

Since the device is mounted on the distribution pole, it is out of reach of human beings. Proper shielding provided in the energy meter makes it immune to external or stray magnetic and electric fields.

Measures Active, Reactive and Harmonic Powers

Robust design and real time processing capability of the DSP enables it to

implement the instantaneous reactive power algorithms to calculate active, Reactive and Harmonic Powers in Real time. Consumers producing more reactive and Harmonic powers can hence be fined for polluting the power system.

Cost effective

Since this meter is based on a multi user concept, it can service a number of customers, so the cost per user decreases.

Automatic Data Recording

The meter transmits the energy consumption readings automatically to the central recording station which eliminates human intervention in the recording process, thereby making it more reliable and efficient

Facilitates online billing and load forecasting

Centralized data recording facilitates online database creation which can be used for online billing, load forecasting and other such studies.

1.5 Need of this concept

Non-Linear loads do not follow ohms law thus if a sinusoidal voltage is applied to a non-linear load, the current waveform would be non-sinusoidal. This non-sinusoidal current causes non-sinusoidal voltage drop across the system impedance and in turn the voltage also becomes non-sinusoidal. A common mistake made while doing power computations for non-linear loads is to apply relationships applicable to sinusoidal waves to those of non-sinusoidal waves. In power system, the non-linear loads are mainly power electronics devices. Power electronics devices can be termed as harmonic sources as they are the cause of the origination of harmonics. An accurate measurement of power amidst harmonics resulting from non-linear loads in power system has become more important because of increased significance of harmonics produced from non-linear loads. However voltage and current waveform distortion resulting from harmonic pollution has made the theory of power delivery a serious issue. Hence the need arises for such a measuring system which decomposes the active,

reactive and harmonic power so that the consumers which are generating reactive and harmonic power can be penalized according to the IEEE norms.

1.6 Organization of Thesis

The remaining chapters of the thesis are organized as follows. Chapter 2 discusses the different types of non linear loads. Chapter 3 deals with the measurement of energy. First the conventional concepts are discussed and then new approach for the single phase power measurement is discussed in detail. Chapter 4 deals with the simulation of methodology for separation of real and reactive power in MatLab environment. The development of interfacing circuit for the energy meter is described in chapter 5. Chapter 6 deals with the characteristics and features of the Digital Signal Processor. Chapter 7 presents the implementation of the algorithms for power calculation on the DSP. Results are presented and discussed in the chapter 8. Finally chapter 9 concludes the thesis and includes the future scope of the work.

Chapter 2

Non Linear Loads

2.1 Introduction

Non-Linear loads do not follow ohms law thus if a sinusoidal voltage is applied to a non-linear load, the current waveform would be non-sinusoidal and can be represented by a Fourier series. If voltage v (t) is given by:

$$v(t) = V_m \sin(\omega t + \theta)$$

then current can be represented by the Fourier series :

$$i(t) = I_0 + \sum_{n=1}^{\infty} I_m \sin(n\omega t + \phi)$$

This non-sinusoidal current causes non-sinusoidal voltage drop across the system impedance and in turn the voltage also becomes non-sinusoidal.

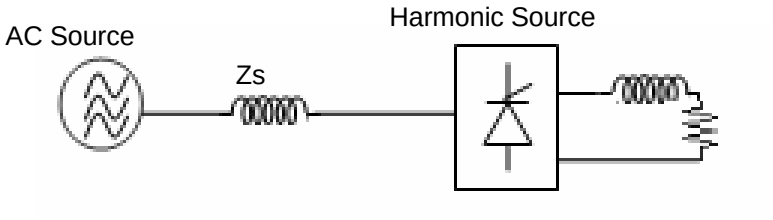
A common mistake made while doing power computations for non-linear loads is to apply relationships applicable to sinusoidal waves to those of non-sinusoidal waves. In power system, the non-linear loads are mainly appear due to power electronics devices. There are no boundaries earmarked for the application of power semiconductor devices, microprocessor and the controlled equipments. Power semi-conductor devices based systems can be termed as harmonic sources as they are the cause of the origination of harmonics (i.e. the voltage or current at frequencies other than fundamental frequency). Broadly speaking these power semi-conductor devices can be divided into two categories:

I. Harmonic Current Sources
II. Harmonic Voltage Sources

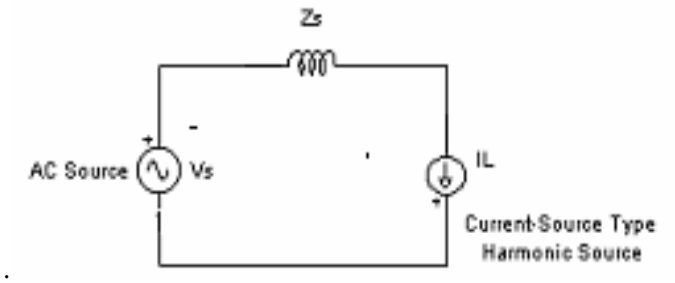
2.2 Harmonic Current Sources

As a well known fact, thyristor converters are a common and typical source of harmonic currents. The distortion of the current waveform, i.e. the generation of harmonics, results from the switching operation. Because the harmonic current contents and

characteristics are less dependent upon the ac side, this type of harmonic source behaves like a current source. Therefore, they are called current source type of harmonic source .A diode rectifier with a sufficient dc choke or interface inductor on ac side can be considered as a current-source type of harmonic source as well. Under ideal conditions, the characteristic harmonics of the current are the 5^{th} (20%), 7th (14%), 11th (9%) and so on.



(a) Thyristor rectifier for dc drives, heater drives, etc.

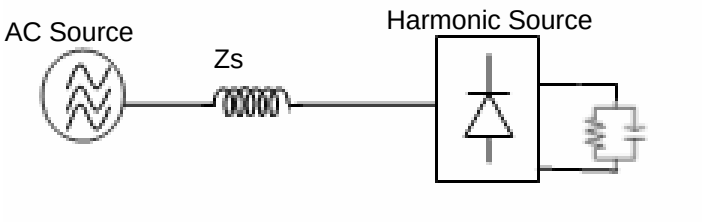


(b) Per-phase equivalent circuit of thyristor rectifier.

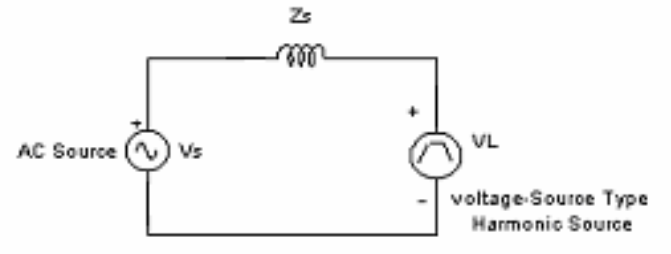
Fig 2.1 Harmonic current source.

2.3 Harmonic Voltage Sources

Nowadays, another type of common harmonic sources is diode rectifiers with smoothing dc capacitors. The load current is highly distorted, its harmonic amplitude is greatly affected by the impedance of the ac side, whereas the rectifier voltage is characteristically determined and less dependent upon the ac impedance. Therefore, the diode rectifiers behave like a voltage source rather than a current source. The harmonic current originates from the rectifier voltage and its content is determined by and dependent upon the rectifier voltage and the ac impedance. Under ideal conditions, the characteristic harmonics of the line to line rectifier voltage are the 5^{th} (20%), 7th (14%), 11th (9%) and so on.



(a) Diode rectifier for ac drives, electronic equipment, etc.



(b) Per-phase equivalent circuit of thyristor rectifier.

Fig 2.2 Harmonic voltage source.

Chapter 3

Measurement of Energy

3.1 Introduction

The active and reactive power for electric circuit with sinusoidal source and linear loads are well established. In the cases of non-linear loads these concepts are not yet sufficiently explained and with the increased use of power electronics circuits, the electric sources had to start supplying power to a large number of these loads. Therefore, nowadays, understanding the reactive and harmonic power is all actual necessity for understanding and accomplishing reactive compensation or harmonic filtering. However, the after the work presented by Akagi et al. a new and concise theory to deal with this problem actually appeared [2]. This theory is well known in Japan as "instantaneous power theory" or "p-q theory" and has been used to develop many types of active power filters.

3.2 Conventional Concepts

For a better understanding of the new concepts, first the conventional concept, which is valid for the steady state, will be presented for single phase system in different circuit conditions.

1. Sinusoidal Voltage Source and Linear Loads

For this study it is assume that the voltage source and the load current are given by

$$v_a(t) = \sqrt{2}\, V \sin wt \quad \text{and} \quad i_a(t) = \sqrt{2}\, I \sin(wt - \phi) \qquad (1)$$

The instantaneous power can be calculated by

$$p_a(t) = v_a \cdot i_a = VI\cos\Phi.(1 - \cos 2wt) - VI\sin\Phi.\sin 2wt \qquad (2)$$

"1" "2"

This decomposition shows that the instantaneous power can be separated in two parts. Part "1" has all average value equal to VI Cos ø and has an alternating component on it, oscillating at twice the line frequency. This part "1" never becomes negative and therefore, is an unidirectional (dc) power.

Part "2" is also an alternating component, oscillating at twice the line frequency has peak value equal to VI Sin ø and zero average value.

The average (active) power is, therefore, given by

$$P = VI \cos ø \quad (3)$$

and the conventional reactive power is just defined as the peak value of part "2" (power component which average value is zero), or

$$Q = VI \sin ø. \quad (4)$$

Now we can re-write (2) as

$$Pa(t) = P(1 - \cos 2\omega t) - Q \sin 2\omega t \quad (5)$$

2. Sinusoidal Voltage Source and Non-linear Load

In this case the voltage source is the same as given in (1), but the current contains harmonics at frequencies multiples of ω, that is

$$i_a(t) = \sum_{n=1}^{\infty} \sqrt{2}\, I_n \sin(nwt - \phi_n) \quad (6)$$

The following relations are known:

- **Instantaneous Power:**

$$p_1(t) = VI_1 \cos \Phi_1.(1 - \cos 2wt) - VI_1 \sin \Phi_1. \sin 2wt$$

$$+ \sum_{n=2}^{\infty} 2VI_n \sin wt. \sin(nwt - \phi_n) \quad (7)$$

- Average active power:

P = average value of $P_a(t) = VI_1 \cos ø_1$

- Current rms value:

$$I = \sqrt{I_1^2 + I_2^2 + I_3^2 + I_4^2 .....} = \sqrt{(1/T)\int_0^T I_a^2 \, dt} \quad (8)$$

where T is the period of $i_a(t)$.

- Apparent Power:

$$S = V.I \quad (9)$$

From (8) and (9) it follows that:

$$S^2 = V^2.I^2 = V^2(I_1^2 + I_2^2 + I_3^2 .....) \quad (10)$$

- Reactive Power:

In this system, with sinusoidal voltage source and non-linear load (having current harmonics at the frequencies multiple of fundamental frequency) reactive power is conventionally defined as

$$Q = VI_1 \sin \phi_1 \quad (11)$$

and the harmonic power as

$$H \triangleq V\sqrt{I_2^2 + I_3^2 + ...} \quad (12)$$

Now, (10) can be re-written as

$$S^2 = P^2 + Q^2 + H^2 \quad (13)$$

- Power Factor:

Effective Power factor or total power factor = $\cos \phi_1 . \cos y$

Where, $\cos \phi_1$ = Displacement factor or fundamental power factor

$\cos y = P/S = I_1/I$, is called distortion factor

The displacement factor corresponds to the power factor of systems without harmonics. This factor may be called fundamental power factor, as it depends only on the current fundamental component. On the other hand, the power factor, as defined above, may be called total power factor, as it depends on fundamental and all harmonic components.

3.3 New Concepts of Active and Reactive Power

In the previous section, the power components of an electric circuit have been arranged in a tetrahedron. The reactive and harmonic power compensation has been discussed, but the theory considered basically the steady-state behavior. As the load may change continuously and the harmonic contents too, a theory for transient conditions is necessary. Akagi et al have proposed new concepts of instantaneous active and reactive power that can be used in transient states and when the voltage and/or current have generic waveforms. This theory has some interesting but difficult aspects that need to be clarified. In the following, this theory, valid for three-phase 4-wires system, wilt be summarized and the meaning of each term explained.

3.4 The Generalized Theory of Instantaneous Power (p-q theory)

This theory has been given for three phase system to calculate the harmonic current for the active filtering. According to this theory three phase voltage may be transferred into a α- β-0 frame as given:

$$\begin{bmatrix} v_0 \\ v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{2/3} \begin{bmatrix} 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \\ 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & \sqrt{3}/2 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{14}$$

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \sqrt{2/3} \begin{bmatrix} 1/\sqrt{2} & 1 & 0 \\ 1/\sqrt{2} & -1/2 & -1/2 \\ 1/\sqrt{2} & -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} v_0 \\ v_\alpha \\ v_\beta \end{bmatrix} \tag{15}$$

Where V_a, V_b, V_c are phase voltages. Identical relations hold for line currents i_a, i_b and i_c.

Instantaneous three phase active power (p) and reactive power (q) has given accordingly as

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} \bar{p} \\ \bar{q} \end{bmatrix} + \begin{bmatrix} \tilde{p} \\ \tilde{q} \end{bmatrix} \tag{16}$$

p and q are active and reactive power due to fundamental component only, and $\tilde{p}$ and $\tilde{q}$ are the power terms corresponding to harmonic components.

3.5 Extension of p-q theory for single phase system

This approach is based on extending instantaneous reactive power theory for single-phase circuit .The equivalent two phase voltage and current in stationary α-β frame are created by lagging the values of voltage and current each by 90^0 from its single phase values [6]. Now in alpha beta system the values may be treated similar to three phase system for computation of power. This two phase system can directly be used to calculate the instantaneous active and reactive power. As reported the theory is applicable only when voltage source is pure sinusoid.

Assuming the existing single-phase values of voltage and current

$$\begin{aligned} v &= \sqrt{2}V \sin \omega t \\ i &= \sum_{n=1,3,5\ldots}^{\infty} \sqrt{2} I_n \sin(n\omega t - \phi_n) \end{aligned} \tag{17}$$

In α-β coordinates consider v and i as voltage and current in phase α respectively. The values in phase β are computed by respectively lagging v and i by 90^0, and constructing an α-β system as follows

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} v(\omega t) \\ v(\omega t - 90^0) \end{bmatrix} = \begin{bmatrix} \sqrt{2}V \sin \omega t \\ -\sqrt{2}V \cos \omega t \end{bmatrix} \tag{18}$$

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} i(\omega t) \\ i(\omega t - 90^0) \end{bmatrix} = \begin{bmatrix} \sum_{n=1,3,5...}^{\infty} \sqrt{2} I_n \sin(n\omega t - \phi_n) \\ \sum_{n=1,3,5...}^{\infty} \sqrt{2} I_n \sin\left(n(\omega t - 90^0) - \phi_n\right) \end{bmatrix} \quad (19)$$

The instantaneous active and reactive power can then be obtained as

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} \bar{p} \\ \bar{q} \end{bmatrix} + \begin{bmatrix} \tilde{p} \\ \tilde{q} \end{bmatrix} \quad (20)$$

Where average components ($\bar{p}$ & $\bar{q}$) of p and q and correspond to the fundamental frequency and the oscillatory parts ($\tilde{p}$ & $\tilde{q}$) correspond to harmonic frequencies.

$$\begin{bmatrix} \bar{p} \\ \bar{q} \end{bmatrix} = \begin{bmatrix} 2VI_1 \cos\phi_1 \\ 2VI_1 \sin\phi_1 \end{bmatrix} \quad (21)$$

As it is clear from the above equation the average part of p and q are equal to twice of the actual estimate of real and reactive power respectively. Therefore real and reactive power can be given by

$$P = \bar{p}/2$$
$$Q = \bar{q}/2 \quad (22)$$

The fundamental component real and reactive current may be obtained by reverse transform of equation (20)

$$\begin{bmatrix} i_{\alpha f} \\ i_{\beta f} \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix}^{-1} \begin{bmatrix} \bar{p} \\ \bar{q} \end{bmatrix} \quad (23)$$

I_1= Fundamental component of current = $\sqrt{i_{\alpha f}^2 + i_{\beta f}^2}$ (24)

Apparent power is given by

$$S = V \times I = \sqrt{P^2 + Q^2 + D^2} \quad (25)$$

Where as D is distortion power, produced due to interaction of currents and voltages of different frequencies and is defined as

$$D = V \times \sqrt{\sum_{n\neq 1}^{\infty} I_n^2} \tag{26}$$

thus distortion power can be computed as

$$D = \sqrt{S^2 - (\overline{p} / 2)^2 - (\overline{q} / 2)^2} \tag{27}$$

The distortion power is used as a measure of losses due to harmonics. As per IEEE519 & IEC61000-2-2 standards, harmonic content is gauged in terms of THD which can be defined in terms of fundamental voltage, fundamental current and distortion power as,

$$THD = \frac{D}{V \times I_1} \tag{28}$$

From above, energy consumed may be computed under heads real energy, reactive energy and losses due to harmonics.

Chapter 4

Simulation of the Measurement System

4.1 Simulink model elements

The method for the separation of Real and Reactive power as described in chapter 3 can be easily simulated using Matlab. Various circuit components used in simulink model are as follows

Sinusoidal Voltage Source

It represents a practical voltage source of 100V, 50 Hz

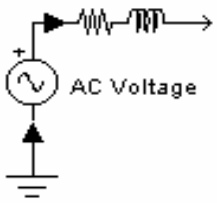


Figure 3.1 Practical Voltage Source

Loads connected to the Generator

It is a parallel RC circuit connected through universal bridge drawing non-sinusoidal current from the source. It creates harmonics on the source side. It can also create harmonics in the current drawn by linear load if attached on the same bus, which will in turn affects the stability of the power system.

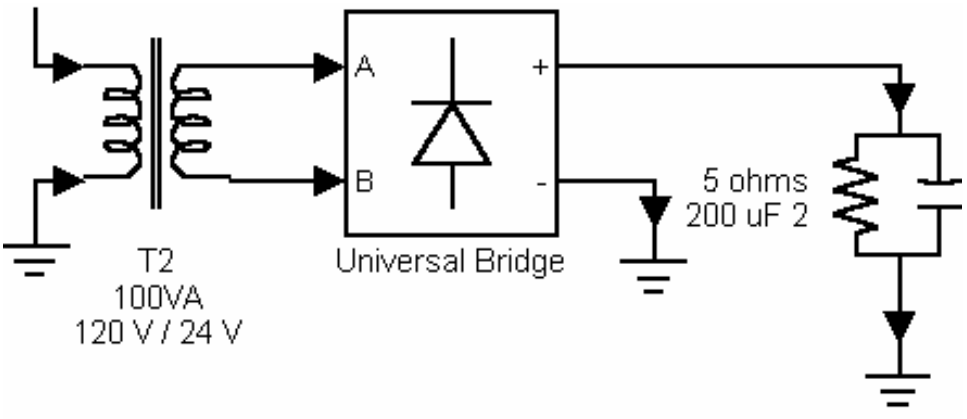


Figure 3.2 Non-Linear Load

Active/Reactive Power Calculation block

The voltage and current samples are first converted to α-β frame using transport delay block (quarter cycle i.e. 5 ms). The real and reactive powers are calculated as per the instantaneous reactive power theory mentioned in Chapter 3. This power contains DC and oscillatory components; from this DC component is separated using Low Pass filter (LPF).

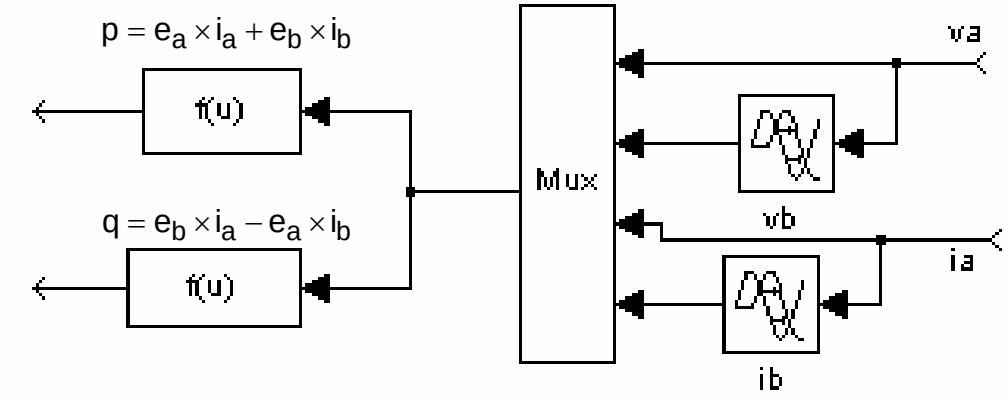


Figure 3.3 Active & Reactive Power Calculation block

Moving Averager (Low Pass Filter) Block

The sampled waveform is lagged by one cycle and the samples of the latter having same phase displacement as that of former are subtracted from the former and the result is integrated to obtain the DC component.

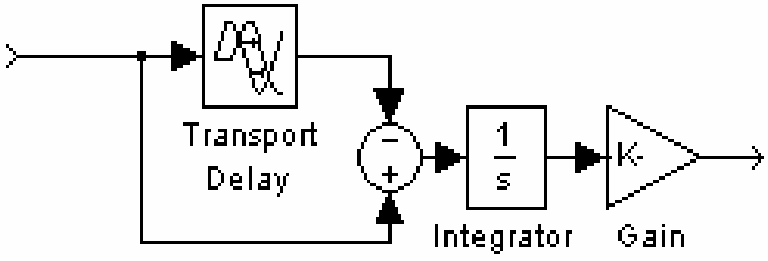


Figure 3.4 Low Pass Filter

4.2 Complete Simulink model

The complete simulink model is shown below. The model given below is simulated for two types of load. In first case, the Loads are as per explained earlier. In second case, a triac is connected which feeds a R-L load. The voltage and current samples are first converted to α-β frame using transport delay block (quarter cycle i.e. 5 ms). The real and reactive instantaneous powers are computed as per equation (4). This power contains an average and oscillatory component. Average components are separated by using moving averager low pass filter. After dividing by 2 the term obtained are real and reactive powers. Distortion power and THD are calculated using equation (9) and equation (10), depicted by block Distortion Power and THD.

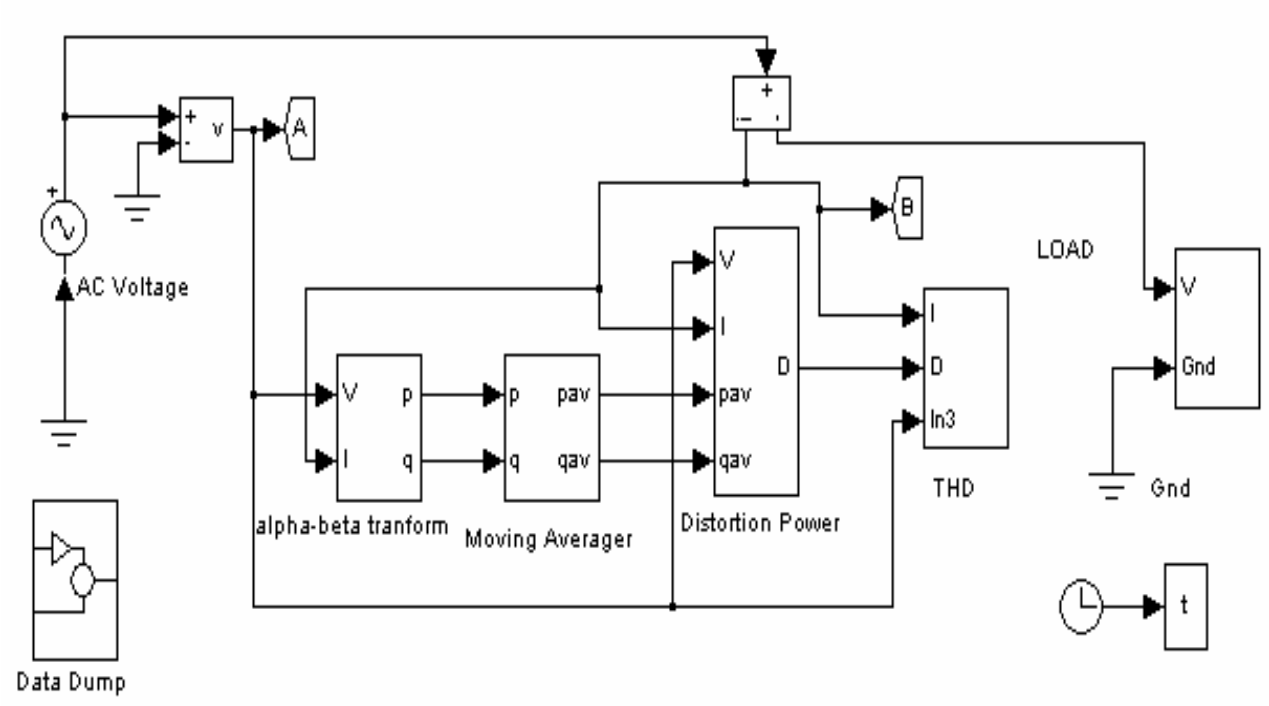


Figure 3.5 Block diagram of the MATLAB model

4.3 Simulation Results

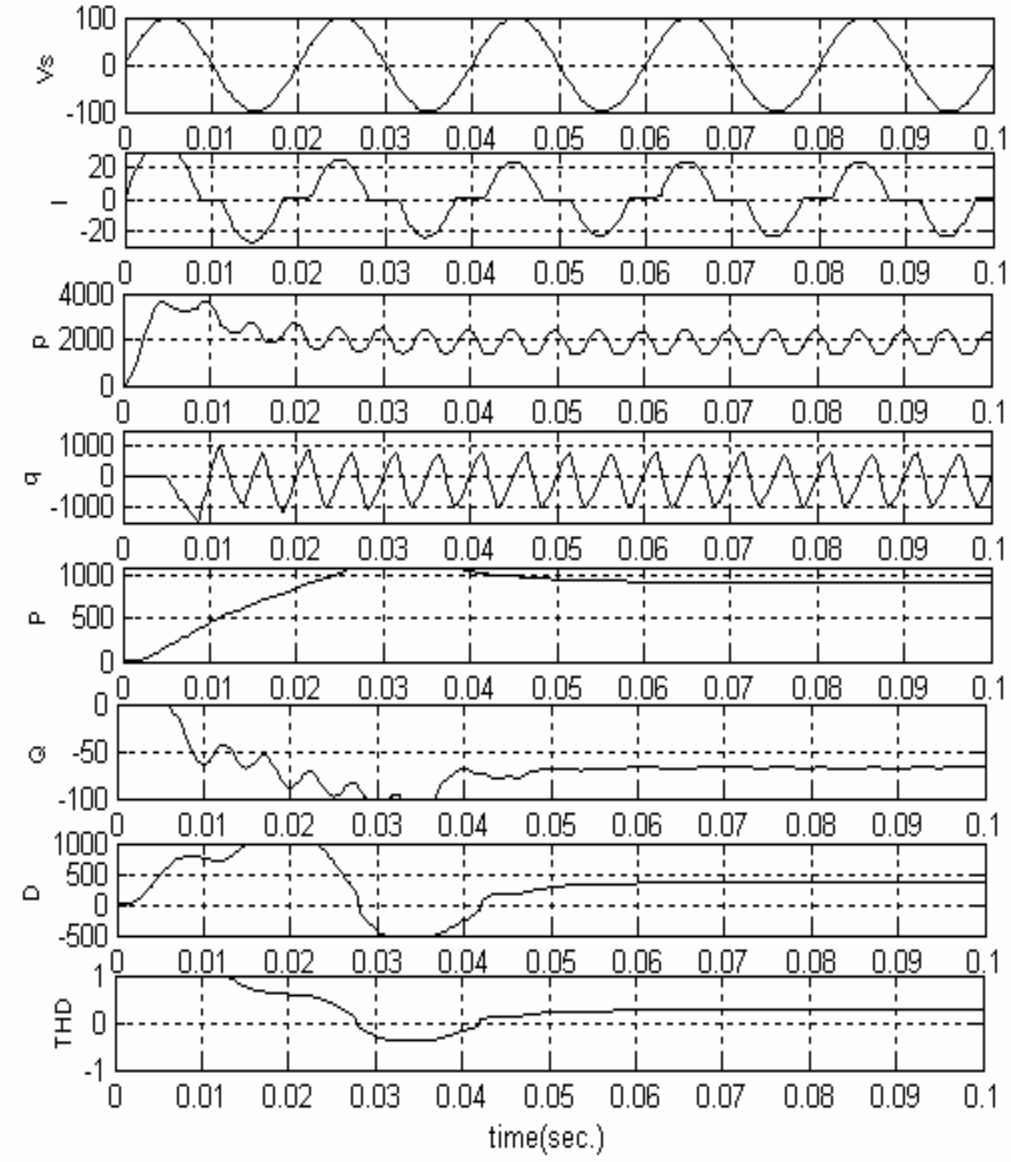


Figure 3.6 Dynamic response of the measuring system to demonstrate decomposition of power into different parts for diode rectifier fed load

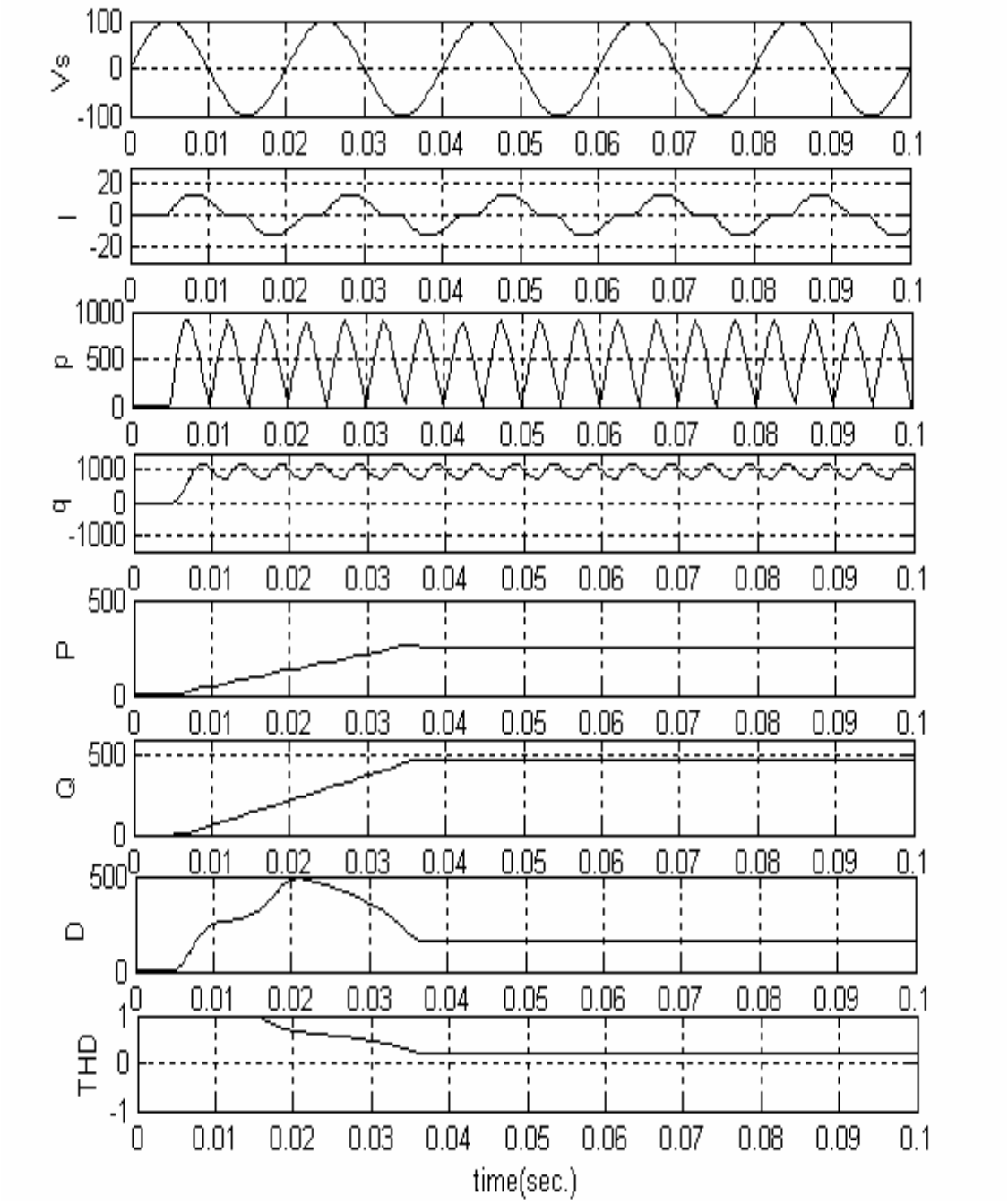


Figure 3.7 Dynamic response of the measuring system to demonstrate decomposition of power into different parts for triac fed AC load

4.4 Discussion of Simulation Results

Figure 3.6 shows the estimation of power components, when load comprises of a resistive load connected across a diode rectifier. Current is peaky due to filter capacitor. Figure 3.7 shows ripple in estimation of p and q depicting presence of distortion power . For the load of value R=5 Ω and rms current of 14 amp, the distortion power is 400 volt-amp. As the fundamental component of current is almost in phase with voltage, the reactive power is negligible as compared to real power. THD in source current is 25 %. Energy dissipated is equal to 91.8 watt-secs.

Figure 3.7 reflects the estimation of power with a load connected across thyristor converter when triacs are fired at 90^0. This kind of load clearly indicates presence of increased reactive power which is 475 var. obtained under such case with load of R=2 and L=10 mh. The rms value of current is 8 amp and its fundamental component is displaced by 61.7^0 to the voltage. Due to distortion in current, distortion power is there and equal to 160 volt-amp. THD is equal to 20% and energy estimated is equal to 25.4 watt-sec.

Chapter 5

Development of Interfacing Hardware

5.1 Introduction

The instantaneous values of voltages and currents are sampled for different consumers using current and voltage transducers (Potential Transformers and Hall Effect Transducers). The output of voltage sensor is first passed through a filtering circuit and then feed to the ADC. This filtering circuit is necessary to remove the fluctuations in the supply voltage. The consumer should not be punished for supply voltage fluctuations as these fluctuations are there because of our faulty distribution system. The output of current channels is first passed through a buffer and then feed to ADC. The block diagram of the system is given below:

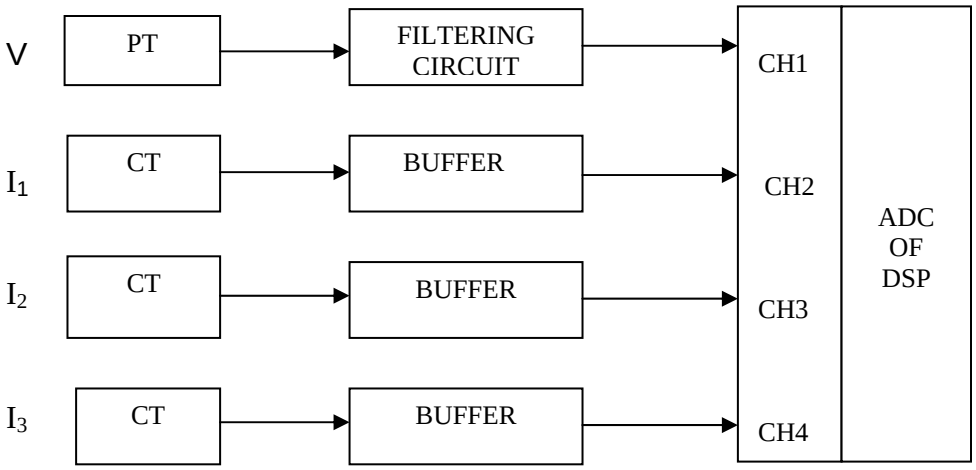


Figure 5.1 Block Diagram of Interfacing Hardware

5.2 Voltage Sensor

The speciality of the voltage sensor is that only electronic components are used in this. It allows the measurement of direct or alternating voltages with electrical insulation between primary and secondary circuits. The primary voltage is to be measured is directly applied to the sensors terminals: +HT (positive high voltage) –HT (negative high voltage). This voltage is passed through an insulating amplifier and is then converted to a secondary output current Is. This secondary current is electrically isolated from the primary voltage to which it is exactly proportional. This secondary current can be then passed through a measuring resistor Rm. The voltage at the terminals of measuring resistance Rm is therefore also exactly proportional to the primary voltage.

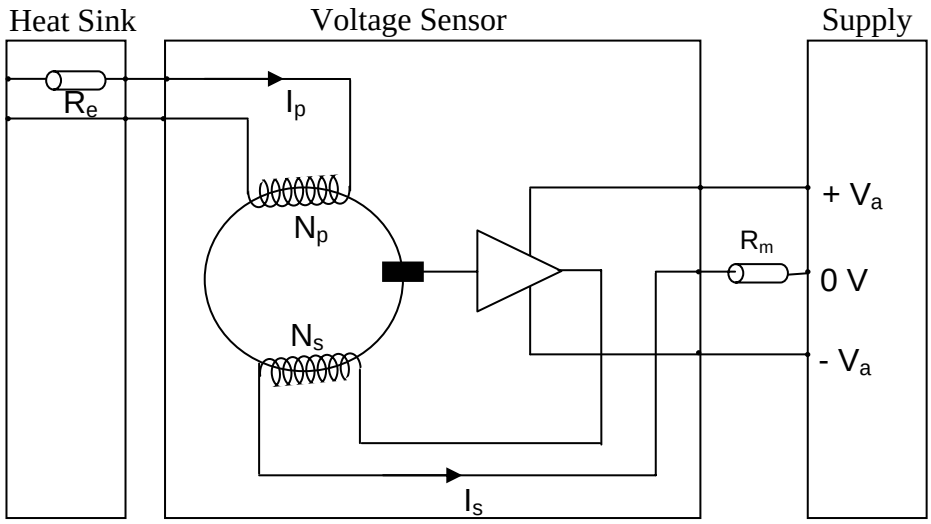


Figure 5.2 Voltage sensor

Advantages

- Electrical insulation between primary and secondary circuits.
- Measurement of all waveforms is possible: direct voltage, alternating voltage, impulse etc.
- Excellent immunity to electromagnetic fields.
- Excellent accuracy.
- High dynamic performance.
- Excellent reliability.

5.3 Hall Effect Transducer

Hall Effect current transducer is used to measure the current in a circuit. Hall effect is a phenomenon in which magnetic field applied perpendicularly to a conductor carrying electric current generates voltage across the edges of the conductor. Edwin H. Hall first discovered the effect in 1879. Hall effect devices are used as sensors in robotics, automobiles, telecommunications equipment, and DC motors. This report describes the

operating principles of a Hall effect transducer and addresses the questions of their applications and performance.

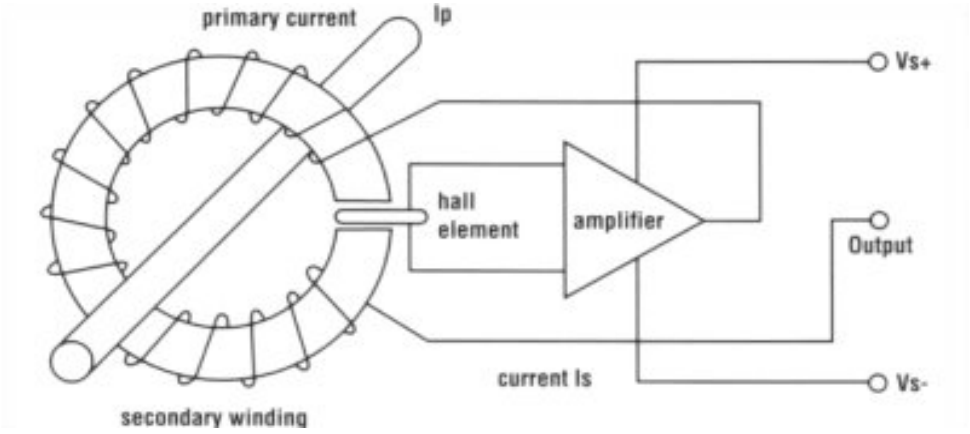


Figure 5.3 Hall Effect Sensor

The Hall Effect current transducer is designed in such a way as to measure circuit current without being physically connected to the circuit. The advantage of this is that the measurements can be made more accurately since the transducer does not affect the circuit current in any way.

Closed loop Hall Effect Current Transformers use the ampere-turn compensation method to enable measurement of current from DC to high frequency with the ability to follow rapidly changing level or wave shapes. The application of a primary current (Ip) causes a change of flux in the air gap. This in turn produces a change in output from the Hall element away from the steady state condition. This output is amplified to produce a current (Is) which is passed through the secondary winding, causing a magnetizing force to oppose that of the primary current, thereby reducing the air gap flux. The secondary current will increase until the flux is reduced to zero. At this point the Hall element output will have returned to the steady state condition and the ampere turn product of the secondary circuit will match that of the primary.

The current that passes through the secondary winding is the output current. The transformation ratio is calculated by the standard current transformer equation.

NpIp = NsIs

Np = primary turns,

Ns = secondary turns,

Ip = primary current,

Is = secondary current

Features

- High Accuracy
- Galvanic isolation between primary and secondary
- Covers AC, DC, and impulse current measurements
- Designed for ease of installation
- Wide dynamic range
- Non invasive (except NP style)

5.4 Buffer

The buffer is used to limit the current drawn from the input or to increase the fanout of the transducer. It is implemented using TL084 IC. The circuit diagram for buffer is as under:

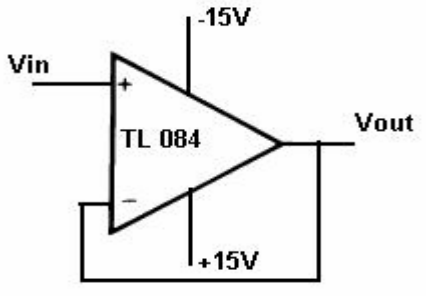


Figure 5.4 Internal configuration of buffer TL084

The TL084 JFET-input operational amplifier is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and

offset currents, and low offset voltage temperature coefficient. Offset adjustment and external compensation options are available within the TL08x family.

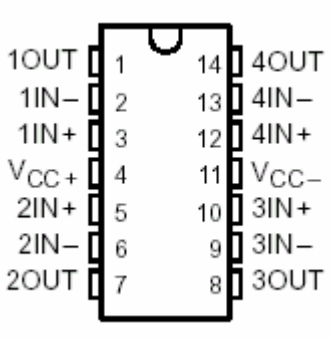


Figure 5.5 Pin Configuration of TL084

5.5 Band Pass Filter

The supply voltage to the consumer may not be pure sinusoid. In this case consumer is not solely responsible for the distortion power. So in this energy metering system band pass filter is used to filter out the harmonics and feed only sinusoidal voltage to the consumer. Operational amplifier OP 07 is used for the development of band pass filter. The pin diagram of the OP 07 is given below:

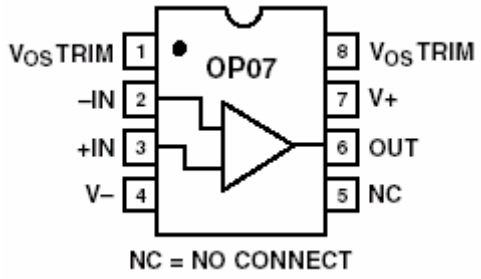


Figure 5.6 Pin Diagram of OP 07

The OP07 has very low input offset voltage (75 µV max for OP07E) which is obtained by trimming at the wafer stage. These low offset voltages generally eliminate any need for external nulling. The OP07 also features low input bias current (±4 nA for OP07E) and high open-loop gain (200 V/mV for OP07E). The low offsets and high open-loop gain make the OP07 particularly useful for high gain instrumentation applications. The wide input

voltage range of ±13 V minimum combined with high CMRR of 106 dB (OP07E) and high input impedance provides high accuracy in the noninverting circuit configuration. Excellent linearity and gain accuracy can be maintained even at high closed-loop gains. Stability of offsets and gain with time or variations in temperature is excellent. The accuracy and stability of the OP07, even at high gain, combined with the freedom from external nulling have made the OP07 an industry standard for instrumentation applications. Hence it is most suitable for such applications.

The band pass filter used in the system to filter unwanted harmonics or distortion in voltage waveform is implemented using operational amplifier OP07. The circuit diagram of the filter is shown below:

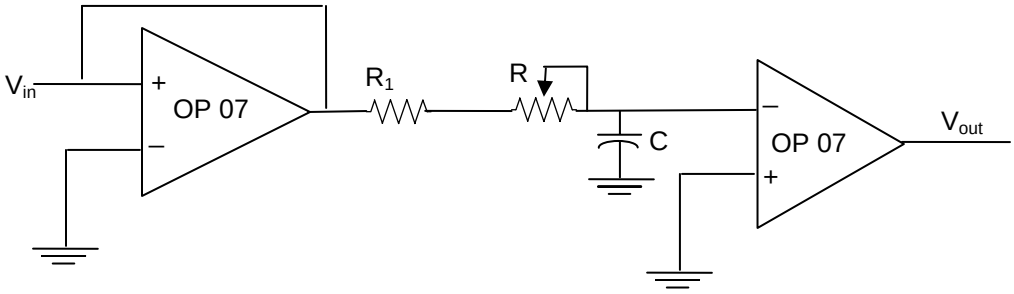


Figure 5.7 Band Pass Filter

RC coupling is used to insert delay in the system. To set the delay a variable resistance is used in the RC circuit. The value of resistance and capacitance is selected so that the delay caused is 180 degree. Thus the waveform now is in phase opposition with the original one. So the final output is taken from the negative terminal, therefore making the waveform again in phase with the original one. There are two significant reasons to include the delay in the system:

1. If the consumer is a not generating harmonics and the voltage waveform consists of the harmonics then there will be a significant amount of distortion power for the consumer, and he will be penalized without any fault. Therefore our waveform must be free from harmonics so that only faulty consumers (which are generating harmonics in the current waveforms) are penalized.
2. The p-q theory which we have used for calculation of power (as described in chapter 3) is only valid if the voltage waveform is purely sinusoidal. So again the need arises for a filtering circuit for voltage waveform.

Chapter 6

Digital Signal Processor

6.1 Introduction

A digital signal processor (DSP) is a type of microprocessor - one that is incredibly fast and powerful. A DSP is unique because it processes data in real time. This real-time capability makes a DSP perfect for applications that cannot tolerate any delays [20]. For example, did you ever talk on a cell phone where two people couldn't talk at once? You had to wait until the other person finished talking. If you both spoke simultaneously, the signal was cut--you didn't hear the other person. With today's digital cell phones, which use DSP, you can talk normally. The DSP processors inside cell phones process sounds so rapidly you hear them as quickly as you can speak - in real time. Here are just some of the advantages of designing with DSPs over other microprocessors:

- Single-cycle multiply-accumulate operations
- Real-time performance, simulation and emulation
- Flexibility
- Reliability
- Increased system performance
- Reduced system cost

Like a general-purpose microprocessor, a DSP is a *programmable* device, with its own native instruction code. DSP chips are capable of carrying out millions of floating point operations per second, and like their better-known general-purpose cousins, faster and more powerful versions are continually being introduced.

A Little History

DSPs began to appear roughly around 70s, with the Bell Labs DSP1 and NEC7720 being the first to qualify. The Bell Labs DSP1 was never marketed outside AT&T. All of these DSPs had internal memory, permitting stand-alone system implementations. A signal processor available before 1979 is the Intel 2920, which included A/D and D/A capability on

chip, but lacked a hardware multiplier. A number of microcontrollers are also excluded of the same reason.

In 1982, Texas Instruments introduced the TMS32010, the first member of what was to become the most popular DSP family. Its popularity was due in no small part to TI's emphasis on development of software and hardware. At about the same time, Hitachi introduced the first CMOS DSP, the HD61810(HSP). It was also the first DSP to use a floating point format (a 12 bit mantissa and 4 bit exponent). One year later, Fujitsu greatly increased the speed of commercially available programmable DSPs with the MB8764 which has 120 nsec multiply and accumulate time. In 1984, the Bell Labs DSP32 appeared on the market. It was first in two important respects: the first DSP that AT&T would market, and the first 32-bit floating point DSP.

6.2 TMS320C54x DSP Overview

The C54x DSP has a high degree of operational flexibility and speed. It combines an advanced modified Harvard architecture (with one program memory bus, three data memory buses, and four address buses), a CPU with application-specific hardware logic, on-chip memory, on-chip peripherals, and a highly specialized instruction set. Spin off devices that combine the C54x CPU with customized on-chip memory and peripheral conFigureurations have been, and continue to be, developed for specialized areas of the electronics market.

The C54x devices offer these advantages:

- Enhanced Harvard architecture built around one program bus, three data buses, and four address buses for increased performance and versatility
- Advanced CPU design with a high degree of parallelism and application specific hardware logic for increased performance
- A highly specialized instruction set for faster algorithms and for optimized high level language operation
- Modular architecture design for fast development of spin off devices
- Advanced IC processing technology for increased performance and low power consumption

- Low power consumption and increased radiation hardness because of new static design techniques

TMS320C54x DSP Key Features

Following are the key features of the C54x DSPs.

- Central Processing Unit (CPU)
- Advanced multi bus architecture with one program bus, three data buses, and four address buses
- 40-bit arithmetic logic unit (ALU), including a 40-bit barrel shifter and two independent 40-bit accumulators
- 17-bit × 17-bit parallel multiplier coupled to a 40-bit dedicated adder for non pipelined single-cycle multiply/accumulate (MAC) operation
- Compare, select, store unit (CSSU) for the add/compare selection of the Viterbi operator
- Exponent encoder to compute the exponent of a 40-bit accumulator value in a single cycle
- Two address generators, including eight auxiliary registers and two auxiliary register arithmetic units
- Multiple-CPU/core architecture on some devices
- Memory
    - 192K words × 16-bit addressable memory space (64K-words program, 64K-words data, and 64K-words I/O), with extended program memory in the C548, C549, C5402, C5410, and C5420.
- Instruction set
    - Single-instruction repeat and block repeat operations
    - Block memory move instructions for better program and data management
    - Instructions with a 32-bit long operand
    - Instructions with 2- or 3-operand simultaneous reads
    - Arithmetic instructions with parallel store and parallel load
    - Conditional-store instructions

- Fast return from interrupt
- On-chip peripherals
- Software-programmable wait-state generator
- Programmable bank-switching logic
- On-chip phase-locked loop (PLL) clock generator with internal oscillator or external clock source.

6.3 Architectural Overview

TMS320C54xE DSP comprises the central processing unit (CPU), memory, and on-chip peripherals. The C54xE DSPs use an advanced modified Harvard architecture that maximizes processing power with eight buses. Separate program and data spaces allow simultaneous access to program instructions and data, providing a high degree of parallelism. For example, three reads and one write can be performed in a single cycle. Instructions with parallel store and application-specific instructions fully utilize this architecture. In addition, data can be transferred between data and program spaces. Such parallelism supports a powerful set of arithmetic, logic, and bit-manipulation operations that can all be performed in a single machine cycle. Also, the C54x DSP includes the control mechanisms to manage interrupts, repeated operations, and function calling. Figure 2-1 shows a functional block diagram of the C54x DSP, which includes the principal blocks and bus structure.

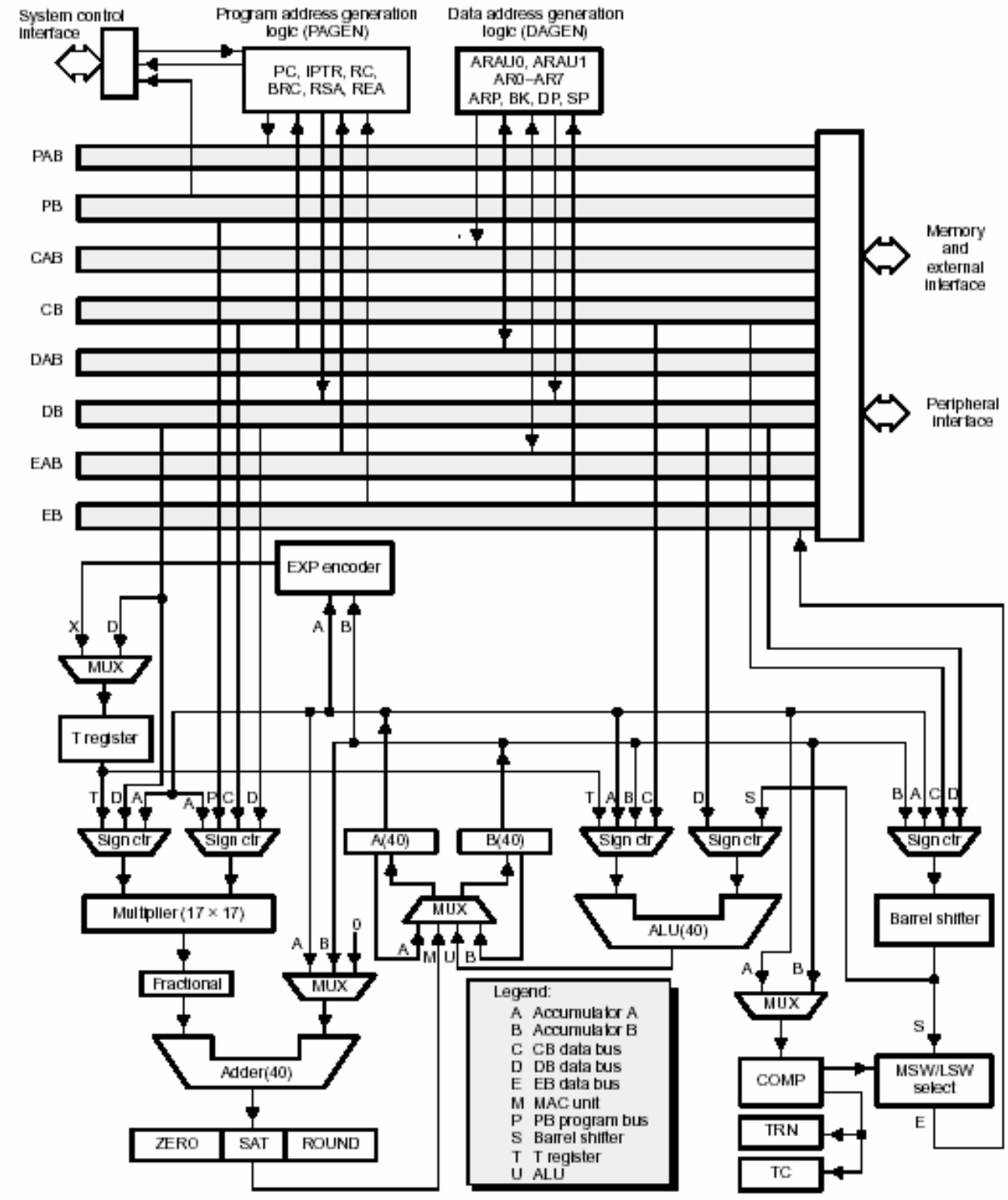


Figure 6.1 Block Diagram of TMS320C54x DSP Internal Hardware

Bus Structure

The C54xE DSP architecture is built around eight major 16-bit buses (four program/data buses and four address buses):

- The program bus (PB) carries the instruction code and immediate operands from program memory.
- Three data buses (CB, DB, and EB) interconnect to various elements, such as the CPU, data address generation logic, program address generation logic, on-chip peripherals, and data memory.
- The CB and DB carry the operands that are read from data memory.
- The EB carries the data to be written to memory.
- Four address buses (PAB, CAB, DAB, and EAB) carry the addresses needed for instruction execution.

The C54x DSP can generate up to two data-memory addresses per cycle using the two auxiliary register arithmetic units (ARAU0 and ARAU1).The PB can carry data operands stored in program space (for instance, a coefficient table) to the multiplier and adder for multiply/accumulate operations or to a destination in data space for data move instructions (MVPD and READA). This capability, in conjunction with the feature of dual-operand read, supports the execution of single-cycle, 3-operand instructions such as the FIRS instruction. The C54x DSP also has an on-chip bidirectional bus for accessing on-chip peripherals. This bus is connected to DB and EB through the bus exchanger in the CPU interface. Accesses that use this bus can require two or more cycles for reads and writes, depending on the peripheral's structure.

6.4 Internal Memory Organization

The C54xE DSP memory is organized into three individually selectable spaces: program, data, and I/O space. The C54x devices can contain random access memory (RAM) and read-only memory (ROM). Among the devices, the following types of RAM are represented: dual-access RAM (DARAM), single-access RAM (SARAM), and two-way shared RAM. The DARAM or SARAM can be shared within subsystems of a multiple-CPU

core device. You can configure the DARAM and SARAM as data memory or program/data memory. The C54x DSP also has 26 CPU registers plus peripheral registers that are mapped in data-memory space.

On-Chip ROM

The on-chip ROM is part of the program memory space and, in some cases, part of the data memory space. On most devices, the ROM contains a bootloader that is useful for booting to faster on-chip or external RAM. On devices with large amounts of ROM, a portion of the ROM may be mapped into both data and program space. The larger ROMs are also custom ROMs: you provide the code or data to be programmed into the ROM in object file format, and Texas Instruments generates the appropriate process mask to program the ROM.

On-Chip Dual-Access RAM (DARAM)

The amount of on-chip DARAM available on each device varies. The DARAM is composed of several blocks. Because each DARAM block can be accessed twice per machine cycle, the CPU and peripherals, such as a buffered serial port (BSP) and host-port interface (HPI), can read from and write to a DARAM memory address in the same cycle. The DARAM is always mapped in data space and is primarily intended to store data values. It can also be mapped into program space and used to store program code.

On-Chip Single-Access RAM (SARAM)

The amount of on-chip SARAM available on each device varies. The SARAM is composed of several blocks. Each block is accessible once per machine cycle for either a read or a write. The SARAM is always mapped in data space and is primarily intended to store data values. It can also be mapped into program space and used to store program code.

On-Chip Two-Way Shared RAM

The amount of on-chip two-way shared RAM available on certain devices varies. The devices with multiple CPU cores include two-way shared RAM blocks that allow simultaneous program space access from two CPU cores. Each CPU can perform a single access with zero-states to any location in the two-way shared RAM during each clock cycle. All the shared memory is program write-protected or read only by the CPU, only the DMA controller can write to the shared memory. This shared RAM is most efficiently used when the two CPUs are executing identical programs. In this case, the amount of program memory required for the application is effectively reduced by 50% since both CPUs can execute from the same RAM.

Memory-Mapped Registers

The data memory space contains memory-mapped registers for the CPU and the on-chip peripherals. These registers are located on data page 0, simplifying access to them. The memory-mapped access provides a convenient way to save and restore the registers for context switches and to transfer information between the accumulators and the other registers.

6.5 Central Processing Unit (CPU)

The CPU is common to all C54xE devices. The C54x CPU contains:

- 40-bit arithmetic logic unit (ALU)
- Two 40-bit accumulators
- Barrel shifter
- 17 × 17-bit multiplier
- 40-bit adder
- Compare, select, and store unit (CSSU)
- Data address generation unit
- Program address generation unit

Arithmetic Logic Unit (ALU)

The C54x DSP performs 2s-complement arithmetic with a 40-bit arithmetic logic unit (ALU) and two 40-bit accumulators (accumulators A and B). The ALU can also perform Boolean operations. The ALU uses these inputs:

- 16-bit immediate value
- 16-bit word from data memory
- 16-bit value in the temporary register, T
- Two 16-bit words from data memory
- 32-bit word from data memory
- 40-bit word from either accumulator

The ALU can also function as two 16-bit ALUs and perform two 16-bit operations simultaneously.

Accumulators

Accumulators A and B store the output from the ALU or the multiplier/adder block. They can also provide a second input to the ALU. Accumulator A can be an input to the multiplier/adder. Each accumulator is divided into three parts:

- Guard bits (bits 39–32)
- High-order word (bits 31–16)
- Low-order word (bits 15–0)

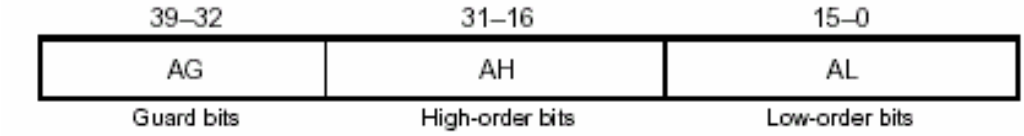


Figure 6.2 Accumulator A

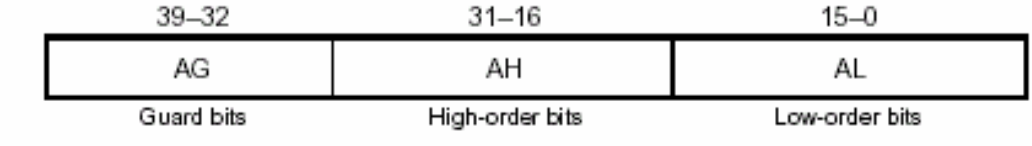


Figure 6.3 Accumulator B bits

The guard bits are used as a head margin for computations. Head margins allow you to prevent some overflow in iterative computations such as autocorrelation. AG, BG, AH, BH, AL, and BL are memory-mapped registers that can be pushed onto and popped from the stack for context saves and restores by using PSHM and POPM instructions. These registers can also be used by other instructions that use memory-mapped registers (MMR) for page 0 addressing. The only difference between accumulators A and B is that bits 32–16 of A can be used as an input to the multiplier in the multiplier/adder unit.

Storing Accumulator Contents

Accumulator contents can be stored in data memory by using the STH, STL, STLM, and SACCD instructions or by using parallel-store instructions. To store the 16 MSBs of the accumulator in memory with a shift, use the STH, SACCD, and parallel-store instructions. For right-shift operations, bits from AG and BG shift into AH and BH. For left-shift operations, bits from AL and BL shift into AH and BH, respectively. To store the 16 LSBs of the accumulator in memory with a shift, use the STL instruction. For right-shift operations, bits from AH and BH shift into AL and BL, respectively, and the LSBs are lost. For left-shift operations, the bits in AL and BL are filled with zeros. Since shift operations are performed in the shifter, the contents of the accumulator remain unchanged.

Multiplier/Adder Unit

The multiplier/adder unit performs 17*17 bit 2s-complement multiplication with a 40-bit addition in a single instruction cycle. The multiplier/adder block consists of several elements: a multiplier, an adder, signed/unsigned input control logic, fractional control logic, a zero detector, a rounder (2s complement), overflow/saturation logic, and a 16-bit temporary storage register (T). The multiplier has two inputs: one input is selected from T, a data-memory operand, or accumulator A; the other is selected from program memory, data memory, accumulator A, or an immediate value. The fast, on-chip multiplier allows the C54x DSP to perform operations efficiently such as convolution, correlation, and filtering. In addition, the multiplier and ALU together execute multiply/accumulate (MAC) computations and ALU operations in parallel in a single instruction cycle.

6.6 CPU Memory-Mapped Registers

A brief summary of one or more of the CPU memory-mapped registers is given in the following section:

Interrupt Mask Registers (IMR)

The interrupt mask register (IMR) individually masks off specific interrupts at required times. If INTM = 0 in ST1, a 1 in any IMR bit enables the corresponding interrupt. Neither NMI nor RS is included in the IMR, because IMR has no effect on these interrupts. You can read or write to the IMR.

Interrupt Flag Register (IFR)

IFR is a memory-mapped CPU register that identifies and clears active interrupts. An interrupt sets its corresponding interrupt flag in IFR until it is recognized by the CPU. Any of the following four events clear an interrupt flag:

- The C54x DSP is reset (RS is low).
- An interrupt trap is taken.
- A 1 is written to the appropriate bit in IFR.
- The INTR instruction is executed using the appropriate interrupt number.

Status Registers (ST0, ST1)

The status registers ST0 and ST1 contain the status of the various conditions and modes for the C54x devices. ST0 contains the flags (OVA, OVB, C, and TC) produced by arithmetic operations and bit manipulations, in addition to the DP and the ARP fields. ST1 reflects the status of modes and instructions executed by the processor.

The individual bits of the ST0 and ST1 registers can be set or cleared with the SSBX and RSBX instructions. For example, the sign-extension mode is set with SSBX 1, SXM, or reset with RSBX 1, SXM. The ARP, DP, and ASM bit fields can be loaded using the LD instruction with a short-immediate operand. The ASM and DP fields can be also loaded with data-memory values by using the LD instruction.

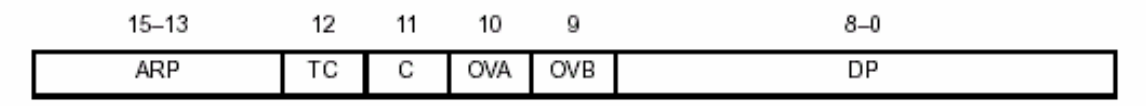


Figure 6.4 Status Register 0 (ST0) Diagram

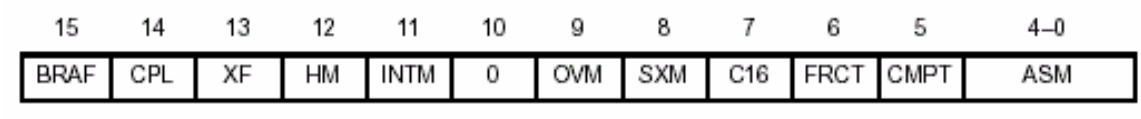


Figure 6.5 Status Register 1 (ST1) Diagram

Processor Mode Status Register (PMST)

The processor mode status register (PMST) controls memory configurations of the C54x devices The PMST register is loaded with memory-mapped register instructions such as STM.

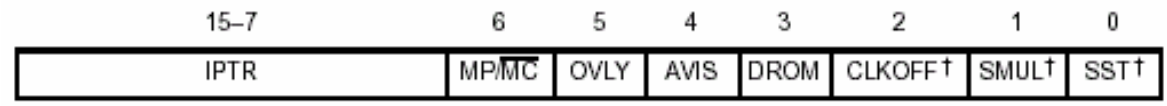


Figure 6.6 Processor Mode Status Register (PMST) Diagram

Temporary Register (T)

The temporary (T) register has many uses. For example, it may hold:

- One of the multiplicands for multiply and multiply/accumulate instructions
- A dynamic (execution-time programmable) shift count for instructions with
- shift operation such as the ADD, LD, and SUB instructions
- A dynamic bit address for the BITT instruction
- Branch metrics used by the DADST and DSADT instructions for ACS

Transition Register (TRN)

The 16-bit transition (TRN) register holds the transition decision for the path to new metrics to perform the Viterbi algorithm. The CMPS (compare select max and store) instruction updates the contents of TRN register on the basis of the comparison between the accumulator high word and the accumulator low word.

Auxiliary Registers (AR0–AR7)

The eight 16-bit auxiliary registers (AR0–AR7) can be accessed by the CPU and modified by the auxiliary register arithmetic units (ARAUs). The primary function of the auxiliary registers is to generate 16-bit addresses for data space. However, these registers can also act as general-purpose registers or counters.

Stack-Pointer Register (SP)

The 16-bit stack-pointer register (SP) contains the address of the top of the system stack. The SP always points to the last element pushed onto the stack. The stack is manipulated by interrupts, traps, calls, returns, and the PSHD, PSHM, POPD, and POPM instructions. Pushes and pops of the stack predecrement and postincrement, respectively, the 16-bit value in the stack pointer.

Circular-Buffer Size Register (BK)

The ARAUs use16-bit circular-buffer size register (BK) in circular addressing to specify the data block size.

Block-Repeat Registers (BRC, RSA, REA)

The 16-bit block-repeat counter (BRC) register specifies the number of times a block of code is to repeat when a block repeat is performed. The 16-bit block repeat start address (RSA) register contains the starting address of the block of program memory to be repeated.

The 16-bit block-repeat end address (REA) register contains the ending address of the block of program memory to be repeated.

6.7 Addressing Modes

Immediate Addressing

In immediate addressing, the instruction syntax contains the specific value of the operand. Two types of values can be encoded in an instruction:

- Short immediate values can be 3, 5, 8, or 9 bits in length.
- Long immediate values are always 16 bits in length.

Immediate values can be encoded in 1-word or 2-word instructions. The 3, 5, 8, or 9 bit values are encoded into 1-word instructions; 16-bit values are encoded into 2-word instructions. The length of the immediate value encoded in an instruction depends on the type of instruction used.

Accumulator Addressing

Accumulator addressing uses the value in the accumulator as an address.
This addressing mode is used to address program memory as data.
Two instructions allow you to use the accumulator as an address:

- READA Smem
- WRITA Smem

READA transfers a word from a program-memory location specified by accumulator A to a data-memory location specified by the single data-memory (Smem) operand of the instruction. WRITA transfers a word from a data-memory location specified by the Smem operand of the instruction to a program-memory location specified by accumulator A. In repeat mode, an increment may be used to increment accumulator A.

Direct Addressing

In direct addressing, the instruction contains the lower seven bits of the data memory address (dma). The 7-bit dma is an address offset that is combined with a base address, with the data-page pointer (DP), or with the stack pointer (SP) to form a 16-bit data-memory address. Using this form of addressing, you can access any of 128 locations in random order without changing the DP or the SP. Either DP or SP can be combined with the dma offset to generate the actual address. The compiler mode bit (CPL), located in status register ST1, selects which method is used to generate the address:

- When CPL = 0, the dma field is concatenated with the 9-bit DP field to form the 16-bit data-memory address.
- When CPL = 1, the dma field is added (positive offset) to SP to form the 16-bit data-memory address.

The syntax for direct addressing uses a symbol or a number to specify the offset value. For example, to add the contents of the memory location SAMPLE to accumulator B, provided that the correct base address is in DP (CPL = 0) or SP (CPL = 1), you would write:

ADD SAMPLE, B

The lower seven bits of the address of SAMPLE are stored in the instruction word.

Indirect Addressing

In indirect addressing, any location in the 64K-word data space can be accessed using the 16-bit address contained in an auxiliary register. The C54xE DSP has eight 16-bit auxiliary registers (AR0–AR7). Indirect addressing is used mainly when there is a need to step through sequential locations in memory in fixed-size steps. When memory is addressed with indirect addressing, the auxiliary register and the address can be optionally modified by a decrement, an increment, an offset, or an index. Special modes offer circular and bit-reversed addressing. A circular buffer size register (BK) is used with circular addressing. The AR0 register is used for indexed and bit-reversed addressing modes in addition to being used to point to memory as the other auxiliary registers do. Indirect addressing is flexible enough not only to read or write a single 16-bit data operand from memory with one instruction, but also to access two data memory locations with one instruction. Accesses of two data memory

locations include reads of two independent memory locations, reads and writes of two consecutive memory locations, and a read of one memory location combined with a write to a memory location.

Memory-Mapped Register Addressing

Memory-mapped register addressing is used to modify the memory-mapped registers without affecting either the current data-page pointer (DP) value or the current stack-pointer (SP) value. Because DP and SP do not need to be modified in this mode, the overhead for writing to a register is minimal. Memory-mapped register addressing works for both direct and indirect addressing. Addresses are generated by:

- Forcing the nine most significant bits (MSBs) of data-memory address to 0, regardless of the current value of DP or SP when direct addressing is used.
- Using the seven LSBs of the current auxiliary register value when indirect addressing is used.

For example, if AR1 is used to point to a memory-mapped register in memory mapped register addressing mode and it contains a value of FF25h, then AR1 points to the timer period register (PRD), since the seven LSBs of AR1 are 25h and the address of the PRD is 0025h. After execution, the value remaining in AR1 is 0025h.

Stack Addressing

The system stack is used to automatically store the program counter during interrupts and subroutines. It can also be used at your discretion to store additional items of context or to pass data values. The stack is filled from the highest to the lowest memory address. The processor uses a 16-bit memory mapped register, the stack pointer (SP), to address the stack. SP always points to the last element stored onto the stack. Four instructions access the stack using the stack addressing mode:

- PSHD pushes a data-memory value onto the stack.
- PSHM pushes a memory-mapped register onto the stack.
- POPD pops a data-memory value from the stack.

6.8 Branches

Branches break the sequential flow of instructions by transferring control to another location in program memory. Therefore, branches affect the program address generated and stored in PC. The C54xE DSP performs both unconditional and conditional branches, and both of these types can be either nondelayed or delayed.

Unconditional Branches

An unconditional branch is always executed when it is encountered. During the execution, PC is loaded with the specified branch-to-program-memory address and execution of the new section of code begins at that address. The address loaded into PC comes from either the second word of the branch instruction or the lower 16 bits of an accumulator (accumulator A or accumulator B). By the time the branch instruction reaches the execute phase of the pipeline, the next two instruction words have already been fetched. How these two instruction words are handled depends in part on whether the branch is nondelayed or delayed:

- **Nondelayed:** The two instruction words are flushed from the pipeline so that they are not executed, and then execution continues at the branched to address.

- **Delayed:** The one 2-word instruction or two 1-word instructions following the branch instruction are executed. This allows you to avoid flushing the pipeline, which requires extra cycles.

Conditional Branches

Conditional branches operate like unconditional branches, but they execute only when one or more user-specified conditions are met. If all the conditions are met, PC is loaded with the second word of the branch instruction, which contains the address to branch to, and execution continues at this address. By the time the conditions have been tested, the two instruction words following the conditional branch instruction have already been fetched

and are in the pipeline. How these two instruction words are handled depends in part on whether the branch is nondelayed or delayed:

- **Nondelayed:** If all the conditions are met, these two instruction words are flushed from the pipeline so that they are not executed, and then execution continues at the branched-to address. If the conditions are not met, the two instruction words are executed instead of the branch.

- **Delayed:** The one 2-word instruction or two 1-word instructions following the branch instruction are executed. This allows you to avoid flushing the pipeline, which requires extra cycles. The conditions tested are not affected by the instructions following the delayed branch.

Far Branches

To allow branches to extended memory, there are two far branch instructions:

- FB[D] branches to the extended memory address specified by the instruction.
- FBACC[D] branches to the extended memory address specified in the designated accumulator.

6.9 Calls

Like branches, calls break the sequential flow of instructions by transferring control to some other location in program memory. However, unlike branches, this transfer is intended to be temporary. When a subroutine or function is called, the address of the next instruction following the call is saved in the stack. This address is used to return to the calling program and resume execution. The C54xE DSP performs both unconditional and conditional calls, and both of these types can be either nondelayed or delayed.

Unconditional Calls

An unconditional call is always executed when it is encountered. When the call is executed, the PC is loaded with the specified program-memory address and execution of the called routine begins at that address. The address loaded into PC can come from either the second word of the call instruction or the lower 16 bits of an accumulator (accumulator A or accumulator B). Before the PC is loaded, the return address is saved in the stack. After the subroutine or function is executed, a return instruction loads the PC with the return address from the stack, and execution resumes at the instruction following the call. By the time the unconditional call instruction reaches the execute phase of the pipeline, the next two instruction words have already been fetched. How these two instruction words are handled depends in part on whether the call is nondelayed or delayed:

- **Nondelayed:** The two instruction words are flushed from the pipeline so that they are not executed, the return address is stored to the stack, and then execution continues at the beginning of the called function.

- **Delayed:** The one 2-word instruction or two 1-word instructions following the call instruction are executed. This allows you to avoid flushing the pipeline, which requires extra cycles.

Conditional Calls

Conditional calls operate like unconditional calls, but they execute only when one or multiple conditions are met. If all the conditions are met, the PC is loaded with the second word of the call instruction, which contains the starting address of the function to be called. Before branching to the called function, the processor stores the address of the instruction following the call instruction to the stack. The function must end with a return instruction, which takes the address off the stack and loads PC, allowing the processor to resume execution of the calling program. By the time the conditions of the conditional call instruction have been tested, the two instruction words following the call instruction have already been fetched in the pipeline. How these two instruction words are handled depends in part on whether the call is nondelayed or delayed:

- **Nondelayed:** If all the conditions are met, these two instruction words are flushed from the pipeline so that they are not executed, and then execution continues at the beginning of the called function. If the conditions are not met, the two instructions are executed instead of the call.

- **Delayed:** The one 2-word instruction or two 1-word instructions following the call instruction are always executed. This allows you to avoid flushing the pipeline, which requires extra cycles. The conditions tested are not affected by the instructions following the delayed call. If the conditions are not met, the processor executes the two instruction words instead of the call.

Far Calls

To allow calls to extended memory, there are two far call instructions:

- The FCALL instruction pushes XPC onto the stack, pushes PC onto the stack, and branches to the extended memory address specified by the instruction.
- The FCALA pushes XPC onto the stack, pushes PC onto the stack, and branches to the extended memory address specified in the designated accumulator.

6.10 Interrupts

Interrupts are hardware-driven or software-driven signals that cause the C54xE DSP to suspend its main program and execute another function called an interrupt service routine (ISR). Typically, interrupts are generated by hardware devices that need to give data to or take data from the C54x DSP (for example, ADCs, DACs, and other processors). Interrupts can also be used to signal that a particular event has taken place (for example, the timer is finished counting).

The C54x DSP supports both software and hardware interrupts:

- A software interrupt is requested by a program instruction (INTR, TRAP, or RESET).
- A hardware interrupt is requested by a signal from a physical device. Two types exist:
- External hardware interrupts are triggered by signals at external interrupt ports.
- Internal hardware interrupts are triggered by signals from the on-chip peripherals.
- When multiple hardware interrupts are triggered at the same time, the C54x DSP services them according to a set priority ranking in which 1 has the highest priority. To determine the priorities for the hardware interrupts, refer to the table for your particular C54x device in section 6.10.10, Interrupt Tables, on page 6-38. Each of the C54x DSP interrupts, whether hardware or software, can be placed in one of the following two categories:

Maskable Interrupts

These are hardware or software interrupts that can be blocked (masked) or enabled (unmasked) using software. The C54x DSP supports up to 16 user-maskable interrupts (SINT15–SINT0). Each device uses a subset of these 16 interrupts. For example, the C541 uses only nine of these interrupts (the others are tied high internally). Some of these have two names because they can be initiated by software or hardware; for the C541, the hardware names for these interrupts are:

- INT3 through INT0
- RINT0, XINT0, RINT1, and XINT1 (serial port interrupts)
- TINT (timer interrupt)

Nonmaskable interrupts

These interrupts cannot be blocked. The C54x DSP always acknowledges this type of interrupt and branches from the main program to an ISR. The C54x DSP nonmaskable interrupts include all software interrupts and two external hardware interrupts: RS (reset) and NMI. (RS and NMI can also be asserted using software.) RS is a nonmaskable interrupt that affects all C54x DSP operating modes. NMI is a nonmaskable interrupt. Interrupts are globally disabled when NMI is asserted. NMI is different from RS because it does not affect any of the C54x DSP modes. The C54x DSP handles interrupts in three phases:

- **Receive interrupt request**. Suspension of the main program is requested via software (program code) or hardware (a pin or an on-chip peripheral). If the interrupt source is requesting a maskable interrupt, the corresponding bit in the interrupt flag register (IFR) is set when the interrupt is received.

- **Acknowledge interrupt**. The C54x DSP must acknowledge the interrupt request. If the interrupt is maskable, predetermined conditions must be met in order for the C54x DSP to acknowledge it. For nonmaskable hardware interrupts and for software interrupts, acknowledgment is immediate.

- **Execute interrupt service routine (ISR)**. Once the interrupt is acknowledged, the C54x DSP executes the branch instruction you place at a predetermined address (the vector location) and performs the ISR.

6.11 Pipeline Operation

The C5416 DSP has a six-level deep instruction pipeline. The six stages of the pipeline are independent of each other, which allows overlapping execution of instructions. During any given cycle, from one to six different instructions can be active, each at a different stage of completion. The six levels and functions of the pipeline structure are:

Program prefetch: Program address bus (PAB) is loaded with the address of the next instruction to be fetched.

Program fetch: An instruction word is fetched from the program bus (PB) and loaded into the instruction register (IR). This completes an instruction fetch sequence that consists of this and the previous cycle.

Decode: The contents of the instruction register (IR) are decoded to determine the type of memory access operation and the control sequence at the data- address generation unit (DAGEN) and the CPU.

Access: DAGEN outputs the read operand's address on the data address bus, DAB. If a second operand is required, the other data address bus, CAB, is also loaded with an appropriate address. Auxiliary registers in indirect addressing mode and the stack pointer (SP) are also updated. This is considered the first of the 2-stage operand read sequence.

Read: The read data operand(s), if any, are read from the data buses, DB and CB. This completes the two-stage operand read sequence. At the same time, the two-stage operand write sequence begins. The data address of the write operand, if any, is loaded into the data write address bus (EAB). For memory-mapped registers, the read data operand is read from memory and written into the selected memory-mapped registers using the DB.

Execute: The operand write sequence is completed by writing the data using the data write bus. The instruction is executed in this phase. Figure 6.7 shows the six stages of the pipeline and the events that occur in each stage. The first two stages of the pipeline: prefetch and fetch, are the instruction fetch sequence. In one cycle, the address of a new instruction is loaded. In the following cycle, an instruction word is read. In case of multiword instructions, several such instruction fetch sequences are needed.

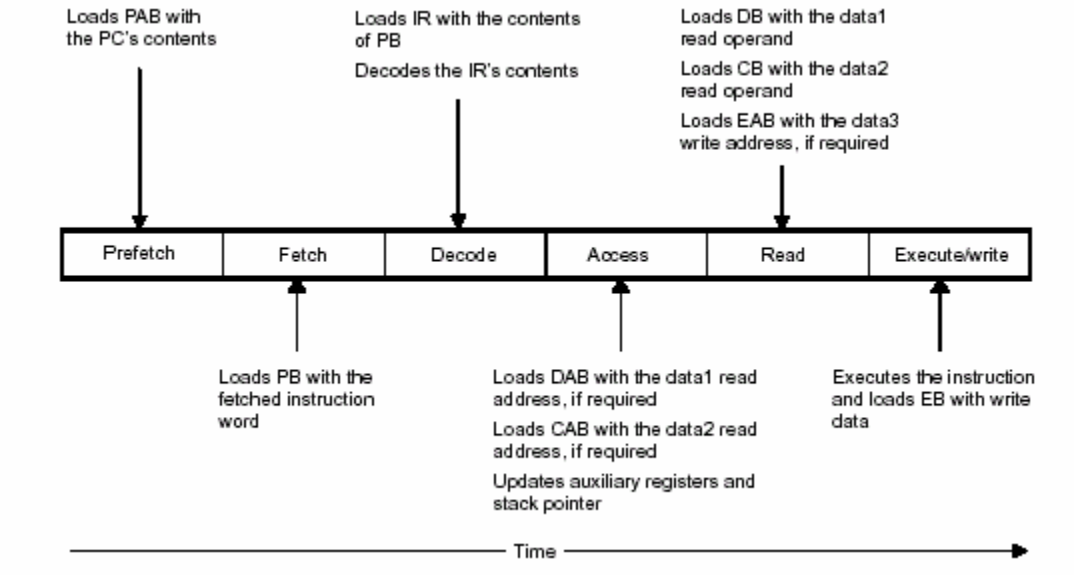


Figure 6.7 Pipeline structure of DSP 5416

During the third stage of the pipeline: decode, the fetched instruction is decoded so that appropriate control sequences are activated for proper execution of the instruction. The next two pipeline stages: access and read, are an operand read sequence. If required by the instruction, the data address of one or two operands are loaded in the access phase and the operands are read in the following read phase. Any write operation is spread over two stages of the pipeline, the read and execute stages. During the read phase, the data address of the write operand is loaded onto EAB. In the following cycle, the operand is written to memory using EB. Each memory access is performed in two phases by the C54x DSP pipeline. In the first phase, an address bus is loaded with the memory address. In the second phase, a corresponding data bus reads from or writes to that memory address.

Chapter 7

DSP Based Implementation

7.1 Introduction

This energy metering system facilitates the real time processing and separation of real, reactive and harmonic power using proposed algorithms. To process the algorithm in real time there arises a need of a powerful processor. The faster the processor the more will be number of consumer that can be taken care of it. Other major concern is the format of data which must be as compact as possible, but allows further analysis of events with the sufficient details to determine the possible origin of faults. The processor must also be capable of temporal storage of sampled data and supporting the most time consuming computations. The Digital Signal Processor simplifies all these tasks. Hence DSP TMS320VC5416 is used to develop the energy metering system.

The peripherals of the DSP used in the development of the energy meter such as analog to digital converter (ADC), digital to analog converter (DAC) and serial port are described below:

7.2 Analog to Digital Converter (ADC)

The DSP uses IC AD7862 for analog to digital conversion. The AD7862 is a high speed, low power, dual 12-bit analog to digital converter that operates from a single +5V supply. The part contains two 4 micro second successive approximation ADCs, two track and hold amplifiers, an internal +2.5V reference and a high speed parallel interface. There are four analog inputs that are grouped into two channels A &B, selected by A0 input. Each channel has two inputs (VA1 & VA2 for channel A and VB1 & VB2 for channel B) that can be sampled and converted simultaneously. The part accepts analog input range of +/- 10Vwithout causing damage.

Conversion is initiated on the AD7862 by pulsing the CONVST input. On the falling edge of CONVST, both on chip track and holds are placed into hold simultaneously, and the conversion sequence is started on both channels. The conversion clock for the part is generated internally using a laser trimmed clock oscillator circuit. The busy signal indicates the end of conversion, and this time the conversion results for both channels are available to be read. The first read after a conversion accesses the result from VA1 or VB1 while the

second read access the result from VA2 or VB2, depending on whether the multiplexer select A0 is low or high, respectively. Data is read from the part via a 12 bit parallel data bus with standard CS and RD signals. Conversion time for the AD7862 is 3.6 micro second and the track and hold acquisition time is 0.3 microsecond.

The track and hold amplifiers on the AD7862 allow the ADCs to accurately convert an input sine wave of full scale value to 12 bit accuracy. The track and hold amplifiers acquire input signals to 12 bit accuracy in less than 400 ns. The two track and hold amplifiers sampler their respective channels simultaneously on the falling edge of CONVST. The aperture time for the track and holds (i.e. the delay time between the external CONVST signal and the track and hold actually going into hold) is typically 15 ns. At the end of conversion, the part returns to its tracking mode. The acquisition time of the track and hold amplifiers begins at this point.

7.3 Digital to Analog Converter (DAC)

The DSP uses IC AD8582 for digital to analog conversion. The AD8582 is a complete, parallel input, dual 12 bit, voltage output DAC designed to operate from a single +5V supply. The DAC AD8582 offers the user low cost and ease of use +5V systems. Included on the chip, in addition to the DACs, are a amplifier, latch and reference. The reference is trimmed to 2.5 volts output, and the on chip amplifier gains the DAC output to 4.095 volts full scale. The parallel data interface consists of twelve data bits, DB0 to DB11, an address select pin A/B, two load strobe pins LDA and LDB, and an active low CS strobe. In addition an asynchronous RST pin will set all DAC register bits to zero causing the VOUT to become zero volts.

7.4 Algorithm Implemented on DSP

One of the four ADC channels is for sampling the voltage wave form. Rest three ADC channels are sampling current of three different consumers. These sampled voltage and current values are stored in the memory location defined by the algorithms. After taking 256

samples at each channel, the processor starts calculation of power for different consumers one by one, accessing data from the corresponding memory location. The power calculated by the processor is stored in the memory from where it can be accessed for different usages. After calculating the power for each sample and for the each consumer the process is repeated so that continuous monitoring of power is possible. The block diagram given below depicts the whole process starting from sampling up to the calculation of energy.

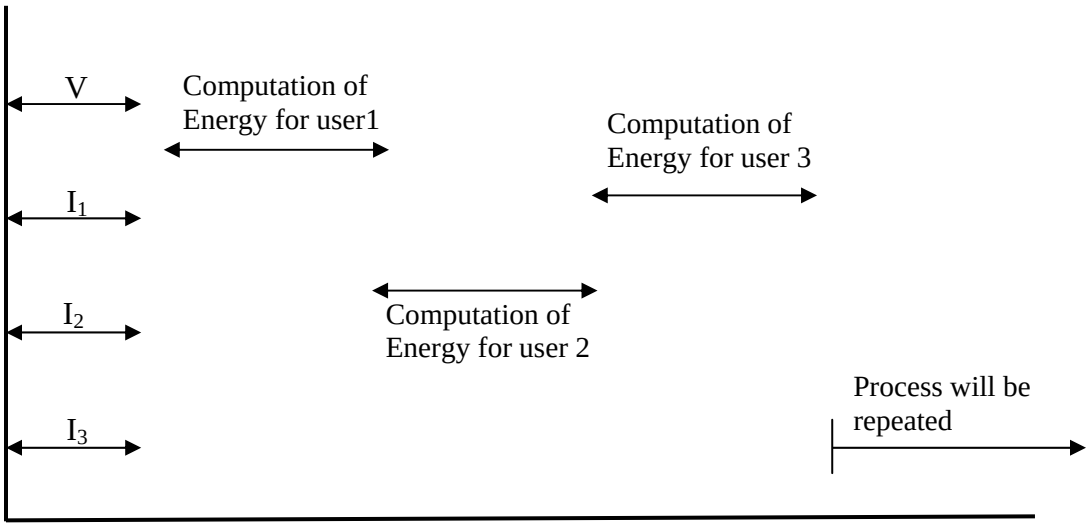


Figure 7.1 Block Diagram of Sampling & Energy calculation Process

The flowchart for the program implemented on DSP to calculate the energy consumed by each consumer is given below at fig 7.2. The program first stores the voltage and current waveforms for different consumer and then instantaneous values of real (P) and reactive power (Q) are calculated and stored. These values of P & Q are averaged and halved to get final values of fundamental components of real and reactive power.

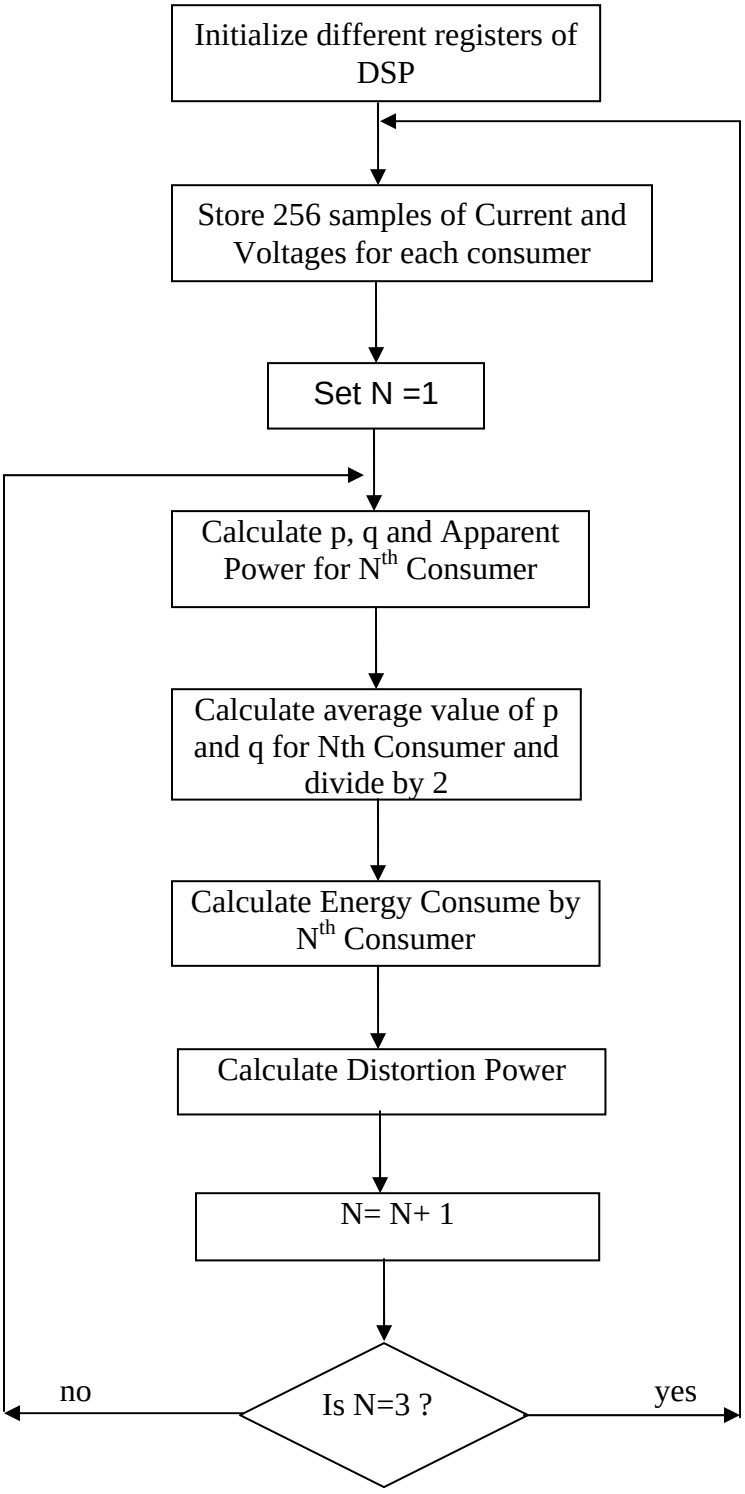


Figure 7.2 Flowchart of the Power calculation program

Chapter 8

Results and Discussion

8.1 General

The complete system was first simulated in the MatLab environment (as described in chapter 4). Dynamic response of the measuring system to demonstrate decomposition of power into different parts was presented for diode rectifier fed load and triac fed ac load. These results were verified with the practical ones. The algorithm implemented through DSP has been tested for three different kinds of loads to demonstrate the capabilities claimed in the thesis. First load is selected as diode rectifier fed resistive load. And then other two are conventional loads R-L load (real + reactive power) and resistive load (real power only). The results obtained are presented in the following scheme in the afore said sequence followed by discussion on the results.

8.2 Performance of the Metering System

The prototype system is tested separately for three load connected simultaneously to the power system. The hardware interface is adjusted and probes are set s per details below for each load.

Resistive Load

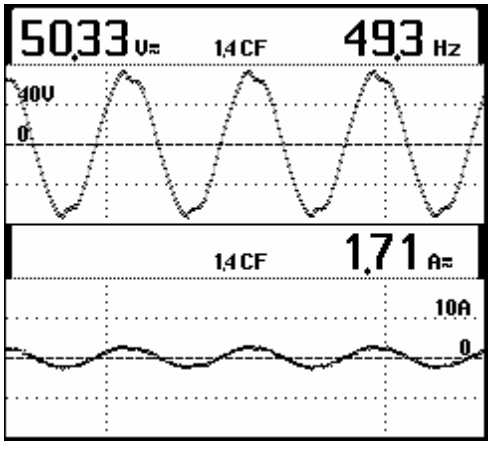


Figure 8.1 Voltage and current values for resistive load

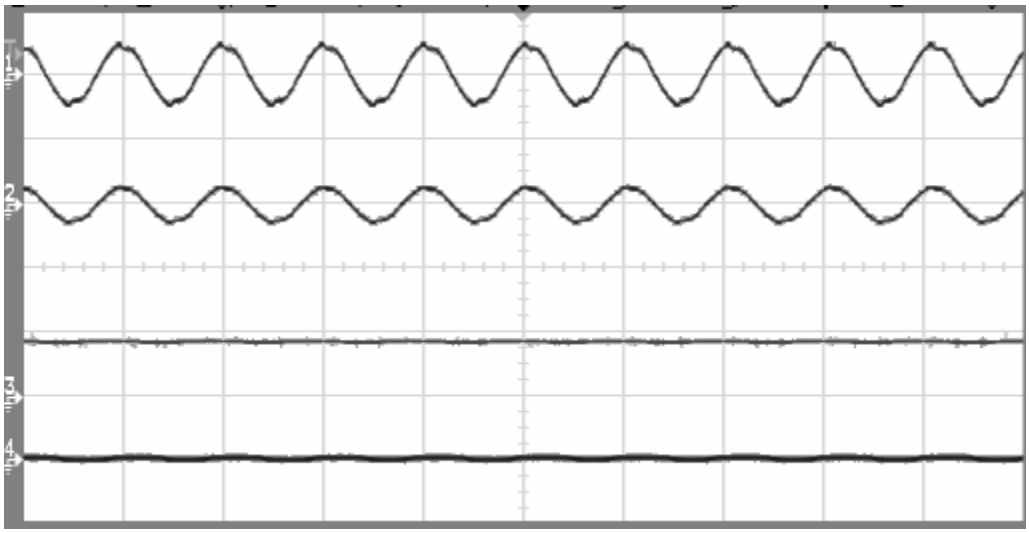


Figure 8.2 Voltage, Current, Real & Reactive Power waveforms for resistive load

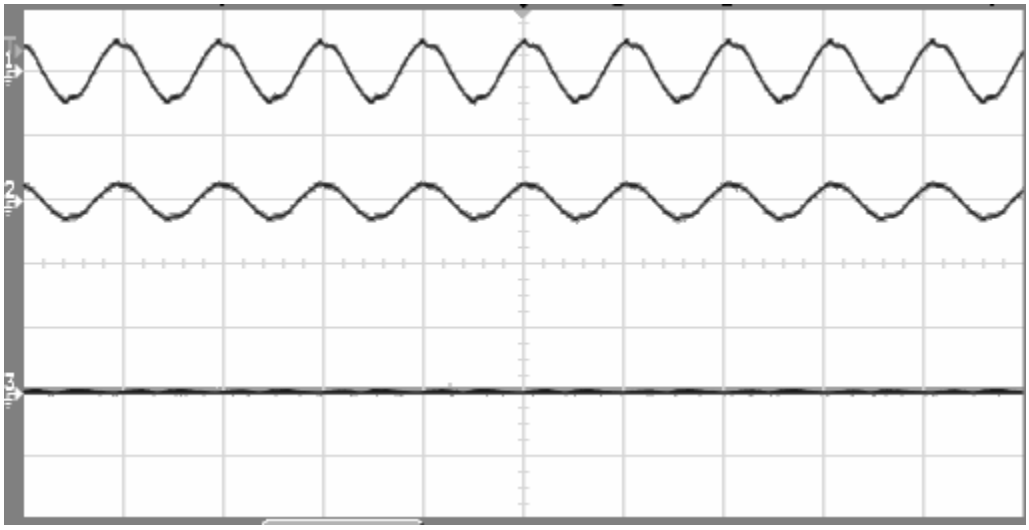


Figure 8.3 Voltage, Current & Distortion Power waveforms for resistive load

The overall gain of the system is 10. Therefore the waveforms of powers seen at the DAC terminal must be multiplied by a factor of 10. Figure 8.1 shows four wave forms of Voltage, Load Current, Real Power and Reactive Power respectively at different probes. It is

clear from the figure that load current is pure sinusoidal. There is no reactive component of the power. Resistive load is consuming only Real power. The value of the resistance taken is 30 ohms. Figure 8.1 shows the values of voltage and current. The real power consumed by the load comes out to be 86.06 watts by the mathematical calculations. It matches with the power calculated by DSP and taken out at DAC as seen in the third probe of figure 8.1. Figure 8.2 shows voltage at first probe, current at second probe and Distortion Power at third probe. It can be observed from figure 8.2 that the distortion power is nearly zero for resistive load. The voltage waveform at the point of common coupling is distorted due to influence of third harmonic produced by diode rectifier load.

Series R – L load

The other load chosen is a series R-L load which is intentional chosen to verify the algorithm for load demanding reactive power. Here also the interface is calibrated as per details below.

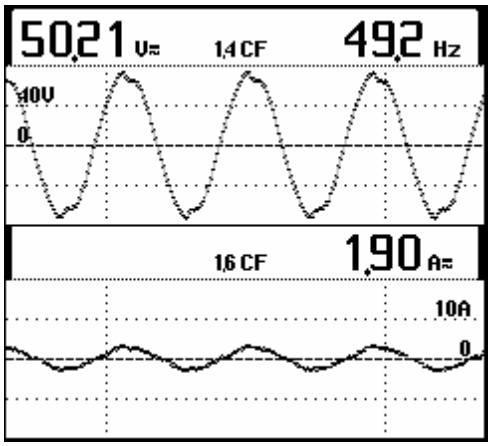


Figure 8.4 Voltage and current values for R-L load

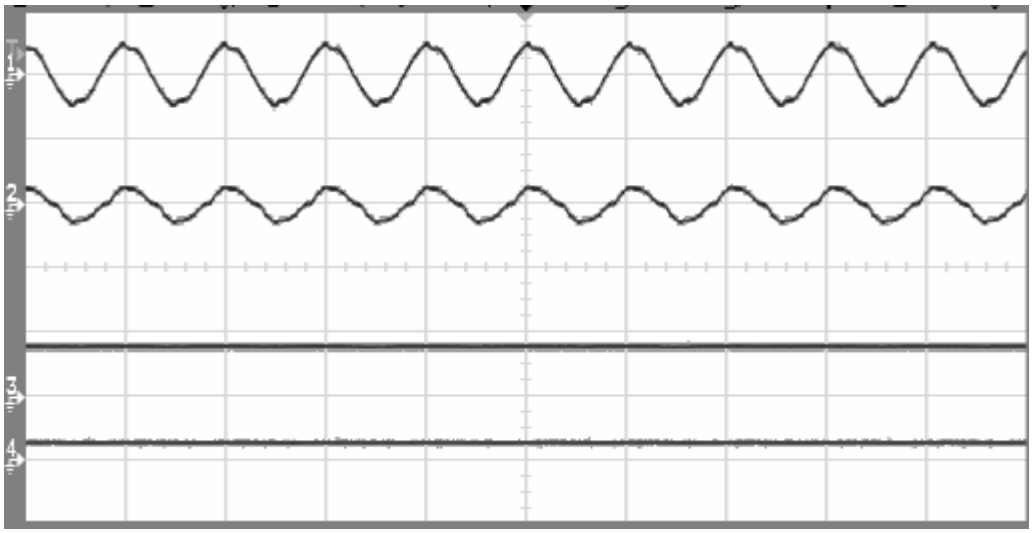


Figure 8.5 Voltage, Current, Real & Reactive Power waveforms for R-L load

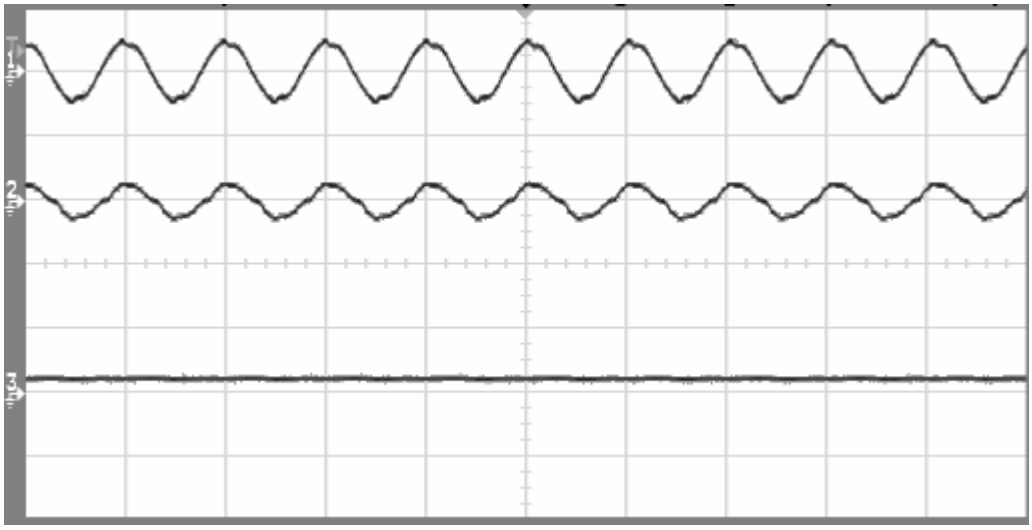


Figure 8.6 Voltage, Current & Distortion Power waveforms for R-L load

The overall gain of the system is 10. Therefore the waveforms of powers seen at the DAC terminal must be multiplied by a factor of 10. The values of resistance and inductance taken for the load are 26 ohms and 9.02 mH. Figure 8.5 shows the values of voltage and current. Figure 8.5 shows four wave forms of Voltage, Load Current, Real Power and

Reactive Power respectively at different probes. The real power consumed by the loads comes out to be 93.85 watts by mathematical calculations. It matches with the output of DSP as shown in the figure 8.5 at probe 3. The reactive power comes out to be 10.06 VARs. This result is similar to the output from DSP as shown at probe 4. Figure 8.6 shows voltage at first probe, current at second probe and Distortion Power at third probe. The distortion power comes out to be 13.85 VA. It also verifies the result from the DSP as shown in figure 8.6 at probe 3.

Diode Rectifier Load

The load having highest harmonic content and a nuisance to power system is a diode rectifier with ac line reactor. This load consumes all the three types of power, namely real, reactive and harmonic power. As per the details of probe setting and hardware following are the results.

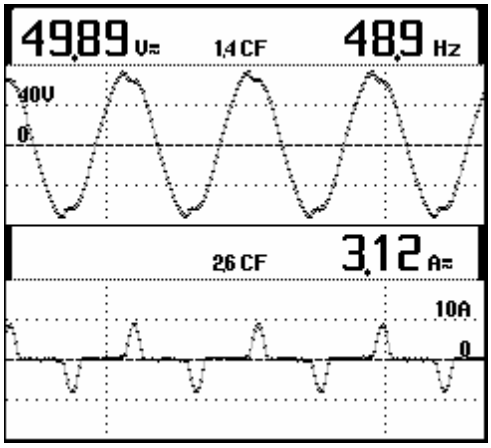


Figure 8.7 Voltage and current values for diode rectifier

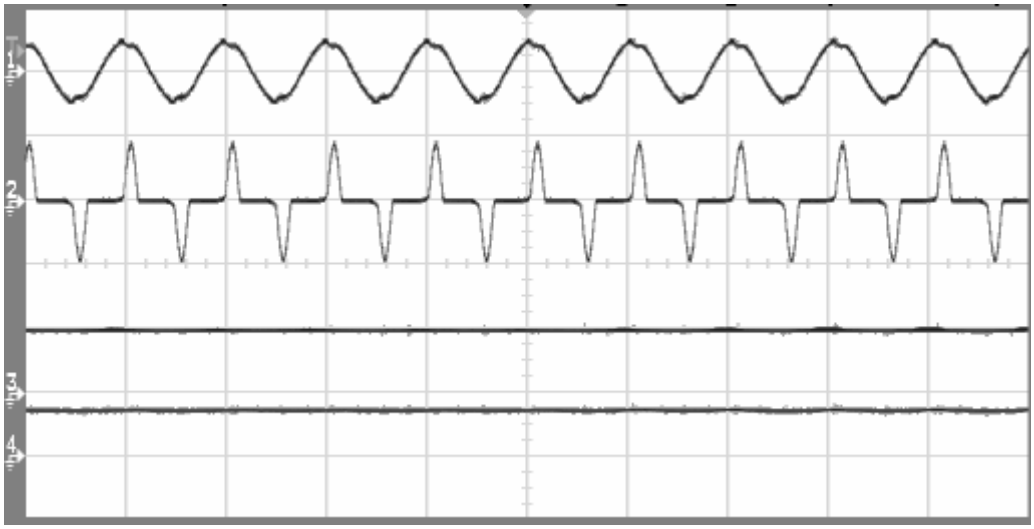


Figure 8.8 Voltage, Current, Real & Reactive Power waveforms for diode rectifier load

Figure 8.9 Voltage, Current & Distortion Power waveforms for diode rectifier load

The overall gain of the system is 10. Therefore the waveforms of powers seen at the DAC terminal must be multiplied by a factor of 10. The values of resistance and inductance taken for the load are 10 ohms and 30.6 mH. Figure 8.7 shows the values of voltage and current. Figure 8.8 shows four wave forms of Voltage, Load Current, Real Power and

Reactive Power respectively at different probes. The real power consumed by the loads comes out to be 97.3 watts by mathematical calculations. It matches with the output of DSP as shown in the figure 8.8 at probe 3. The reactive power comes out to be 89.52 VARs. This result is similar to the output from DSP as shown at probe 4. Figure 8.9 shows voltage at first probe, current at second probe and Distortion Power at third probe. The distortion power comes out to be 82.14 VA. This result is also similar to the one which is at the DAC output of the DSP as shown in figure 8.9 at probe 3.

Results obtained from both ways, one by mathematical calculations and other one by practical implementation of algorithms on DSP are nearly same. But there is a little bit of difference between the calculated values and the values obtained from the DAC for some quantities. The magnitude of error is very small. The errors may be further minimized by using some corrections namely; the algorithm for power calculation can be made more optimized to get more accurate results. The interfacing circuit can be modified for better sampling and sensing of voltage and currents waveforms. The more advanced processor can be more beneficial in many ways such that better storing and handling of data, fast processing of algorithms used for power calculation, more accurate arithmetic operations.

Chapter 9

Conclusion and Future Scope of Work

Conclusion

Proposed DSP based metering system presents simple and effective measurement for single-phase power and energy measurement. It is proposed that in light of IEEE519 and IEC555-2-2 the energy measurement may be adapted for reactive power and also for harmonic distortion in terms of Total Harmonic Distortion (THD). Based on this, the proposed meter got the advantages over presently used energy meters as it measures not only active power but also reactive power and THD. The meter is capable of handling many consumers at a time as the operational speed of DSP is 50 nsec per instructions thus can calculate energy for all consumers in less than one cycles (0.02 sec). At the same time meter data can be stored in external memory and can be used for billing, load analysis, load forecasting. The results form simulation of the model in MATLAB environment and the results receives after successful implementation of the model using current and voltage sensors and processing of data with TMS320VC5416 DSP are similar and proves the validity of the effective and efficient operation of the meter giving the precise measurement of the active, reactive and THD of the respective consumers.

Future Scope of Work

1. The present work does not incorporate the transmission of measured power to the central recording station. This can be done by connecting a transmitter (based on Bluetooth, PLCC, or any other short range RF communication technique) to the serial port of the DSK. The readings may be periodically sent to the serial port of DSK for transmission.

2. The transmitted data is to be received at the central recording station. A receiving and recording system can be developed. Such a system must create an online database that which can then be used for load management studies and online billing etc.

3. A surge protection system can be incorporated using zener diodes (for voltage surges) and MOVs (Metal Oxide Varisters) for current surges.

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Appendix

Appendix A

Symbols and Abbreviations

Symbols	*Meaning*
A	Accumulator A
ALU	Arithmetic logic unit
AR	Auxiliary register, general usage
ARx	Designates a specific auxiliary register (0 _ x _ 7)
ARP	Auxiliary register pointer field in ST0; this 3-bit field points to the current auxiliary register (AR).
ASM	5-bit accumulator shift mode field in ST1 (–16 _ ASM _ 15)
B	Accumulator B
BRAF	Block-repeat active flag in ST1
BRC	Block-repeat counter
BITC	4-bit value that determines which bit of a designated data memory value is tested by the test bit instruction (0 __ BITC__15)
C16	Dual 16-bit/double-precision arithmetic mode bit in ST1
C	Carry bit in ST0
CC	2-bit condition code (0 _ CC _ 3)
CMPT	Compatibility mode bit in ST1
CPL	Compiler mode bit in ST1
cond	An operand representing a condition used by instructions that execute conditionally
[D]	Delay option
DAB	D address bus
DAR	DAB address register
dmad	16-bit immediate data-memory address (0 _ dmad _ 65 535)
Dmem	Data-memory operand
DP	9-bit data-memory page pointer field in ST0 (0 _ DP _ 511)

dst	Destination accumulator (A or B)
dst_	Opposite destination accumulator: If dst = A, then dst_ = B If dst = B, then dst_ = A
EAB	E address bus
EAR	EAB address register
extpmad	23-bit immediate program-memory address
FRCT	Fractional mode bit in ST1
hi(A)	High part of accumulator A (bits 31–16)
HM	Hold mode bit in ST1
IFR	Interrupt flag register
INTM	Interrupt mode bit in ST1
K	Short-immediate value of less than 9 bits
k3	3-bit immediate value (0 _ k3 _ 7)
k5	5-bit immediate value (–16 _ k5 _ 15)
k9	9-bit immediate value (0 _ k9 _ 511)
lk	16-bit long-immediate value
Lmem	32-bit single data-memory operand using long-word addressing
MMR	Memory-mapped register
MMRx, MMRy	Memory-mapped register, AR0–AR7 or SP
n	Number of words following the XC instruction; n = 1 or 2
N	Designates the status register modified in the RSBX, SSBX, and XC instructions: N = 0 Status register ST0 N = 1 Status register ST1
OVA	Overflow flag for accumulator A in ST0
OVB	Overflow flag for accumulator B in ST0
OVdst	Overflow flag for the destination accumulator (A or B)
OVdst_	Overflow flag for the opposite destination accumulator (A or B)

OVsrc	Overflow flag for the source accumulator (A or B)
OVM	Overflow mode bit in ST1
PA	16-bit port immediate address (0 _ PA _ 65 535)
PAR	Program address register
PC	Program counter
pmad	16-bit immediate program-memory address (0 _ pmad _ 65 535)
Pmem	Program-memory operand
PMST	Processor mode status register
prog	Program-memory operand
[R]	Rounding option
RC	Repeat counter
REA	Block-repeat end address register
rnd	Round
RSA	Block-repeat start address register
RTN	Fast-return register used in RETF[D] instruction
SBIT	4-bit value that designates the status register bit number modified in the RSBX, SSBX, and XC instructions (0 _ SBIT _ 15)
SHFT	4-bit shift value (0 _ SHFT _ 15)
SHIFT	5-bit shift value (–16 _ SHIFT _ 15)
Sind	Single data-memory operand using indirect addressing
Smem	16-bit single data-memory operand
SP	Stack pointer
src	Source accumulator (A or B)
ST0, ST1	Status register 0, status register 1
SXM	Sign-extension mode bit in ST1
T	Temporary register
TC	Test/control flag in ST0
TOS	Top of stack
TRN	Transition register
TS	Shift value specified by bits 5–0 of T (–16 _ TS _ 31)
uns	Unsigned

XF	External flag status bit in ST1
XPC	Program counter extension register
Xmem	16-bit dual data-memory operand used in dual-operand instructions and some single-operand instructions
Ymem	16-bit dual data-memory operand used in dual-operand instructions
– – SP	Stack pointer value is decremented by 1
+ + SP	Stack pointer value is incremented by 1
+ + PC	Program counter value is incremented by 1

Appendix B

Different operators

Symbols	*Operators*	*Evaluation*
+	Unary plus	Right to left
–	Unary minus	Right to left
~	1’s complement	Right to left
*	Multiplication	Left to right
/	Division	Left to right
%	Modulo	Left to right
+	Addition	Left to right
–	Subtraction	Left to right
<<	Left shift	Left to right
>>	Right shift	Left to right
<<<	Logical left shift	Left to right
<	Less than	Left to right
≤	LT or equal	Left to right
>	Greater than	Left to right
≥	GT or equal	Left to right
!=	Not equal to	Left to right
&	Bitwise AND	Left to right
^	Bitwise exclusive OR	Left to right
|	Bitwise OR	Left to right

Appendix C

Instruction Set of TMS320VC5416

Mnemonic	*Description*
Arithmetic Operations	
ABDST	Absolute value of the distance between two vectors
ABS	Absolute value of the src
ADD	Adds a 16-bit value to the content of the selected accumulator or to a 16-bit operand Xmem
ADDC	Adds the 16-bit single data-memory operand Smem and the value of the carry bit (C) to src
ADDM	Adds the 16-bit single data-memory operand Smem to the 16-bit immediate memory value and stores the result in Smem
ADDS	Adds the 16-bit single data-memory operand Smem to src and stores the result in src
CMPL	Calculates the 1s complement of the content of src
DADD	Adds the content of src to the 32-bit long data-memory operand Lmem Adds the content of T to the 32-bit long data-memory operand Lmem
DADST	Copies the content of a single data-memory location Smem into the next higher address. When data is copied, the content of the addressed location
DELAY	remains the same
	Subtracts the content of src from the 32-bit long data-memory operand Lmem and stores the result in src
DRSUB	Subtracts the 32-bit long data-memory operand Lmem from the content of src, and stores the result in src
DSUB	Subtracts the content of T from the 32-bit long data-memory operand Lmem and stores the result in dst
DSUBT	Multiplies and adds with or without rounding
	Multiplies the content of T or a data-memory value by a data memory

MAC	value or an immediate value, and stores the result in dst
MPY	Multiplies the high part of accumulator A (bits 32–16) by a single data-memory operand Smem or by the content of T, and stores the result in dst
MPYA	or accumulator B
	Multiplies the unsigned content of T by the unsigned content of the single data-memory operand Smem, and stores the result in dst
MPYU	Computes the 2s complement of the content of src (either A or B) and stores the result in dst or src, if dst is not specified
NEG	Squares a single data-memory operand Smem or the high part of accumulator A (bits 32–16) and stores the result in dst
SQUR	Stores the data-memory value Smem in T, then it squares Smem and adds the product to src
SQURA	Stores the data-memory value Smem in T, then it squares Smem and subtracts the product from src
SQURS	Subtracts a 16-bit value from the content of the selected accumulator or from the 16-bit operand Xmem
SUB	Subtracts the content of the 16-bit single data-memory operand Smem and the logical inverse of the carry bit, C, from src without sign extension
SUBB	Subtracts the 16-bit single data-memory operand Smem, leftshifted 15 bits, from the content of src
	Subtracts the content of the 16-bit single data-memory operand Smem from
SUBC	the content of src
SUBS	

Logical Operations

AND	ANDs the 16-bit single operand Smem or 16-bit immediate operand lk or src or dst to src
ANDM	ANDs the 16-bit single data-memory operand Smem with a 16-bit long constant lk

BIT	Copies the specified bit of the dual data-memory operand Xmem into the TC bit of status register ST0
BITF	Tests the specified bit or bits of the data-memory value Smem copies the specified bit of the data-memory value Smem into the TC bit in status register ST0
CMPM	Compares the 16-bit single data-memory operand Smem to the 16-bit constant lk
CMPR	Compares the content of the designated auxiliary register (ARx) to the content of AR0
OR	ORs the src with a single data-memory operand Smem, a leftshifted 16-bit immediate value lk, dst, or with itself
ORM	ORs the single data-memory operand Smem with a 16-bit constant lk, and stores the result in Smem
ROL	Rotates each bit of src left 1 bit
ROR	Rotates each bit of src right 1 bit
XOR	Executes an exclusive OR of the 16-bit single data-memory operand Smem with the content of the selected accumulator
XORM	Executes an exclusive OR of the content of a data-memory location Smem with a 16-bit constant lk

Program-Control Operations

B	Passes control to the designated program-memory address (pmad)
BACC	Passes control to the 16-bit address in the low part of src
BANZ	Branches to the specified program-memory address (pmad) if the value of the current auxiliary register ARx is not 0
BC	Branches to the program-memory address (pmad) if the specified condition(s) is met
FB	Passes control to the program-memory address pmad (bits 15–0) on the page specified by pmad (bits 22–16)
CALA	Passes control to the 16-bit address in the low part of src

CALL	Passes control to the specified program-memory address (pmad)
CC	Passes control to the program-memory address (pmad) if the specified condition(s) is met.
FCALA	Loads the XPC with the value in src (bits 22–16) and passes control to the 16-bit address in the low part of src (bits 15–0)
FCALL	Passes control to the specified program-memory address pmad (bits 15–0) on the page specified by pmad (bits 22–16)
FRAME	Adds a short-immediate offset K to the SP
FRET	Replaces the XPC with the 7-bit value from the TOS and replaces the PC with the next 16-bit value on the stack
FRETE	Replaces the XPC with the 7-bit value from the TOS and replaces the PC with the next 16-bit value on the stack continuing execution from the new PC value
IDLE	Forces the program being executed to wait until an unmasked interrupt or reset occurs
INTR	Transfers program control to the interrupt vector specified by K
MAR	Modifies the content of the selected auxiliary register (ARx) as specified by Smem
NOP	No operation is performed. Only the PC is incremented
POPD	Moves the content of the data-memory location addressed by SP to the memory location specified by Smem
POPM	Moves the content of the data-memory location addressed by SP to the specified memory-mapped register MMR
RC	If the conditions given by cond are met, this instruction replaces the PC with the data-memory value from the TOS and increments the SP by 1. If the conditions are not met, this instruction just increments the PC by 1
RESET	Performs a non maskable software reset that can be used at any time to put the 5416 into a known state
RET	Replaces the value in the PC with the 16-bit value from the TOS
RETE	Replaces the value in the PC with the 16-bit value from theTOS. Execution continues from this address

RPT	The repeat counter (RC) is loaded with the number of iterations when this instruction is executed
RPTB	Repeats a block of instructions the number of times specified by the memory-mapped block-repeat counter (BRC)
RPTZ	Clears dst and repeats the next instruction n + 1 times, where n is the value in the repeat counter (RC)
RSBX	Clears the specified bit in status register 0 or 1 to a logic 0
SSBX	Sets the specified bit in status register 0 or 1 to a logic 1
TRAP	Transfers program control to the interrupt vector specified by K

Load and Store Operations

CMPS	Compares the two 16-bit 2s-complement values located in the high and low parts of src and stores the maximum value in the single data memory location Smem
DLD	Loads dst with a 32-bit long operand Lmem
DST	Stores the content of src in a 32-bit long data-memory location Lmem
LD	Loads the accumulator (dst, or src if dst is not specified) with a data-memory value or an immediate value
LDM	Loads dst with the value in memory-mapped register MMR
LDR	Loads the data-memory value Smem shifted left 16 bits into the high part of dst (bits 31–16)
LDU	Loads the data-memory value Smem into the low part of dst (bits 15–0)
LTD	Copies the content of a single data-memory location Smem into T and into the address following this data-memory location
MVDM	Copies data from a data-memory location dmad (address is in the DAB address register DAR) to a memory-mapped register MMR
MVDP	Copies a 16-bit single data-memory operand Smem to a Program memory location addressed by a 16-bit immediate value pmad
	Moves data from a memory-mapped register MMR to data

	memory
MVMD	Moves the content of memory-mapped register MMRx to the memory mapped register MMRy
MVMM	Moves a word in program memory addressed by a 16-bit immediate value pmad to a data-memory location addressed by Smem
MVPD	Reads a 16-bit value from an external I/O port PA (16-bit immediate address) into the specified data-memory location Smem
PORTR	Writes a 16-bit value from the specified data-memory location Smem to an external I/O port PA
PORTW	Transfers a word from a program-memory location specified by accumulator A to a data-memory location specififed by Smem
ST	Stores the content of T, the transition register (TRN), or a 16-bit constant lk in data-memory location Smem
	Stores the high part of src (bits 31–16) in data-memory location Smem
	Stores the low part of src (bits 15–0) in data-memory location Smem
STH	Stores the low part of src (bits 15–0) into the addressed memory-mapped register MMR
STL	Stores a 16-bit constant lk into a memory-mapped register MMR or a
STLM	memory location on data page 0
	Transfers a word from a data-memory location specified by Smem to a
STM	program-memory location
WRITA	

Appendix D

Photographs of the System