A DISSERTATION
ON

STUDY AND IMPLEMENTATION OF CURRENT CONVEYOR BASED WAVE ACTIVE FILTER

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CERTIFICATE

Date: _____

This is certified that the dissertation entitled **"Study and Implementation of Current Conveyor based Wave Active Filter"** is a work of **Mr. Hanuman Prasad Solanki** (University Roll No- 8573) a student of Delhi College of Engineering. This work is completed under my direct supervision and guidance and forms a part of master of engineering (Electronics and communication) course and curriculum. He has completed his work with utmost sincerity and diligence.

The work embodied in this major project has not been submitted to any other Institute/University for the award of any other degree to the best of my knowledge.

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ABSTRACT

In IC technology during the last some decade, designers used current mode technique to solve the several circuit design problem. The current-mode approach to signal processing has often been claimed to provide one or more of the following advantages: higher frequency range of operation, lower power consumption, higher slew rates, improved linearity, and better accuracy.

In this thesis current mode building block namely current conveyor and its application as higher order current mode filter has been studied. The higher order filter is realized using wave equivalent method. A detailed discussion of wave equivalent of series inductor has been given. This is also realized using current conveyor. This technique offers design simplicity and modularity as the equivalents of the other reactive elements in the series or shunt branch can be readily obtained by interchanging the outputs of the elementary block and/or using current inverters. A third-order lowpass filters has been realized using current conveyor based wave equivalents and its performance is evaluated through PSPICE simulations using 0.18 micron TSMC CMOS technology parameters.

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Chapter-1

INTRODUCTION

The demand for electronic circuits with extremely low supply voltages and power consumption is important in development of microelectronic technologies [1]. In many applications, additional requirements appear, particularly the extreme speed or the accuracy of signal processing. Simultaneous fulfillment of the above demands is problematic. In the last two decades, the evolution of modern applications of analog signal processing has followed the trends of so-called current mode [2], where signals, representing the information, are in the form of electric currents.

In contrast to the conventional voltage mode, which utilizes electric voltages, the current mode circuits can exhibit under certain conditions among other things higher bandwidth and better signal linearity. Since they are designed for lower voltage swings, smaller supply voltages can be used. Simultaneously with the development of current-mode applications, the mixed-mode circuits are also analyzed because of the necessity of optimizing the interface between the sub-blocks, which are working in different modes. The mixed-mode operation and even the comeback to the conventional voltage mode also have another justification: it appears that some generally accepted statements about the advantages of the current mode probably have no real basis [3].

However, the criticism of [3] notwithstanding, the current-mode techniques have given way to a number of important analog signal processing/signal generating circuits as is evident from a vast amount of literature on current-mode circuits and techniques published in the recent past. Due to the advances made in integrated circuit (IC) technology during the last two decades, circuit designers have quite often exploited the potential of current-mode analog techniques for evolving elegant and efficient solutions to several circuit design problems. As a consequence, the current-mode approach to signal processing has often been claimed to provide

one or more of the following advantages: higher frequency range of operation, lower power consumption, higher slew rates, improved linearity, and better accuracy.

The purpose of wave filter is to describe a method of deriving active RC filters from analogue passive prototype filters in such a way that desirable attributes of the passive filters are retained in the active realization. The insensitive properties of a doubly terminated passive lossless ladder filter are well known, and there exist several methods that enable the determination of active RC filters from these [4]-[6]. These methods are based either on a direct interpretation of the ladder network in terms of active components [4], [6] or on a signal-flow interpretation, from which a voltage transfer ratio is obtained in a multiple-feedback arrangement [5].

Recently, in the theory of digital-filter synthesis, scattering parameters are used for deriving digital-filter structures from passive doubly terminated lossless ladder filters. The scattering waves have been represented in the voltage [7]-[9]. The behavior of passive doubly terminated lossless ladder can be simulated using active RC filters using wave variables. The active filters so derived are referred wave active filters.

Higher-order filters can be designed with the well-known leapfrog approach. According to this, the voltage-current relationships of an LC ladder prototype are expressed in such a way that all variables are currents thus all the required operations are current operations. Another technique for designing high-order filters is the topological simulation of the passive prototypes. In this, the inductors are substituted by appropriate active configurations that try to be like inductor operation. The drawbacks of this configuration are the following: (a) a floating capacitor is required which degrades the performance of the derived filter topologies in high-frequency applications, and (b) two matched floating resistors are needed, whose values should be equal to the inverse of the transconductance parameter of the input transistors of the employed current conveyor.

An alternative systematic design procedure for emulating the topology of the corresponding LC ladder prototype is the well-known wave method [10], [11]. According to this method, the corresponding passive prototype filter is split into two-port sub networks which are fully described using the wave variables, defined as incident and reflected waves.

One way for obtaining the wave equivalents of the two-port sub networks is by using the scattering parameters matrix description. By choosing an inductor in a series branch as the elementary building block, its wave equivalent includes an appropriately configured lossy integrator. The wave equivalents of the other passive elements are derived by interchanging the terminals of the appropriate wave signals and/or adding current inverters. Thus, the essential difference between the leapfrog and the wave method is that leapfrog type circuits rely on lossless integrators, whereas wave filters rely only on lossy integrators. Absolute losslessness is not possible in practice, so the implementation of wave circuits in integrated form seems to be more realistic [11].

An attractive building block for designing current-mode active filters is the current conveyor**,** which is constructed with translinear loop and current mirror blocks. The advantages of this are wider signal bandwidth than that of conventional operational amplifier RC filters.

A current conveyor-based configuration for obtaining the wave equivalents of passive elements of the corresponding prototype filters is introduced in this report. Benefits of this method are: (a) the design procedure of high-order filters is much easier, in comparison to the leapfrog filters; (b) modular filter topologies are derived, as the equivalents of the other reactive elements are readily obtained from the equivalent of the elementary building block, and (c) only a grounded capacitor is used for obtaining the wave equivalents of the passive elements, instead of the floating capacitor and two matched floating resistors that are employed in the topological simulation of passive prototypes.

The thesis is organized in 5 chapters.

Chapter-2 gives literature survey of the current mode building blocks. In this chapter the basic building block Current conveyor is simulate and port relationship is verified.

In chapter-3 the wave equivalent of an inductor in a series branch, which is chosen to be the elementary building block, is realized using appropriately configured current conveyor blocks. The wave equivalents of the other reactive elements are also presented in this chapter, In order to evaluate the behaviour of the proposed filter configurations.

In chapter-4 the realization of wave active equivalent of passive elements is realized also a third-order filter transfer function is realized using CC based wave equivalents. The performance of the wave filter is evaluated using 0.18 micron TSMC CMOS technology parameters and simulation results are verified.

Chapter 5 shows the conclusion and discusses about future directions in this project.

Chapter-2

CURRENT MODE BUILDING BLOCKS

This chapter presents the survey of current mode building blocks available in various forms. Thereafter CMOS implementations and simulation for verifying the port relationships of current conveyor is discussed. These building blocks are used in later chapters for constructing wave active filters.

2.0 Introduction

The growth of analog IC design has been impeded by the process technologies that are mostly optimized for digital applications only. With the evolution of submicron technologies such as 0.18 micron and 0.13 micron, the supply voltages have been reduced to 3.3 Volts and lower. This makes it difficult to design a voltage mode CMOS circuits with high linearity and wide dynamic range. Recently, current mode circuits have become a viable alternative for future applications because of their inherent advantages over voltage mode circuits.

The main advantage of using current mode technique is because the non-linear characteristics exhibited by most field effect transistors. A small change in the input or controlling voltage results in a much larger change in the output current. Thus for a fixed supply voltage, the dynamic range of a current mode circuit is much larger than that of a voltage mode circuit. If a supply voltage is lowered, one can still get the required signals represented by the current.

A second advantage of current mode circuits is that they are much faster as compared to voltage mode circuits. The parasitic capacitances present in the analog circuits must be charged and discharged with the changing voltage levels. In a current mode circuit, a change in current level is not necessarily accompanied by a change in the voltage level. Hence, the parasitic capacitances will not affect the operating speed of the circuit by a significant amount.

Other advantages of using current mode circuits are that they do not require specially processed capacitors or resistors; they are more compatible with digital CMOS technology making integration of mixed signal circuits more feasible.

2.1 Current Conveyor

The current conveyor (CC) is the basic building block of a number of applications both in the current and voltage and the mixed modes. The principle of the current conveyor of the first generation was published in 1968 by K. C. Smith and A. S. Sedra [12]. Two years later, today's widely used second-generation CCII was described in [13], and in 1995 the third-generation CCIII [14]. However, initially, during that time, the current conveyor did not find many applications because its advantages compared to the classical operational amplifier (OpAmp) and were not widely appreciated. An IC Current Conveyor, namely PA630, was introduced by Wadsworth in 1989 (mass produced by Phototronics Ltd. of Canada) and about the same time, the now well known AD844 (operational transimpedance amplifier or more popularly known as a current feedback op-amp) was recognized to be internally a CCII+ followed by a voltage follower. An excellent review of the state-of-the-art of current-mode circuits prior to 1990 was provided by Wilson in [15]. Today, the current conveyor is considered a universal analog building block with wide spread applications in the current mode, voltage mode, and mixed mode signal processing. Its features find most applications in the current mode, when its so-called voltage input *y* is grounded and the current, flowing into the low-impedance input *x*, is copied by a simple current mirror into the *z* output.

Since 1995 in particular, we have witnessed many successive modifications and generalizations of the basic principle of CCII in order to use this circuit element more efficiently in various applications. A summary of the behavioral models of selected conveyors is presented here:

2.1.1First current conveyor: CCI

The current conveyor as initially introduced, is a 3-port device whose black-box representation is as shown in figure 2.1.

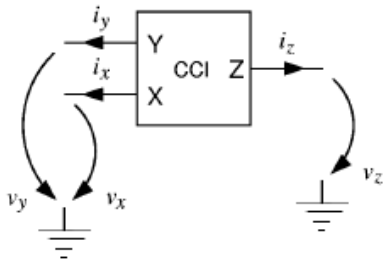


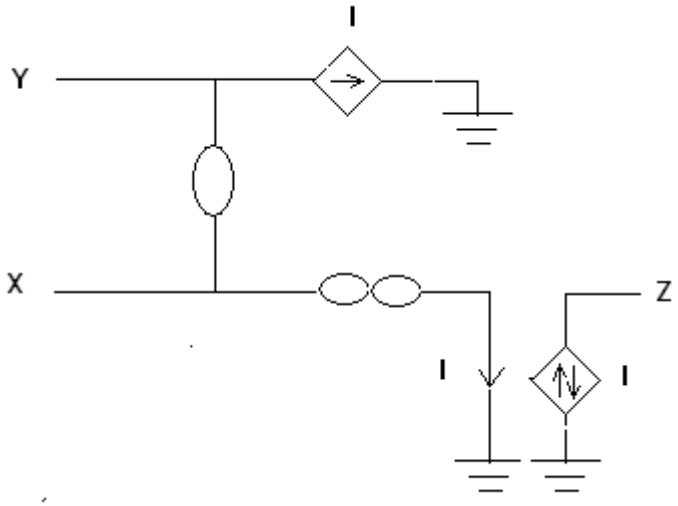
Fig. 2.1 Black box representation of current conveyor.

The operation of this device is such that if a voltage is applied to input terminal Y, an equal potential will appear on the input terminal X. In a similar fashion, an input current I being forced into terminal X will result into an equal amount of current flowing into terminal Y. As well as the current I will be conveyed to the output terminal Z such that terminal z has the characteristics of a current source, of value I, with high output impedance. As can be seen, the potential of X being set by that of Y, is independent of the current being forced into port X. Similarly, the current through input y, being fixed by that of X, is independent of the voltage applied at Y. Thus, the device exhibits a virtual short circuit input characteristics at port X and a dual virtual open-circuit input characteristics at port Y.

Mathematically, the input-output characteristics of CCI can be described by the following equation-

$$\begin{bmatrix} Iy \\ Vx \\ Iz \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} Vx \\ Ix \\ Vz \end{bmatrix}$$

Where the variables represent total instantaneous quantities. The + sign applies for the CCI in which both Iz and Ix flow into the conveyor and it is denoted by CCI+. The – sign applies for the opposite polarity case denoted by CCI-. To visualize the interaction of the port voltages



and currents described by the above matrix equations the nullator-norator representation as shown in Fig. 2.2 may be used-

Fig. 2.2 Nullator-Norator representation of CCI

In this figure, single ellipse is used to represent the nullator element and two intersecting ellipses to represent the norator element. The nullator element has constitutive equation V=0 and I=0 whereas the norator has an arbitrary current-voltage relationship. Clearly the nullator element is used to represent the virtual short circuit apparent between the X and Y terminals. Also included in the circuit are two dependent current sources. These are used to convey the current at port X to ports Y and Z.

Negative Impedance Converter:

An early application of CCI was its use as a negative impedance converter (NIC).

For this application terminal Z is grounded and the resistor to be converted is connected either between X and ground or between Y and ground. If resistor R is connected between X and ground, then looking into Y one sees a resistance –R that is short circuit stable. Alternatively if R is connected between Y and the ground then the input resistance at X is –R and is open circuit stable.

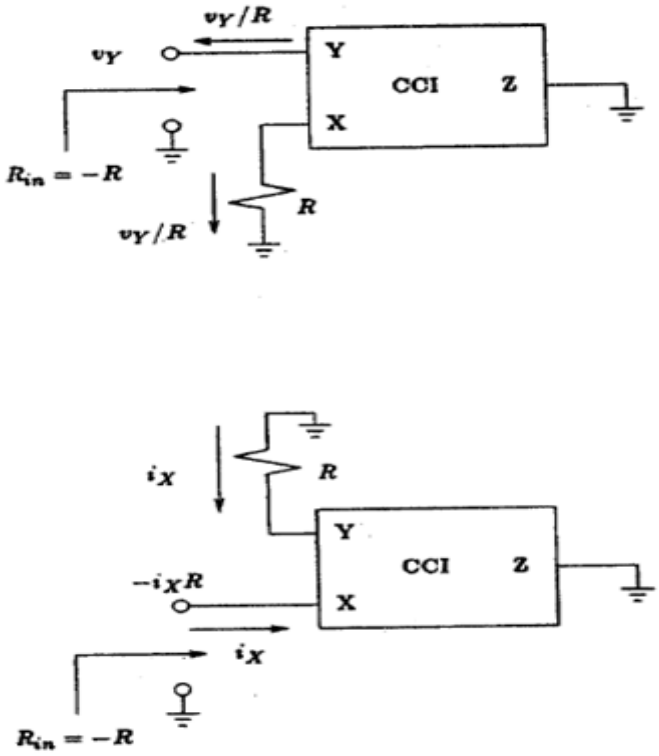


Figure 2.3 **CCI implementation of Negative Impedance Converter (NIC)**

A major problem that hindered the fabrication of the CCI in IC form in the 1960s is its use of high quality PnP devices. Since complimentary devices are available in CMOS technology, it is easy to fabricate a CMOS current conveyor.

2.1.2 The Second generation Current conveyor: CCII

To increase the versatility of current conveyor, a second version in which no current flows in terminal Y was introduced. This building block has since proven to be more useful than CCI. Utilizing the same block diagram representation of Fig. 2.1, CCII is described by-

$$\begin{bmatrix} Iy \\ Vx \\ Iz \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} Vx \\ Ix \\ Vz \end{bmatrix}$$

Thus, terminal Y exhibits an infinite input impedance. The voltage at X follows that applied to Y, thus X exhibits a zero input impedance. The current supplied to X is conveyed to the high impedance output terminal Z where it is supplied with either positive polarity (in CCII+) or negative polarity (in CCII-). In terms of nullor the port behavior of the second generation current conveyor (positive or negative) can be depicted as shown in Fig. 3.1.

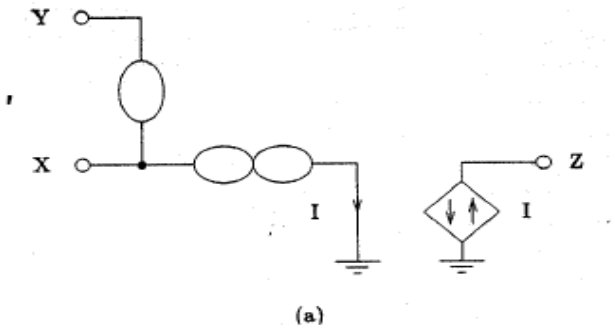


Figure 2.4 **Nullator-Norator representation of a CCII**

The similarity and difference between CCI and CCII are clearly evident from their equivalent circuits. In the case of a CCII-, the dependent current source is redundant, current flowing into terminal X must flow out of terminal Z. Hence the equivalent circuit of CCII- can be represented with a single nullor element as shown in Fig. 3.2.

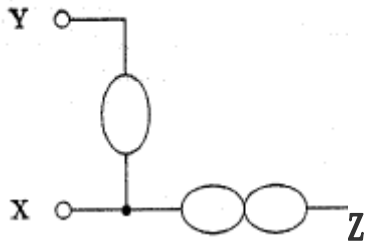


Figure 2.5 **A simplified representation of CCII-**

The first widely recognized applications of CCII were in realization of controlled sources, impedance converters, impedance inverters, gyrators, and various analog computation devices.

2.1.3 The Third Generation Current conveyor: CCIII

This structure was published by Fabre in 1995. Structurally it is quiet similar to CCI with the exception that the current in port X and Y flow in opposite directions. It is represented by push-pull topology built from four simple CCIs. Its main application is Current measurement.

Utilizing the same block diagram representation of Fig. 2.1, CCIII is described by-

$$\begin{bmatrix} Iy \\ Vx \\ Iz \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} Vx \\ Ix \\ Vz \end{bmatrix}$$

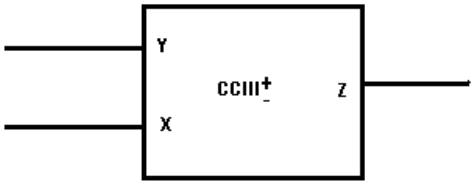
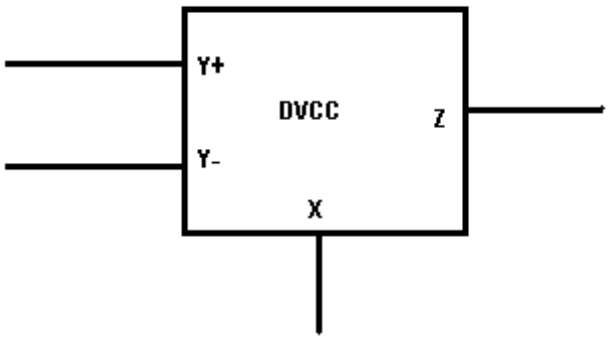
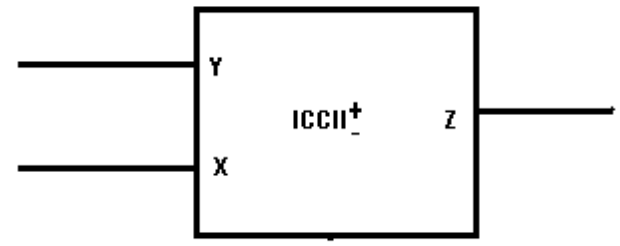
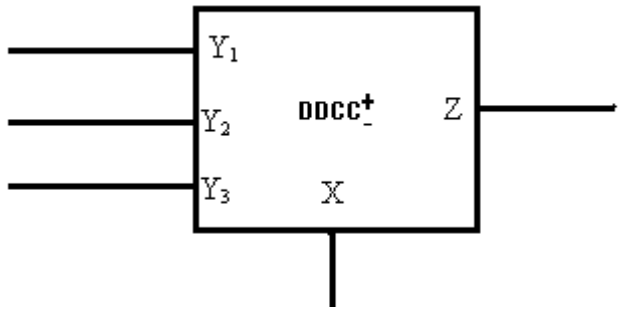
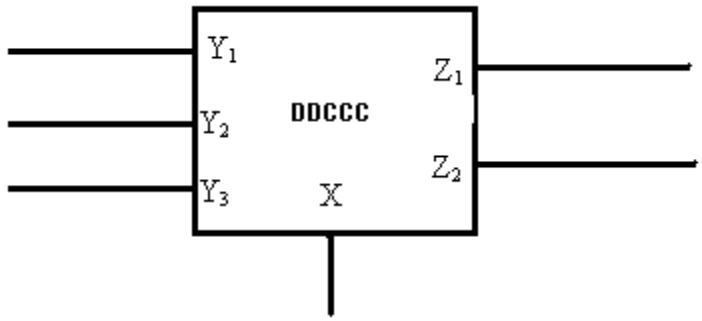
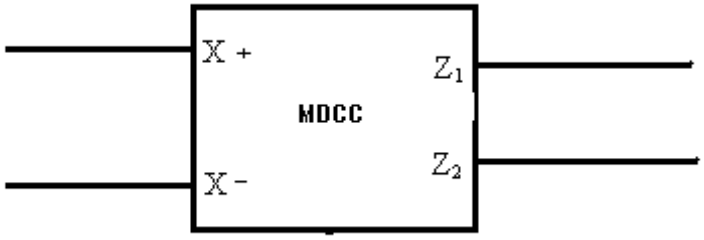


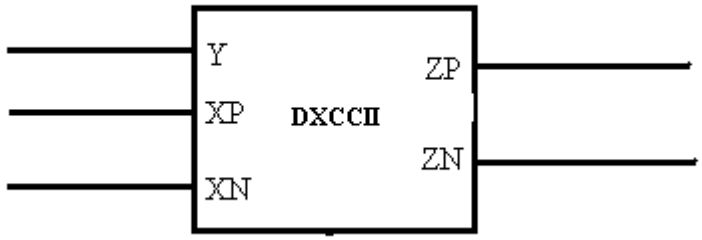
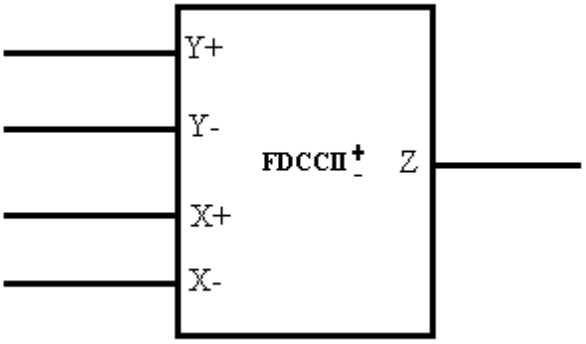
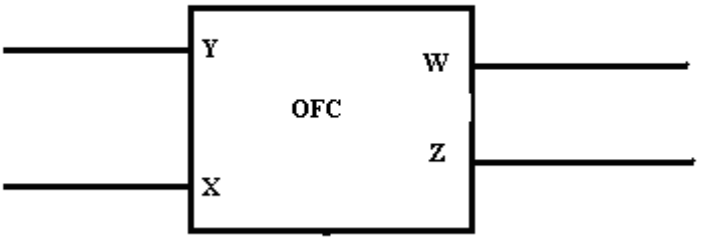
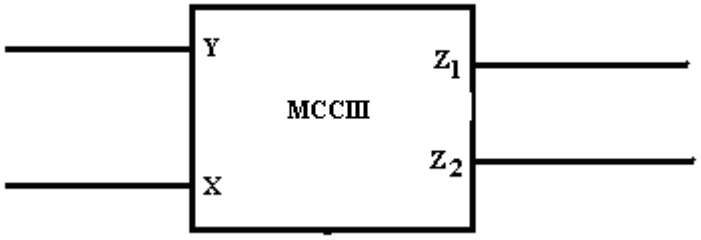
Figure 2.5(b) Block diagram representation

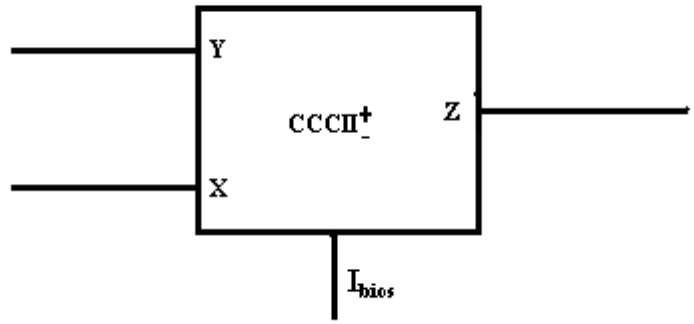
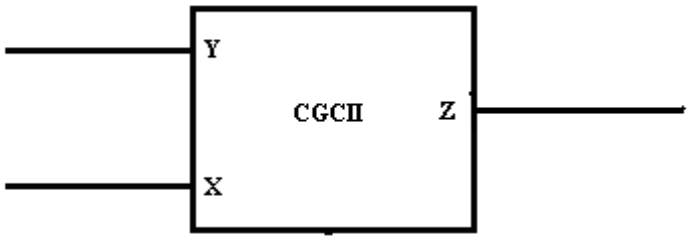
A summary of the behavioral models of selected conveyors. Some basic blocks and their port relationships of Current Conveyor derivatives are presented here.

Table 1: Basic block and port relationship of Current Conveyor derivatives

	Differential Voltage Current Conveyor $I_{Y+} = I_{Y-} = 0$ $V_X = V_{Y+} - V_{Y-}$ $I_Z = I_X$

	Inverting Current Conveyor II $I_Y = 0$ $V_X = -V_Y$ $I_Z = \pm I_X$
	Differential Difference Current Conveyor $I_{Y1} = I_{Y2} = I_{Y3} = 0$ $I_X = V_{Y1} - V_{Y2} + V_{Y3}$ $I_Z = \pm I_X$
	Differential Difference Current Controlled Conveyor $I_{Y1} = I_{Y2} = I_{Y3} = 0$ $I_X = V_{Y1} - V_{Y2} + V_{Y3}$ $I_{Z1} = I_X$ $I_{Z2} = -I_X$
	Differential Current Conveyor II $I_Y = 0$ $V_{X+} = V_{X-} = V_Y$ $I_{Z1} = -I_{Z2} = I_{X+} - I_{X-}$
	Modified Differential Current Conveyor $V_{X+} = V_{X-} = 0$ $I_{Z1} = -I_{Z2} = I_{X+} - I_{X-}$

	Dual-X Current Conveyor $I_Y = 0$ $V_{XP} = -V_{XN} = V_Y$ $I_{ZP} = I_{XP}$ $I_{ZN} = I_{XN}$
	Fully Differential Current Conveyor II $I_{Y+} = I_{Y-} = 0$ $V_{X+} = V_{X-} = V_{Y+} - V_{Y-}$ $I_Z = \pm(I_{X+} - I_{X-})$
	Operational Floating Conveyor $I_Y = 0$ $V_X = V_Y$ $V_W = Z_T I_X$ $I_Z = -I_W$
	Modified Current Conveyor III $I_Y = I_X$ $V_Y = V_X$ $I_{Z1} = -2I_X$ $I_{Z2} = I_X$

	Current Controlled Conveyor III $I_Y = 0$ $I_Z = \pm I_X$
	Current Gain conveyor $I_Y = 0$ $V_X = V_Y$ $I_Z = AI_X$

The demand for a multiple-output current conveyor led to the DO-CCII (Dual-Output CCII), which provides currents Iz of both directions, thus combining both the positive and the negative CCII in a single device [16]. If both currents are of the same polarity, the conveyors are of the CFCCIIp or CFCCIIn types (Current Follower CCII), where the symbol *p* or *n* means positive or negative current conveyor [17]. Another generalization is represented by the so-called DVCC (Differential Voltage Current Conveyor) [18], in which the original "voltage" input y is split into a pair of inputs y1 and y2. The voltage of the x terminal is then given by the voltage difference of the voltage inputs. This offers more freedom during the design of voltage- and mixed-mode applications.

DVCC with the complementary pair of z1 and z2 terminals is known as DVCCC (Differential Voltage Complementary CC) [21]. As a special case of DVCC for y1 grounded, the ICCII (Inverting CCII) is described in [19]. On the contrary, DDCC (Differential Difference CCII) [20] is an extension of DVCC: Voltage at the x terminal is given by a combination of voltages at three terminals y1, y2, and y3. Splitting the z terminal of DDCC into a pair of z terminals with currents Iz = Ix yields DDCCC (Differential Difference Complementary CC) [21]. Another generalization of the classical CCII is DCC (Differential

Current Conveyor) [22], in which the x input is replaced by the pair of x1 and x2. The current through the z terminal is given by the difference of currents through the x1 and x2 terminals. MDCC (Modified Differential Current Conveyor) [22] is a simplification of DCC on the assumption that signal (voltage) at the y terminal is zero.

In [23], Zeki and Toker proposed the Dual-X Second-Generation Current Conveyor (DXCCII) which is a combination of CCII and ICCII. Instead of a single xterminal, DXCCII has two terminals xp and xn as outputs of non-inverting and inverting unity-gain amplifiers with their inputs connected to y terminal. Copies of xp and xn terminal currents are provided at zp and zn terminals.

FDCCII (Fully Differential CCII) [24] is an important generalization of the conventional CCII. The x, y, and z terminals occur here in pairs. The basic circuit equations of the CCII are now valid for differences of voltages or currents which correspond to these pairs. FDCCII is thus designed for applications with fully differential architecture for fast signal processing. In [25], this type of conveyor is called FBCCII (Fully Balanced CCII).

The so-called modified CCII (MCCII) is published in [26]. Its special internal structure provides such an operation that the current through the z terminal does not depend on the direction of current Ix, i.e. Iz = abs (Ix). This feature can be used with advantage to implement economically full-wave rectifiers [27]. Joining two current conveyors CCII- yields the so-called Operational Floating Conveyor (OFC) [30]. OFC is a universal differential-input differential-output building block, enabling current-, voltage-, and mixed-mode applications. An extreme embodiment of universality is the so-called UCC (Universal Current Conveyor) [28]. By means of this element, one can implement all the above types of current conveyor. However, such universality is at the cost of non-optimal parameters for a concrete application.

A modification of the third-generation current conveyor is described in [29]. The so-called MCCIII (Modified CCIII) is equipped with a couple of z1 and z2 terminals. Currents through these terminals are of opposite directions and the following equalities hold: $Iz_1 = -2Ix$, $Iz_2 = Ix$. Unequal values of the currents enable the design of interesting applications [30].

The non-zero x-terminal impedance is an important parasitic parameter of the current conveyor, which negatively affects its behavior, particularly in filtering applications. However, this phenomenon is paradoxically utilized in a new type of conveyor, namely CCCII (Current Controlled Conveyor) [31-32], where the resistance of x terminal is controlled electronically via the bias current. It can be shown that this active device can be

used in filters whose parameters may be controlled electronically. Such a feature has been inherent in the so-called g_mC filters, i.e. filters, compounded only of OTAs and capacitors.

Another method for controlling electronically the parameters of applications employing current conveyors is based on conveyors with variable current gain Iz/Ix. In [33], such a conveyor is identified by the abbreviation CGCCII (Current Gain CCII). The current conveyor of such a type, concretely CCII-, was formerly manufactured by Élantec under the code EL2717. The variable gain is implemented via transforming current Iz into voltage by means of resistors, and via back transformation of voltage into current by means of electronically gm-controlled OTA. The most recent solution is characterized by digital control of the gain, utilizing the so-called CDN (Current Division Network) and DCCF (Digitally Controlled Current Follower).

2.2 Realization of Current Conveyor (CCII)

Several generations of current conveyors have been defined over the years**.** Undoubtedly, the second generation conveyor (CCII) is the more well known of the device. The demand for a multiple-output current conveyor led to the DO-CCII (Dual-Output CCII), which provides currents *Iz* of both directions, thus combining both the positive and the negative CCII in a single device. If both currents are of the same polarity, the conveyors are of the CCII+ or CCII- types

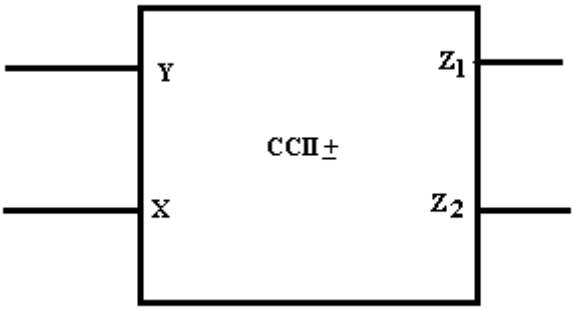


Figure 2.6 Block diagram of CCII

Using standard notation, the terminal relations of a CCII can be characterized by

$$\begin{bmatrix} V_x \\ I_y \\ I_z \end{bmatrix} = \begin{bmatrix} \beta & 0 & 0 \\ 0 & 0 & 0 \\ 0 & \pm\alpha & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix}$$

where $\alpha = 1 - \epsilon_i$ and $\beta = 1 - \epsilon_v$,$|\epsilon_i| << 1$ and $|\epsilon_i| << 1$ represent the current and voltage tracking errors, respectively. where the subscripts *x*, *y***,** and *z* refer to the terminals labeled X, Y and Z in fig1 The CCII is defined in both a positive and a negative version where the +sign in the matrix is used for the CCII+ type conveyor and the –sign is used for the CCII- type conveyor.

2.3.1 CMOS realization of CCII+

The DO-CCII has been simulated using the CMOS structure of figure 2.7 with DC supply voltage equal to $\pm$1.8V and bias currents equal to $I_{1,2}$ = 80µa. All MOS transistors are operated in saturation region. The simulations are based on .18µm TSMC CMOS technology.

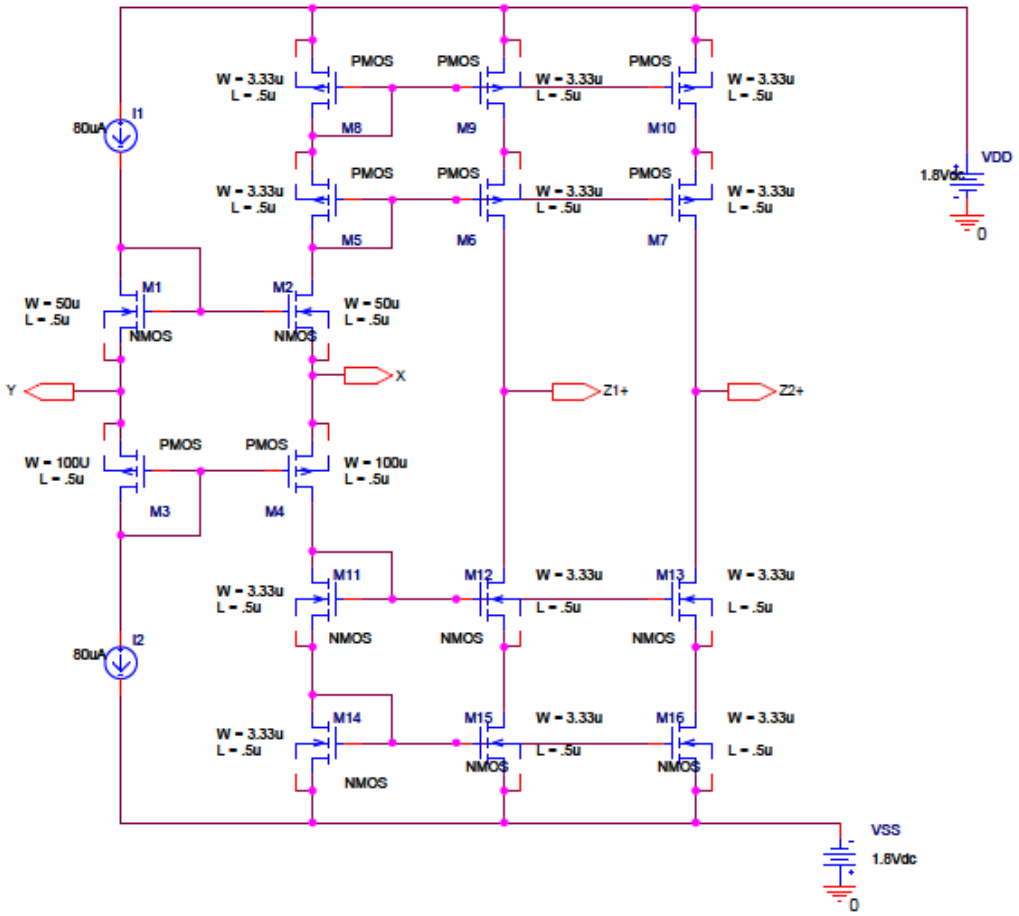


Figure 2.7 CMOS structure of CCII+

In order to demonstrate the port relations of the current conveyor, computer simulations are performed using CMOS based CCII schematic given in fig.3, a pulse input of 200mv connected to Y port and other ports e. g. X, Z_1, Z_2 are terminated by resistances R_1, R_2 and R_3 each having a value of 1KΩ. The simulation results for $V_x = V_y$, $I_z = I_x$ are shown in Fig. 2.9. Figure 2.10. shows current conveyor used as a unity gain amplifier and results (frequency response) are shown in fig 2.11.

2.3.2 Simulation Results

The port relationship of current conveyor is verified and 3dB frequency for current and voltage transfers are 131MHz and 127MHz respectively.

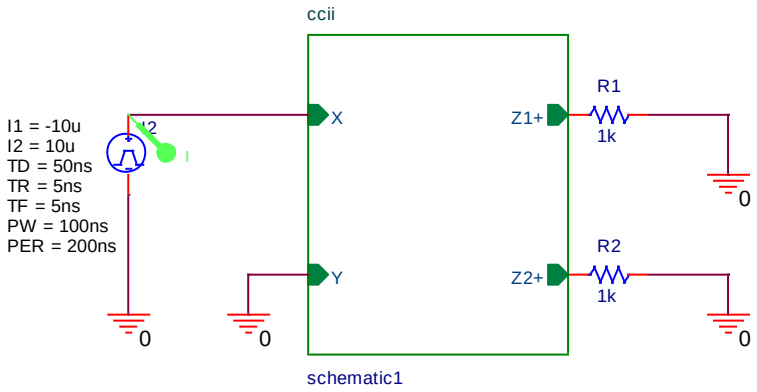


Figure 2.8. Current Conveyor II

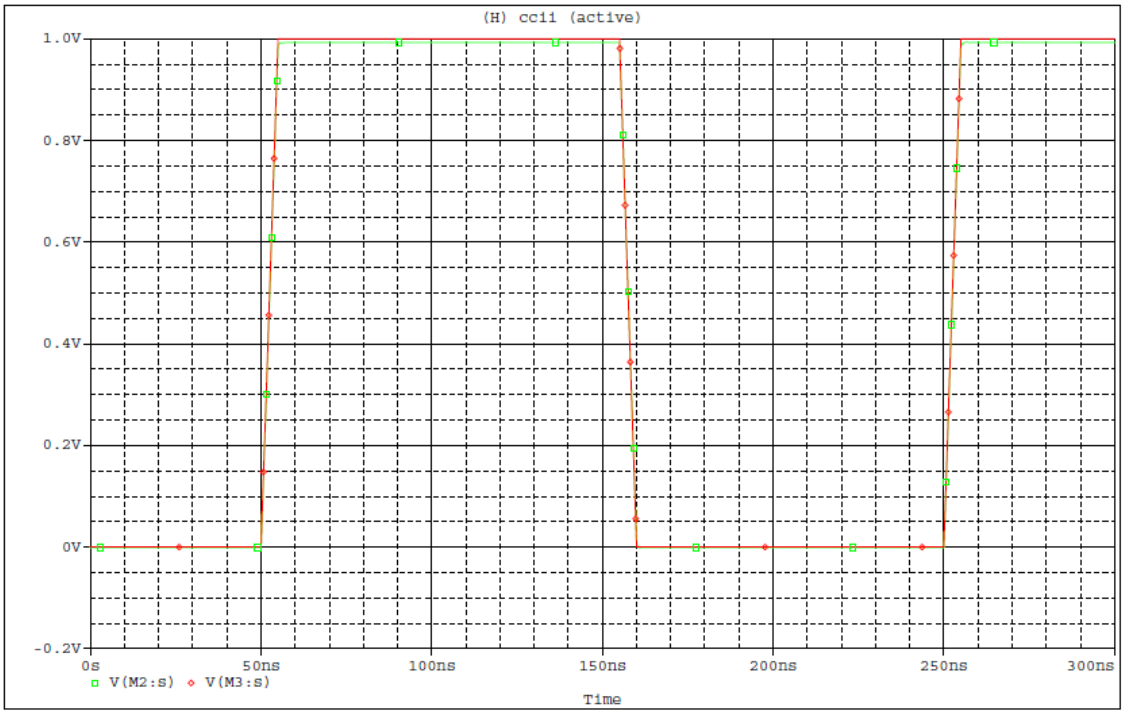


Figure 2.9 (a). Simulated port relationship of CCII $V_x = V_y$

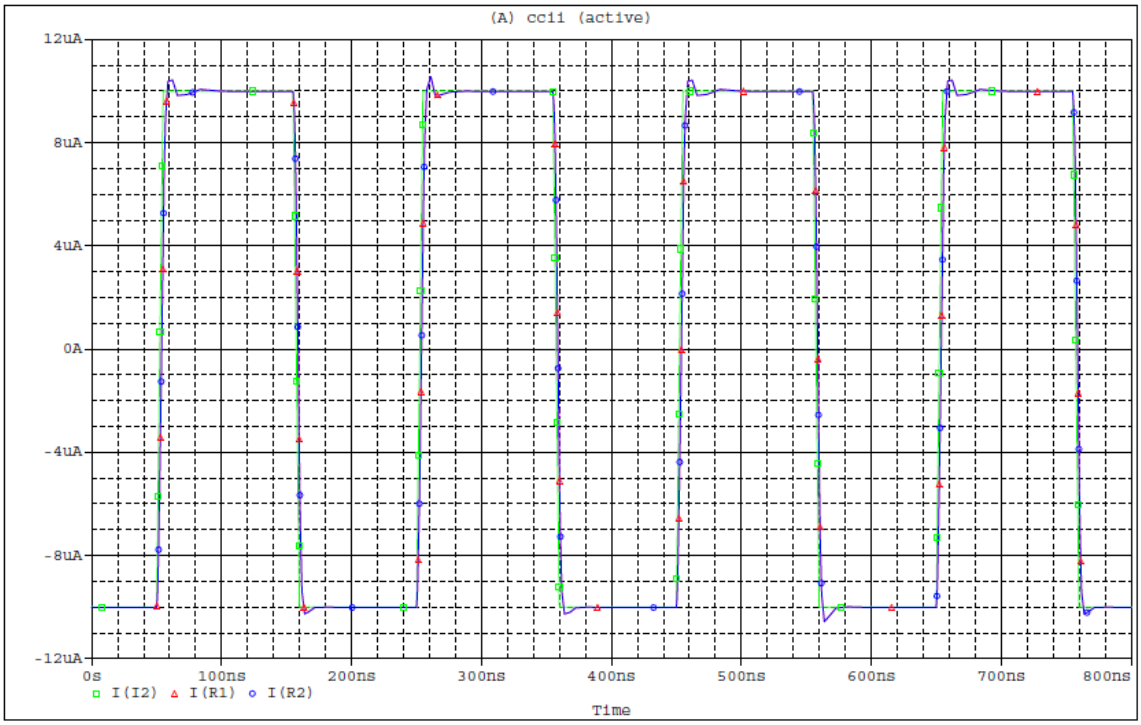


Figure 2.9(b). Simulated port relationship of CCII $I_x = I_{z1} = I_{z2}$

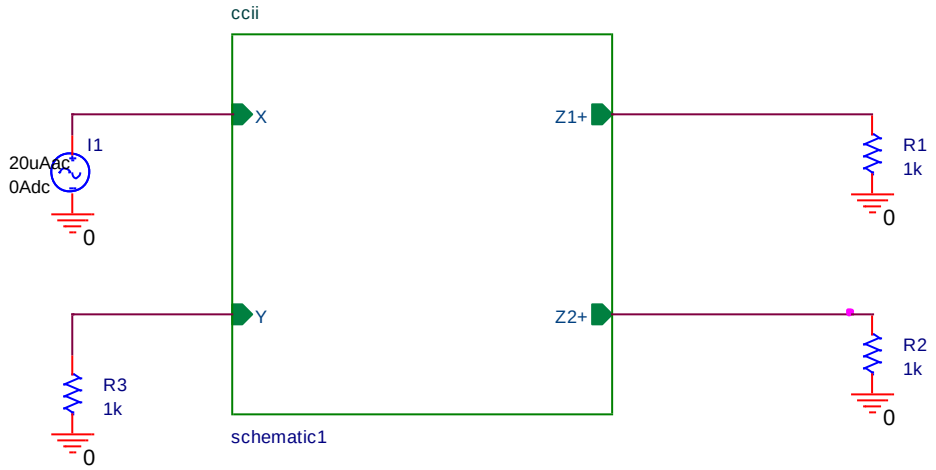


Figure 2.10 Realization of CCII in AC analysis

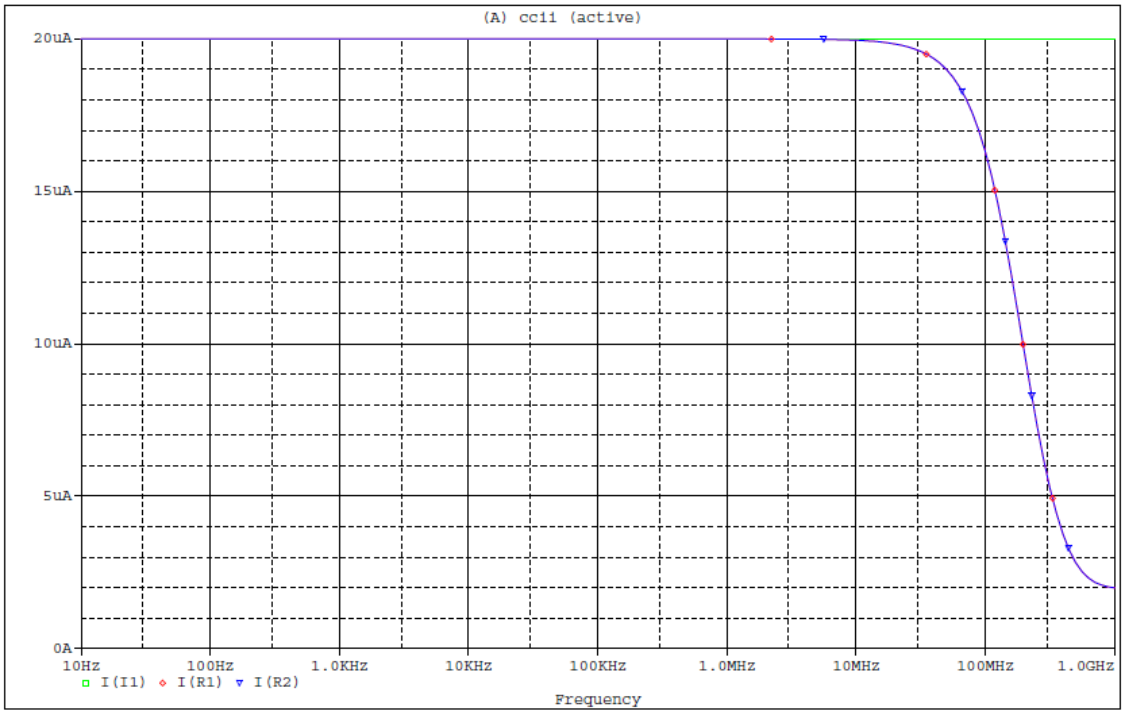


Figure 2.11 Frequency response of ccii

Chapter-3

WAVE ACTIVE FILTER

3.0 Introduction

Wave active filter (WAF) design is an alternative approach to the simulation of resistively terminated LC ladder filter.

An alternative systematic design procedure for emulating the topology of the corresponding LC ladder prototype is the well-known wave method. According to this method, the corresponding passive prototype filter is split into two-port sub networks, which are fully described using the wave variables, defined as incident and reflected waves. One way for obtaining the wave equivalents of the two-port sub networks is by using the scattering parameters matrix description. By choosing an inductor in a series branch as the elementary building block, its wave equivalent includes an appropriately configured lossy integrator. The wave equivalents of the other passive elements are derived by interchanging the terminals of the appropriate wave signals and/or adding current inverters. Thus, the essential difference between the leapfrog and the wave method is that leapfrog type circuits rely on lossless integrators, whereas wave filters rely only on lossy integrators. Absolute losslessness is not possible in practice, so the implementation of wave circuits in integrated form seems to be more realistic.

A current amplifier-based configuration for obtaining the wave equivalents of passive elements of the corresponding prototype filters is introduced in this report.

The achieved benefits are as follows:

1) The design procedure of high-order filters is much easier, in comparison to the leapfrog filters; this is due to the fact that the mathematical relationships related to the SFG representation are avoided in this case.
2) Modular filter topologies are derived, as the equivalents of the other reactive elements are readily obtained from the equivalent of the elementary building block, and

3) Only a grounded capacitor is used for obtaining the wave equivalents of the passive elements, instead of the floating capacitor and two matched floating resistors that are employed in the topological simulation of passive prototypes.

3.1 Wave Active Filter

As already mentioned, our approach to the synthesis of RC-active networks is based on the use of wave quantities rather than voltage-current quantities, hence the scattering matrix will play an important role in our concept. Usually, if scattering parameters are being used, as e.g., in microwave theory, they are derived for power waves; we could adopt this concept for our aim, too, but the use of voltage or current waves seems more convenient for our approach, since it leads sometimes to simpler circuits and, in addition, it simplifies the notation. For the approach presented in this report, we have decided to use voltage waves, which shall be introduced now.

Consider the two-port N shown in Fig. 3.1, where the A1, A2 and B1, B2 denote the incident and reflected voltage waves, respectively. To either port we assign a port resistance (characteristic resistance) R1 and R2 respectively; the port resistances are assumed to be real positive constants.

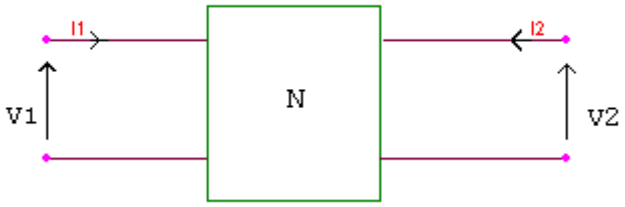


Figure 3.1 An elementary two port Network N

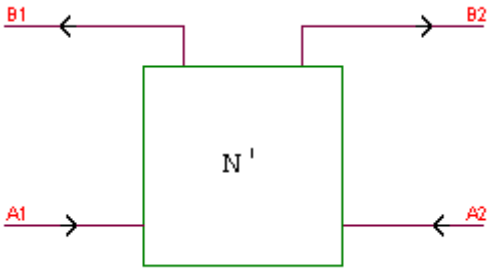


Figure 3.2 Incident wave A_1, A_2 and Reflected waves B_1, B_2 for two port network N'

If we use the following definitions

$$V = \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \; I = \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

$$A = \begin{bmatrix} A_1 \\ A_2 \end{bmatrix} \; B = \begin{bmatrix} B_1 \\ B_2 \end{bmatrix}$$

$$R = \begin{bmatrix} R_1 & 0 \\ 0 & R_2 \end{bmatrix}$$

.....(1)

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} = [A] \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \quad \text{.....(2)}$$

The principle of the method is based on the voltage wave formulation for 2-port networks, for which the respective incident and reflected wave quantities may expressed

$$A_i = I_i + \frac{V_i}{R_i} \qquad i = 1,2$$

$$B_i = I_i - \frac{V_i}{R_i} \qquad i = 1,2$$

.....(3)

In equation (3) variables A_i, $i = 1,2$ are considered to be the incident wave signal, while B_i the reflected wave signal. R_i, $i = 1,2$ are the port resistances or characteristic resistance assigned at each port. This transformation can be represented by the wave equivalent two-port in fig. 3.2.

Representation of scattering matrix in terms of incidence and reflected wave signals,

$$\boldsymbol{B = SA}$$

$$\begin{bmatrix} B_1 \\ B_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} A_1 \\ A_2 \end{bmatrix}$$

.....(4)

S_{ij} , $i, j = 1,2$ are the scattering parameters, which take the following values.

$$s_{11} = \frac{(a_{11} - a_{21}R_1 - a_{12}G_2 + a_{22}R_1G_2)}{\Delta}$$

$$s_{12} = \frac{R_1 G_2}{\Delta}$$

$$s_{21} = \frac{1}{\Delta}$$

$$s_{22} = \frac{(a_{11} + a_{21} R_1 + a_{12} G_2 + a_{22} R_1 G_2)}{\Delta}$$

$$\Delta = a_{11} + a_{21} R_1 - a_{12} G_2 - a_{22} R_1 G_2$$

$$G_2 = \frac{1}{R_2}$$

.....(5)

Since the aim of the procedure is the realization of ladder filters, we need only consider subnetworks for eqn. (2), which are either impedances in the series arms or admittances in the shunt arms. From these subnetworks, we can derive the overall ladder by suitable interconnections.

For a series-arm impedance Z and a parallel-arm admittance Y, we have, in terms of the modified transmission matrix description, the following:

$$\begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix}_Z = \begin{bmatrix} 1 & -Z \\ 0 & -1 \end{bmatrix}$$

$$\begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix}_Y = \begin{bmatrix} 1 & 0 \\ Y & -1 \end{bmatrix}$$

.....(6)

Substituting in eqs. (5) and subsequently in Eqs. (4) we get the following equations relating the wave variables for the two cases:

Series arm Z Shunt arm Y

$$s_{11} = \frac{R_2 - R_1 + Z}{R_2 + R_1 + Z} \qquad s_{11} = \frac{G_1 - G_2 - Y}{G_2 + G_1 + Y}$$

$$s_{12} = \frac{2R_1}{R_2 + R_1 + Z} \qquad s_{12} = \frac{2G_2}{G_2 + G_1 + Y}$$

$$s_{21} = \frac{2R_2}{R_2 + R_1 + Z} \qquad s_{21} = \frac{2G_1}{G_2 + G_1 + Y}$$

$$s_{22} = \frac{R_1 - R_2 + Z}{R_2 + R_1 + Z} \qquad s_{22} = \frac{G_2 - G_1 - Y}{G_2 + G_1 + Y}$$

$$\begin{bmatrix} B_1 \\ B_2 \end{bmatrix} = \begin{bmatrix} \frac{R_2 - R_1 + Z}{R_2 + R_1 + Z} & \frac{2R_1}{R_2 + R_1 + Z} \\ \frac{2R_2}{R_2 + R_1 + Z} & \frac{R_1 - R_2 + Z}{R_2 + R_1 + Z} \end{bmatrix} \begin{bmatrix} A_1 \\ A_2 \end{bmatrix}$$

.....(8)

and

$$\begin{bmatrix} B_1 \\ B_2 \end{bmatrix} = \begin{bmatrix} \frac{G_1 - G_2 - Y}{G_2 + G_1 + Y} & \frac{2G_2}{G_2 + G_1 + Y} \\ \frac{2G_1}{G_2 + G_1 + Y} & \frac{G_2 - G_1 - Y}{G_2 + G_1 + Y} \end{bmatrix} \begin{bmatrix} A_1 \\ A_2 \end{bmatrix}$$

.....(9)

with $G_i = \frac{1}{R_i}$

We shall restrict the port resistances to be equal, i.e. $R_1 = R_2 = R$, and hence we shall have

series arm Z

$$B_1 = \frac{Z}{2R + Z} A_1 + \frac{2R}{2R + Z} A_2$$

$$B_2 = \frac{2R}{2R + Z} A_1 + \frac{Z}{2R + Z} A_2$$

.....(10 (a))

shunt arm Y

$$B_1 = -\frac{Y}{2G+Y}A_1 + \frac{2G}{2G+Y}$$

$$B_2 = \frac{2G}{2G+Y}A_1 - \frac{Y}{2G+Y}A_2$$

.....(10 (b))

The basis of the proposed method relies on the interpretation of the relationships of eqn. 10 as follows:

We note that the reflected waves arise as linear combinations of incident waves. For example, in the series-arm impedance, we see that $B_1$is formed by linearly combining A_1 and A_2, and the constants of such a linear combination are themselves transfer ratios of the form $\frac{Z}{2R+Z}$ or $\frac{2R}{2R+Z}$. Thus, we no longer treat the incident voltage waves as waves, but rather as voltages impressed on an appropriate RC active network conceived so that the reflected voltage waves appear as voltages resulting from such an excitation across some other pairs of terminals. By this means, the relationships can be satisfied.

An attractive building block for designing current mode active filter is the current conveyor which is designed using current conveyor in chapter 2.

3.2 Current Conveyor Based Wave Filter

Using the preceding definitions, the wave description of an inductor in the series branch is given, in terms of the scattering parameters, by the following

Matrix relationship:

$$\begin{bmatrix} B_1 \\ B_2 \end{bmatrix} = \frac{1}{1+\tau.s}\begin{bmatrix} \tau.s & 1 \\ 1 & \tau.s \end{bmatrix}\begin{bmatrix} A_1 \\ A_2 \end{bmatrix}$$

.....(11)

where τ is a time constant defined as τ = L/2R. [49]

Eqn.(11) can be equivalently rewritten as follows:

$$B_1 = A_1 - \frac{1}{1+\tau.s}(A_1 - A_2)$$

.....(12)

$$B_2 = A_1 + \frac{1}{1+\tau.s}(A_1 - A_2) \quad \text{.....(13)}$$

A functional block diagram (FBD) that corresponds to equations (12) and (13) is given in Figure 3.3. This is constructed from unity gain multiple output current conveyors. A typical

current conveyor configuration is shown in Figure3.4. Note that cascade current mirrors are used, in order to improve the accuracy of the currents transfer.. The realized time constant is given by $\tau = \frac{\hat{C}}{g_m}$, by comparing this expression of the time constant with that previously given (τ = L/2R), it is derived that the capacitor value in the active realization (Figure 3.3) should be calculated according to the formula $\hat{C} = \frac{g_m L}{2R}$. Where g_m is the transconductance parameter of MOS transistor with aspect ratio W/L, biased at a dc current Io, is given by the following expression:

$$g_m = \sqrt{2K\frac{W}{L}}\sqrt{I_0} \qquad \text{.....(14)}$$

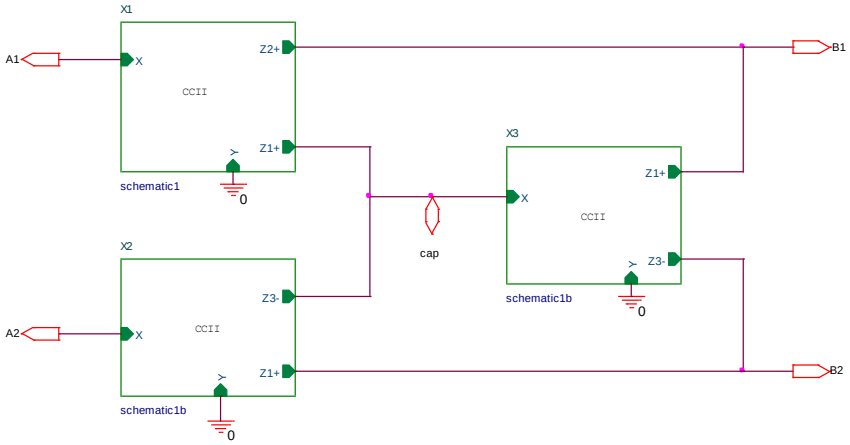


Figure 3.3 Functional Block Diagram of equation (12), equation (13)

Where K is the current gain factor of the MOS transistor. From equation (14) it is obvious that the frequency response of the derived filter topologies could be electronically adjusted by the dc current Io.

Value of gm is derived using simulations of current conveyor. This is 1/313Ω

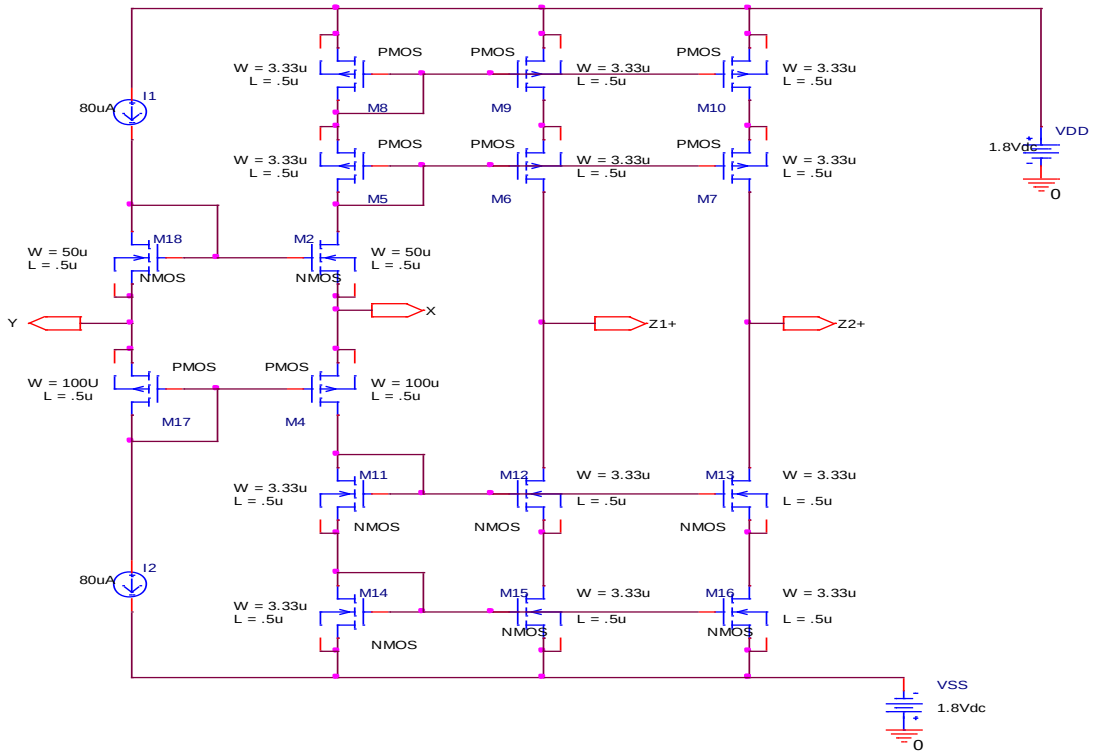
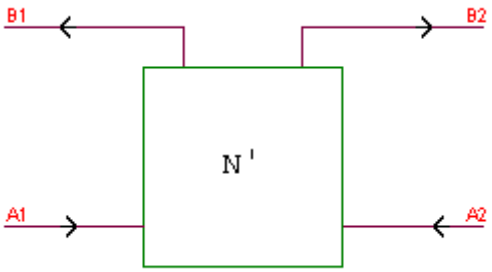


Figure 3.4 current conveyor configuration

Chapter-4

REALIZATION OF WAVE ACTIVE FILTER

In this chapter, the realization of wave active filter is discussed in detail. First the realization of wave active filter elementary building blocks equivalent to respective passive type two port configuration like floating L, floating C, LC series and LC parallel configurations, also grounded type configuration is realize thereafter the realization of 3rd Order lowpass filter is simulate using 0.18 micron TSMC CMOS technology parameter.



4.1 Realization of wave filter elementary building blocks

In this section we realize all the basic passive elements of two port subnetwork in series or shunt branch (floating / grounded) form with respective wave active equivalent.

4.1.1 Wave equivalent of two port sub network in series (floating) branch

a) Inductor in series fashion

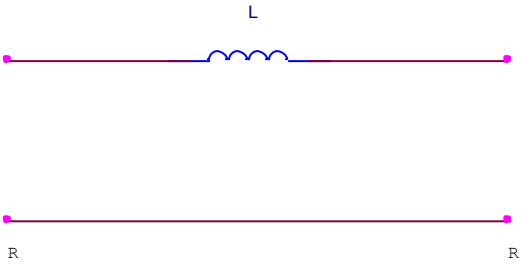


Fig 4.1(a): Two port L subnetwork

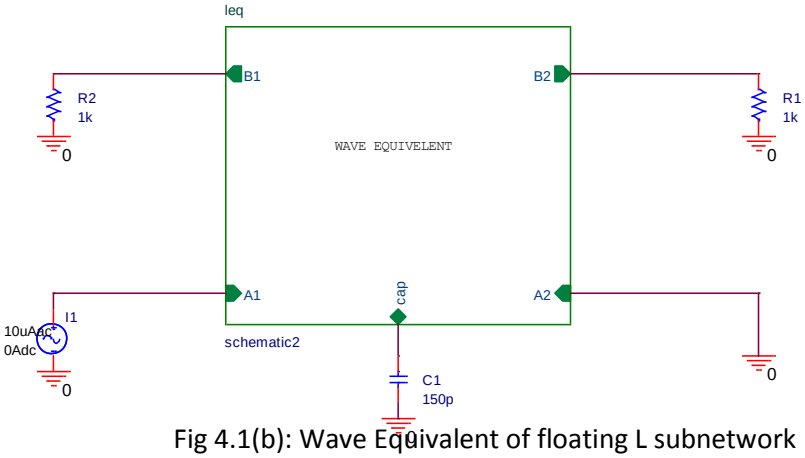


Fig 4.1(b): Wave Equivalent of floating L subnetwork

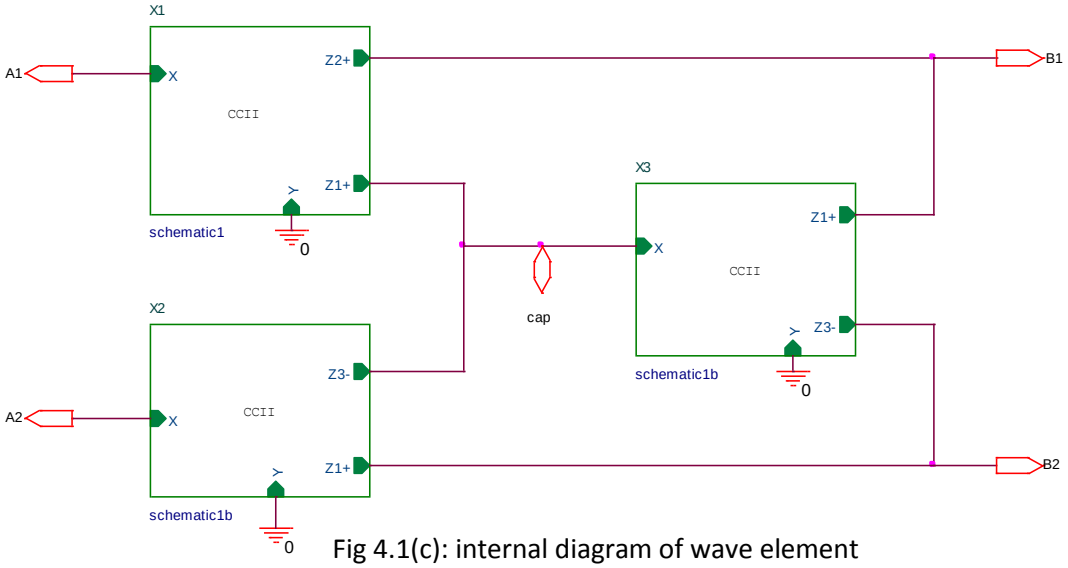


Fig 4.1(c): internal diagram of wave element

Figure 4.1: Realization circuit of floating inductor

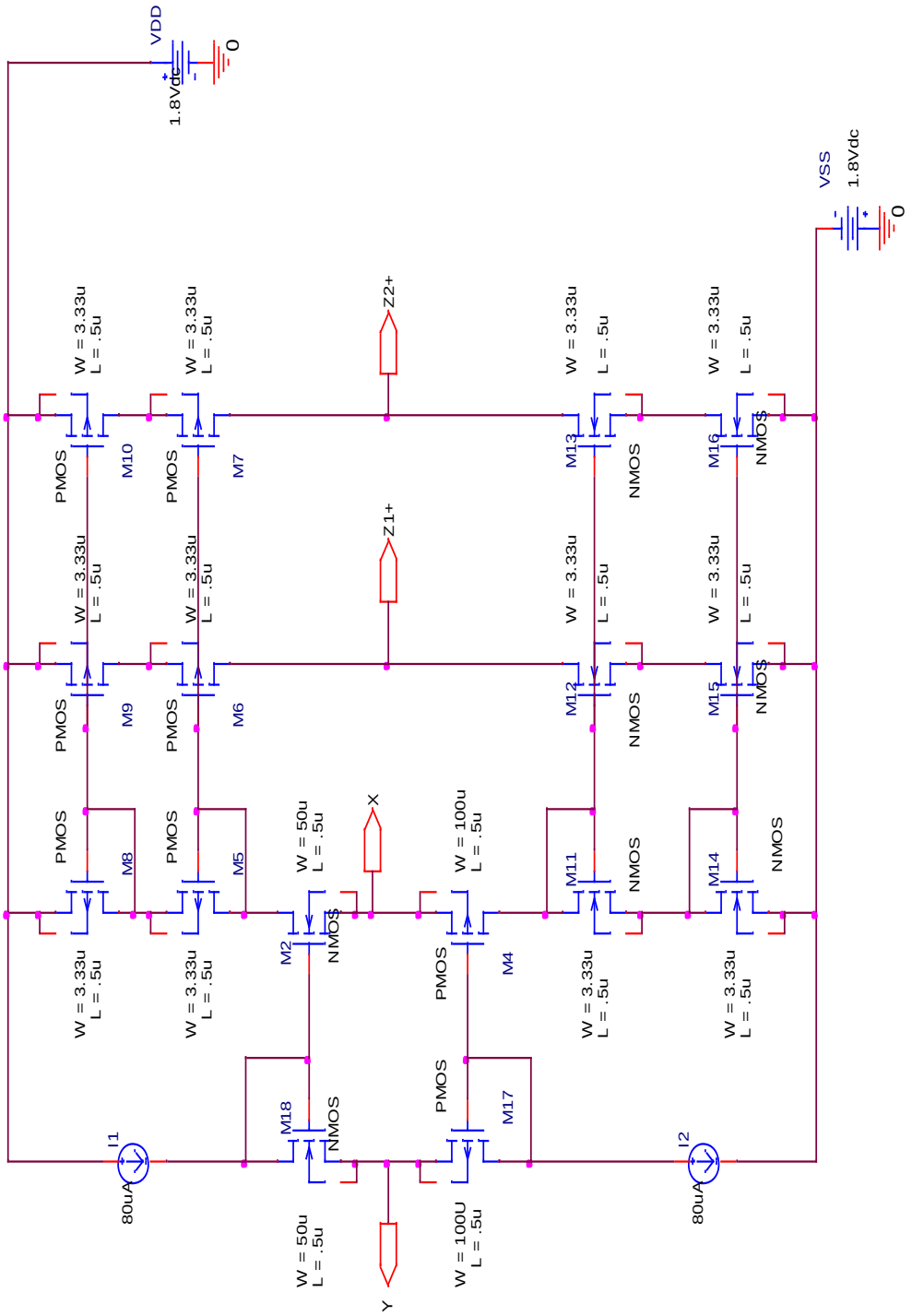


Figure 4.2 Internal circuit of CCII++ block shown in fig 4.1(c)

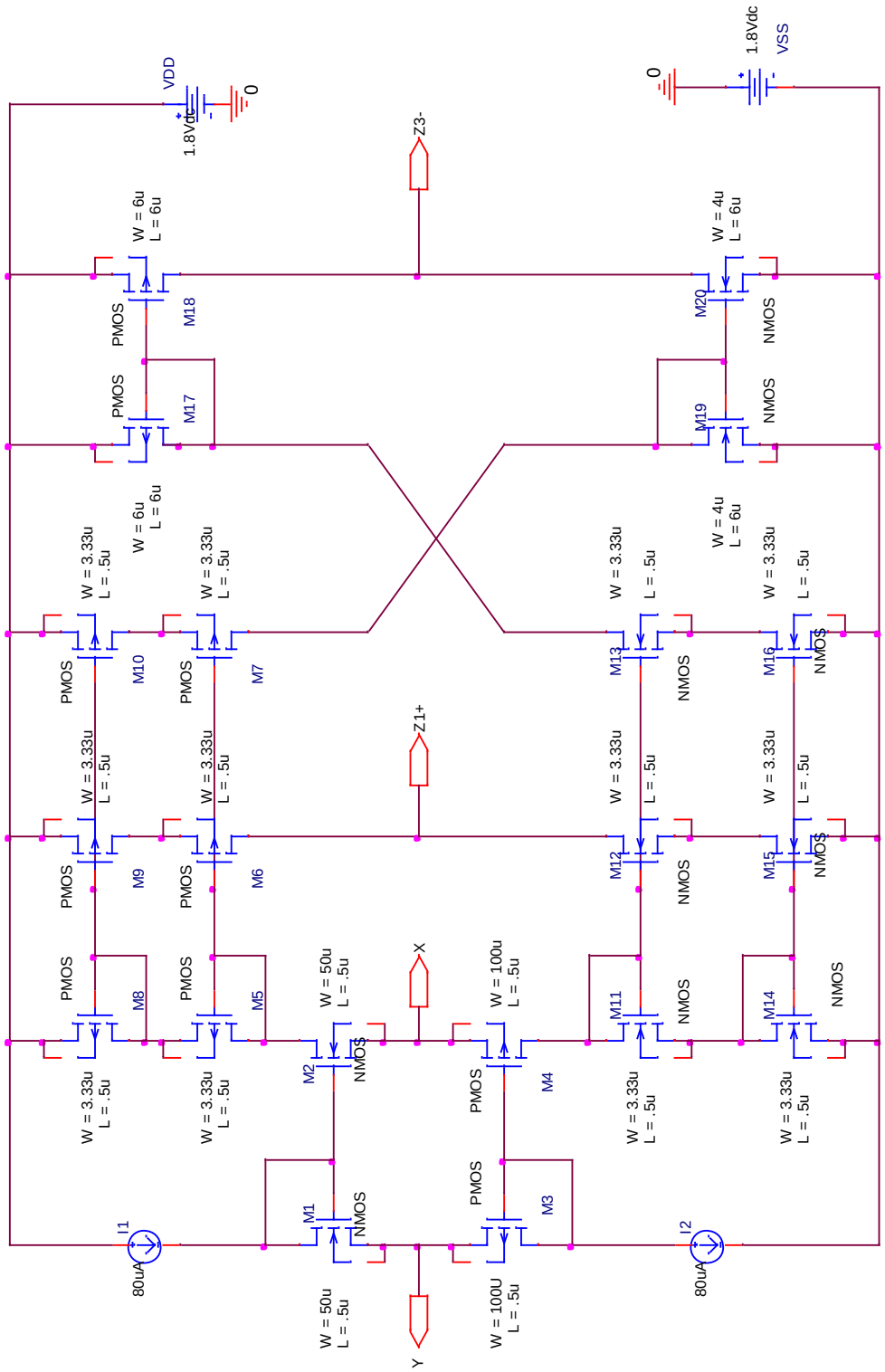


Figure 4.3 Internal circuit of CCII+- block shown in fig 4.1(c)

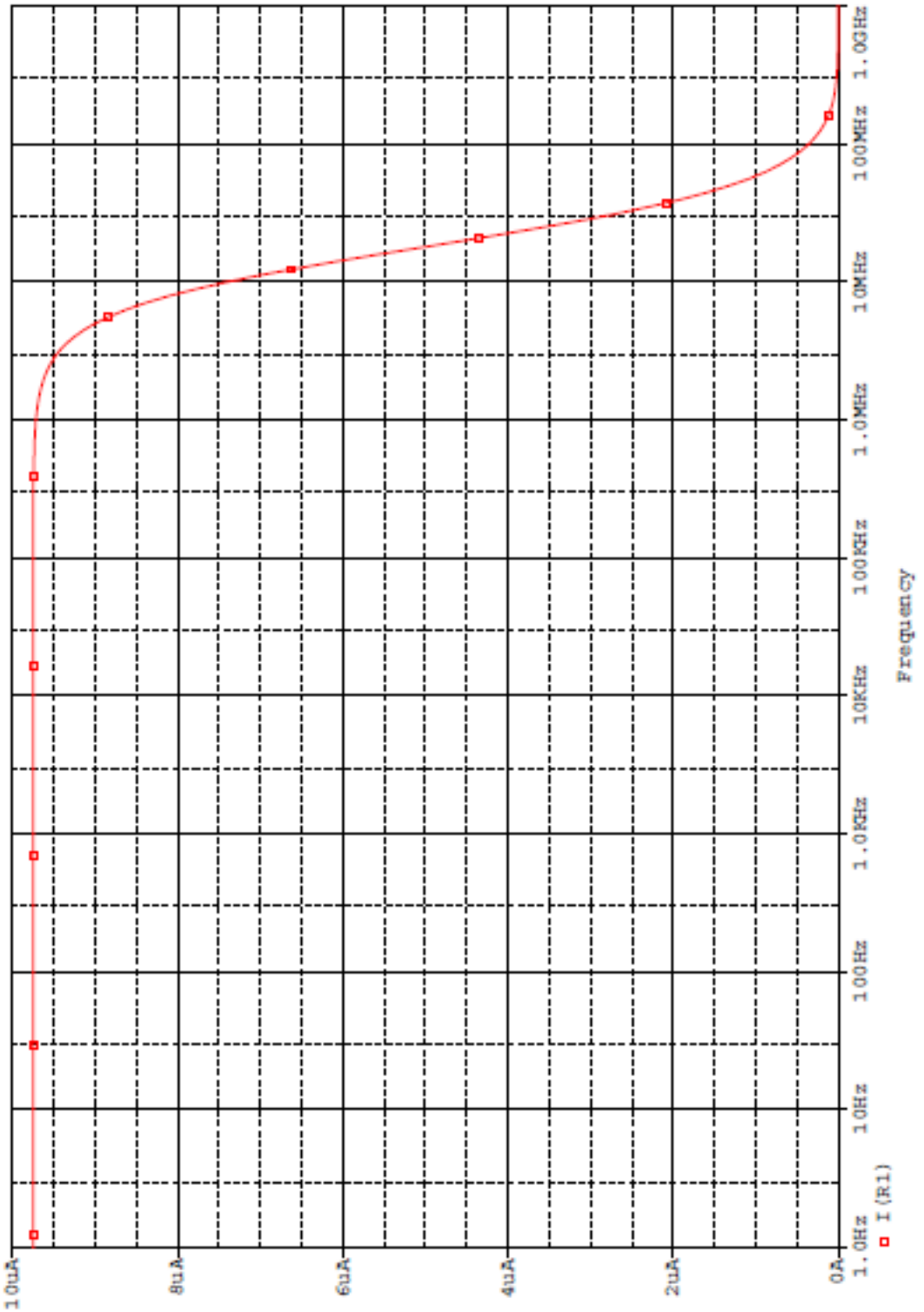


Figure 4.4 Simulation Result of floating inductor

b) Capacitor in series fashion

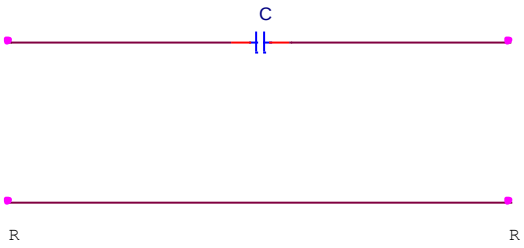


Fig 4.5(a): Two port C subnetwork

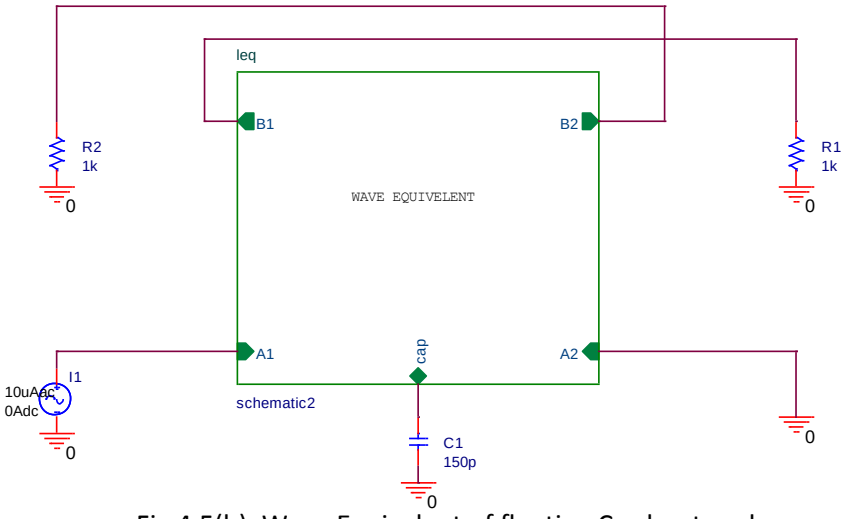


Fig 4.5(b): Wave Equivalent of floating C subnetwork

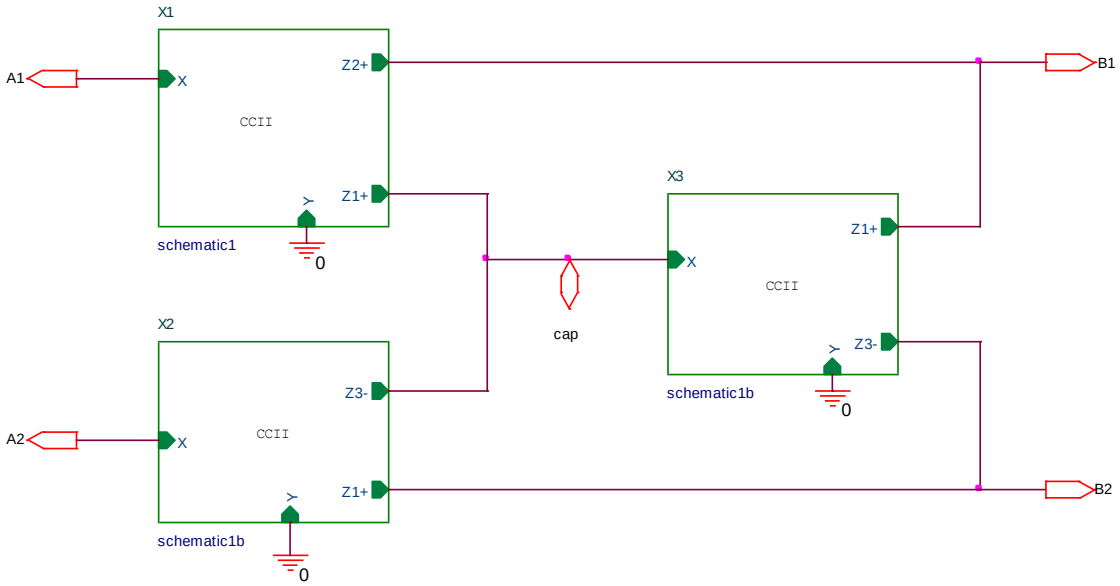


Fig 4.5(c): internal diagram of wave element

Figure 4.5 Realization circuit of floating capacitor

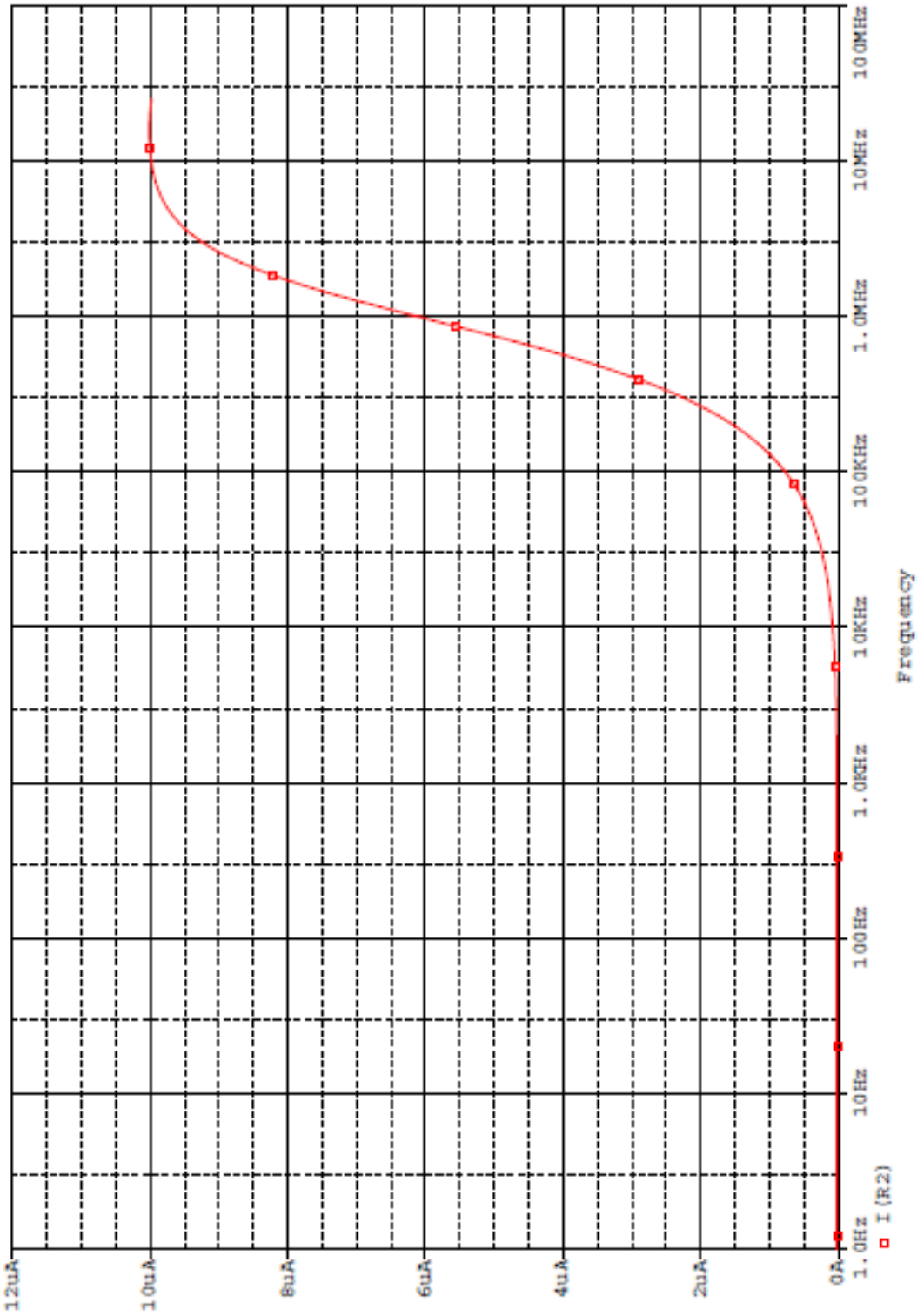


Figure 4.6 Simulation Result of floating Capacitor

c) LC series in floating fashion

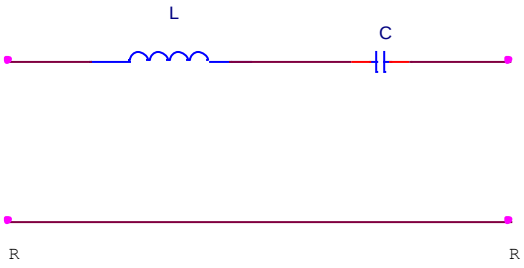


Fig 4.7(a) : Two port LC series

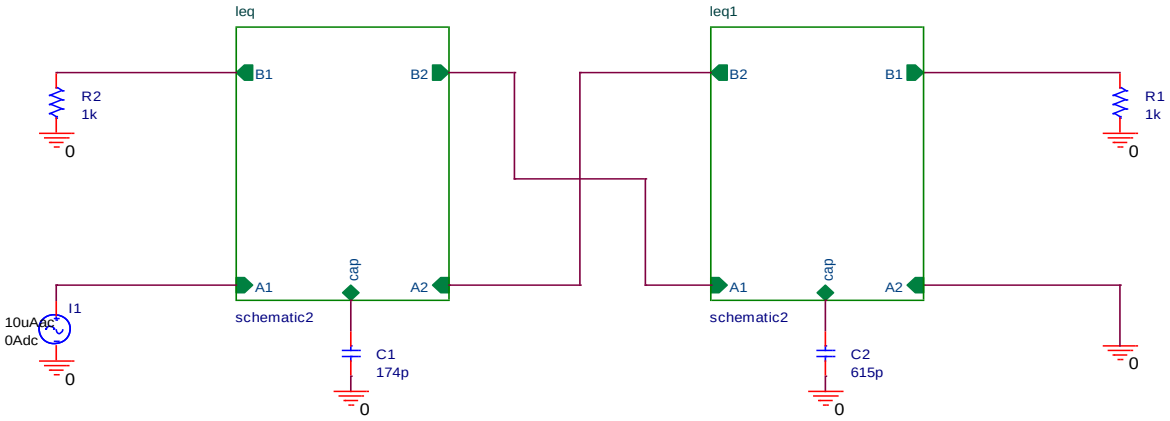


Fig 4.7(b): Wave Equivalent of floating LC series subnetwork

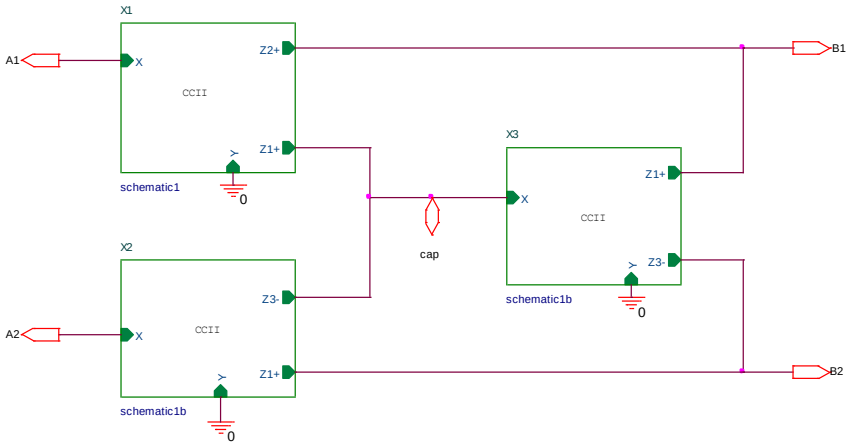


Fig 4.7(c): internal diagram of wave element

Figure 4.7 Realization circuit of floating LC series

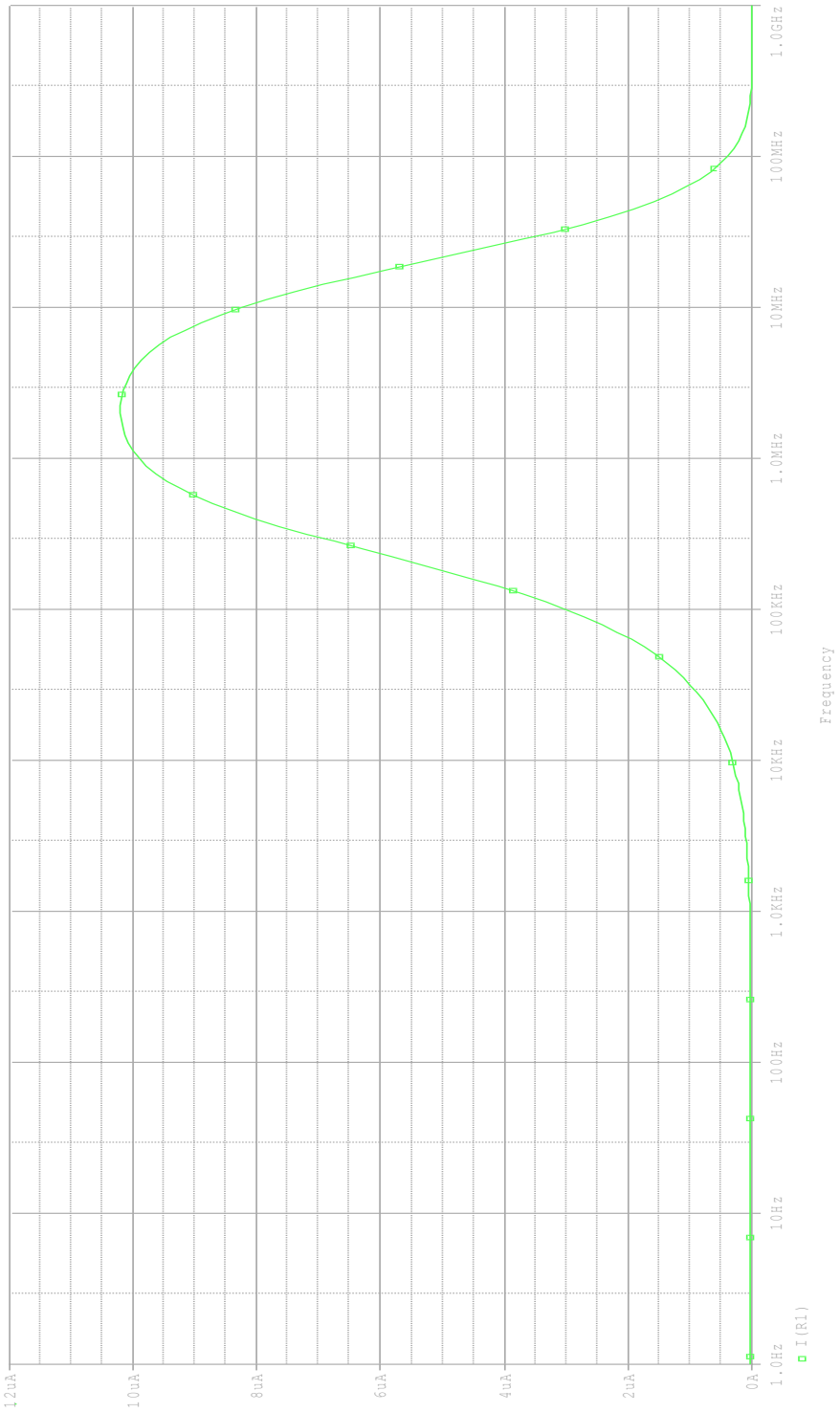


Figure 4.8 Simulation Result of floating LC series

d) LC parallel in floating fashion

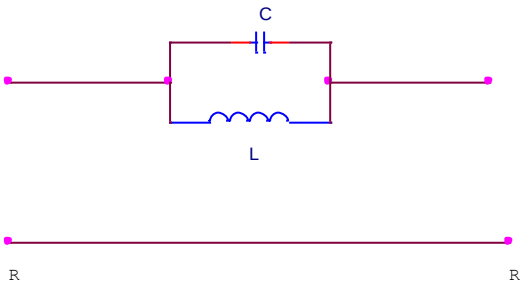


Fig 4.9(a) : Two port LC parallel

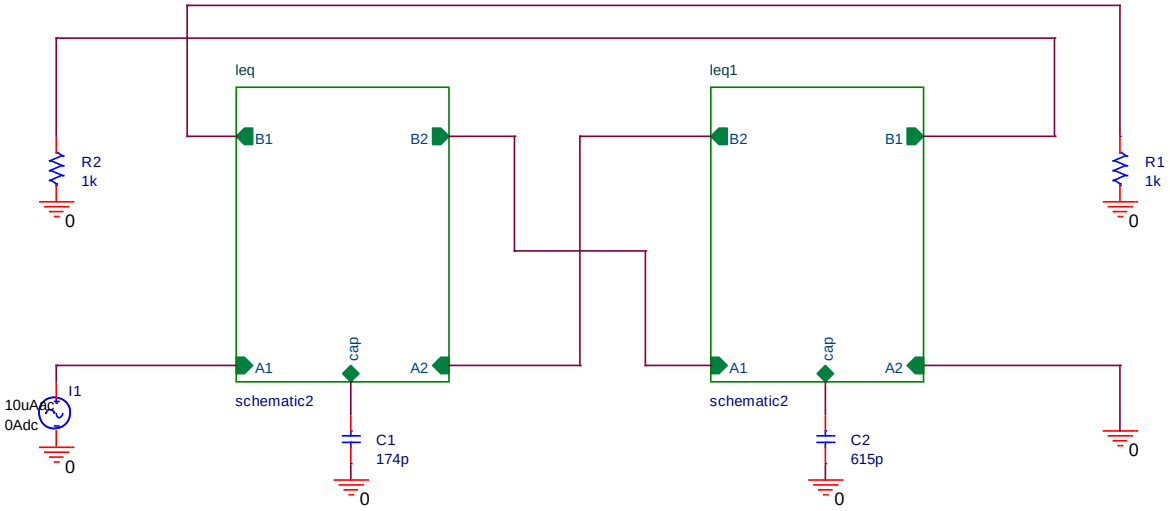


Fig 4.9(b): Wave Equivalent of floating LC parallel subnetwork

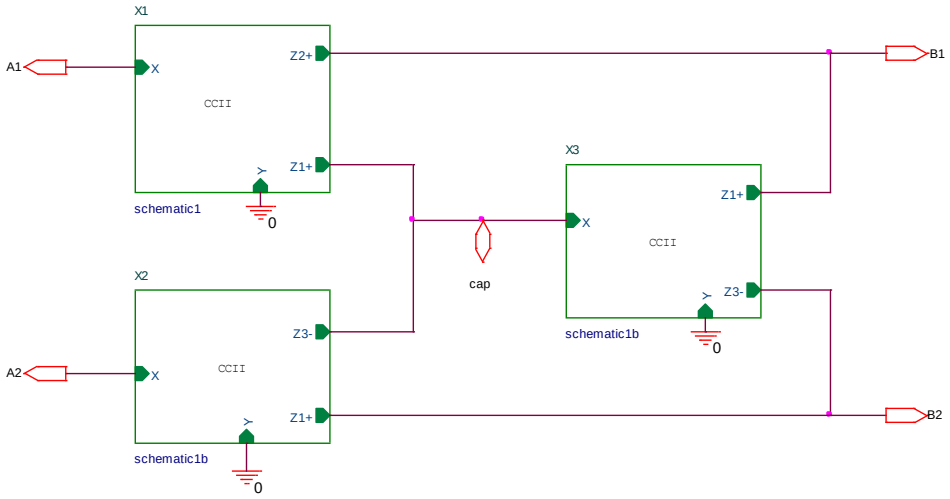


Fig 4.9(c): internal diagram of wave element

Figure 4.9 Realization circuit of floating LC parallel configuration

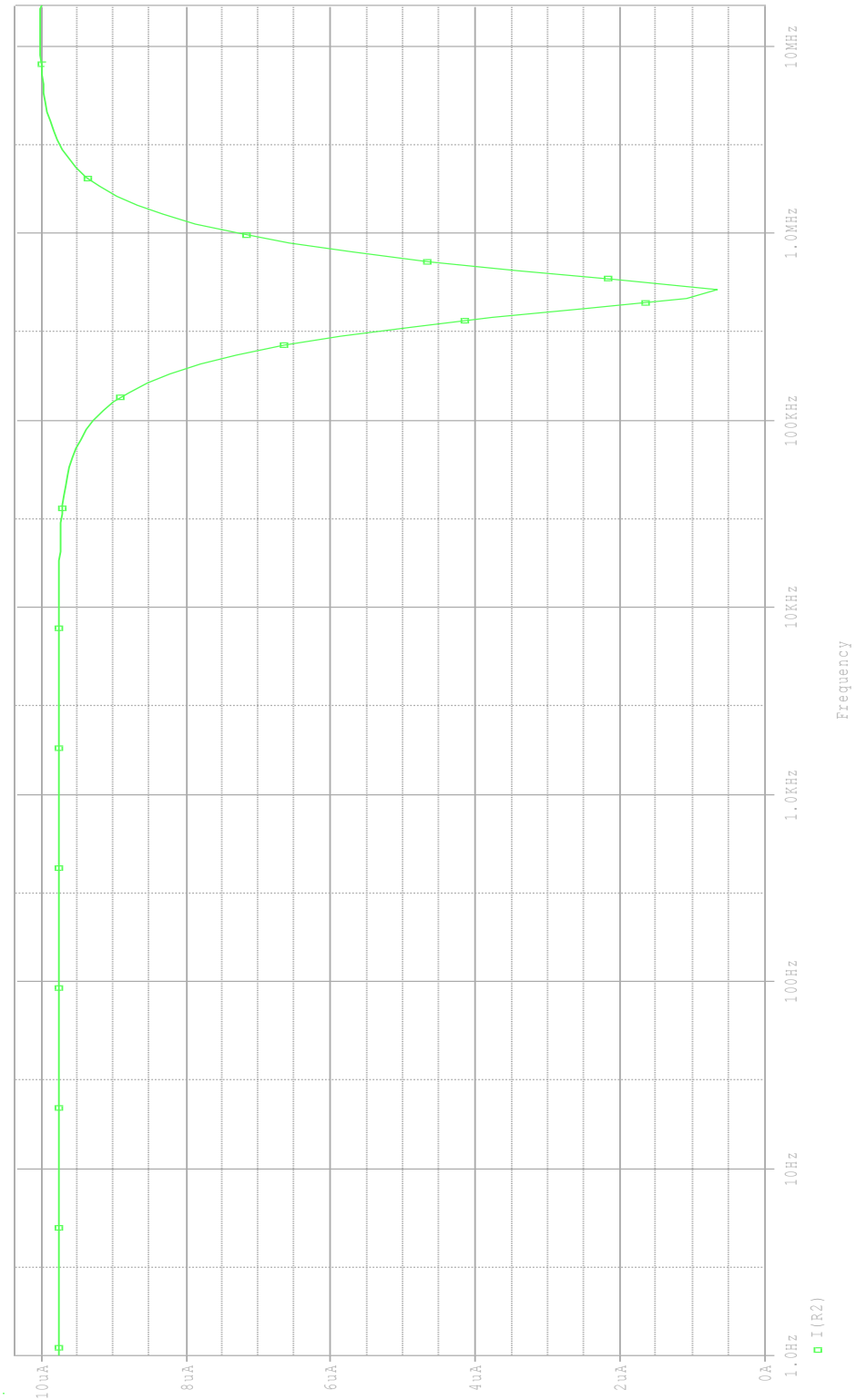


Figure 4.10 Simulation Result of floating LC parallel configuration

4.1.2 Wave equivalent of two-port sub network in shunt (grounded) branch

a) Capacitor in grounded fashion

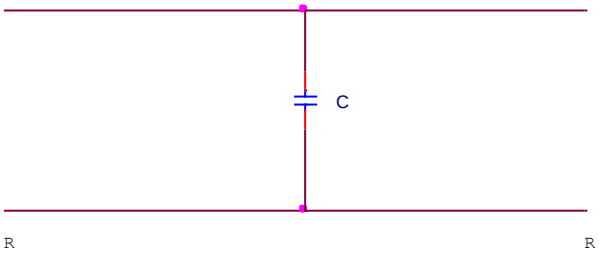


Fig 4. 11(a) : Two port grounded C

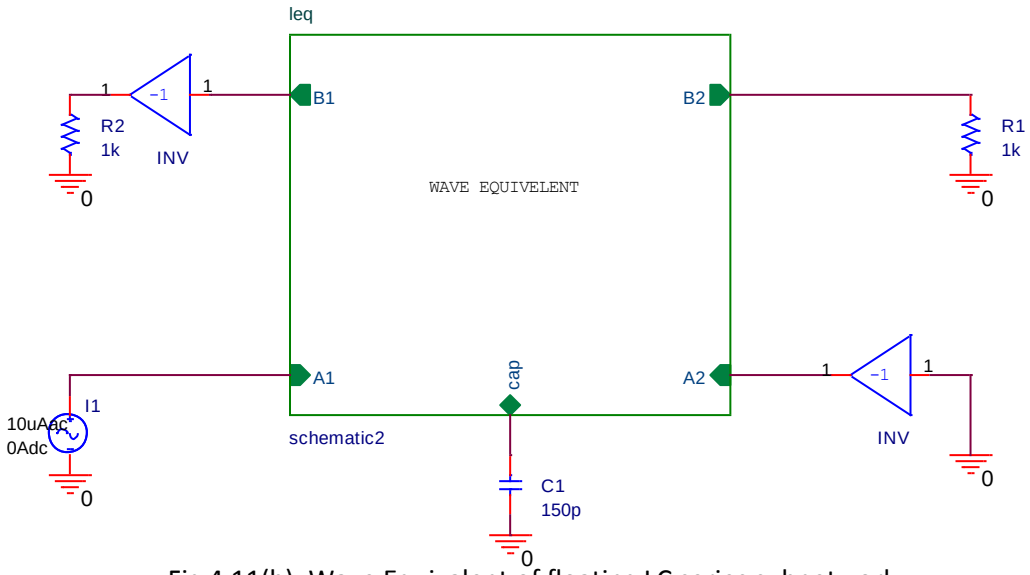


Fig 4.11(b): Wave Equivalent of floating LC series subnetwork

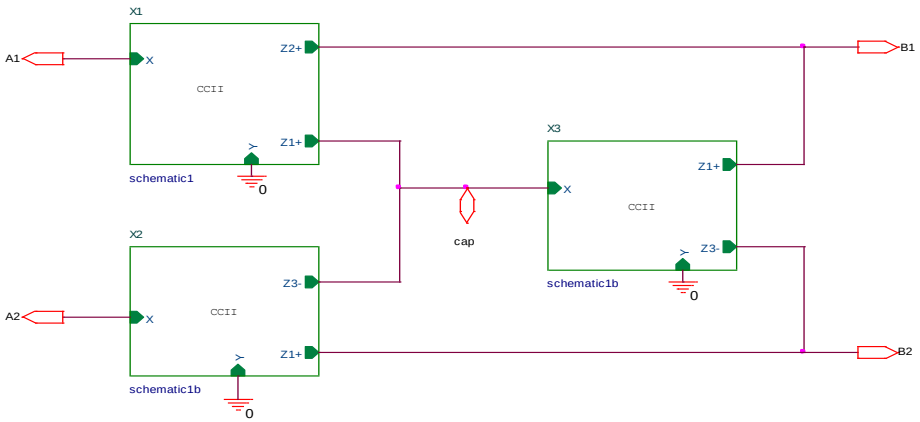


Fig 4.11(c): internal diagram of wave element

Figure 4.11 Realization circuit of grounded capacitor

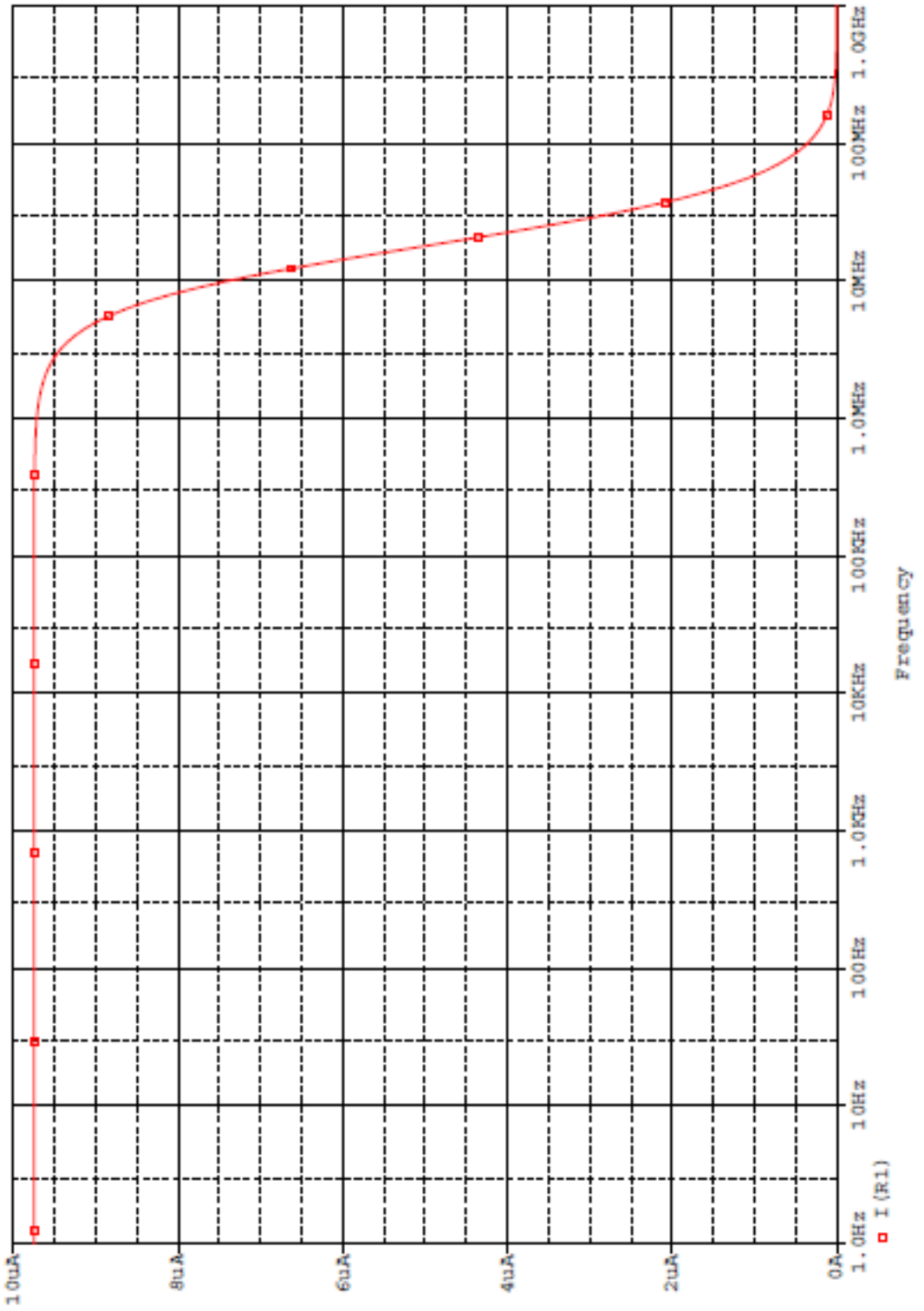


Figure 4.12 Simulation Result of grounded Capacitor

b) Inductor in grounded fashion

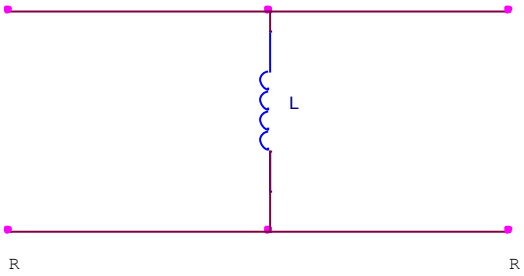


Fig 13(a): Two port grounded L

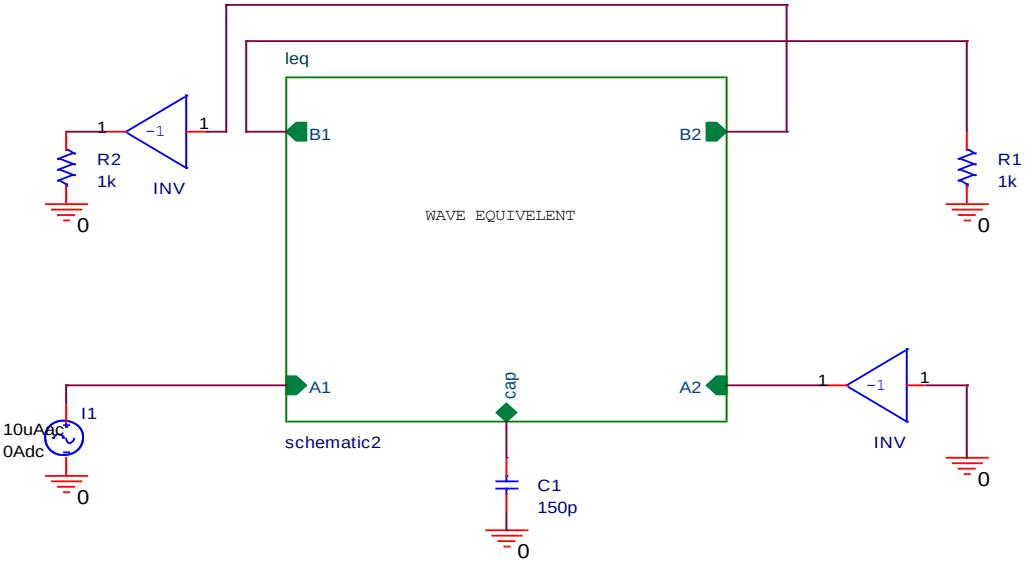


Fig 4.13(b): Wave Equivalent of grounded L

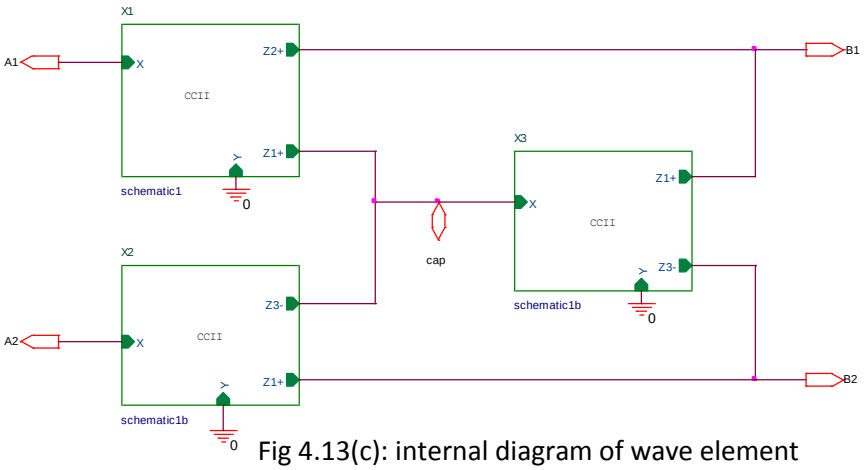


Fig 4.13(c): internal diagram of wave element

Figure 4.13 Realization circuit of grounded inductor

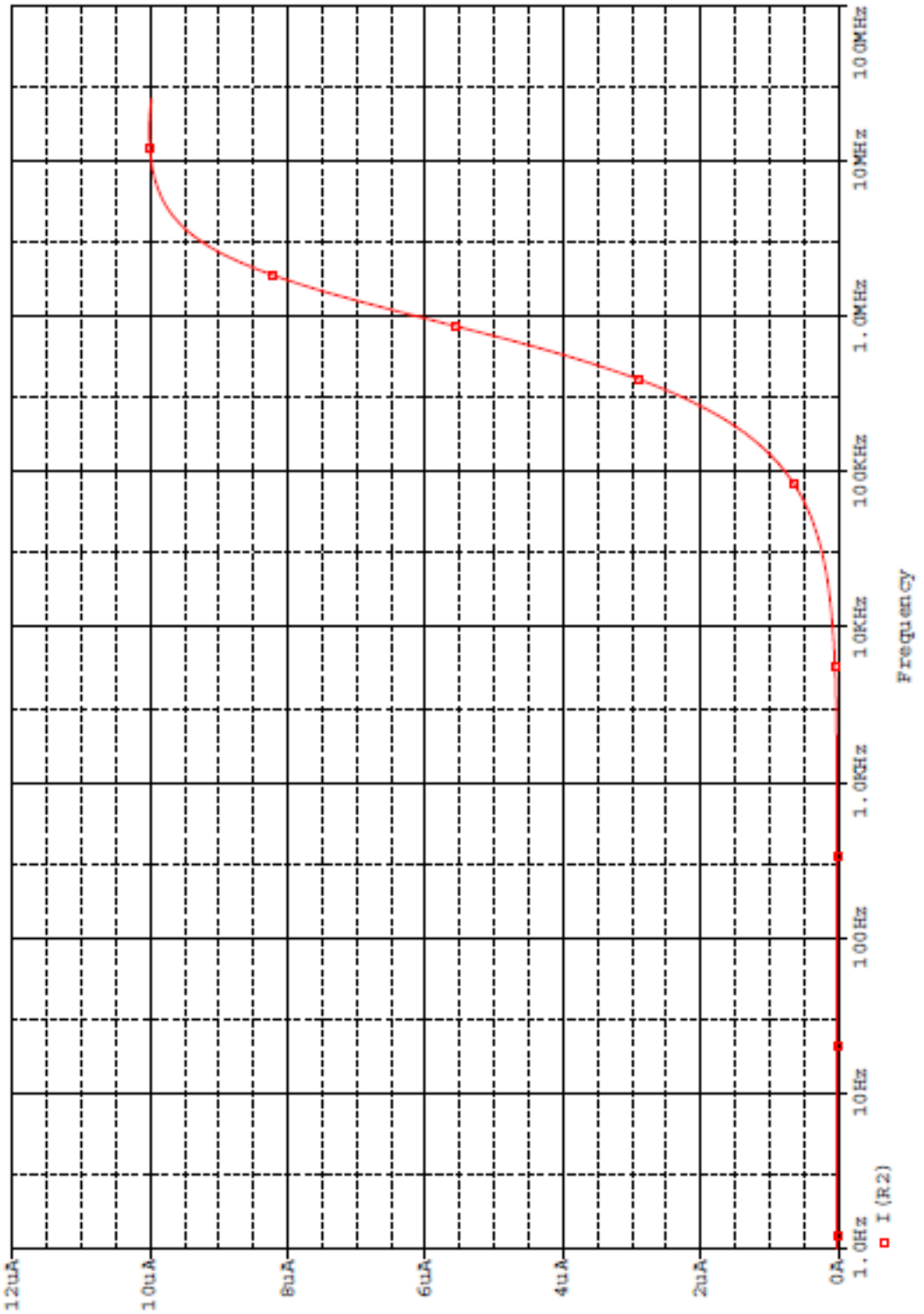


Figure 4.14 Simulation Result of grounded inductor

c) LC series grounded fashion

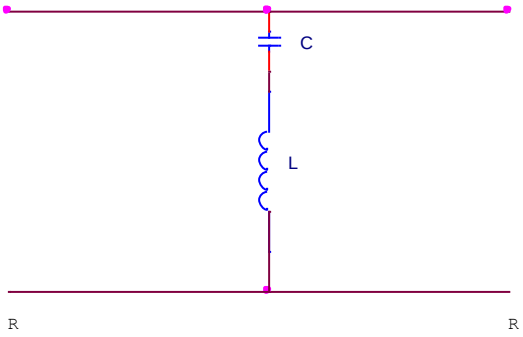


Fig 15(a): Two port grounded LC series

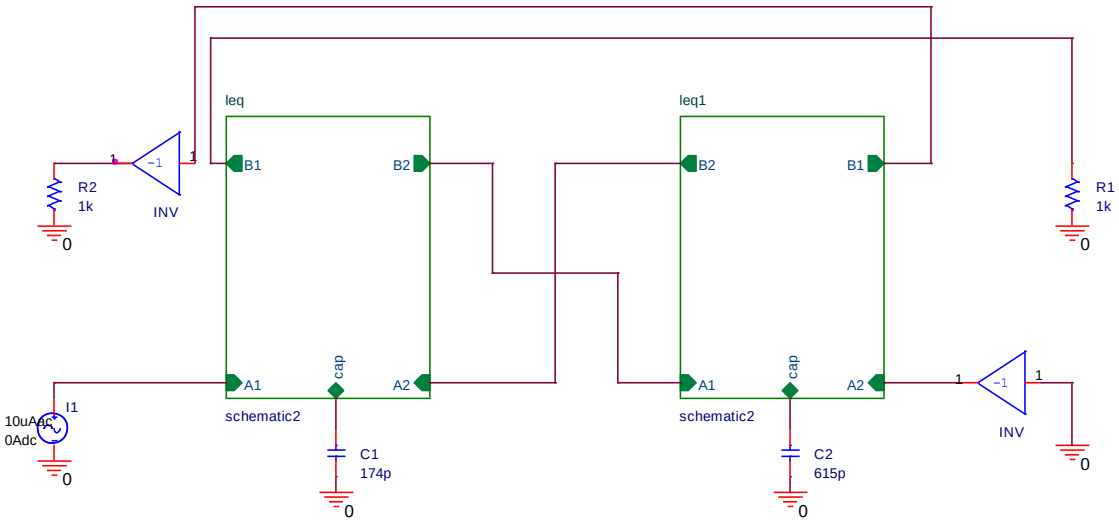


Fig 4.15(b): Wave Equivalent of grounded LC series subnetwork

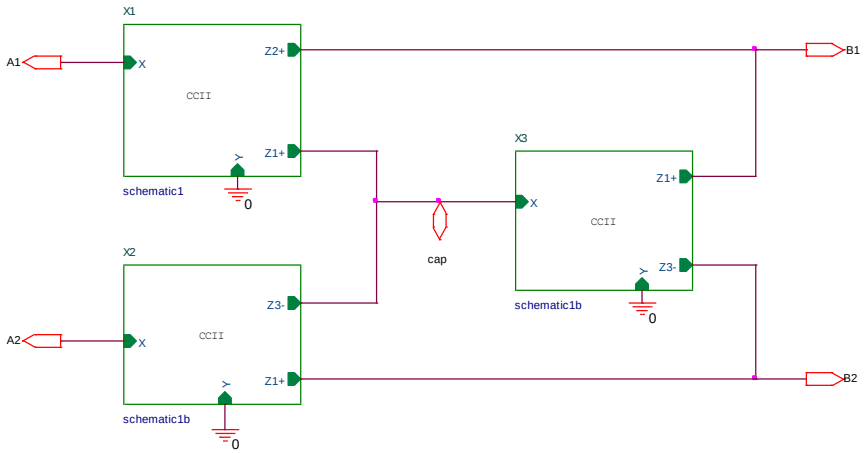


Fig 4.1(c): internal diagram of wave element

Figure 4.15 Realization circuit of grounded LC series

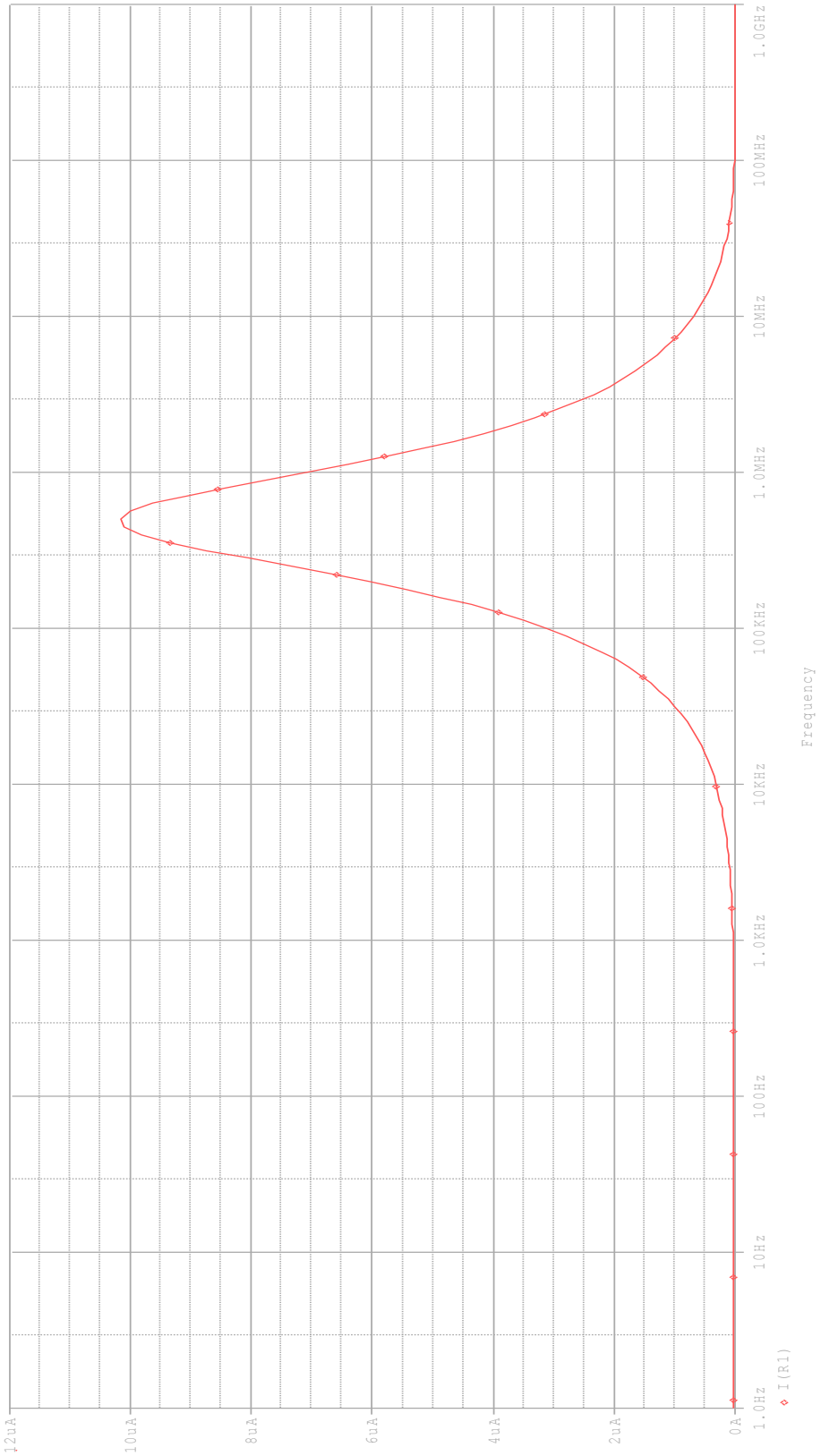


Figure 4.16 Simulation Result of grounded LC series configuration

d) LC parallel grounded fashion

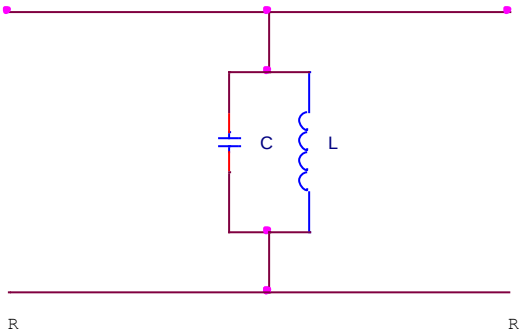


Fig 17(a) : Two port grounded LC parallel subnetwork

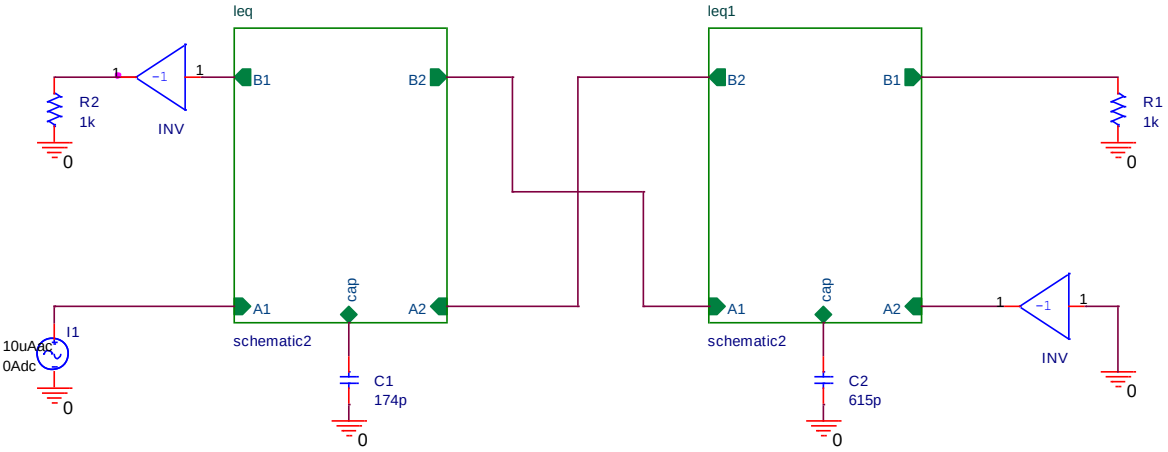


Fig 4.17(b): Wave Equivalent of grounded LC parallel subnetwork

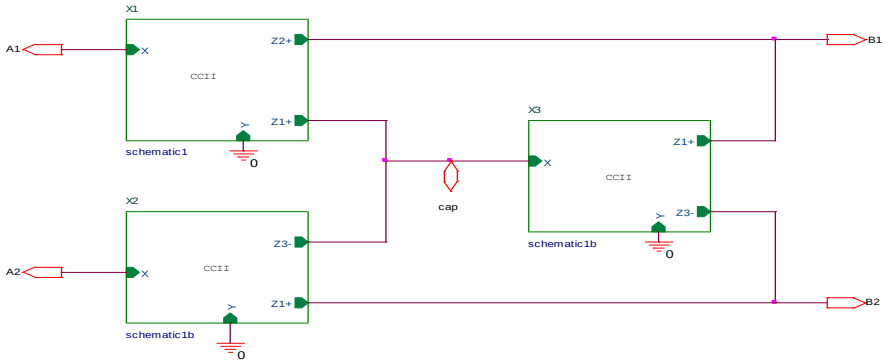


Fig 4.17(c): internal diagram of wave element

Figure 4.17 Realization circuit of grounded LC parallel

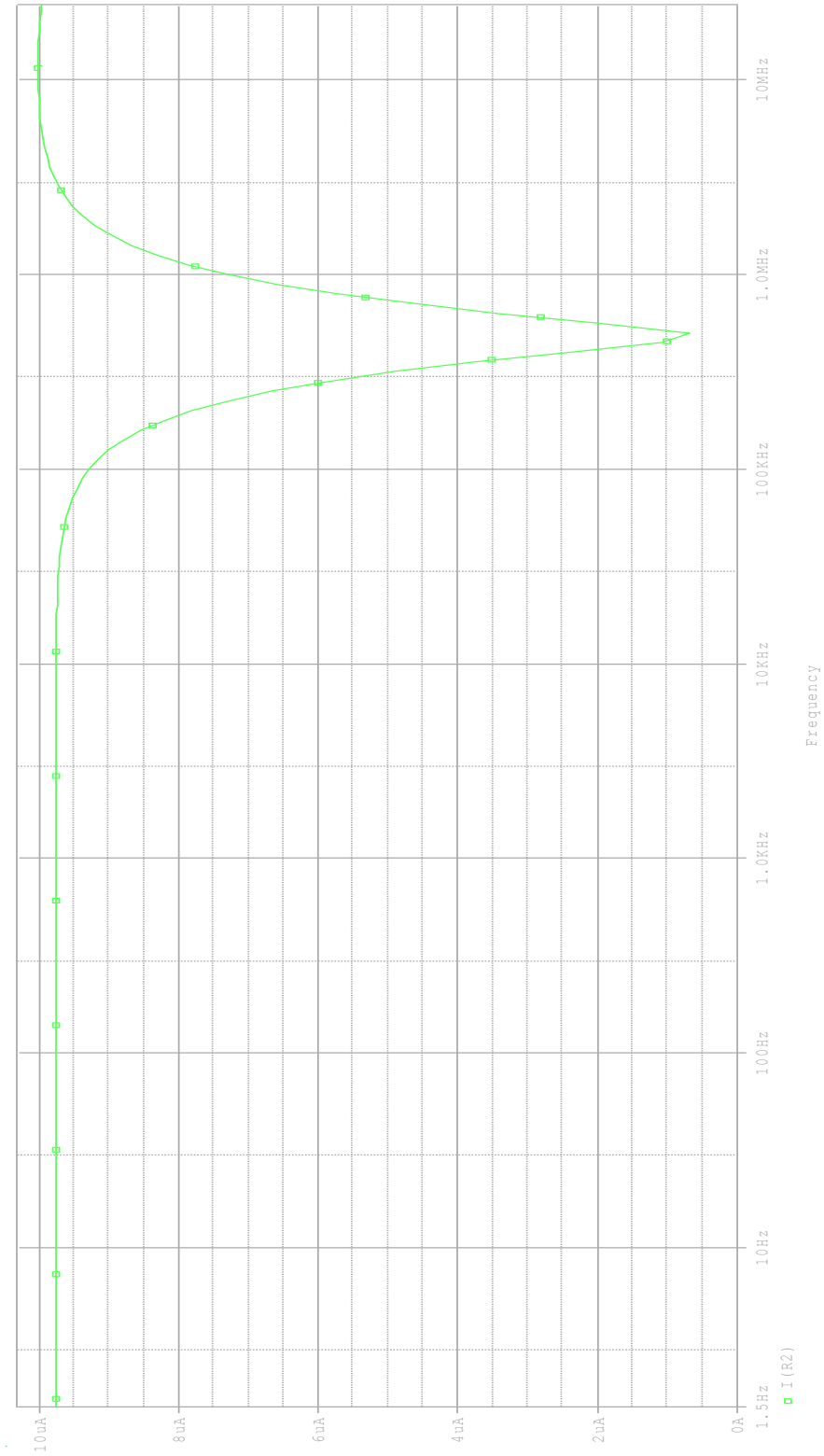


Figure 4.18 Simulation Result of grounded LC parallel configuration

4.2 Realization of 3rd Order lowpass filter

As an example of third order lowpass filter [46] in figure 4.19 is simulated by previously described technique. Filter specifications are the following: cutoff frequency fc = 1MHz and 1dB passband ripple; the element values of the filter are R_S, R_L = 1, C_1 = 259.5 nF, C_2 = 96.26 nF, L_2 = 109 nH, C_3 = 259.5 nF

The achieved cutoff frequency was 900 kHz, and the maximum passband ripple was about 1 dB.

Simulation of third order low pass filter using wave active element.

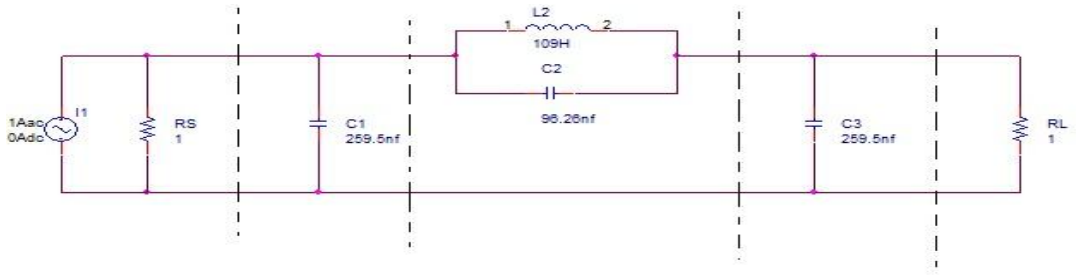


Figure 4.19 third order LC Low Pass filter.

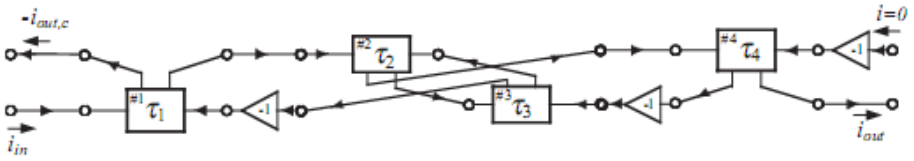


Figure 4.20 Wave model of the LC filter in Figure 18

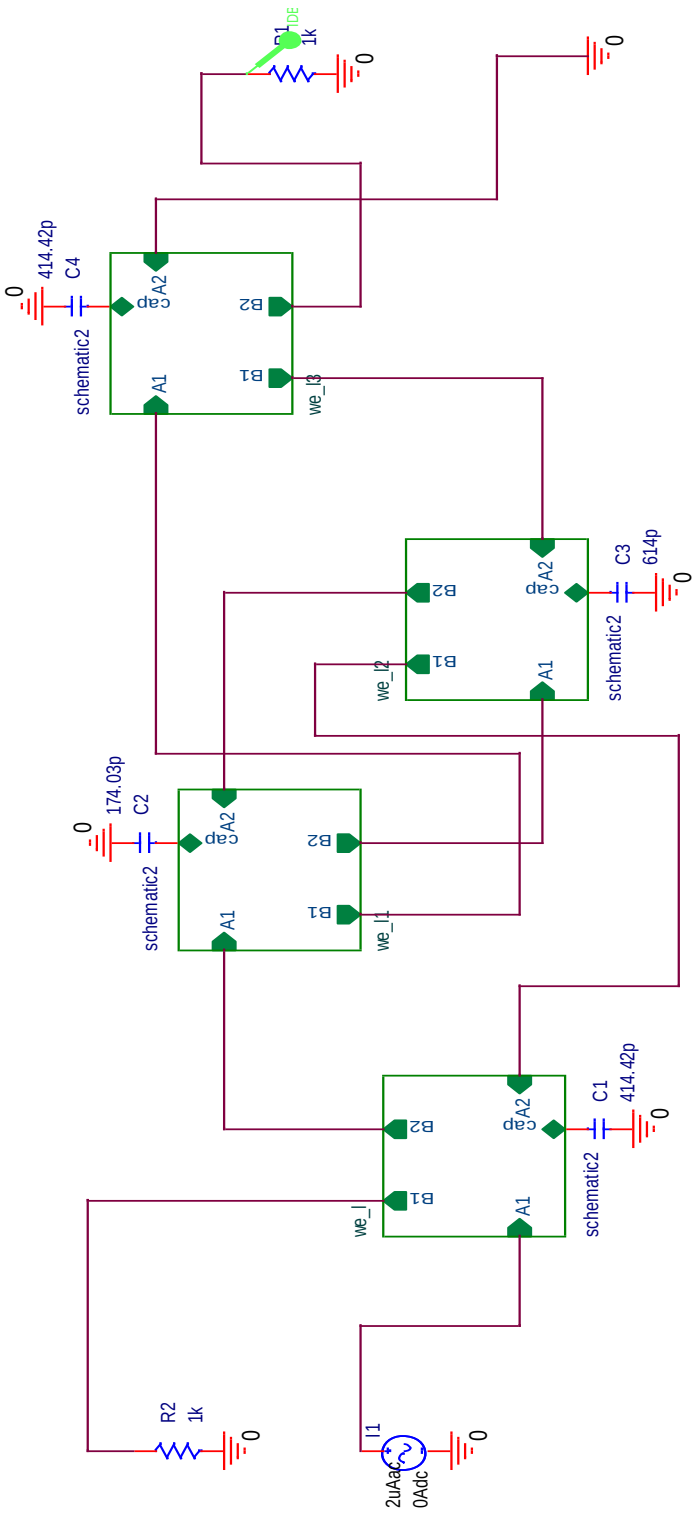


Figure 4.21 Wave model of the LC lowpass filter in Figure 18

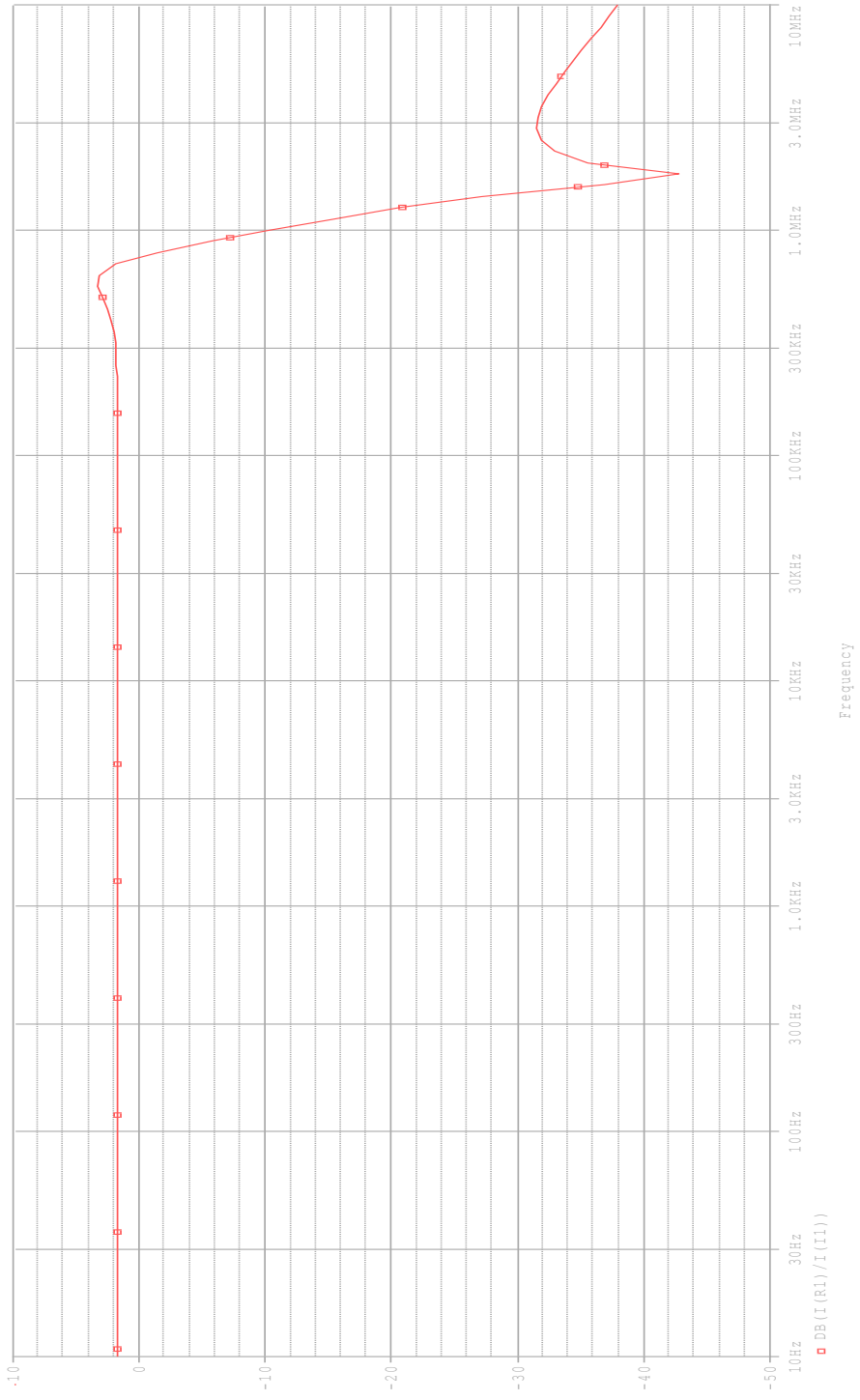


Figure 4.22 Frequency response of wave active low pass filter

Chapter-5

CONCLUSION AND FUTURE SCOPE

In this report a study of current conveyor, current conveyor based wave active filers are presented in details. Thereafter realization of wave filter based on current conveyor has been presented.

Higher order filters can be easily designed using the wave method. For this purpose, the wave equivalent of an inductor in a series branch may be realized using an appropriate current conveyor based configuration. This equivalent is the elementary building block for deriving the wave equivalents of the other reactive elements of the passive prototype filter. This is achieved by employing manipulated versions of the elementary building block. The behavior of the low pass wave filter is evaluate through simulations.

Now any filter specification can be designed using this wave active element topology. With the specifications provided the transfer function is first find out and using that transfer function respective LC ladder circuit can be design. Finally wave active filter circuit can be constructed.

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APPENDIX

Parameter of CMOS realization of CCII

Table 2. Parameters of CMOS transistors

0.18 µm TSMC CMOS parameter		
.MODEL NMOS NMOS (LEVEL = 7		
+TNOM = 27	TOX = 4.1E-9	
+XJ = 1E-7	NCH = 2.3549E17	VTH0 = 0.3750766
+K1 = 0.5842025	K2 = 1.245202E-3	K3 = 1E-3
+K3B = 0.0295587	W0 = 1E-7	NLX = 1.597846E-7
+DVT0W = 0	DVT1W = 0	DVT2W = 0
+DVT0 = 1.3022984	DVT1 = 0.4021873	DVT2 = 7.631374E-3
+U0 = 296.8451012	UA = -1.179955E-9	UB = 2.32616E-18
+UC = 7.593301E-11	VSAT = 1.747147E5	A0 = 2
+AGS = 0.452647	B0 = 5.506962E-8	B1 = 2.640458E-6
+KETA = -6.860244E-3	A1 = 7.885522E-4	A2 = 0.3119338
+RDSW = 105	PRWG = 0.4826	PRWB = -0.2
+WR = 1	WINT = 4.410779E-9	LINT = 2.045919E-8
+XL = 0	XW = -1E-8	DWG = -2.610453E-9
+DWB = -4.344942E-9	VOFF = -0.0948017	NFACTOR = 2.1860065
+CIT = 0	CDSC = 2.4E-4	CDSCD = 0
+CDSCB = 0	ETA0 = 1.991317E-3	ETAB = 6.028975E-5
+DSUB = 0.0217897	PCLM = 1.7062594	PDIBLC1 = 0.2320546
+PDIBLC2 = 1.670588E-3	PDIBLCB = -0.1	DROUT = 0.8388608
+PSCBE1 = 1.904263E10	PSCBE2 = 1.546939E-8	PVAG = 0
+DELTA = 0.01	RSH = 7.1	MOBMOD = 1
+PRT = 0	UTE = -1.5	KT1 = -0.11
+KT1L = 0	KT2 = 0.022	UA1 = 4.31E-9
+UB1 = -7.61E-18	UC1 = -5.6E-11	AT = 3.3E4
+WL = 0	WLN = 1	WW = 0
+WWN = 1	WWL = 0	LL = 0
+LLN = 1	LW = 0	LWN = 1
+LWL = 0	CAPMOD = 2	XPART = 0.5
+CGDO = 6.7E-10	CGSO = 6.7E-10	CGBO = 1E-12
+CJ = 9.550345E-4	PB = 0.8	MJ = 0.3762949
+CJSW = 2.083251E-10	PBSW = 0.8	MJSW = 0.1269477
+CJSWG = 3.3E-10	PBSWG = 0.8	MJSWG = 0.1269477
+CF = 0	PVTH0 = -2.369258E-3	PRDSW = -1.2091688
+PK2 = 1.845281E-3	WKETA = -2.040084E-3	LKETA = -1.266704E-3
+PU0 = 1.0932981	PUA = -2.56934E-11	PUB = 0
+PVSAT = 2E3	PETA0 = 1E-4	PKETA = -3.350276E-3)
*.		

```
.MODEL PMOS PMOS (      LEVEL   = 7
+ TNOM    = 27          TOX     = 4.1E-9
+XJ      = 1E-7         NCH     = 4.1589E17     VTH0    = -0.3936726
+K1      = 0.5750728    K2      = 0.0235926     K3      = 0.1590089
+K3B     = 4.2687016    W0      = 1E-6          NLX     = 1.033999E-7
+DVT0W   = 0            DVT1W   = 0             DVT2W   = 0
+DVT0    = 0.5560978    DVT1    = 0.2490116     DVT2    = 0.1
+U0      = 112.5106786  UA      = 1.45072E-9    UB      = 1.195045E-21
+UC      = -1E-10       VSAT    = 1.168535E5    A0      = 1.7211984
+AGS     = 0.3806925    B0      = 4.296252E-7   B1      = 1.288698E-6
+KETA    = 0.0201833    A1      = 0.2328472     A2      = 0.3
+RDSW    = 198.7483291  PRWG    = 0.5           PRWB    = -0.4971827
+WR      = 1            WINT    = 0             LINT    = 2.943206E-8
+XL      = 0            XW      = -1E-8         DWG     = -1.949253E-8
+DWB     = -2.824041E-9 VOFF    = -0.0979832    NFACTOR = 1.9624066
+CIT     = 0            CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0            ETA0    = 7.282772E-4   ETAB    = -3.818572E-4
+DSUB    = 1.518344E-3  PCLM    = 1.4728931     PDIBLC1 = 2.138043E-3
+PDIBLC2 = -9.966066E-6 PDIBLCB = -1E-3         DROUT   = 4.276128E-4
+PSCBE1  = 4.850167E10  PSCBE2  = 5E-10         PVAG    = 0
+DELTA   = 0.01         RSH     = 8.2           MOBMOD  = 1
+PRT     = 0            UTE     = -1.5          KT1     = -0.11
+KT1L    = 0            KT2     = 0.022         UA1     = 4.31E-9
+UB1     = -7.61E-18    UC1     = -5.6E-11      AT      = 3.3E4
+WL      = 0            WLN     = 1             WW      = 0
+WWN     = 1            WWL     = 0             LL      = 0
+LLN     = 1            LW      = 0             LWN     = 1
+LWL     = 0            CAPMOD  = 2             XPART   = 0.5
+CGDO    = 7.47E-10     CGSO    = 7.47E-10      CGBO    = 1E-12
+CJ      = 1.180017E-3  PB      = 0.8560642     MJ      = 0.4146818
+CJSW    = 2.046463E-10 PBSW    = 0.9123142     MJSW    = 0.316175
+CJSWG   = 4.22E-10     PBSWG   = 0.9123142     MJSWG   = 0.316175
+CF      = 0            PVTH0   = 8.456598E-4   PRDSW   = 8.4838247
+PK2     = 1.338191E-3  WKETA   = 0.0246885     LKETA   = -2.016897E-3
+PU0     = -1.5089586   PUA     = -5.51646E-11  PUB     = 1E-21
+PVSAT   = 50           PETA0   = 1E-4          PKETA   = -3.316832E-3    )
*
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Table 2. Dimensions of the CMOS transistors

Transistors	W (µm) / L (µm)
M1, M2	50/0.5
M3, M4	100/0.5
M5-M16, M19, M20	3.33/0.5
M17,M18	8.8/0.5